Fundamentals of Power Electronics

Second edition

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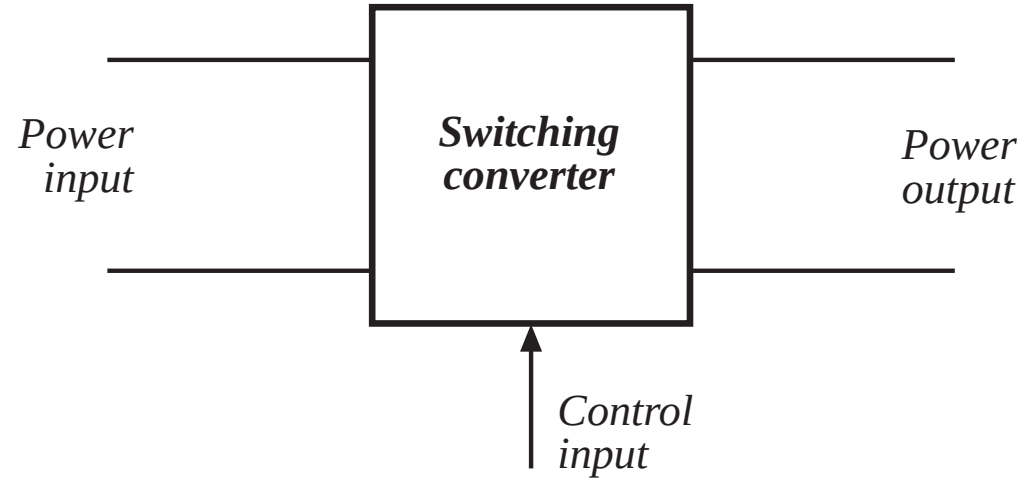
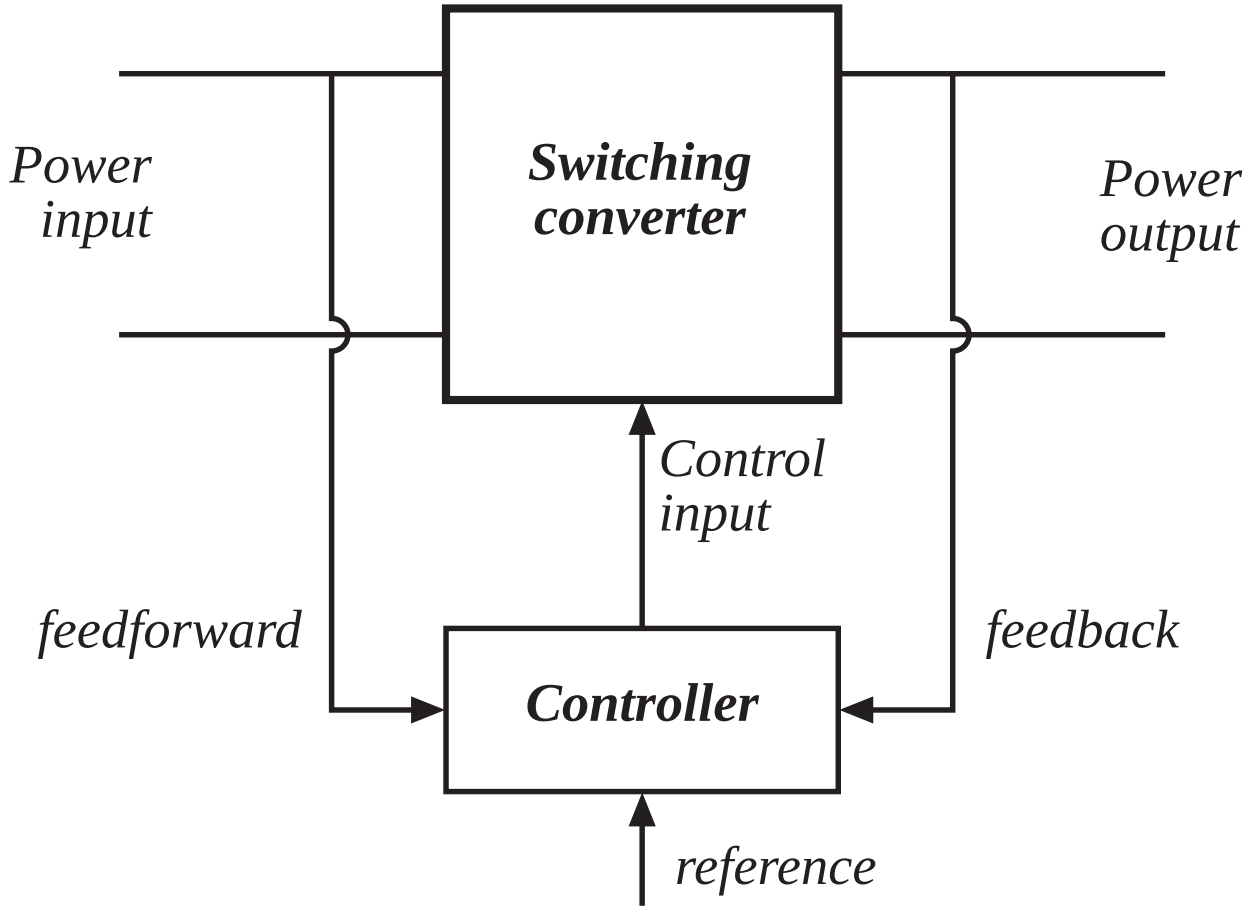
Chapter 1: Introduction

1.1 Introduction to Power Processing



Dc-dc conversion:	Change and control voltage magnitude
Ac-dc rectification:	Possibly control dc voltage, ac current
Dc-ac inversion:	Produce sinusoid of controllable magnitude and frequency
Ac-ac cycloconversion:	Change and control voltage magnitude and frequency

Control is invariably required

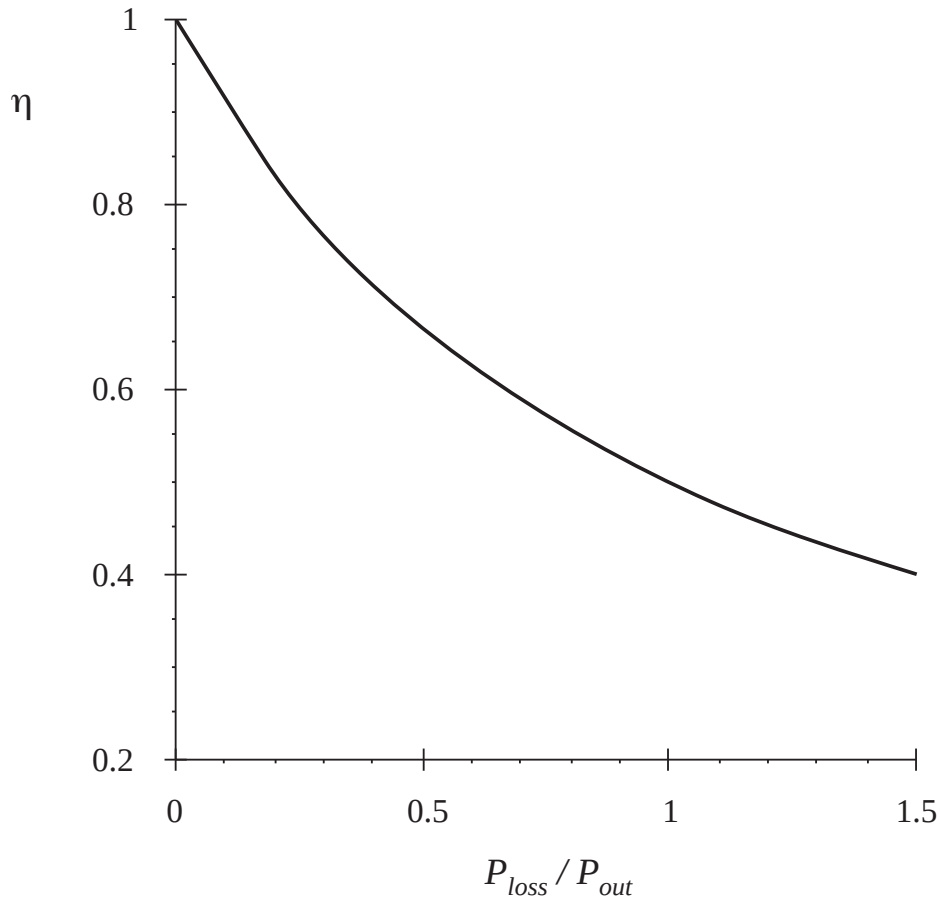


High efficiency is essential

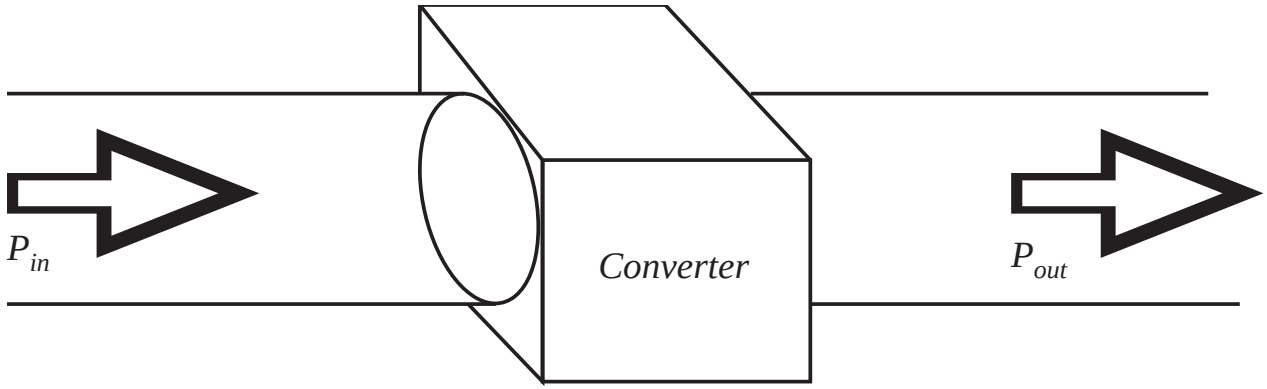
$$\eta = \frac{P_{out}}{P_{in}}$$

$$P_{loss} = P_{in} - P_{out} = P_{out}\left(\frac{1}{\eta} - 1\right)$$

- High efficiency leads to low power loss within converter
- Small size and reliable operation is then feasible
- Efficiency is a good measure of converter performance

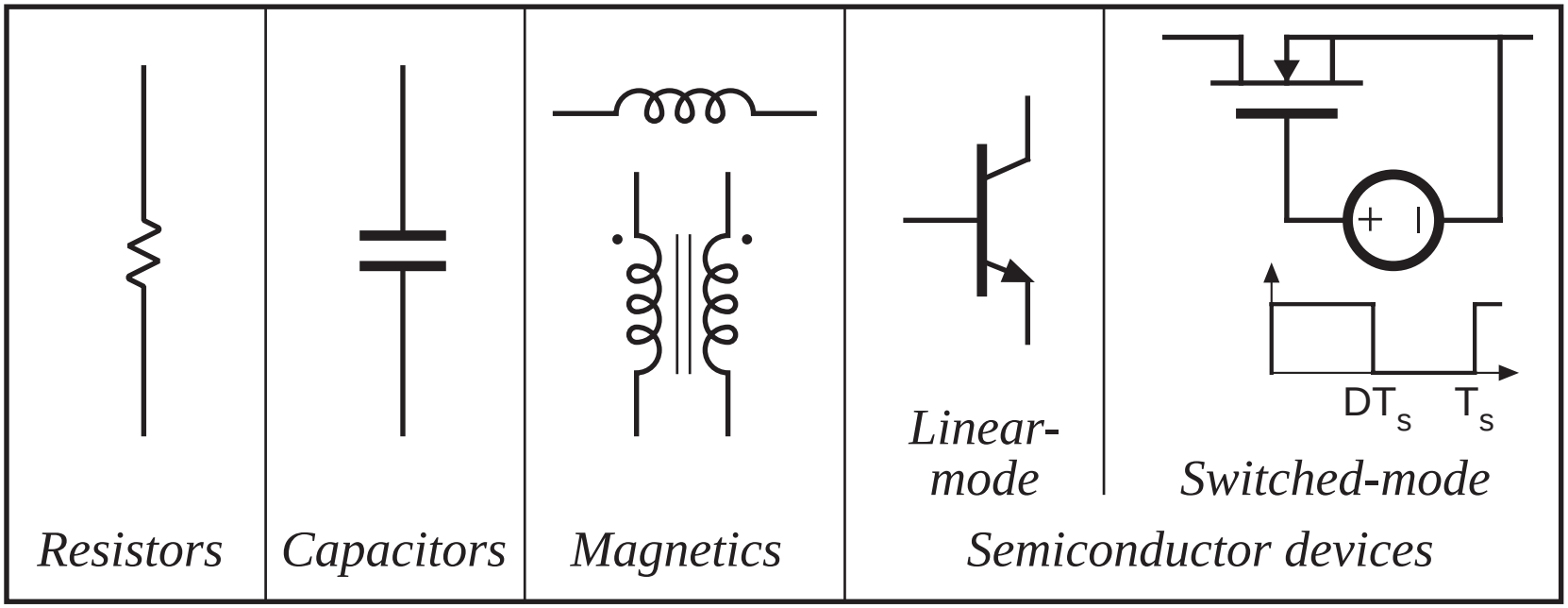


A high-efficiency converter

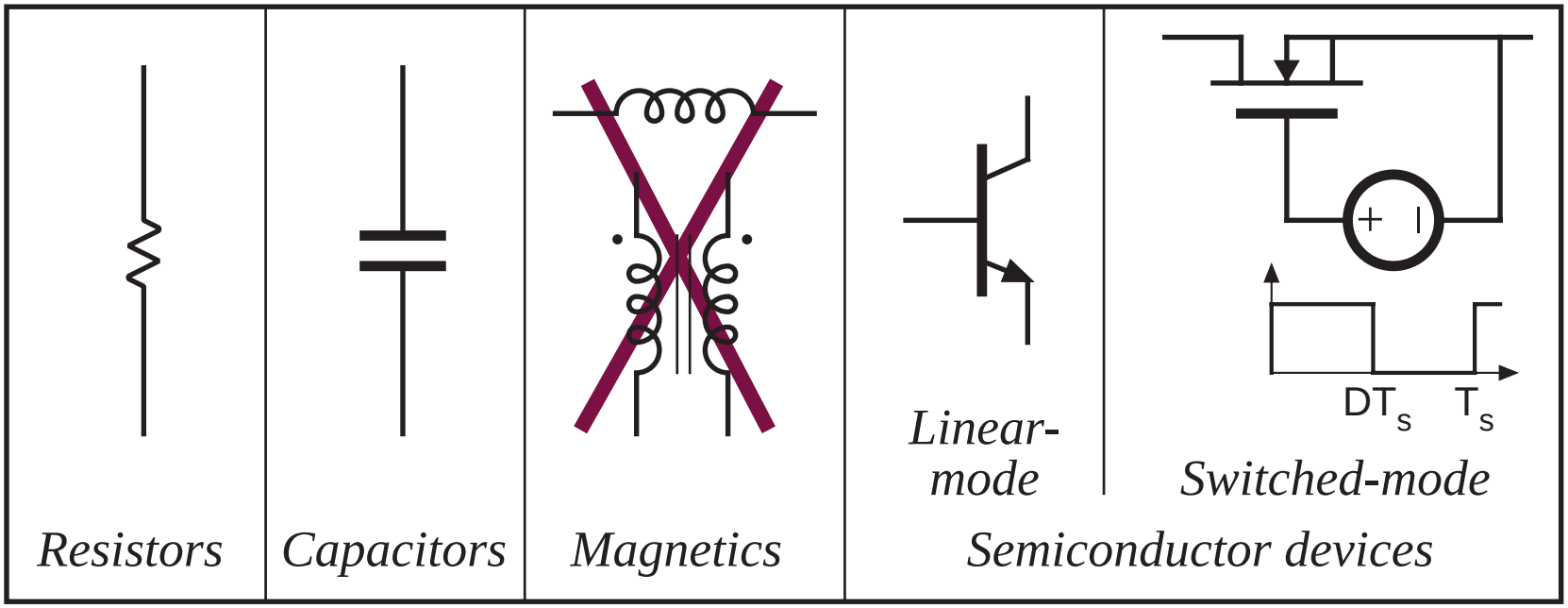


A goal of current converter technology is to construct converters of small size and weight, which process substantial power at high efficiency

Devices available to the circuit designer

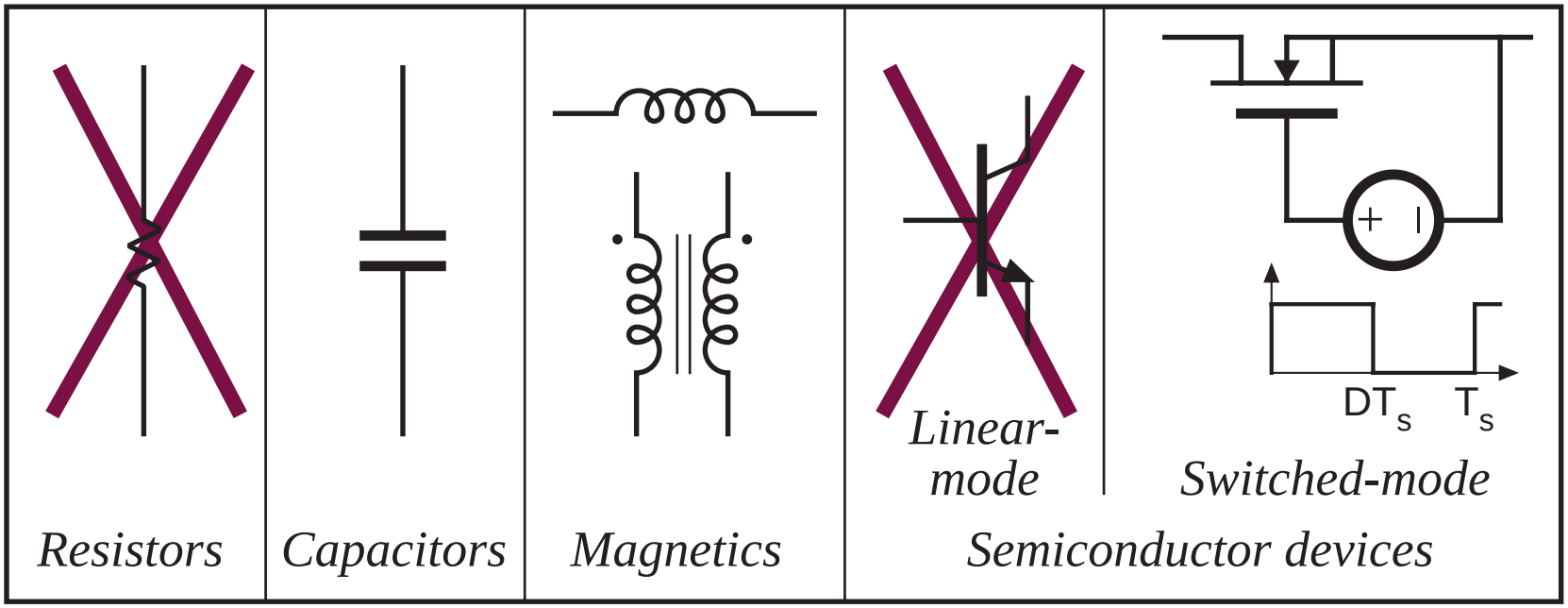


Devices available to the circuit designer



Signal processing: avoid magnetics

Devices available to the circuit designer



Power processing: avoid lossy elements

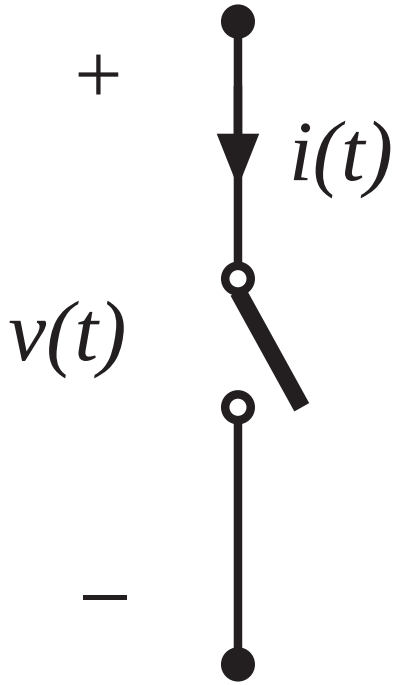
Power loss in an ideal switch

Switch closed: $v(t) = 0$

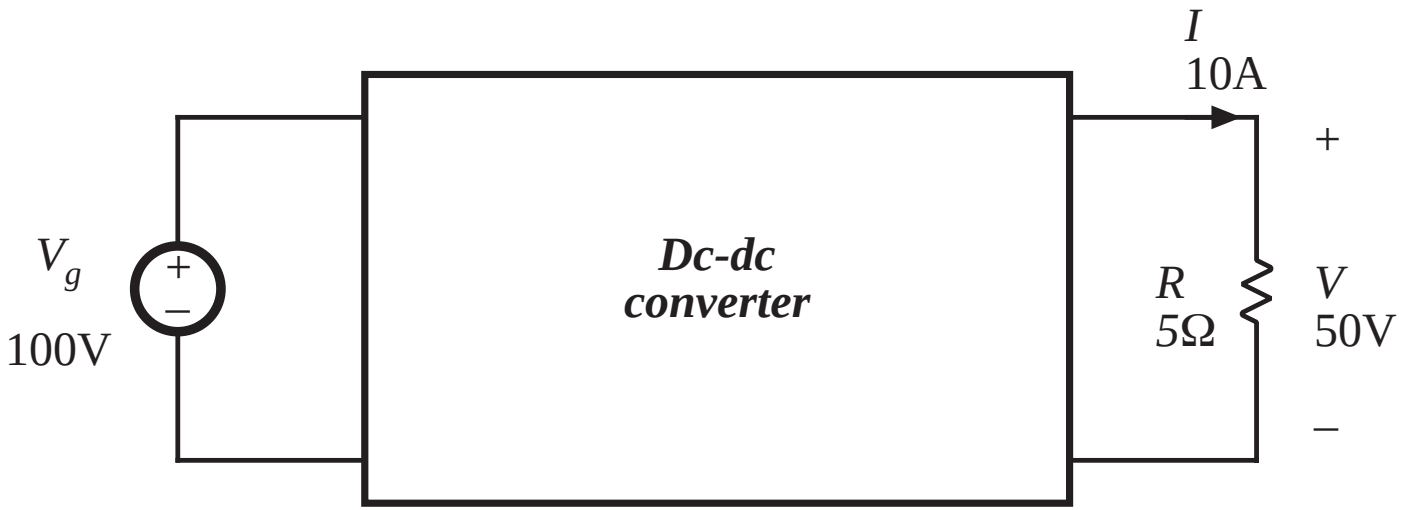
Switch open: $i(t) = 0$

In either event: $p(t) = v(t)\ i(t) = 0$

Ideal switch consumes zero power



A simple dc-dc converter example



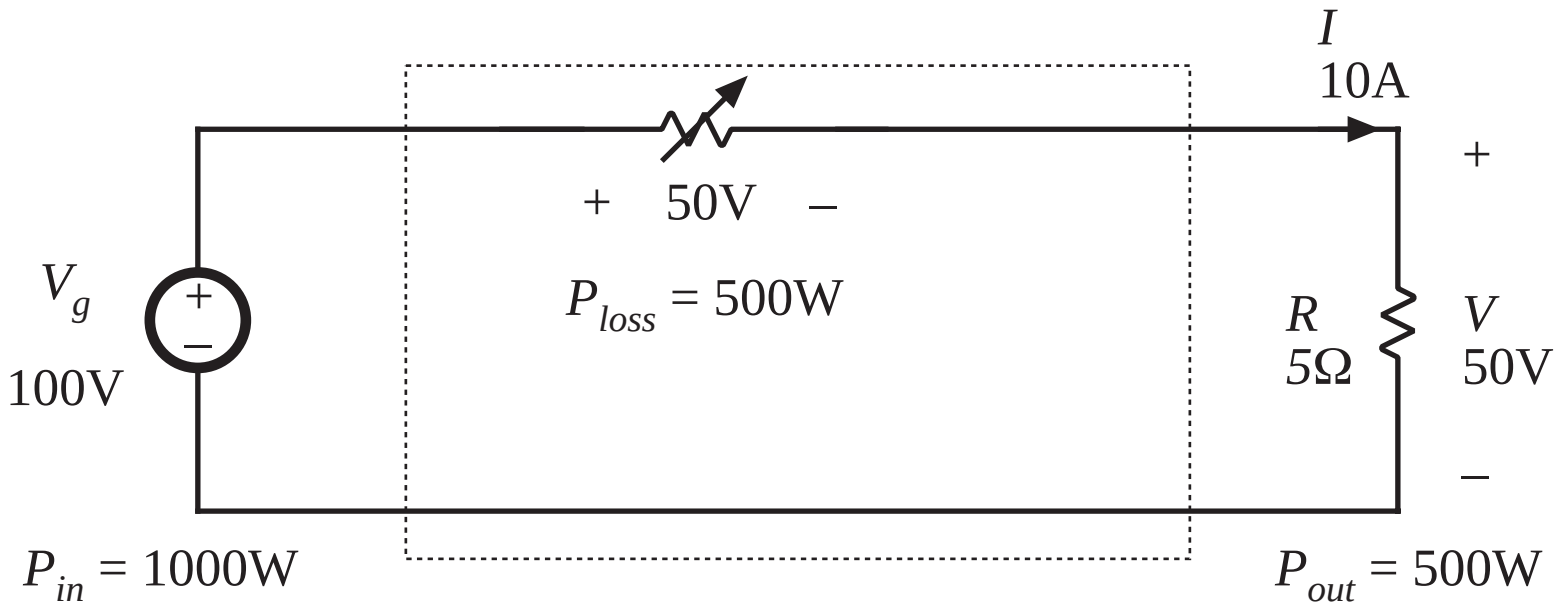
Input source: 100V

Output load: 50V, 10A, 500W

How can this converter be realized?

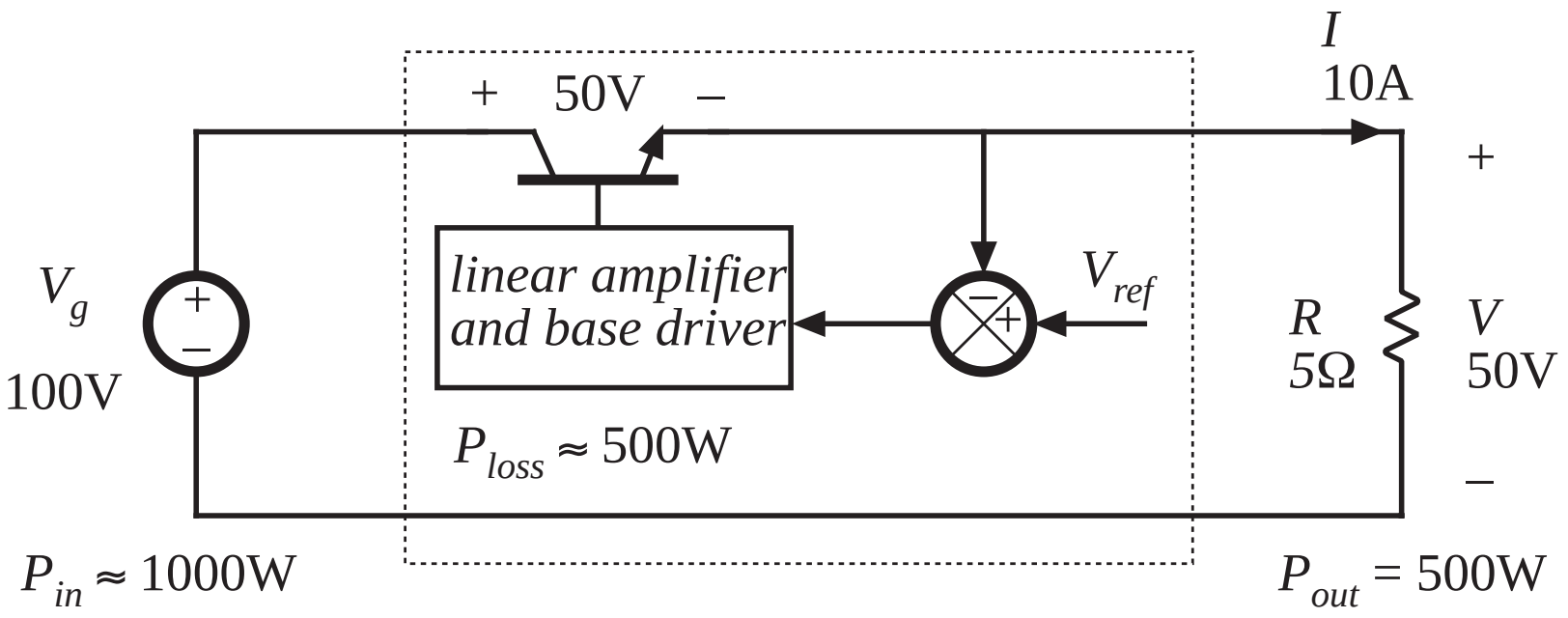
Dissipative realization

Resistive voltage divider

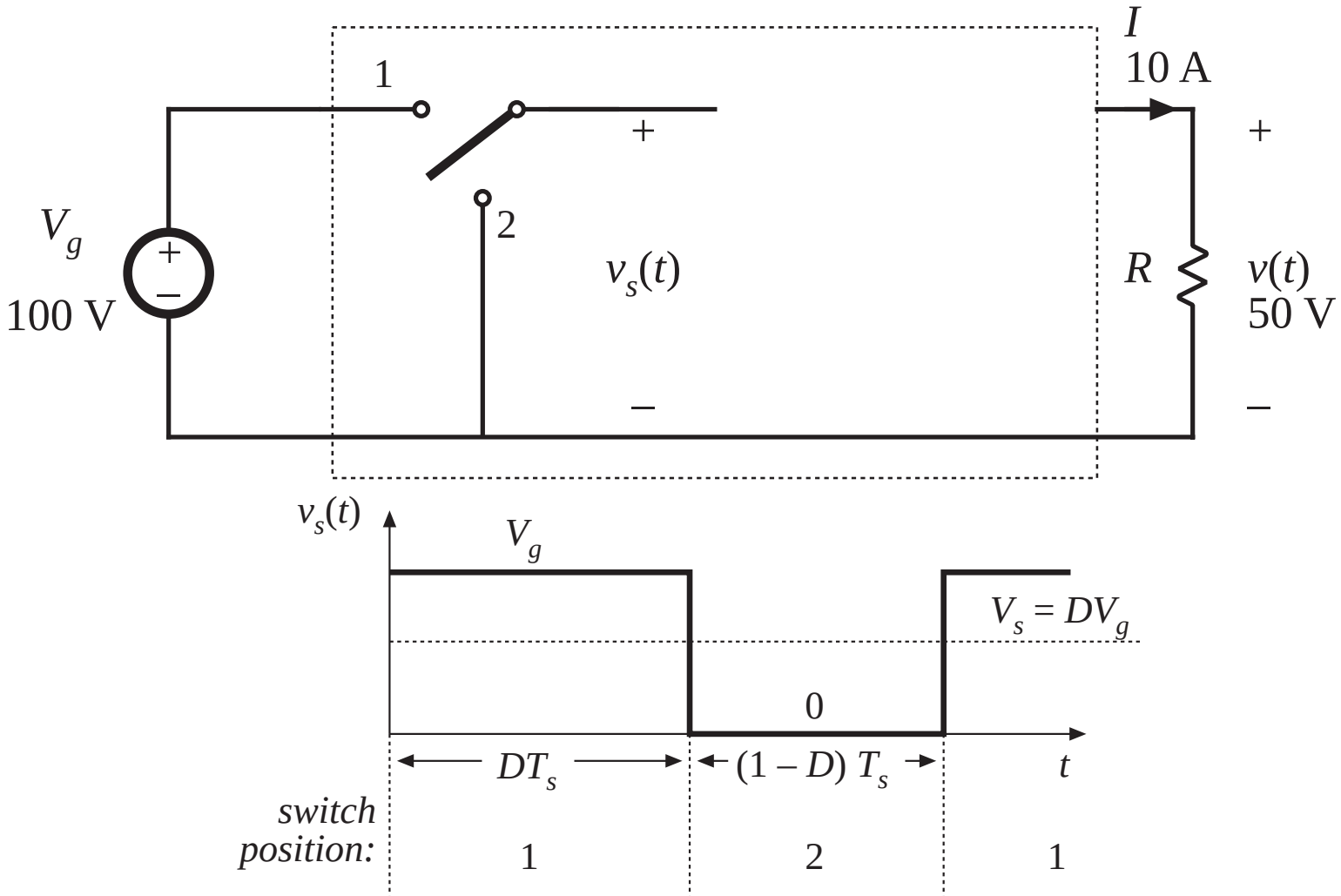


Dissipative realization

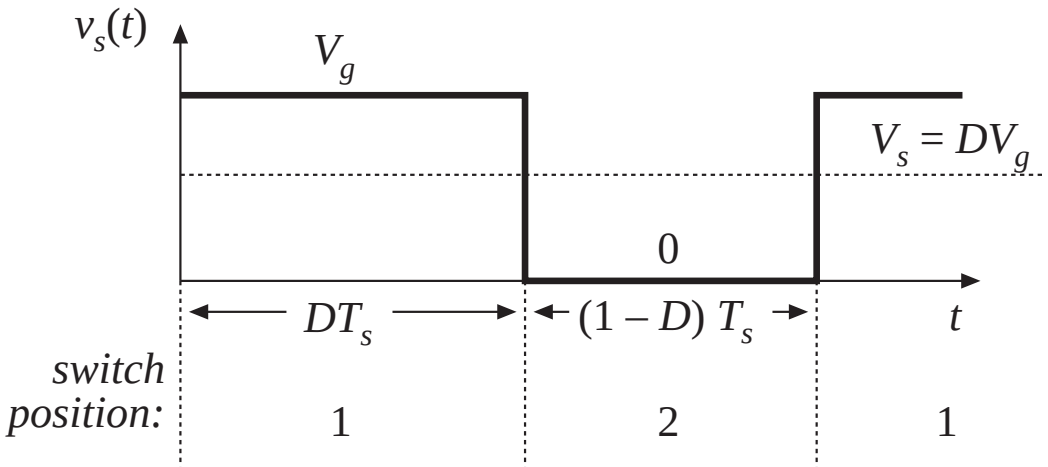
Series pass regulator: transistor operates in active region



Use of a SPDT switch



The switch changes the dc voltage level



D = switch duty cycle

$0 \le D \le 1$

T_s = switching period

f_s = switching frequency

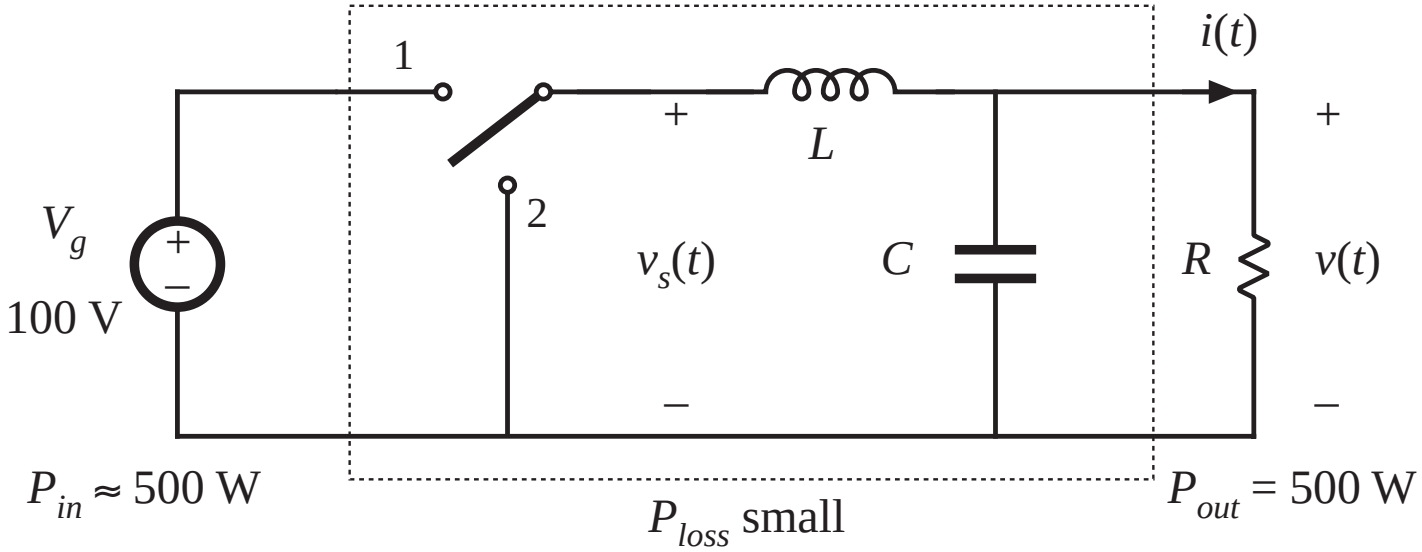
$= 1 / T_s$

DC component of $v_s(t)$ = average value:

$$V_s = \frac{1}{T_s} \int_0^{T_s} v_s(t)\, dt = DV_g$$

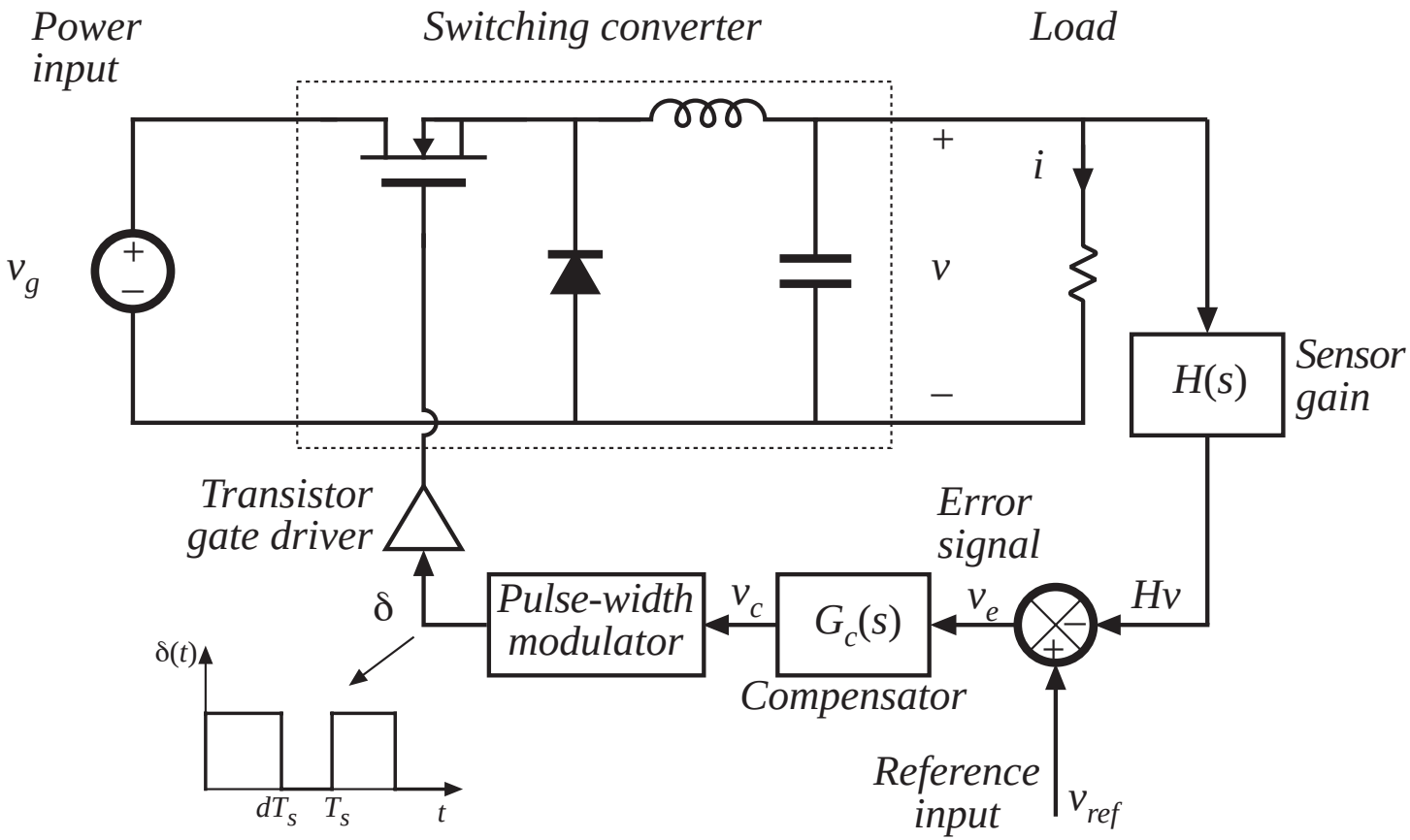
Addition of low pass filter

Addition of (ideally lossless) L-C low-pass filter, for removal of switching harmonics:

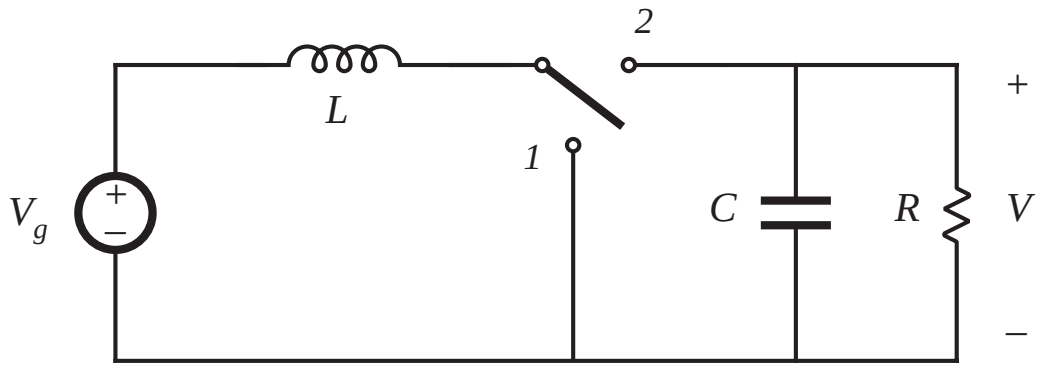


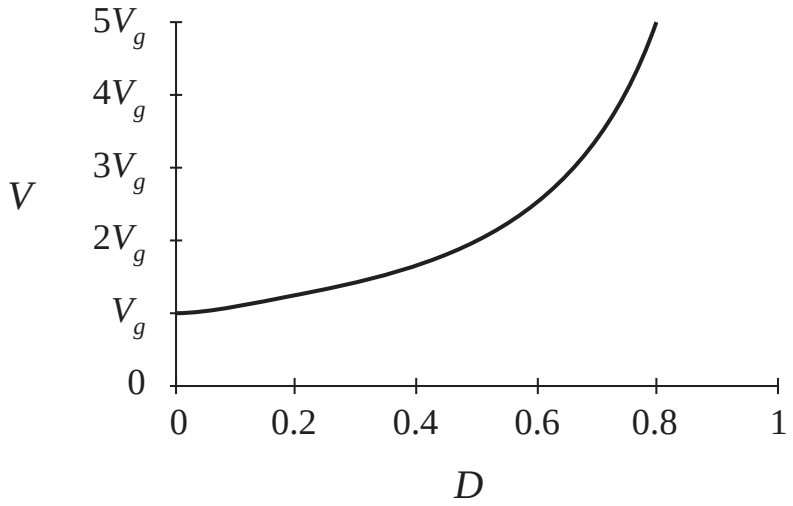
- Choose filter cutoff frequency f_0 much smaller than switching frequency f_s
- This circuit is known as the “buck converter”

Addition of control system for regulation of output voltage

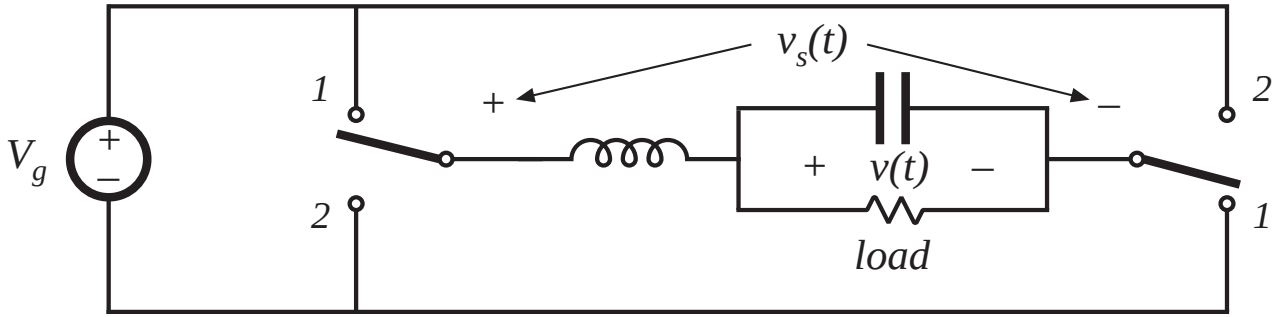


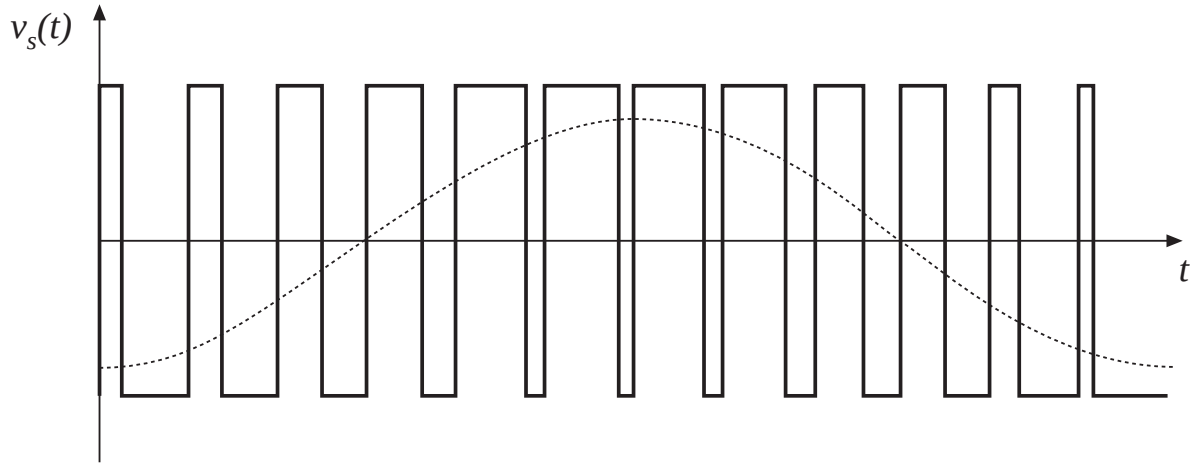
The boost converter





A single-phase inverter





"H-bridge"

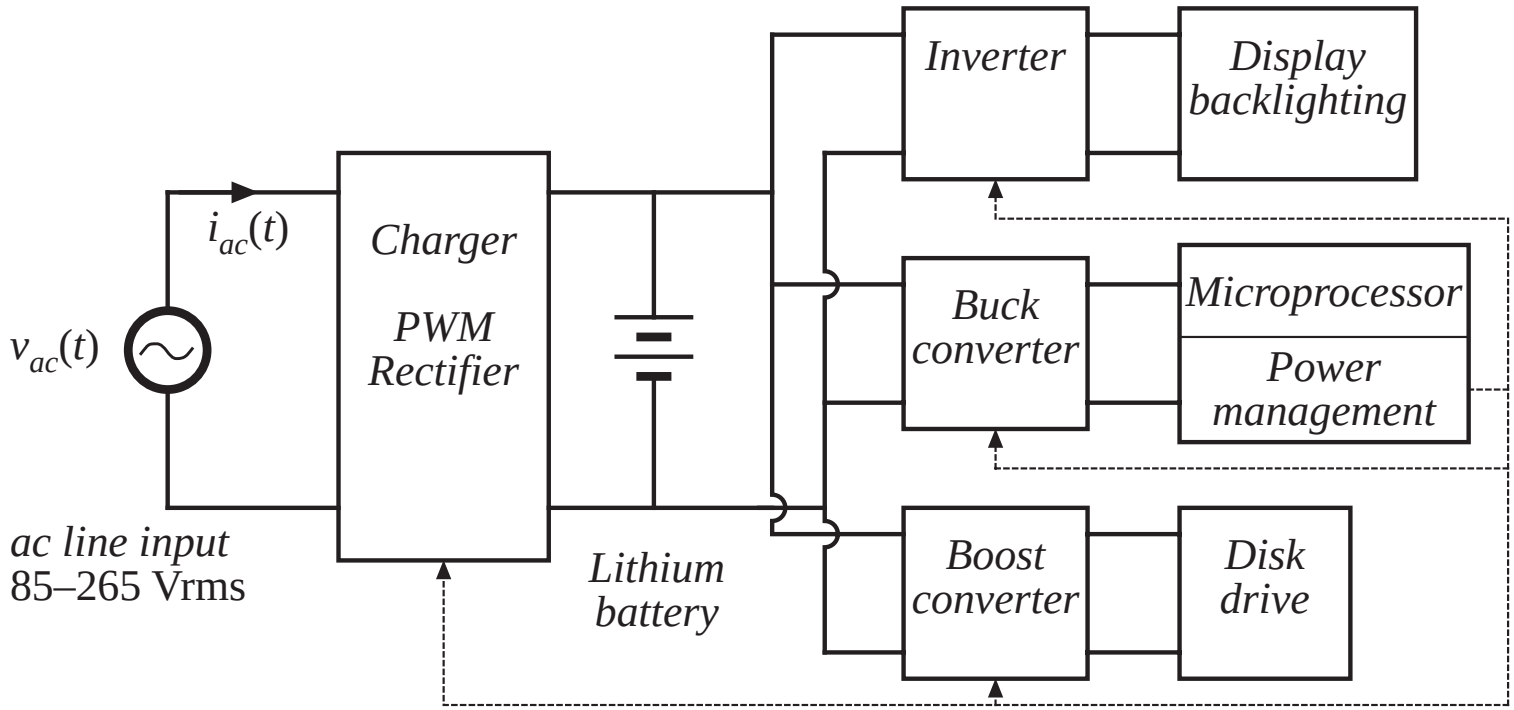
Modulate switch duty cycles to obtain sinusoidal low-frequency component

1.2 Several applications of power electronics

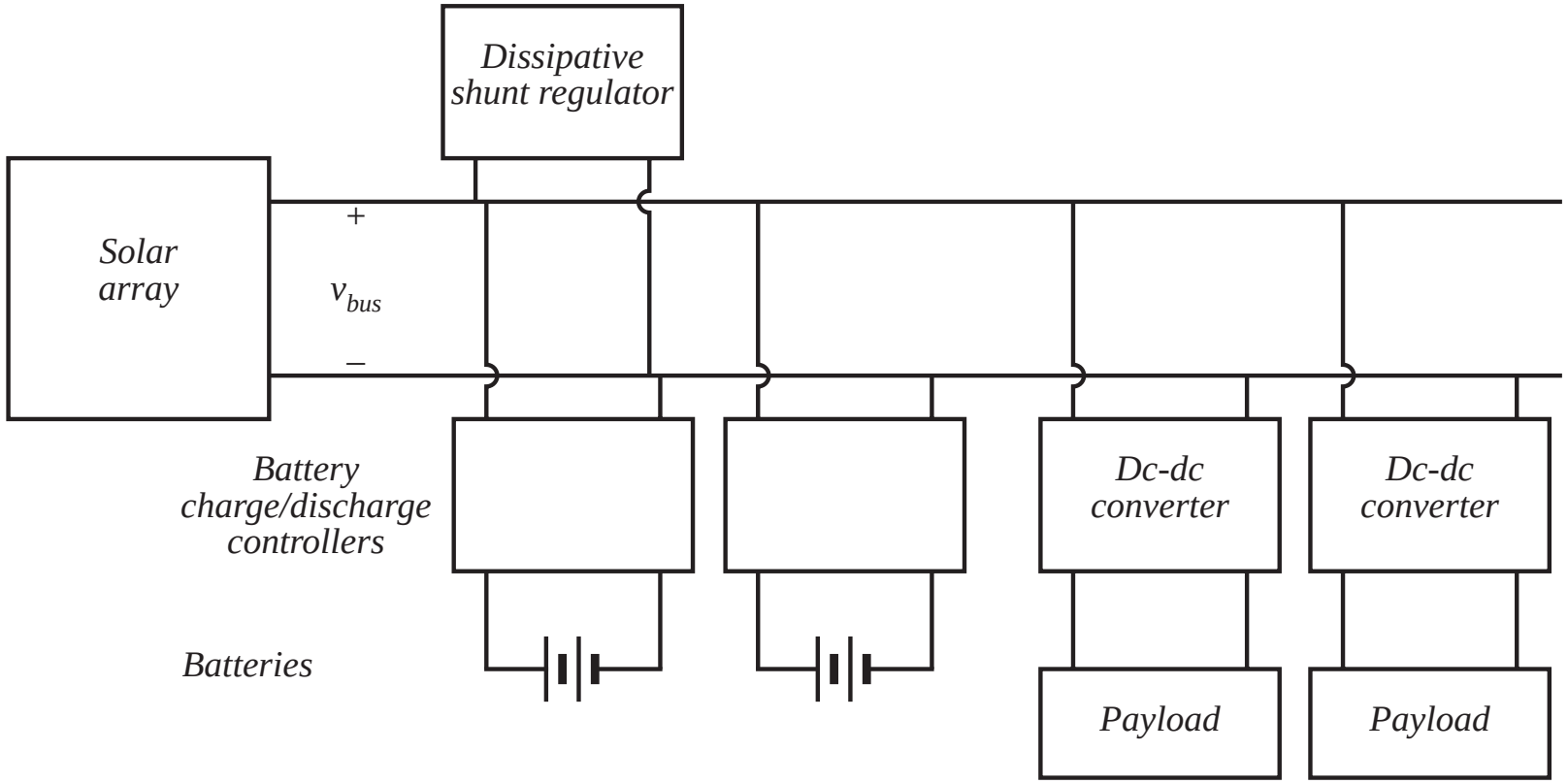
Power levels encountered in high-efficiency converters

- less than 1 W in battery-operated portable equipment
- tens, hundreds, or thousands of watts in power supplies for computers or office equipment
- kW to MW in variable-speed motor drives
- 1000 MW in rectifiers and inverters for utility dc transmission lines

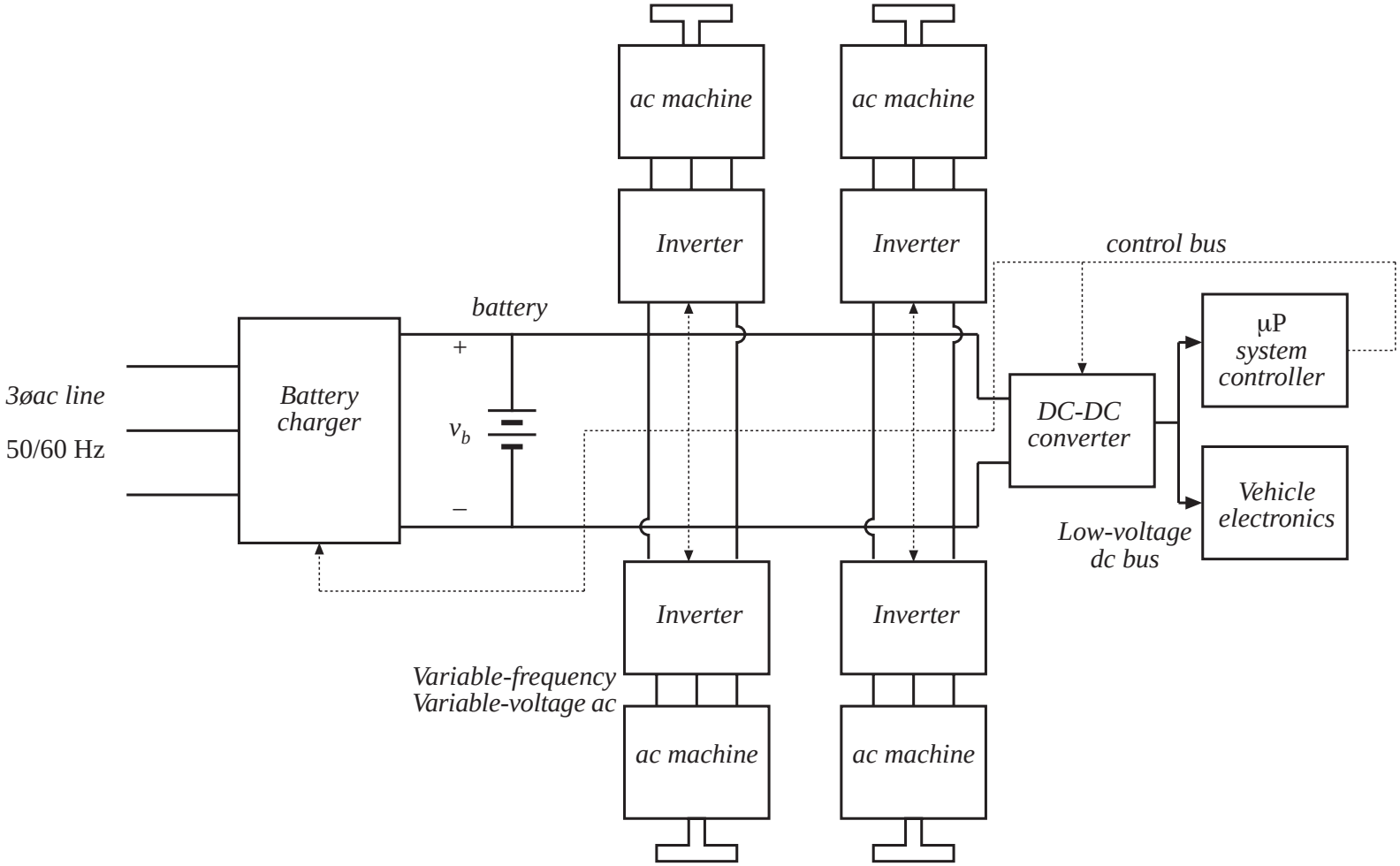
A laptop computer power supply system



Power system of an earth-orbiting spacecraft



An electric vehicle power and drive system



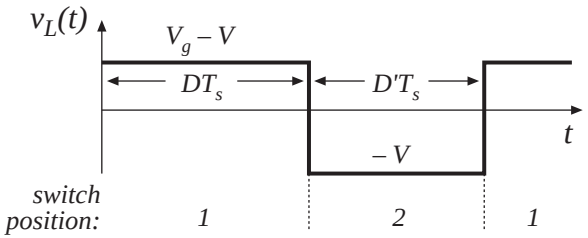
1.3 Elements of power electronics

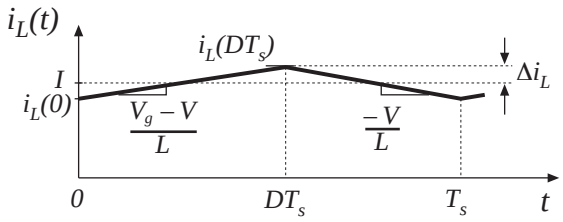
Power electronics incorporates concepts from the fields of

- analog circuits
- electronic devices
- control systems
- power systems
- magnetics
- electric machines
- numerical simulation

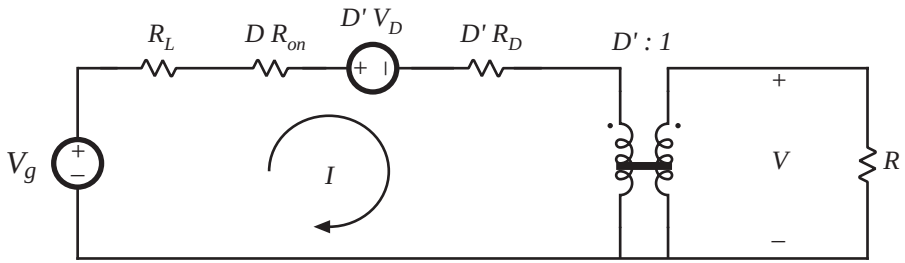
Part I. Converters in equilibrium

Inductor waveforms

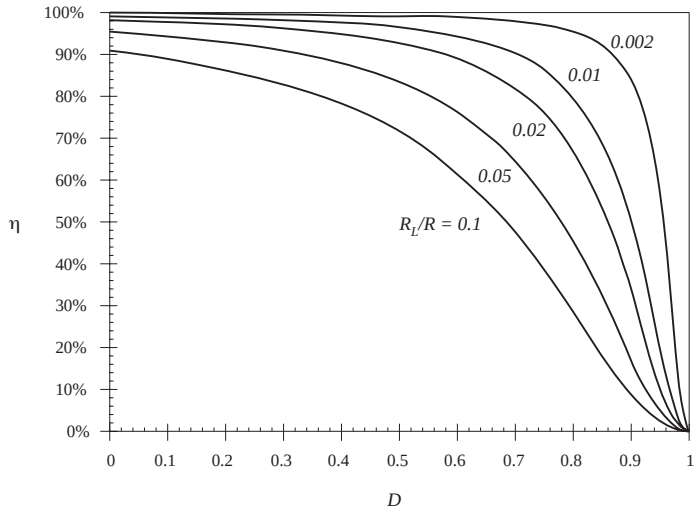




Averaged equivalent circuit



Predicted efficiency

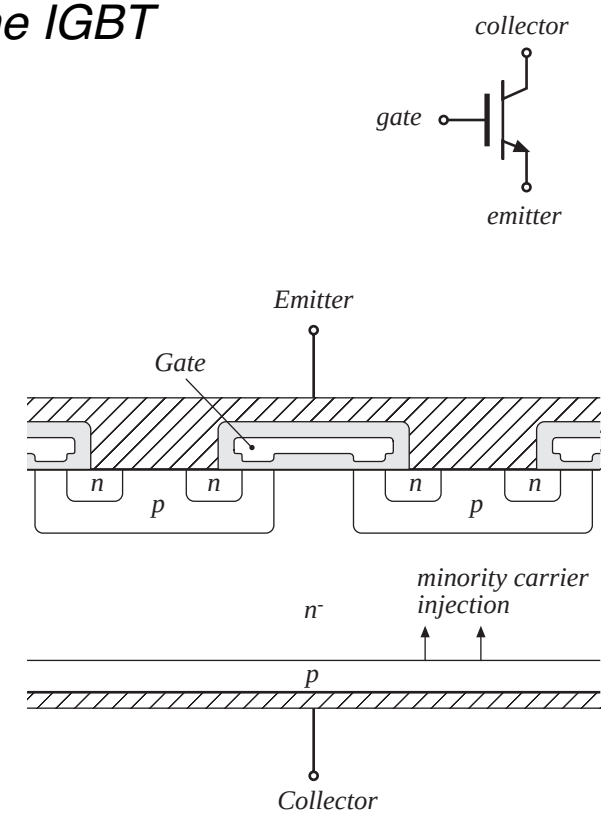


Discontinuous conduction mode

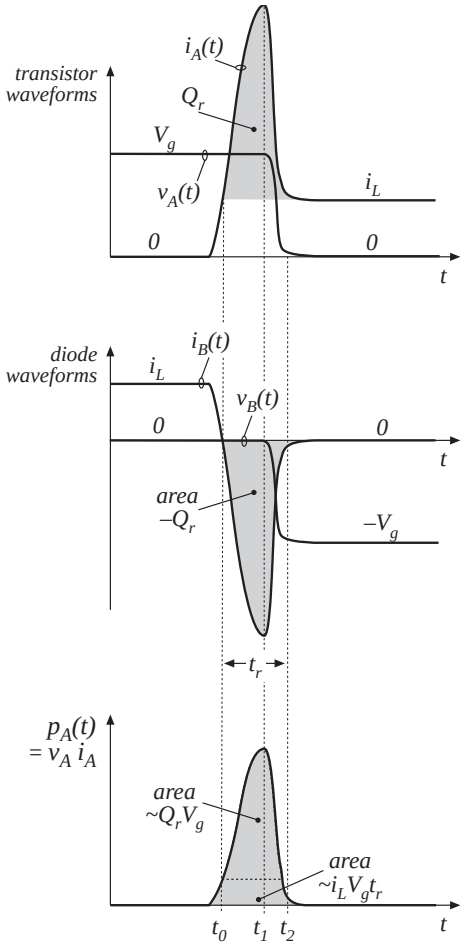
Transformer isolation

Switch realization: semiconductor devices

The IGBT



Switching loss

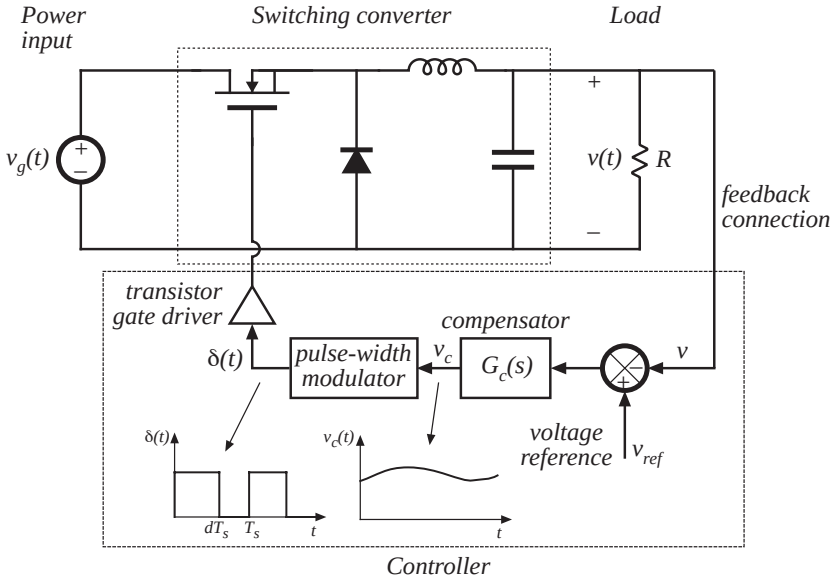


Part I. Converters in equilibrium

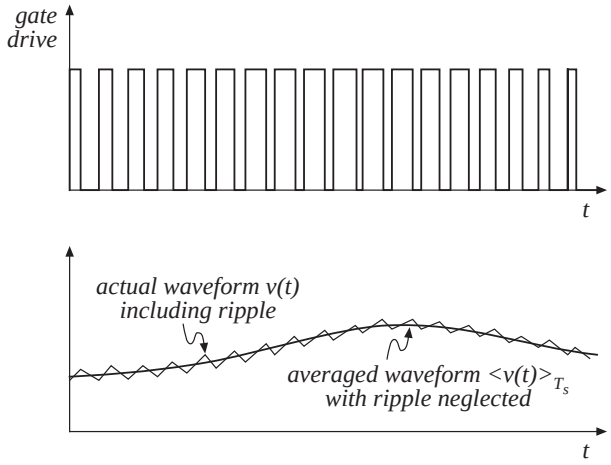
2. Principles of steady state converter analysis
3. Steady-state equivalent circuit modeling, losses, and efficiency
4. Switch realization
5. The discontinuous conduction mode
6. Converter circuits

Part II. Converter dynamics and control

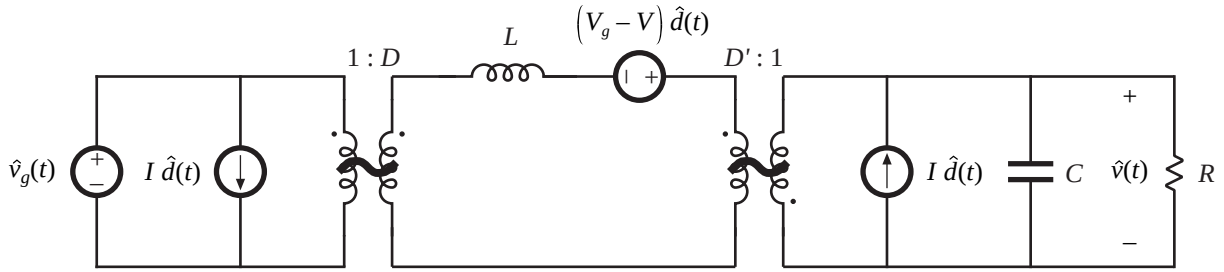
Closed-loop converter system



Averaging the waveforms



Small-signal averaged equivalent circuit

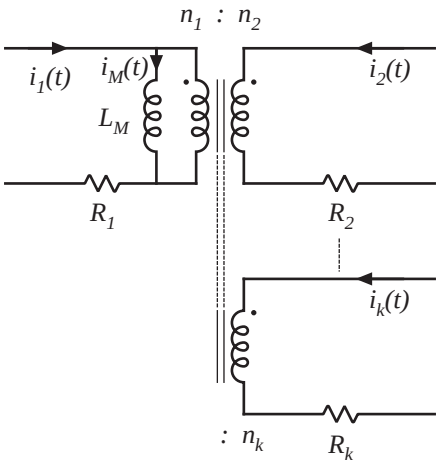


Part II. Converter dynamics and control

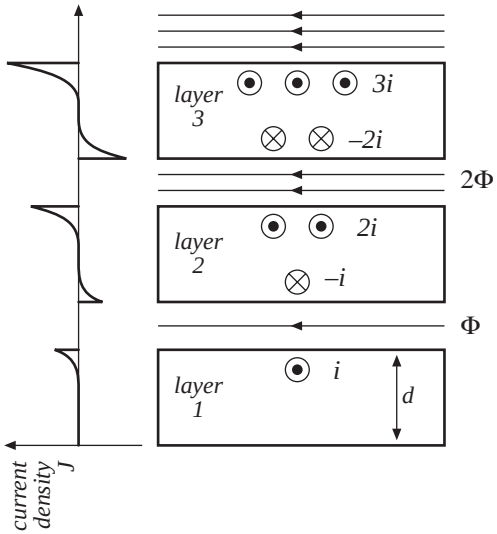
7. Ac modeling
8. Converter transfer functions
9. Controller design
10. Input filter design
11. Ac and dc equivalent circuit modeling of the discontinuous conduction mode
12. Current-programmed control

Part III. Magnetics

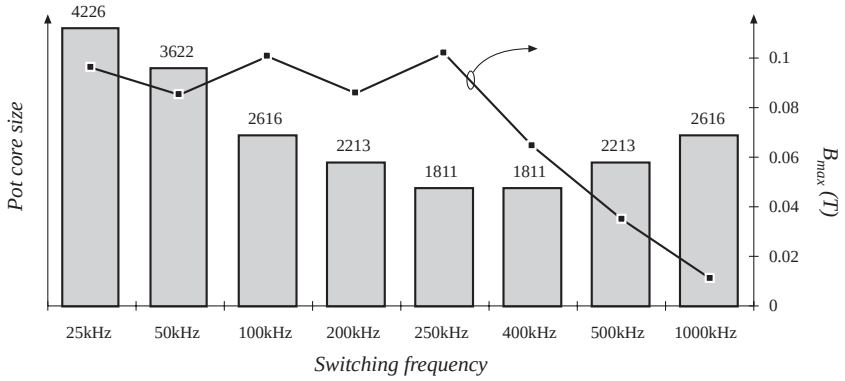
transformer design



the proximity effect



transformer size vs. switching frequency

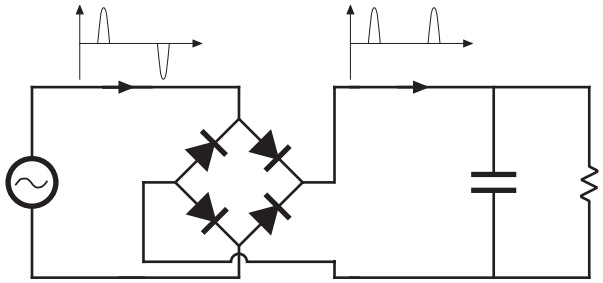


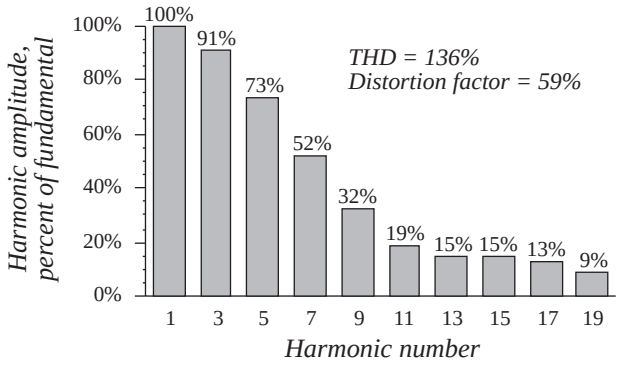
Part III. Magnetics

13. Basic magnetics theory
14. Inductor design
15. Transformer design

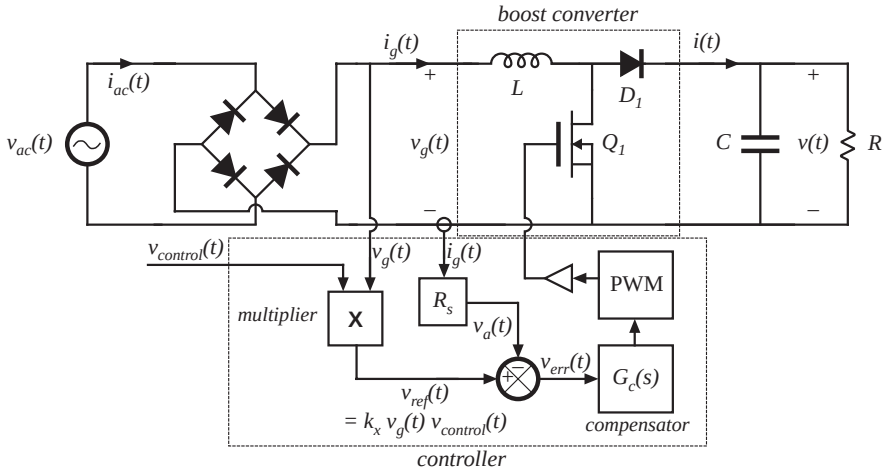
Part IV. Modern rectifiers,
and power system harmonics

Pollution of power system by rectifier current harmonics

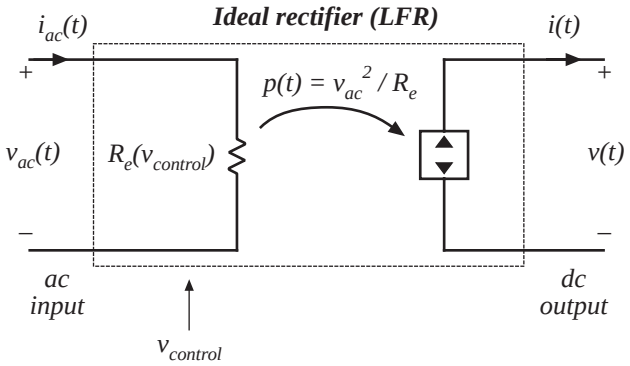




A low-harmonic rectifier system



Model of the ideal rectifier

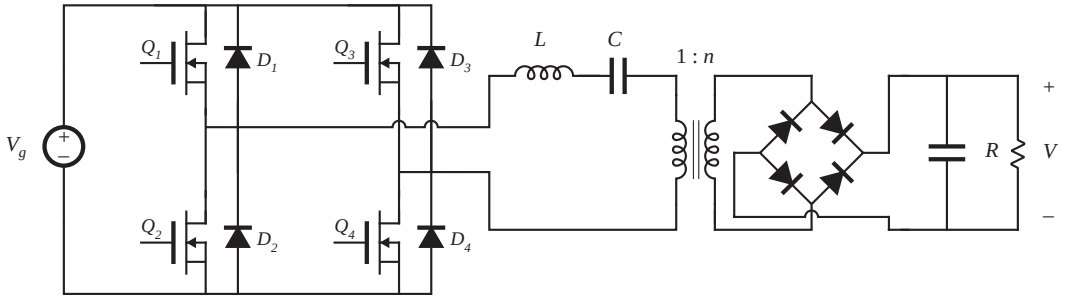


Part IV. Modern rectifiers,
and power system harmonics

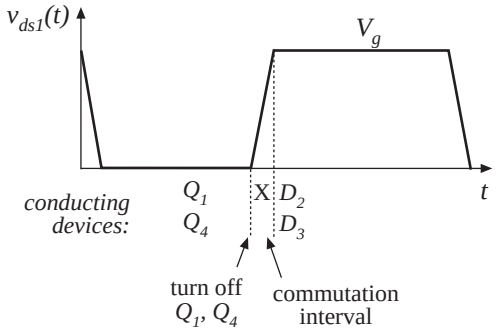
16. Power and harmonics in nonsinusoidal systems
17. Line-commutated rectifiers
18. Pulse-width modulated rectifiers

Part V. Resonant converters

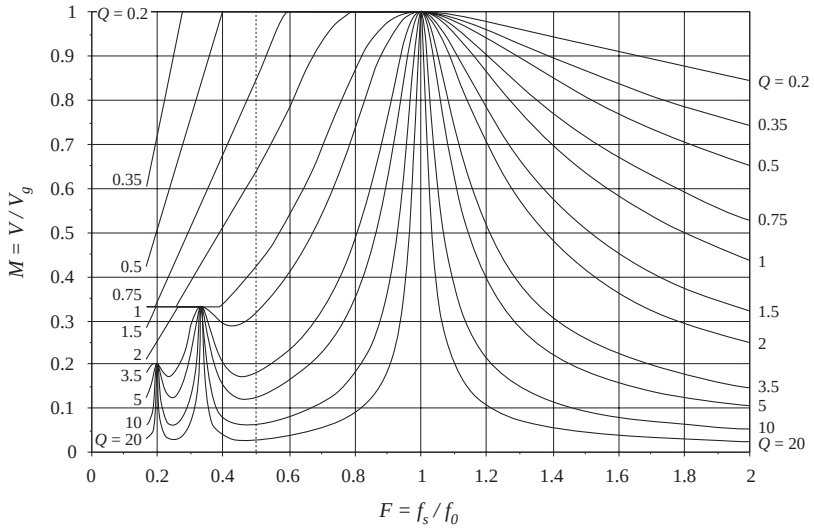
The series resonant converter



Zero voltage switching



Dc characteristics

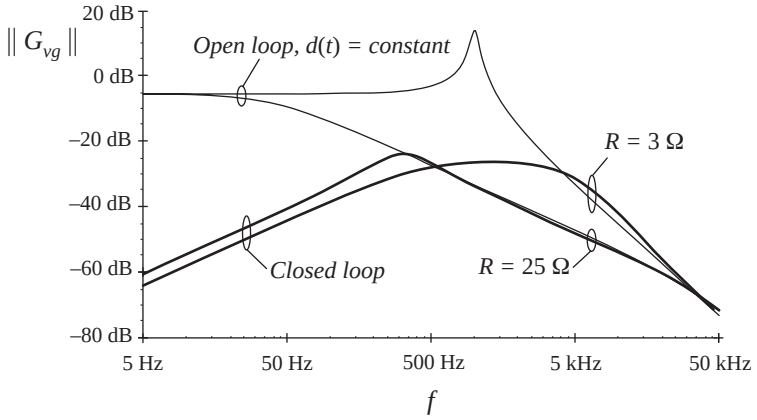


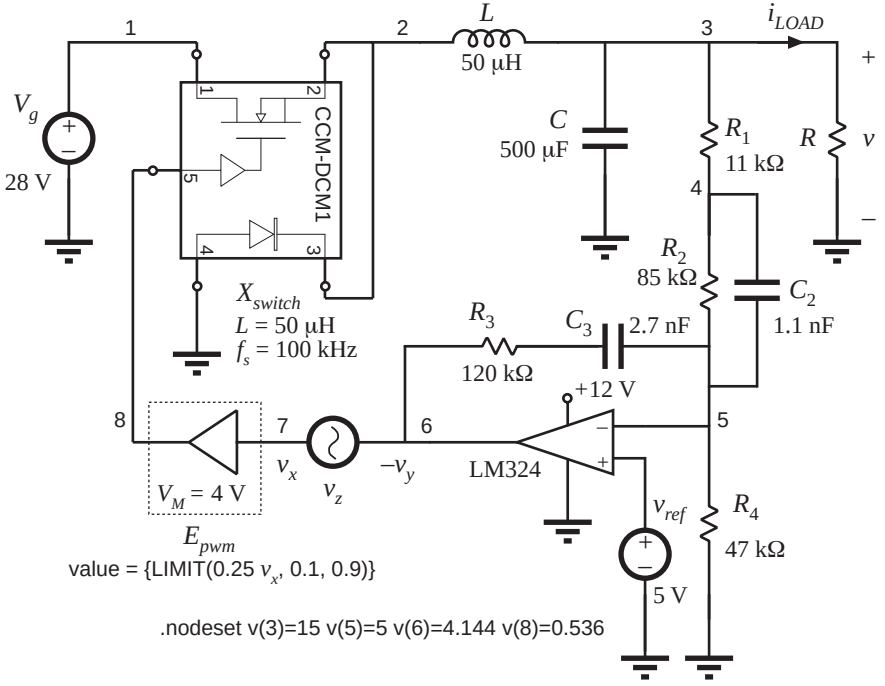
Part V. Resonant converters

19. Resonant conversion
20. Soft switching

Appendices

A. RMS values of commonly-observed converter waveforms
B. Simulation of converters
C. Middlebrook's extra element theorem
D. Magnetics design tables





Chapter 2
Principles of Steady-State Converter Analysis

2.1. Introduction

2.2. Inductor volt-second balance, capacitor charge balance, and the small ripple approximation

2.3. Boost converter example

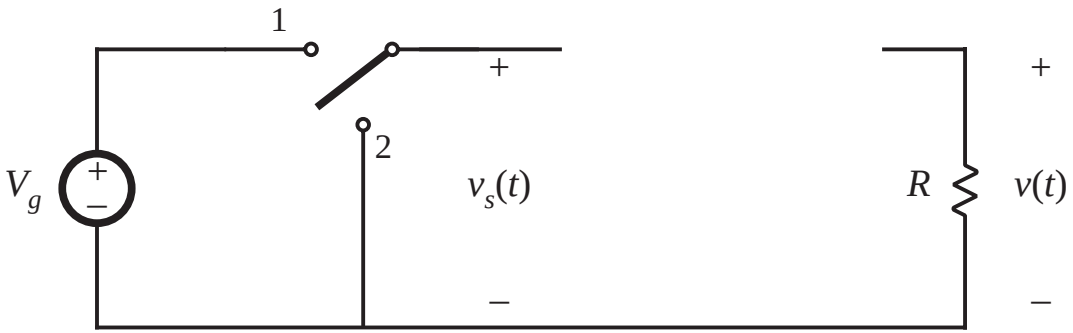
2.4. Cuk converter example

2.5. Estimating the ripple in converters containing two-pole low-pass filters

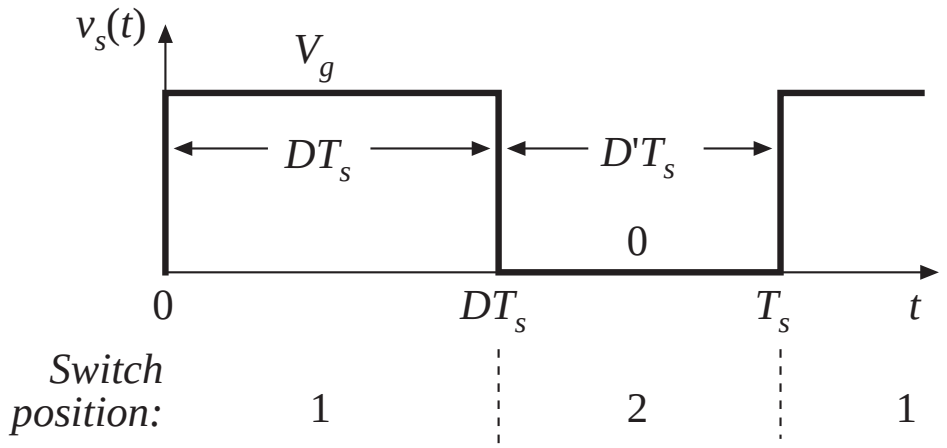
2.6. Summary of key points

2.1 Introduction
Buck converter

SPDT switch changes dc component



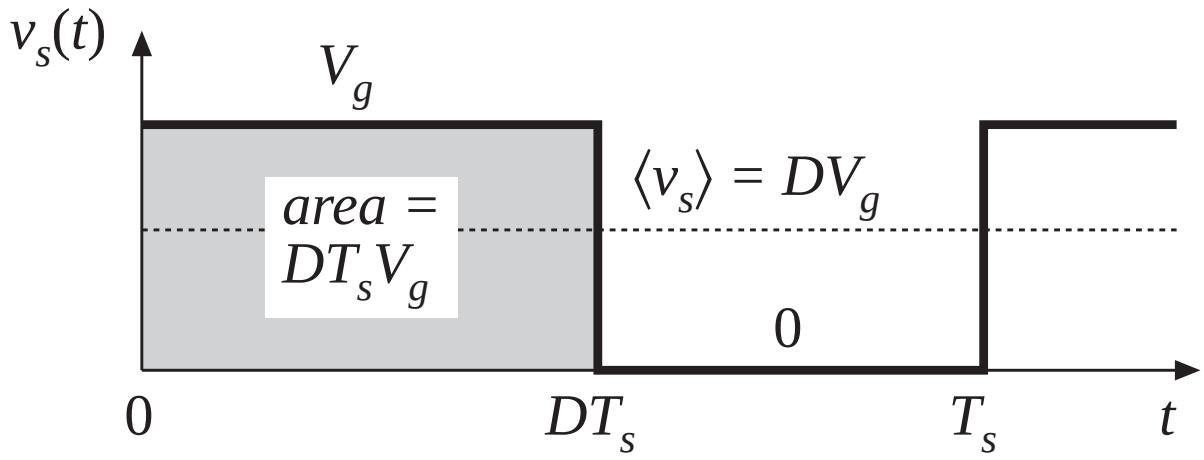
Switch output voltage waveform



Duty cycle *D:*
$0 \le D \le 1$

complement D′:
$D' = 1 - D$

Dc component of switch output voltage

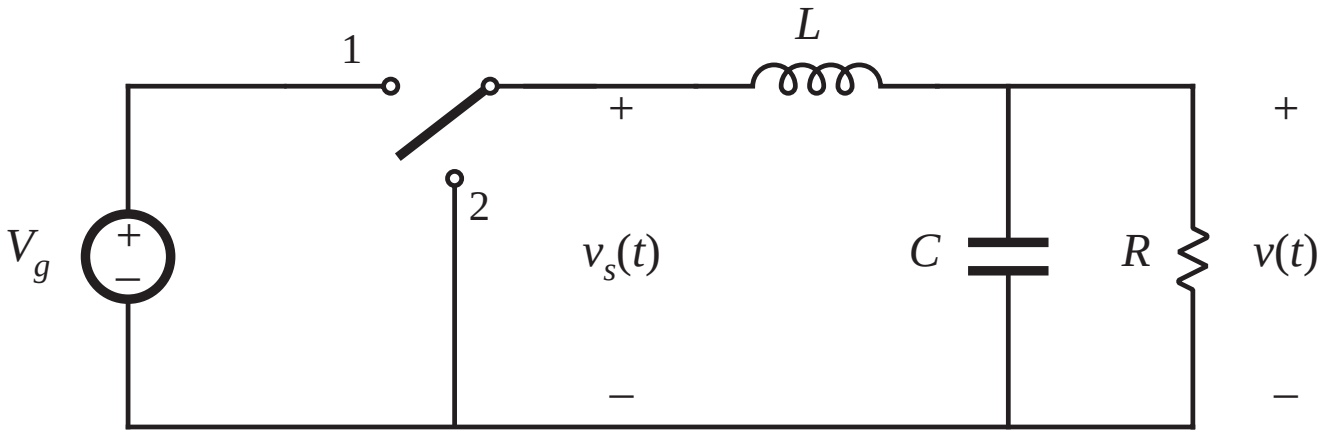


Fourier analysis: Dc component = average value

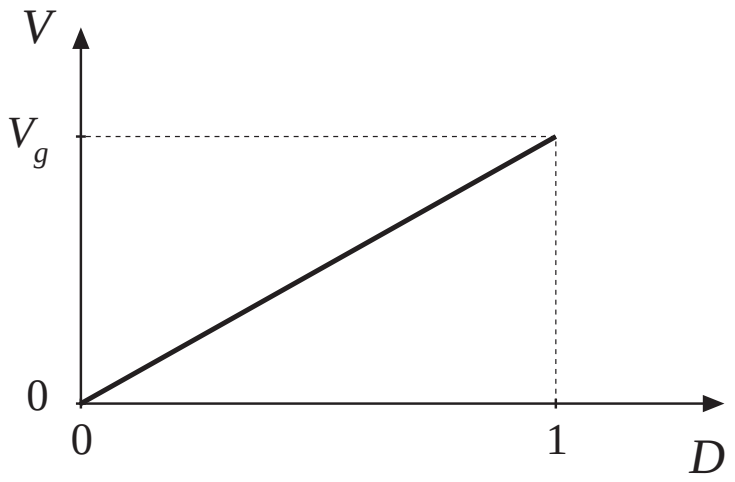
$$\langle v_s \rangle = \frac{1}{T_s} \int_0^{T_s} v_s(t)\, dt$$

$$\langle v_s \rangle = \frac{1}{T_s} (DT_sV_g) = DV_g$$

Insertion of low-pass filter to remove switching harmonics and pass only dc component

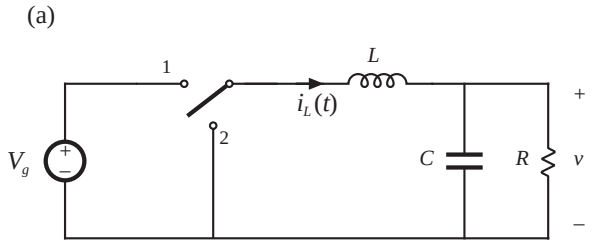


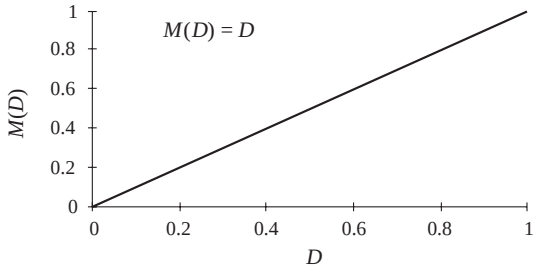
$$v \approx \langle v_s \rangle = DV_g$$



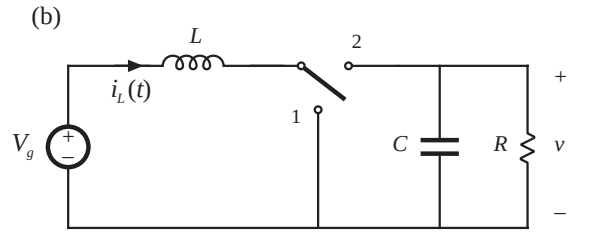
Three basic dc-dc converters

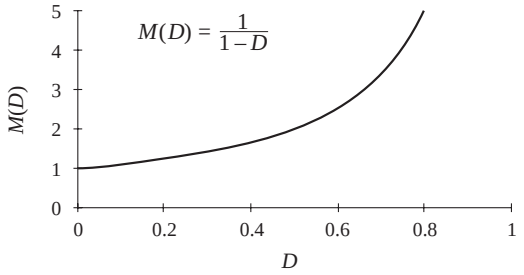
Buck



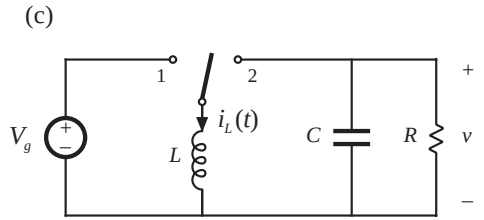


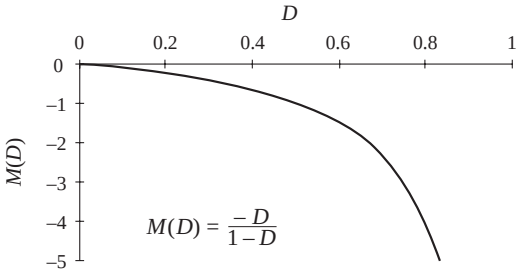
Boost





Buck-boost





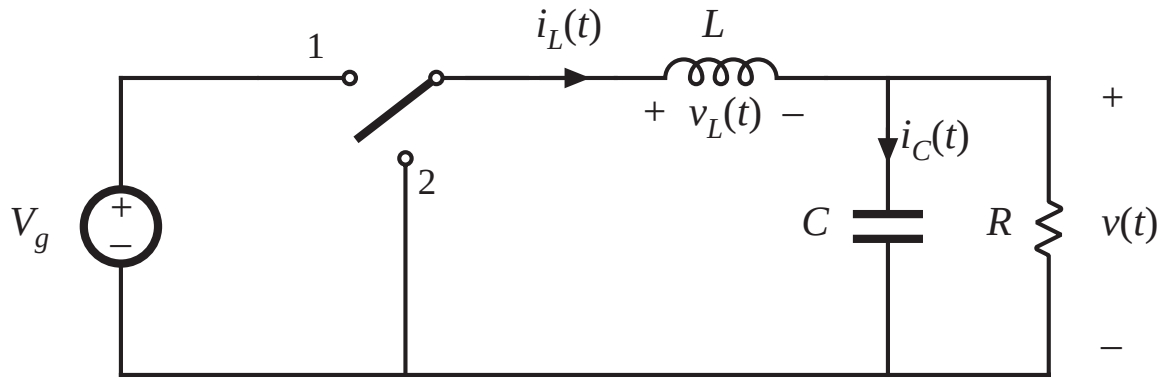
Objectives of this chapter

- Develop techniques for easily determining output voltage of an arbitrary converter circuit
- Derive the principles of *inductor volt-second balance* and *capacitor charge (amp-second) balance*
- Introduce the key *small ripple approximation*
- Develop simple methods for selecting filter element values
- Illustrate via examples

2.2. Inductor volt-second balance, capacitor charge balance, and the small ripple approximation

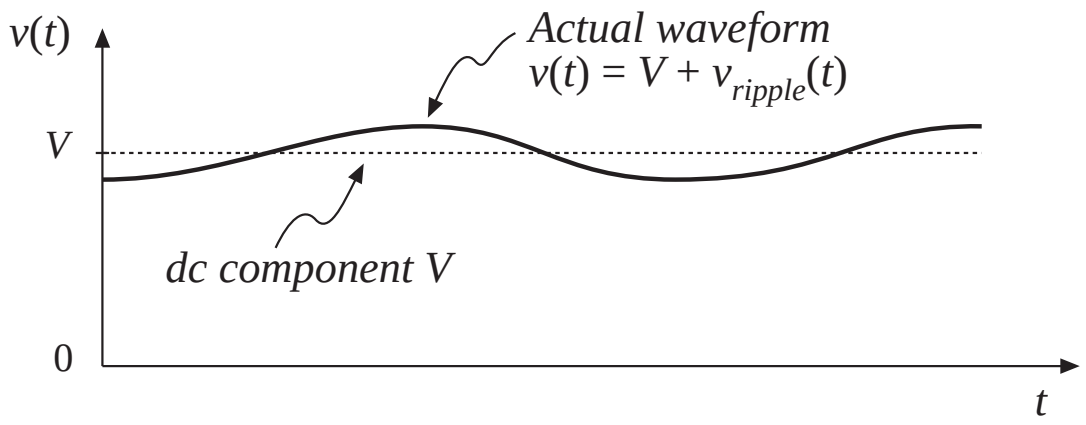
Actual output voltage waveform, buck converter

Buck converter containing practical low-pass filter



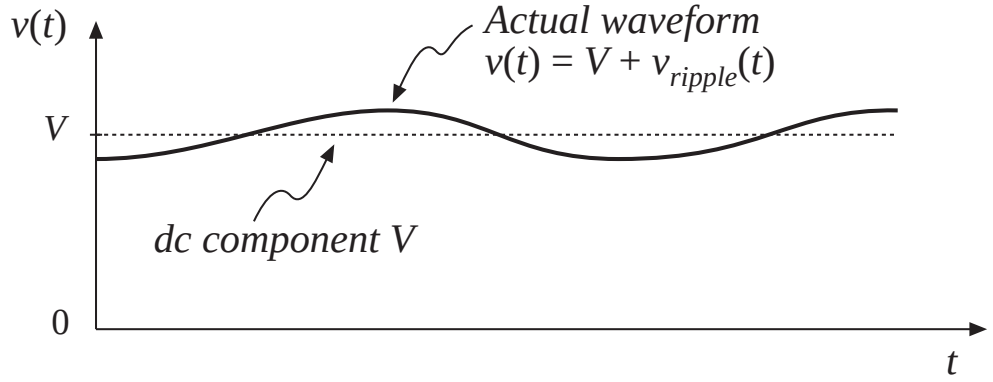
Actual output voltage waveform

$$v(t) = V + v_{ripple}(t)$$



The small ripple approximation

$$v(t) = V + v_{ripple}(t)$$

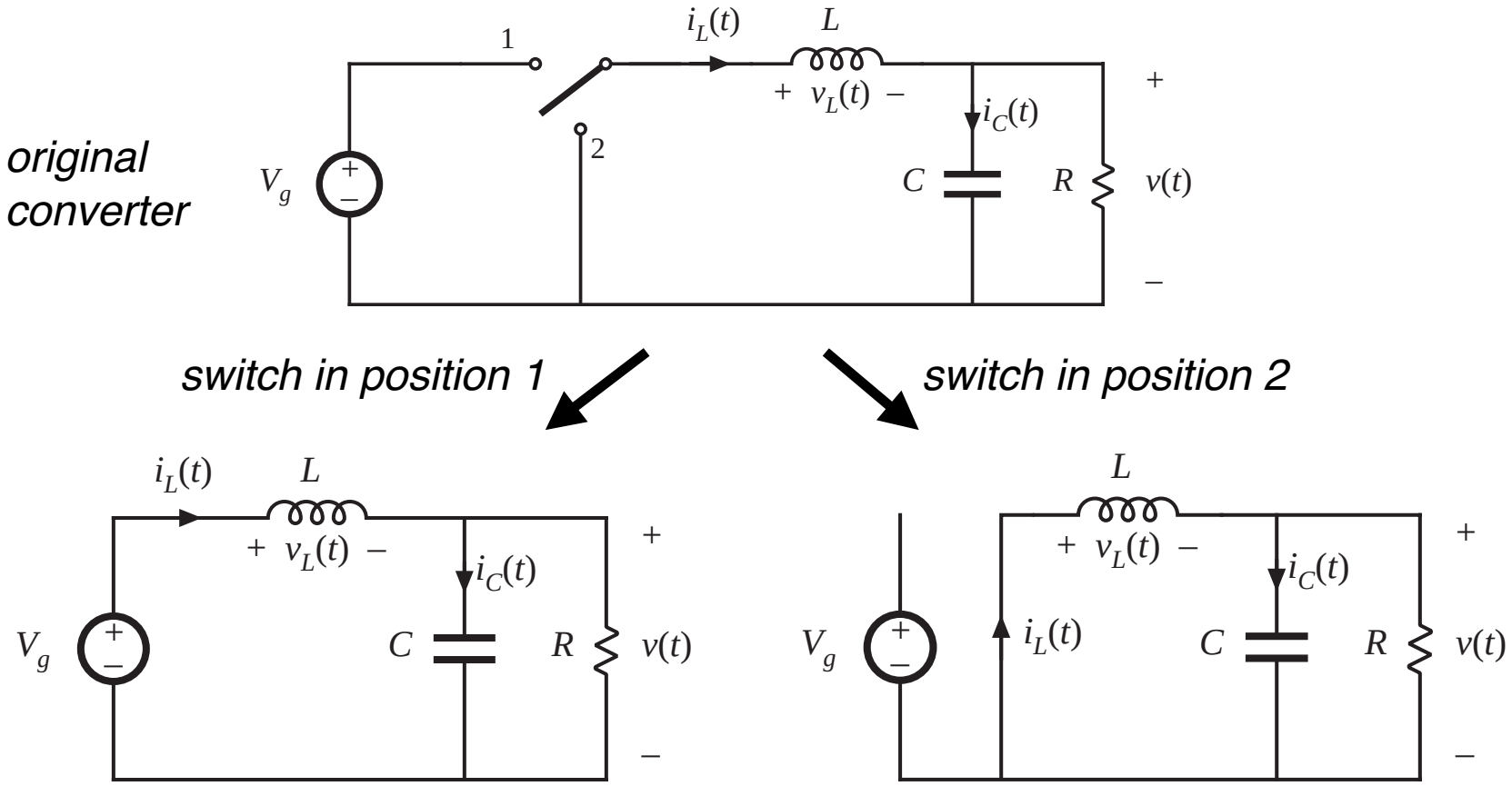


In a well-designed converter, the output voltage ripple is small. Hence, the waveforms can be easily determined by ignoring the ripple:

$$\left\| v_{ripple} \right\| \ll V$$

$$v(t) \approx V$$

Buck converter analysis: inductor current waveform



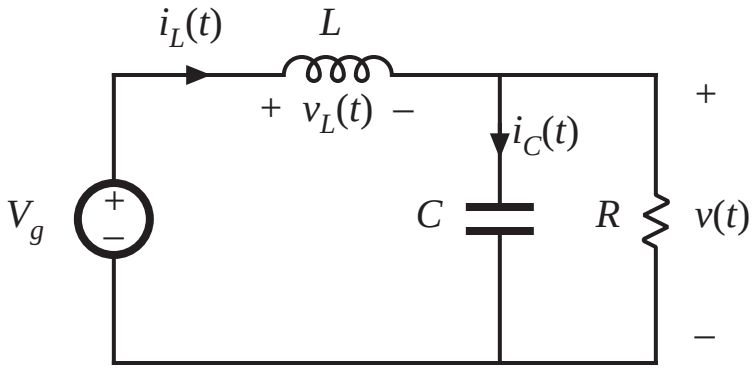
Inductor voltage and current
Subinterval 1: switch in position 1

Inductor voltage

$$v_L = V_g - v(t)$$

Small ripple approximation:

$$v_L \approx V_g - V$$



Knowing the inductor voltage, we can now find the inductor current via

$$v_L(t) = L \frac{di_L(t)}{dt}$$

Solve for the slope:

$$\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} \approx \frac{V_g - V}{L}$$

$\Rightarrow$ *The inductor current changes with an essentially constant slope*

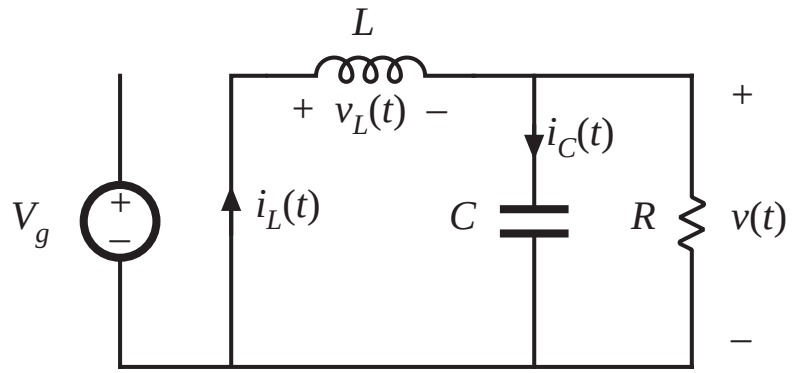
Inductor voltage and current
Subinterval 2: switch in position 2

Inductor voltage

$$v_L(t) = -v(t)$$

Small ripple approximation:

$$v_L(t) \approx -V$$



Knowing the inductor voltage, we can again find the inductor current via

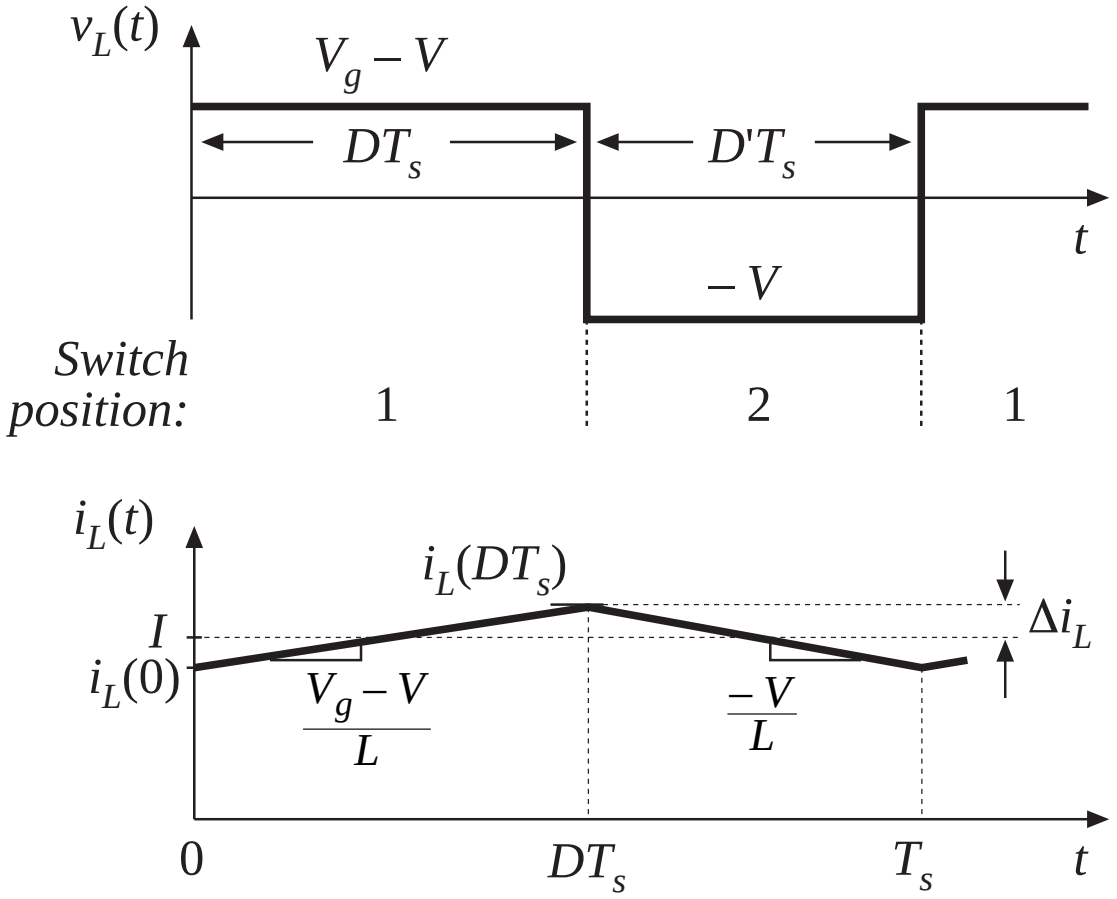
$$v_L(t) = L \frac{di_L(t)}{dt}$$

Solve for the slope:

$$\frac{di_L(t)}{dt} \approx -\frac{V}{L}$$

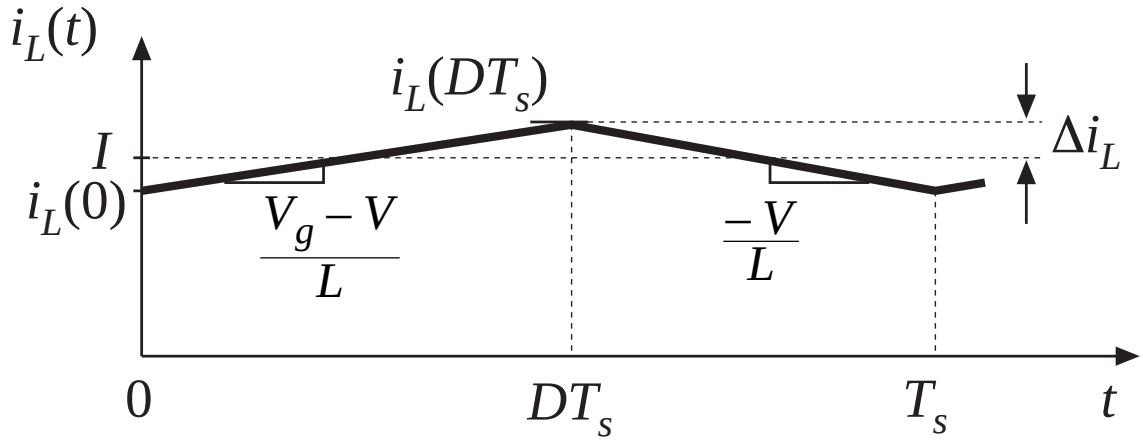
⇒ *The inductor current changes with an essentially constant slope*

Inductor voltage and current waveforms



$$v_L(t) = L \frac{di_L(t)}{dt}$$

Determination of inductor current ripple magnitude

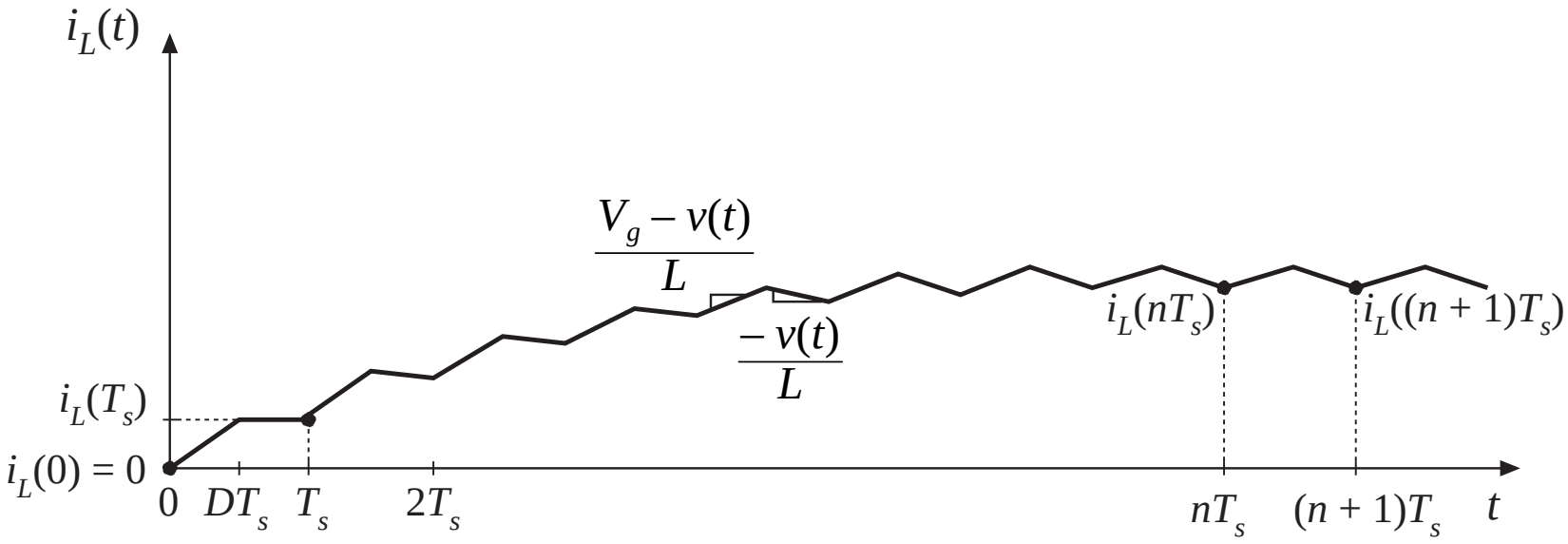


(*change in* i_L) = (*slope*)(*length of subinterval*)

$$\left(2\Delta i_L\right) = \left(\frac{V_g - V}{L}\right)\left(DT_s\right)$$

$$\Rightarrow \qquad \Delta i_L = \frac{V_g - V}{2L} DT_s \qquad\qquad L = \frac{V_g - V}{2\Delta i_L} DT_s$$

Inductor current waveform during turn-on transient



When the converter operates in equilibrium:

$$i_L((n+1)T_s) = i_L(nT_s)$$

The principle of inductor volt-second balance: Derivation

Inductor defining relation:

$$v_L(t) = L \frac{di_L(t)}{dt}$$

Integrate over one complete switching period:

$$i_L(T_s) - i_L(0) = \frac{1}{L} \int_0^{T_s} v_L(t)\, dt$$

In periodic steady state, the net change in inductor current is zero:

$$0 = \int_0^{T_s} v_L(t)\, dt$$

Hence, the total area (or volt-seconds) under the inductor voltage waveform is zero whenever the converter operates in steady state.

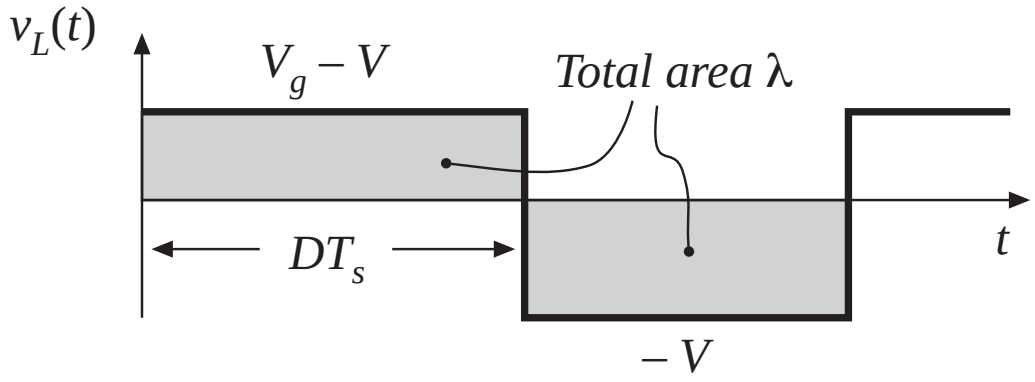
An equivalent form:

$$0 = \frac{1}{T_s} \int_0^{T_s} v_L(t)\, dt = \left\langle v_L \right\rangle$$

The average inductor voltage is zero in steady state.

Inductor volt-second balance: Buck converter example

Inductor voltage waveform, previously derived:



Integral of voltage waveform is area of rectangles:

$$\lambda = \int_0^{T_s} v_L(t)\, dt = (V_g - V)(DT_s) + (-V)(D'T_s)$$

Average voltage is

$$\langle v_L \rangle = \frac{\lambda}{T_s} = D(V_g - V) + D'(-V)$$

Equate to zero and solve for *V:*

$$0 = DV_g - (D + D')V = DV_g - V \qquad \Rightarrow \qquad V = DV_g$$

The principle of capacitor charge balance: Derivation

Capacitor defining relation:

$$i_C(t) = C \frac{dv_C(t)}{dt}$$

Integrate over one complete switching period:

$$v_C(T_s) - v_C(0) = \frac{1}{C} \int_0^{T_s} i_C(t)\, dt$$

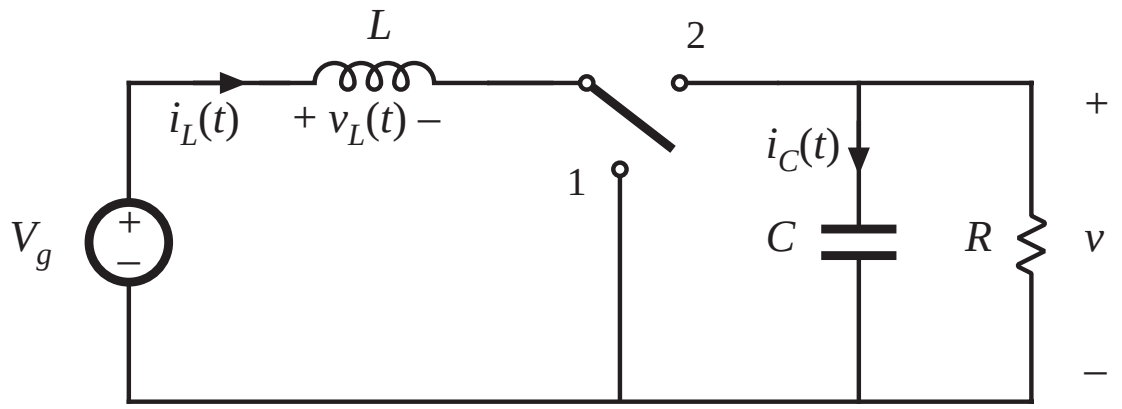
In periodic steady state, the net change in capacitor voltage is zero:

$$0 = \frac{1}{T_s} \int_0^{T_s} i_C(t)\, dt = \left\langle i_C \right\rangle$$

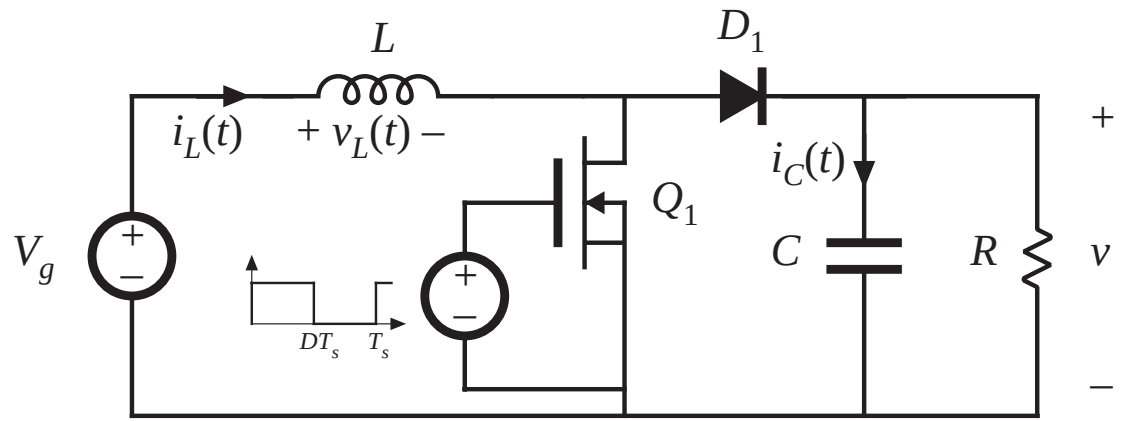
Hence, the total area (or charge) under the capacitor current waveform is zero whenever the converter operates in steady state. The average capacitor current is then zero.

2.3 Boost converter example

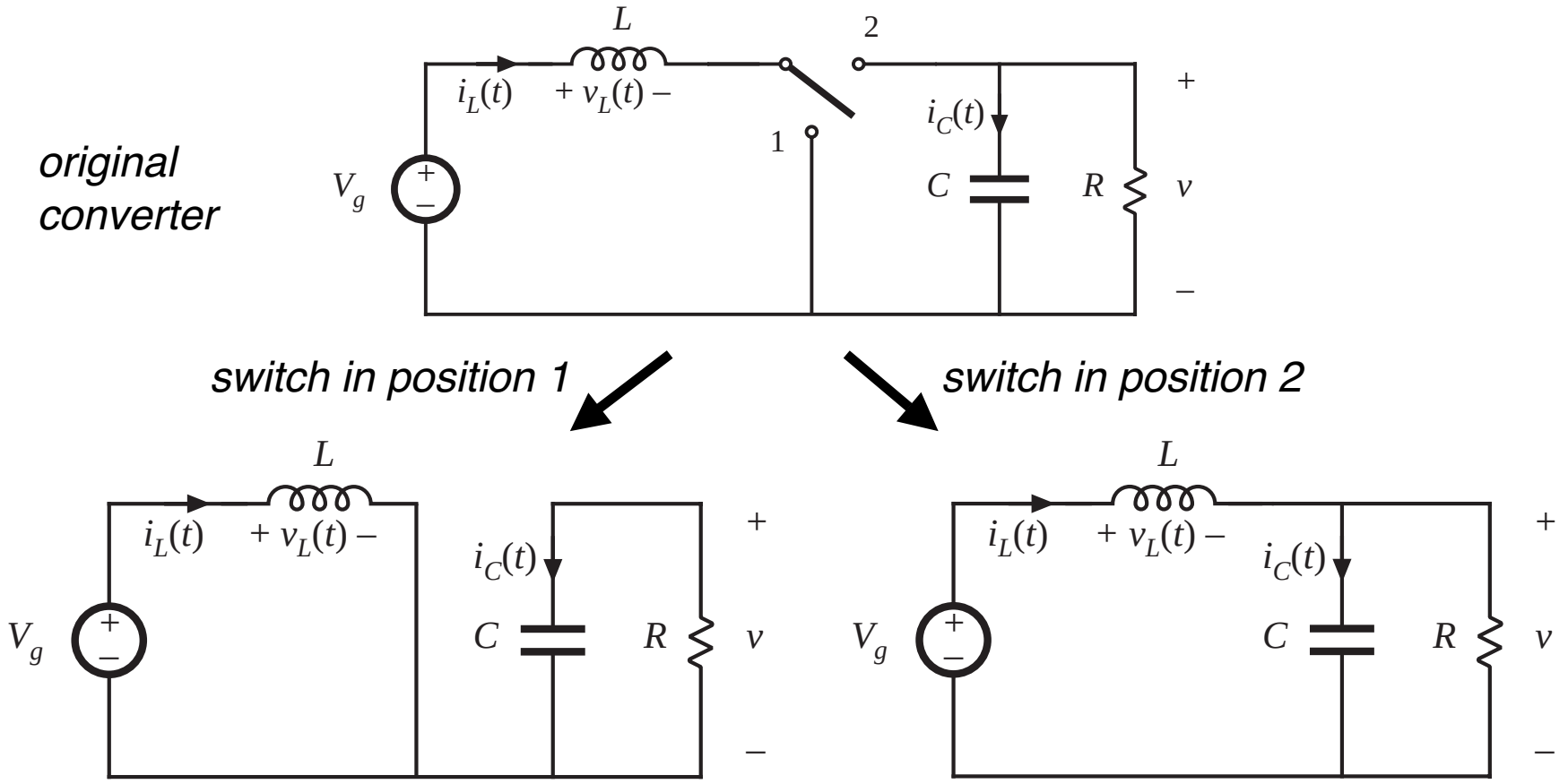
Boost converter with ideal switch



Realization using power MOSFET and diode



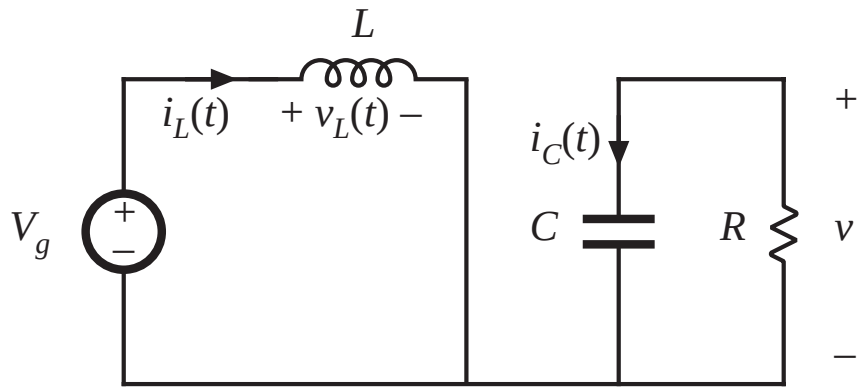
Boost converter analysis



Subinterval 1: switch in position 1

Inductor voltage and capacitor current

$$v_L = V_g$$
$$i_C = -v / R$$



Small ripple approximation:

$$v_L = V_g$$
$$i_C = -V / R$$

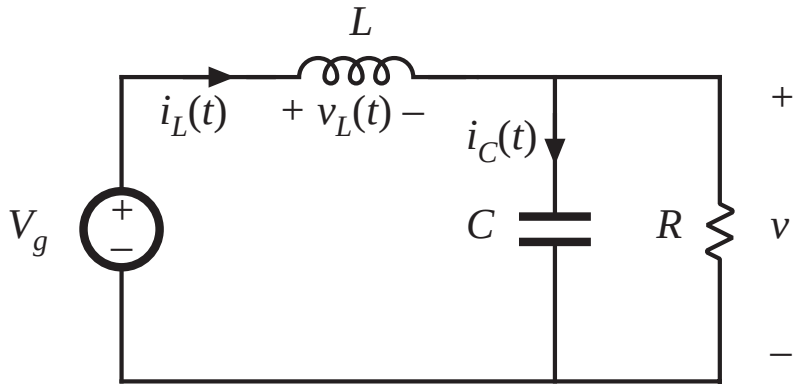
Subinterval 2: switch in position 2

Inductor voltage and capacitor current

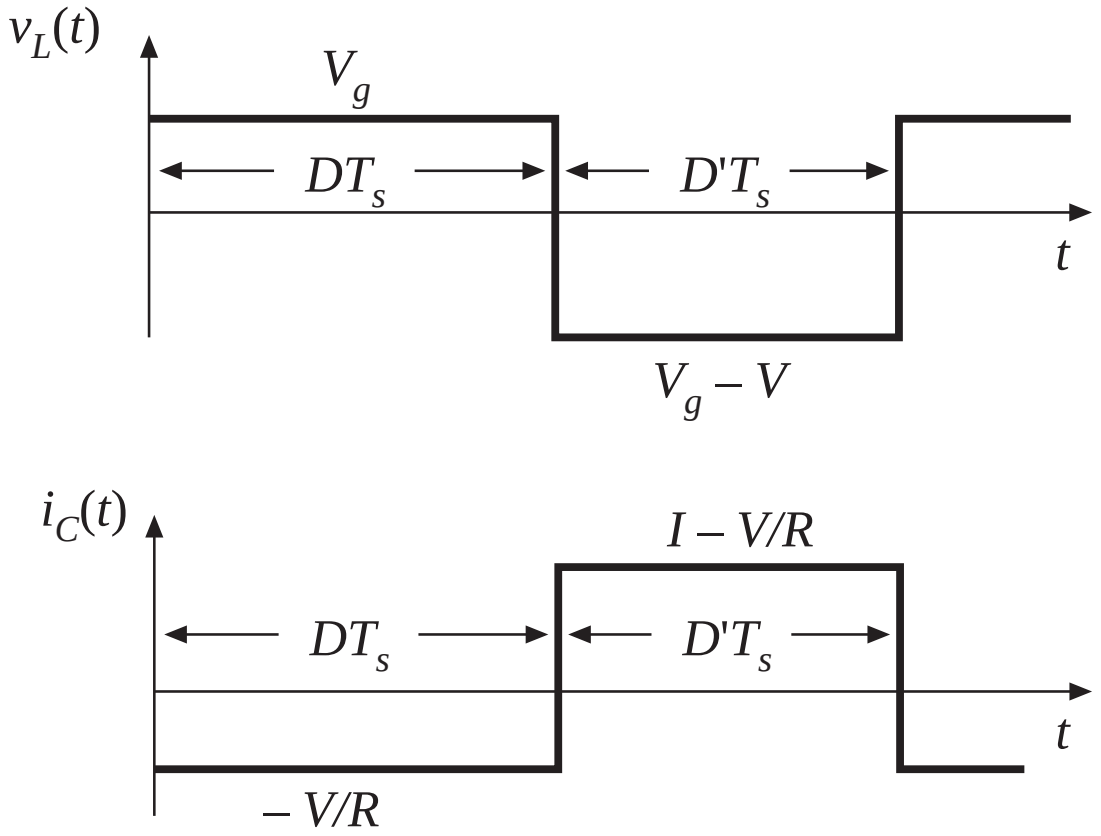
$$v_L = V_g - v$$
$$i_C = i_L - v / R$$

Small ripple approximation:

$$v_L = V_g - V$$
$$i_C = I - V / R$$



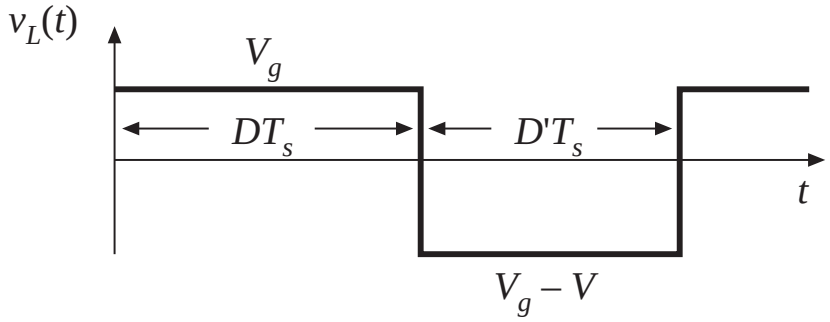
Inductor voltage and capacitor current waveforms



Inductor volt-second balance

Net volt-seconds applied to inductor over one switching period:

$$\int_0^{T_s} v_L(t)\, dt = (V_g)\, DT_s + (V_g - V)\, D'T_s$$



Equate to zero and collect terms:

$$V_g\,(D + D') - V\,D' = 0$$

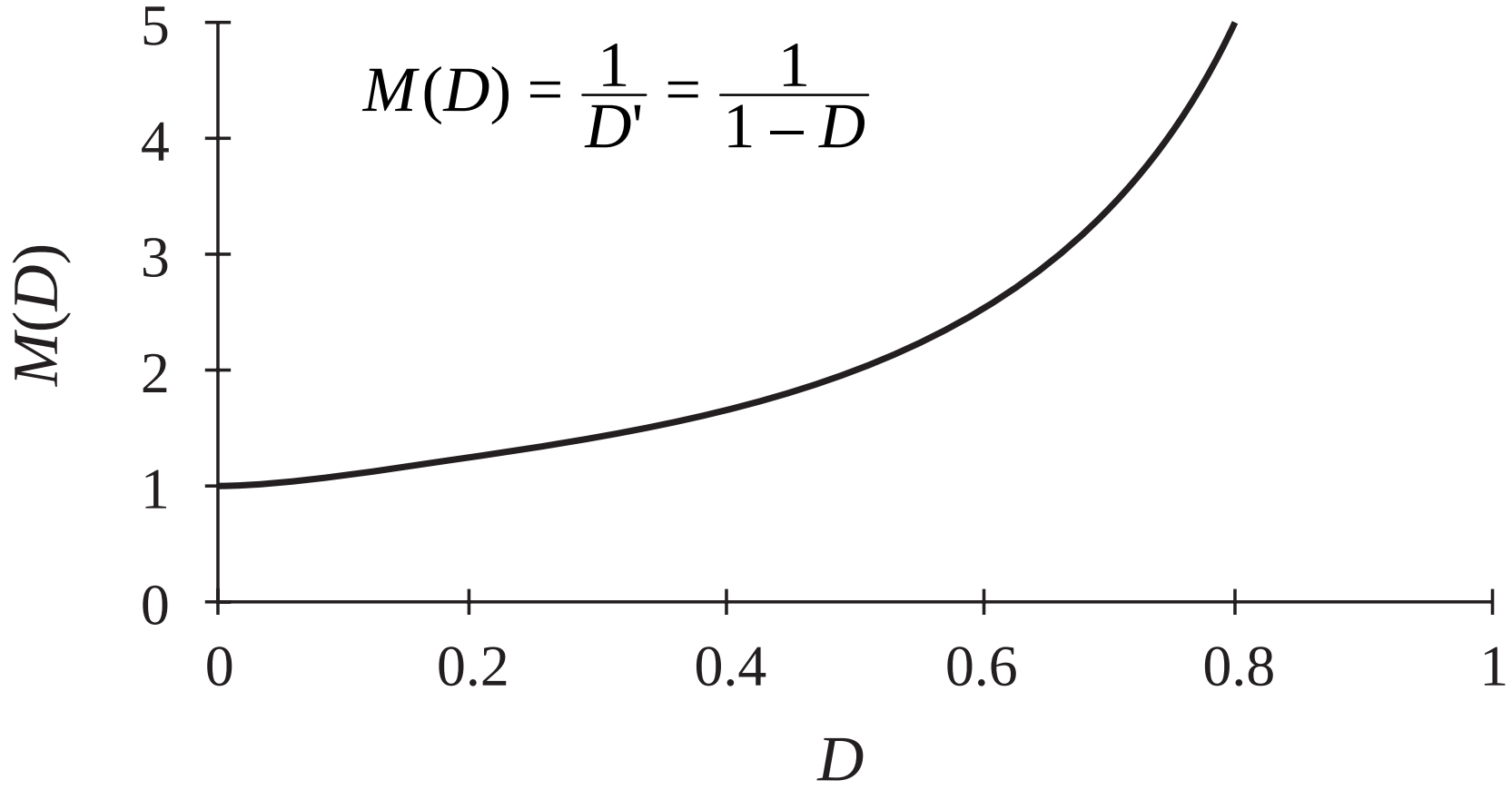
Solve for V:

$$V = \frac{V_g}{D'}$$

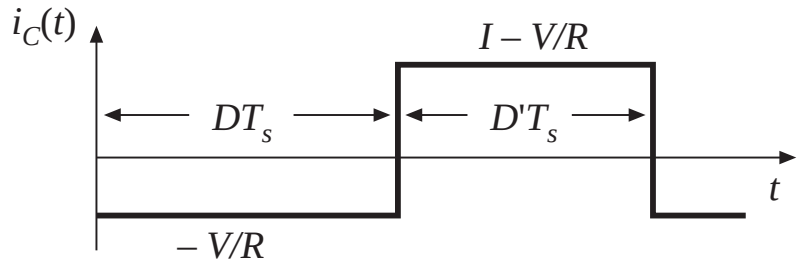
The voltage conversion ratio is therefore

$$M(D) = \frac{V}{V_g} = \frac{1}{D'} = \frac{1}{1 - D}$$

Conversion ratio *M(D)* of the boost converter



Determination of inductor current dc component



Capacitor charge balance:

$$\int_0^{T_s} i_C(t)\,dt = \left(-\frac{V}{R}\right) DT_s + \left(I - \frac{V}{R}\right) D'T_s$$

Collect terms and equate to zero:

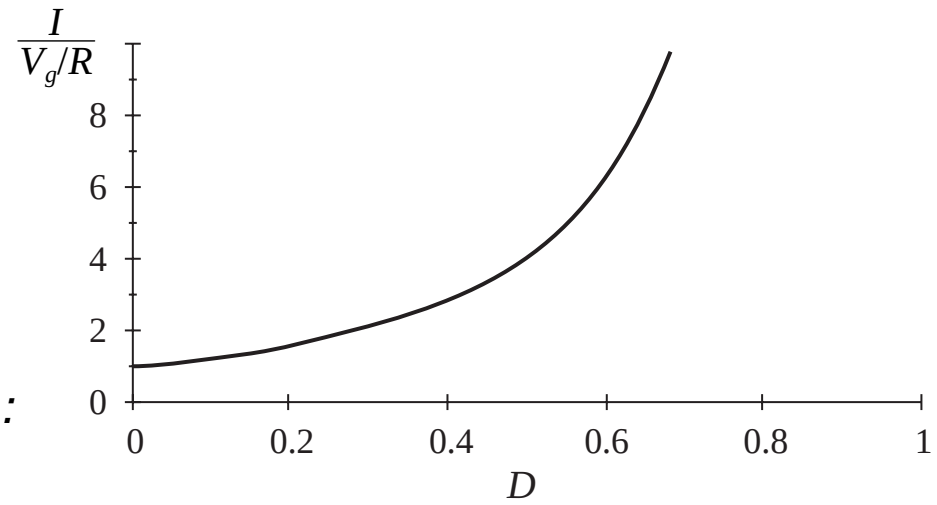
$$-\frac{V}{R}\left(D + D'\right) + I\,D' = 0$$

Solve for I:

$$I = \frac{V}{D'\,R}$$

Eliminate V to express in terms of V_g:

$$I = \frac{V_g}{D'^2\,R}$$



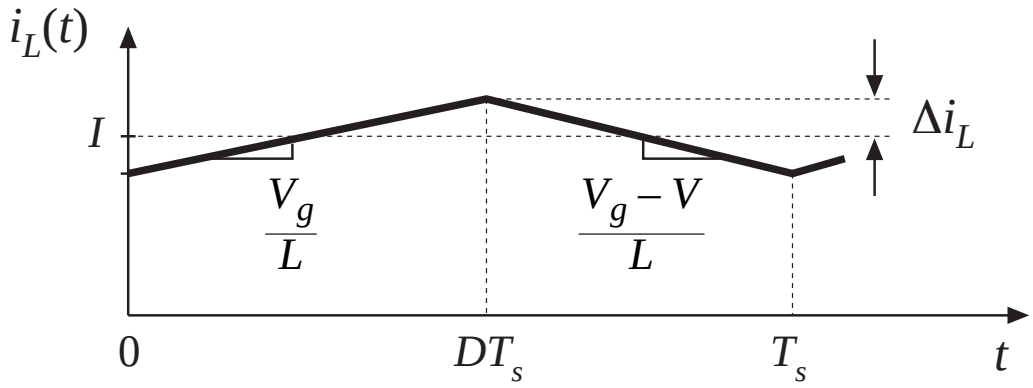
Determination of inductor current ripple

Inductor current slope during subinterval 1:

$$\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} = \frac{V_g}{L}$$

Inductor current slope during subinterval 2:

$$\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} = \frac{V_g - V}{L}$$



Change in inductor current during subinterval 1 is *(slope) (length of subinterval):*

$$2\Delta i_L = \frac{V_g}{L} DT_s$$

Solve for peak ripple:

$$\Delta i_L = \frac{V_g}{2L} DT_s$$

- Choose *L* such that desired ripple magnitude is obtained

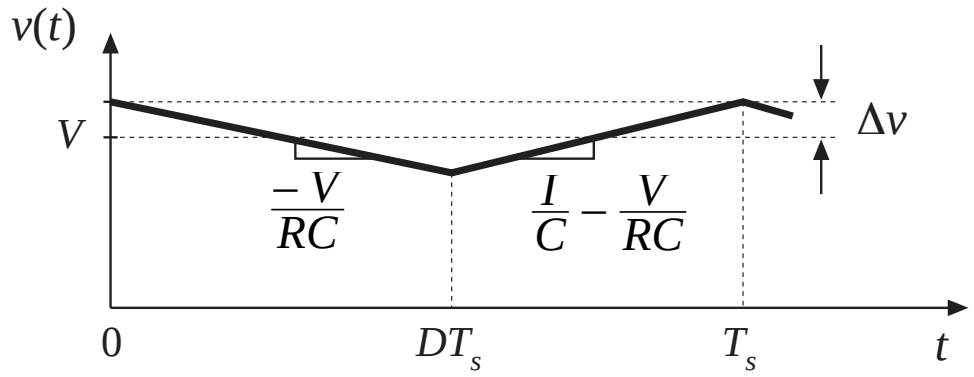
Determination of capacitor voltage ripple

Capacitor voltage slope during subinterval 1:

$$\frac{dv_C(t)}{dt} = \frac{i_C(t)}{C} = \frac{-V}{RC}$$

Capacitor voltage slope during subinterval 2:

$$\frac{dv_C(t)}{dt} = \frac{i_C(t)}{C} = \frac{I}{C} - \frac{V}{RC}$$



Change in capacitor voltage during subinterval 1 is *(slope) (length of subinterval):*

$$-2\Delta v = \frac{-V}{RC} DT_s$$

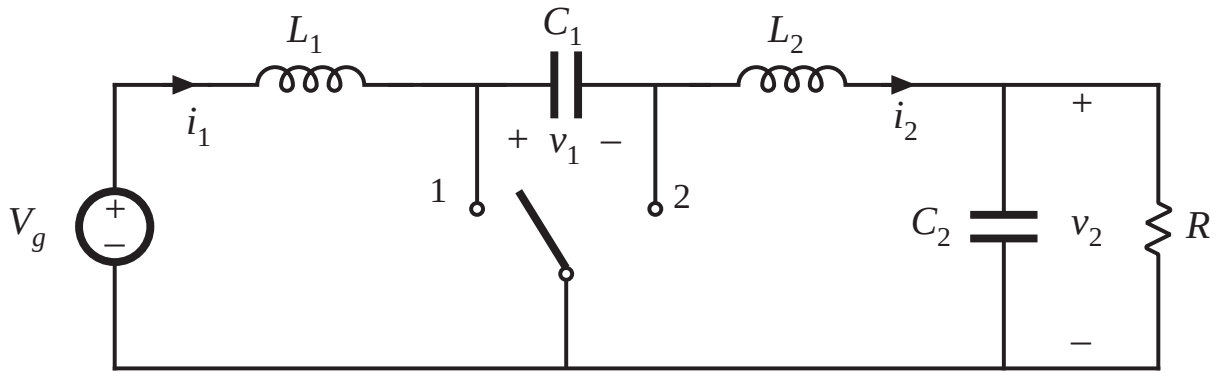
Solve for peak ripple:

$$\Delta v = \frac{V}{2RC} DT_s$$

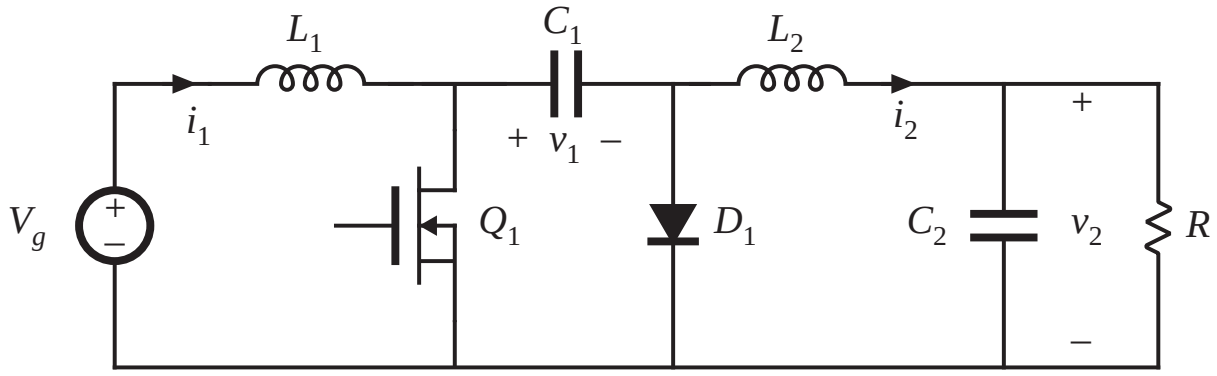
- Choose *C* such that desired voltage ripple magnitude is obtained
- In practice, capacitor *equivalent series resistance* (esr) leads to increased voltage ripple

2.4 Cuk converter example

Cuk converter, with ideal switch



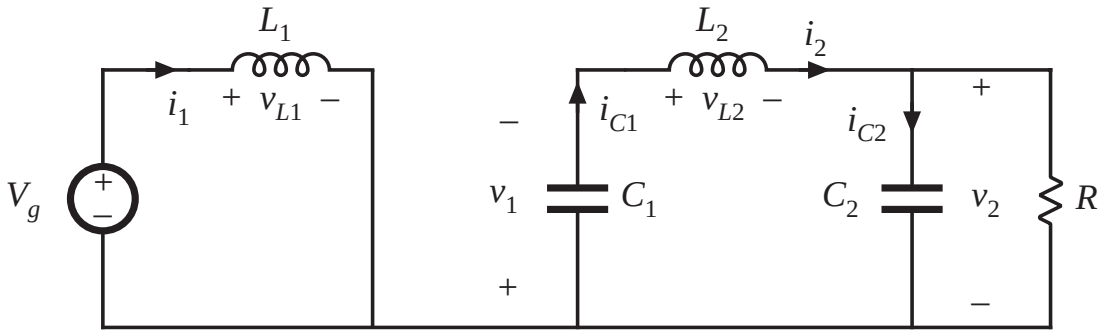
Cuk converter: practical realization using MOSFET and diode



Cuk converter circuit
with switch in positions 1 and 2

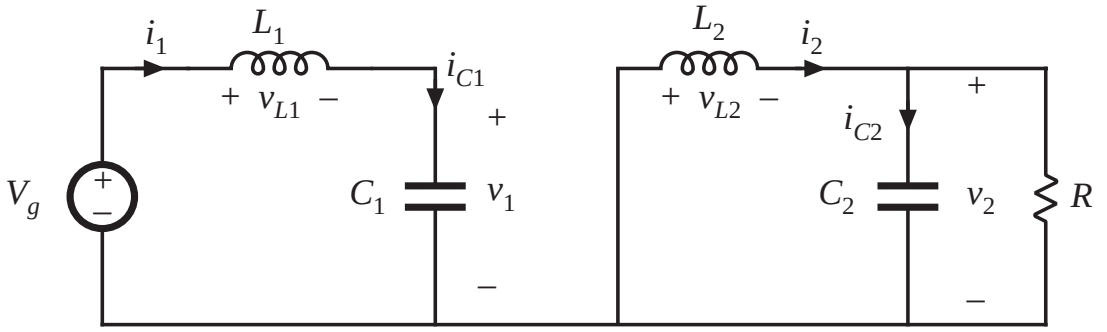
Switch in position 1:
MOSFET conducts

Capacitor C_1 releases energy to output



Switch in position 2:
diode conducts

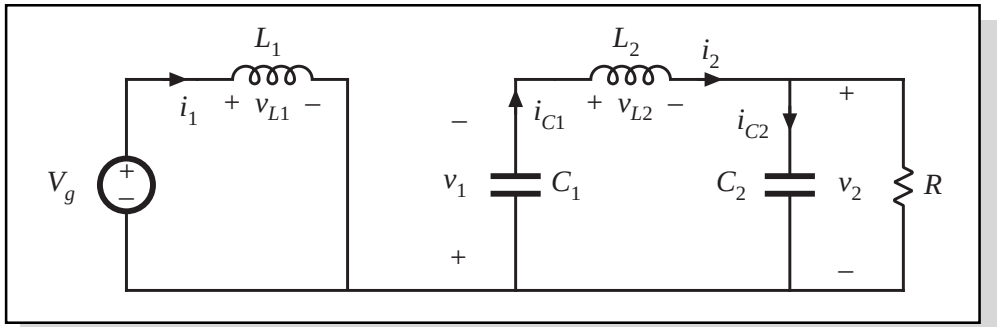
Capacitor C_1 is charged from input



Waveforms during subinterval 1
MOSFET conduction interval

Inductor voltages and capacitor currents:

$$v_{L1} = V_g$$
$$v_{L2} = -v_1 - v_2$$
$$i_{C1} = i_2$$
$$i_{C2} = i_2 - \frac{v_2}{R}$$



Small ripple approximation for subinterval 1:

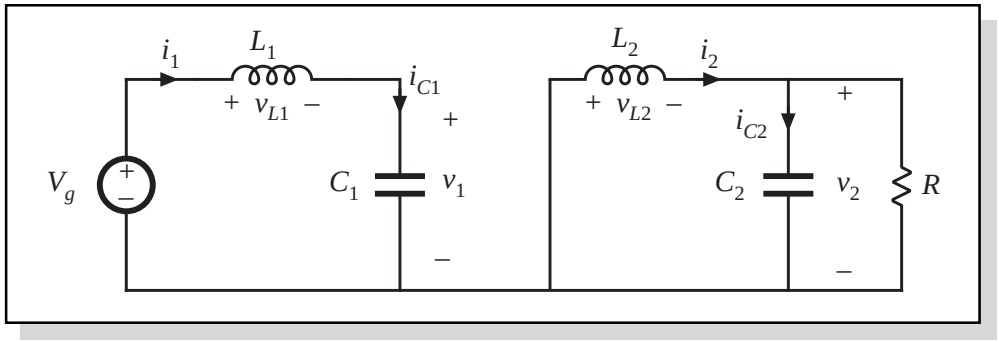
$$v_{L1} = V_g$$
$$v_{L2} = -V_1 - V_2$$
$$i_{C1} = I_2$$
$$i_{C2} = I_2 - \frac{V_2}{R}$$

Waveforms during subinterval 2

Diode conduction interval

Inductor voltages and capacitor currents:

$$v_{L1} = V_g - v_1$$
$$v_{L2} = -v_2$$
$$i_{C1} = i_1$$
$$i_{C2} = i_2 - \frac{v_2}{R}$$



Small ripple approximation for subinterval 2:

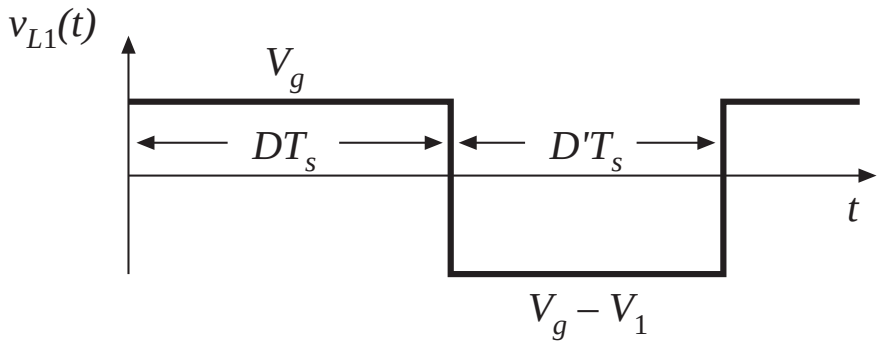
$$v_{L1} = V_g - V_1$$
$$v_{L2} = -V_2$$
$$i_{C1} = I_1$$
$$i_{C2} = I_2 - \frac{V_2}{R}$$

Equate average values to zero

The principles of inductor volt-second and capacitor charge balance state that the average values of the periodic inductor voltage and capacitor current waveforms are zero, when the converter operates in steady state. Hence, to determine the steady-state conditions in the converter, let us sketch the inductor voltage and capacitor current waveforms, and equate their average values to zero.

Waveforms:

Inductor voltage $v_{L1}(t)$

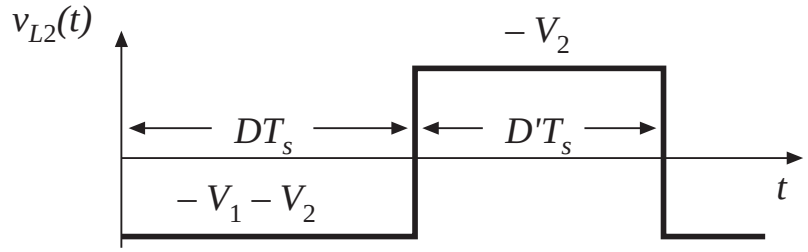


Volt-second balance on L_1:

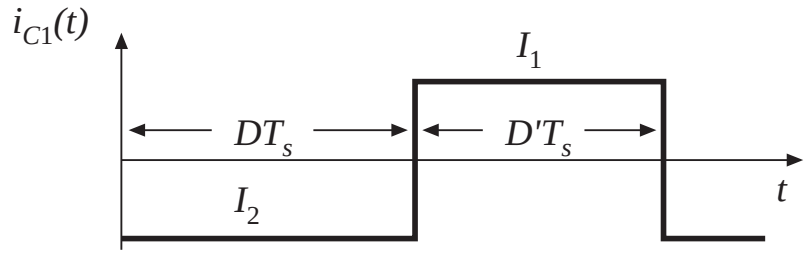
$$\left\langle v_{L1} \right\rangle = DV_g + D'(V_g - V_1) = 0$$

Equate average values to zero

Inductor L_2 voltage



Capacitor C_1 current



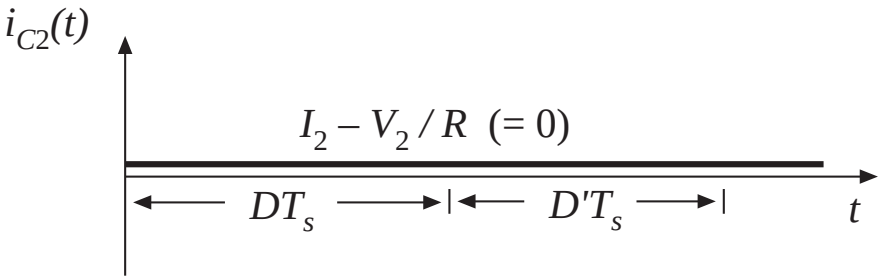
Average the waveforms:

$$\left\langle v_{L2} \right\rangle = D(-V_1 - V_2) + D'(-V_2) = 0$$

$$\left\langle i_{C1} \right\rangle = DI_2 + D'I_1 = 0$$

Equate average values to zero

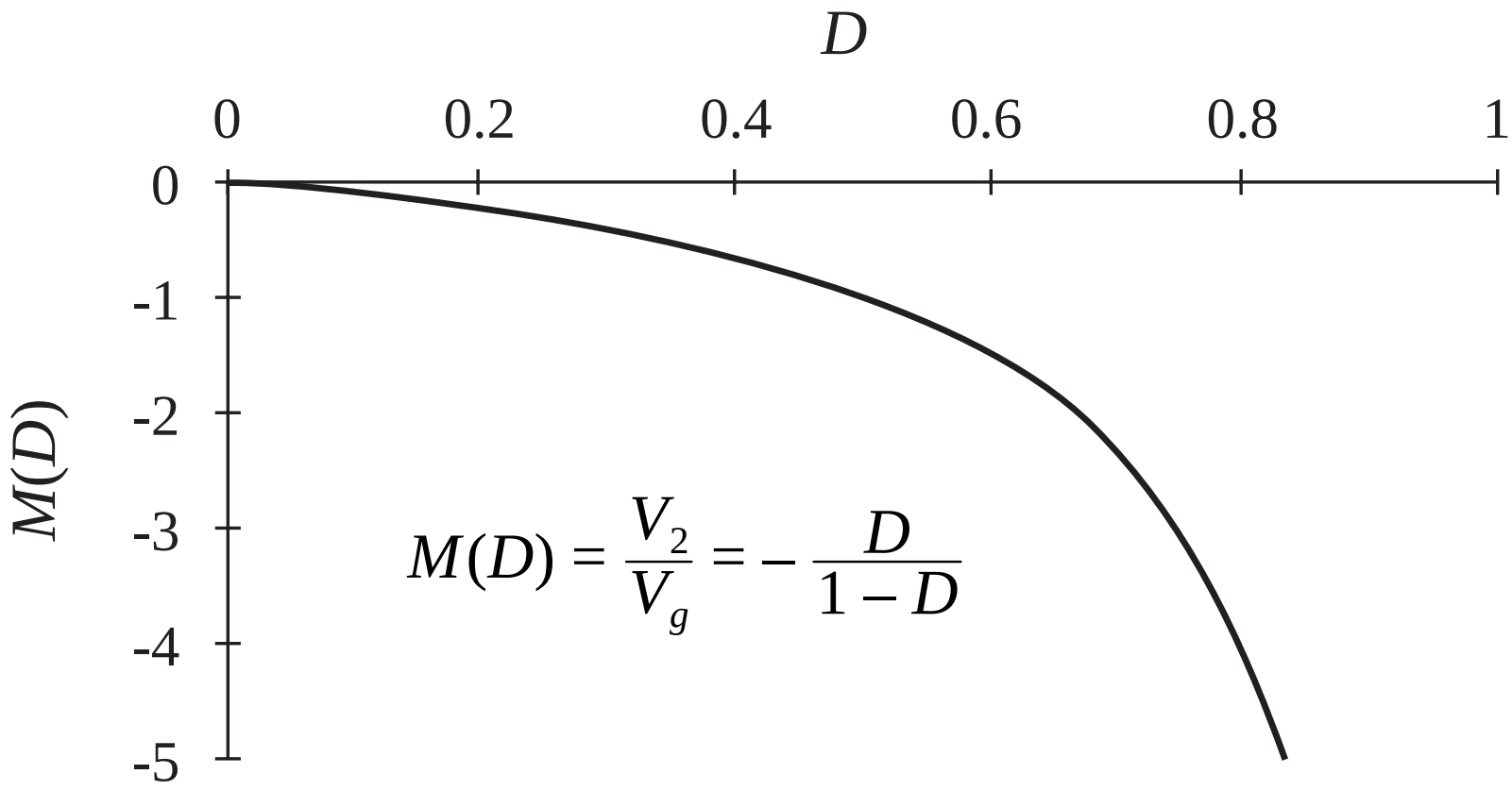
Capacitor current $i_{C2}(t)$ waveform



$$\left\langle i_{C2} \right\rangle = I_2 - \frac{V_2}{R} = 0$$

Note: during both subintervals, the capacitor current i_{C2} is equal to the difference between the inductor current i_2 and the load current V_2/R. When ripple is neglected, i_{C2} is constant and equal to zero.

Cuk converter conversion ratio $M = V / V_g$



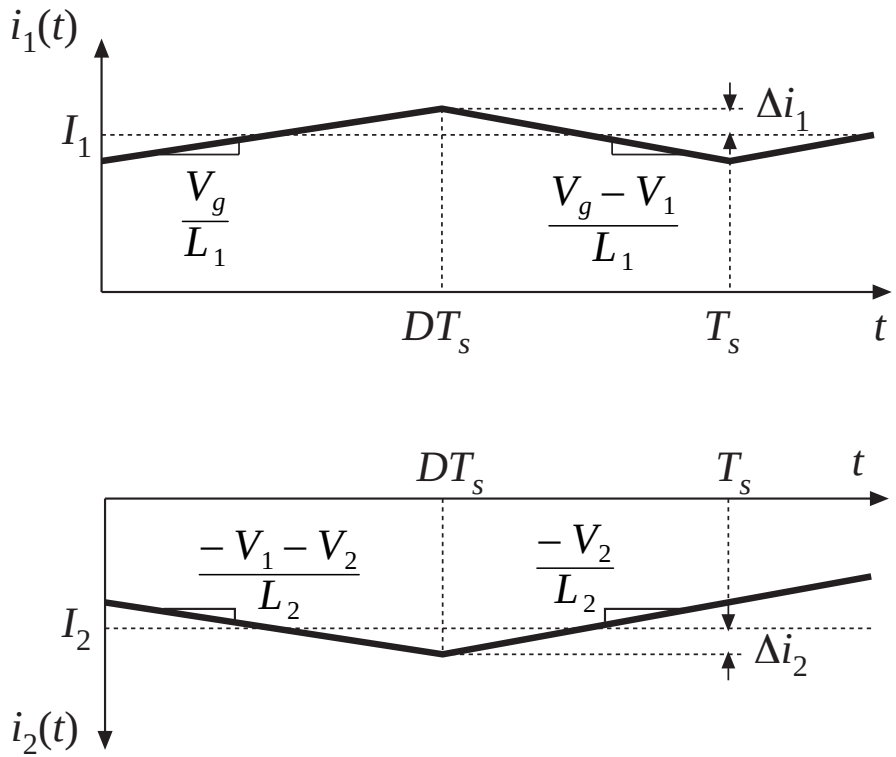
Inductor current waveforms

Interval 1 slopes, using small ripple approximation:

$$\frac{di_1(t)}{dt} = \frac{v_{L1}(t)}{L_1} = \frac{V_g}{L_1}$$
$$\frac{di_2(t)}{dt} = \frac{v_{L2}(t)}{L_2} = \frac{-V_1 - V_2}{L_2}$$

Interval 2 slopes:

$$\frac{di_1(t)}{dt} = \frac{v_{L1}(t)}{L_1} = \frac{V_g - V_1}{L_1}$$
$$\frac{di_2(t)}{dt} = \frac{v_{L2}(t)}{L_2} = \frac{-V_2}{L_2}$$



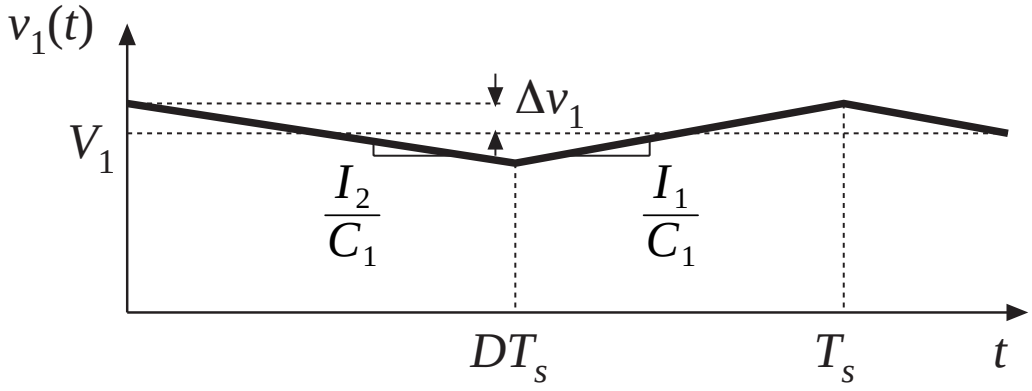
Capacitor C_1 waveform

Subinterval 1:

$$\frac{dv_1(t)}{dt} = \frac{i_{C1}(t)}{C_1} = \frac{I_2}{C_1}$$

Subinterval 2:

$$\frac{dv_1(t)}{dt} = \frac{i_{C1}(t)}{C_1} = \frac{I_1}{C_1}$$



Ripple magnitudes

Analysis results

$$\Delta i_1 = \frac{V_g D T_s}{2 L_1}$$

$$\Delta i_2 = \frac{V_1 + V_2}{2 L_2} D T_s$$

$$\Delta v_1 = \frac{-I_2 D T_s}{2 C_1}$$

Use dc converter solution to simplify:

$$\Delta i_1 = \frac{V_g D T_s}{2 L_1}$$

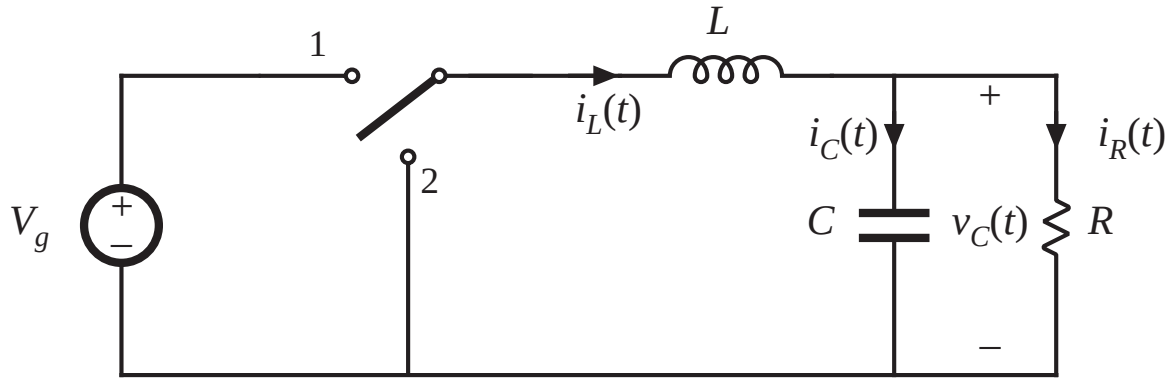
$$\Delta i_2 = \frac{V_g D T_s}{2 L_2}$$

$$\Delta v_1 = \frac{V_g D^2 T_s}{2 D' R C_1}$$

Q: How large is the output voltage ripple?

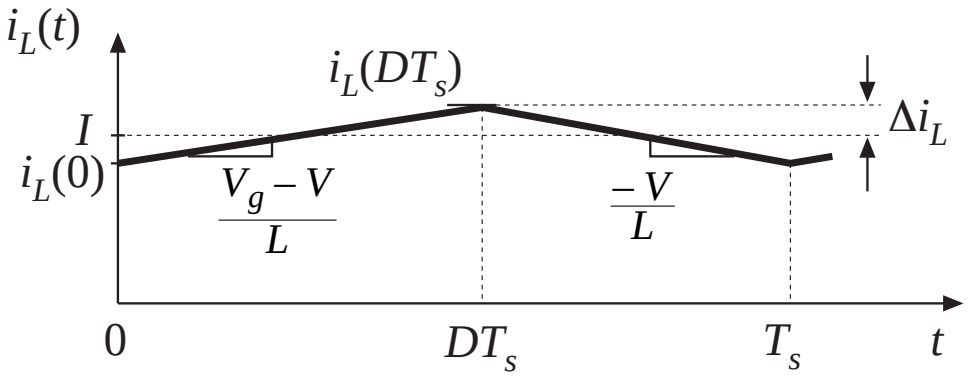
2.5 Estimating ripple in converters containing two-pole low-pass filters

Buck converter example: Determine output voltage ripple



Inductor current waveform.

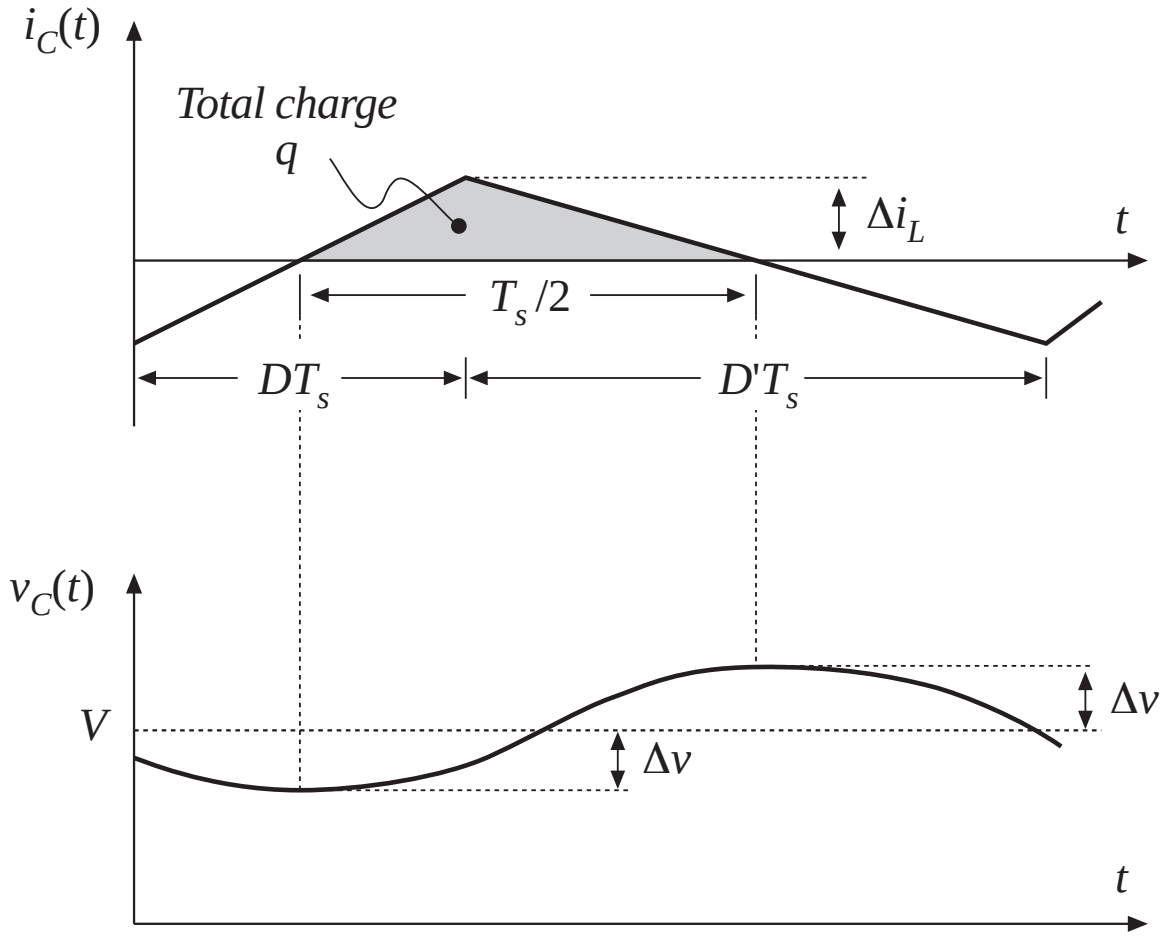
What is the capacitor current?



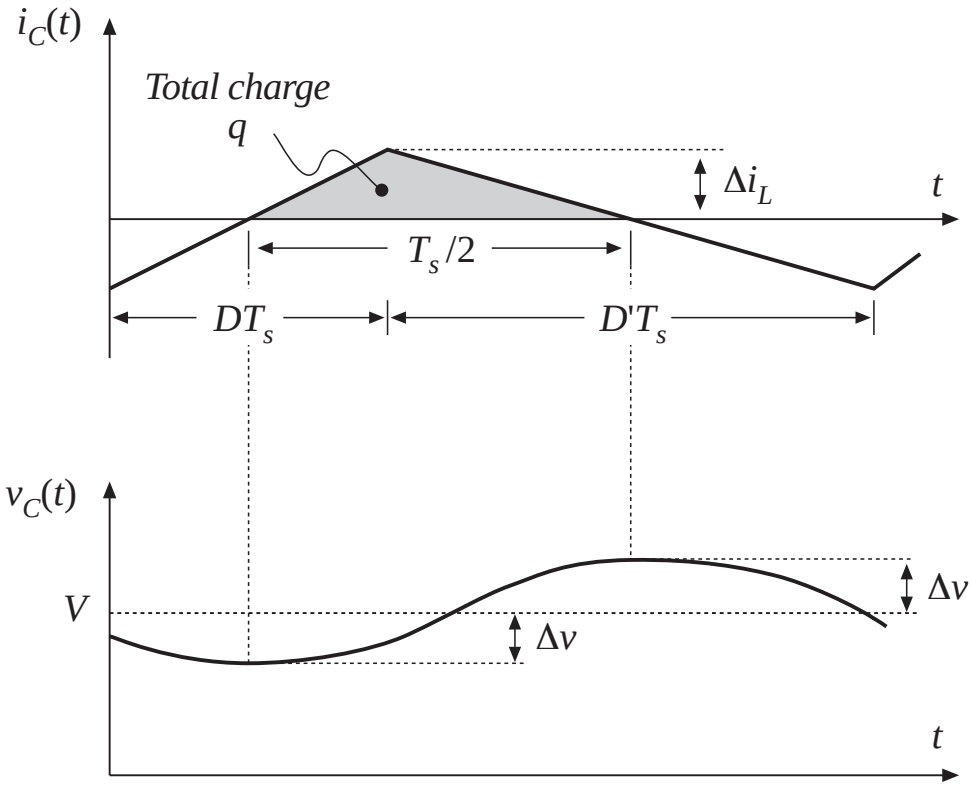
Capacitor current and voltage, buck example

Must not neglect inductor current ripple!

If the capacitor voltage ripple is small, then essentially all of the ac component of inductor current flows through the capacitor.



Estimating capacitor voltage ripple Δv

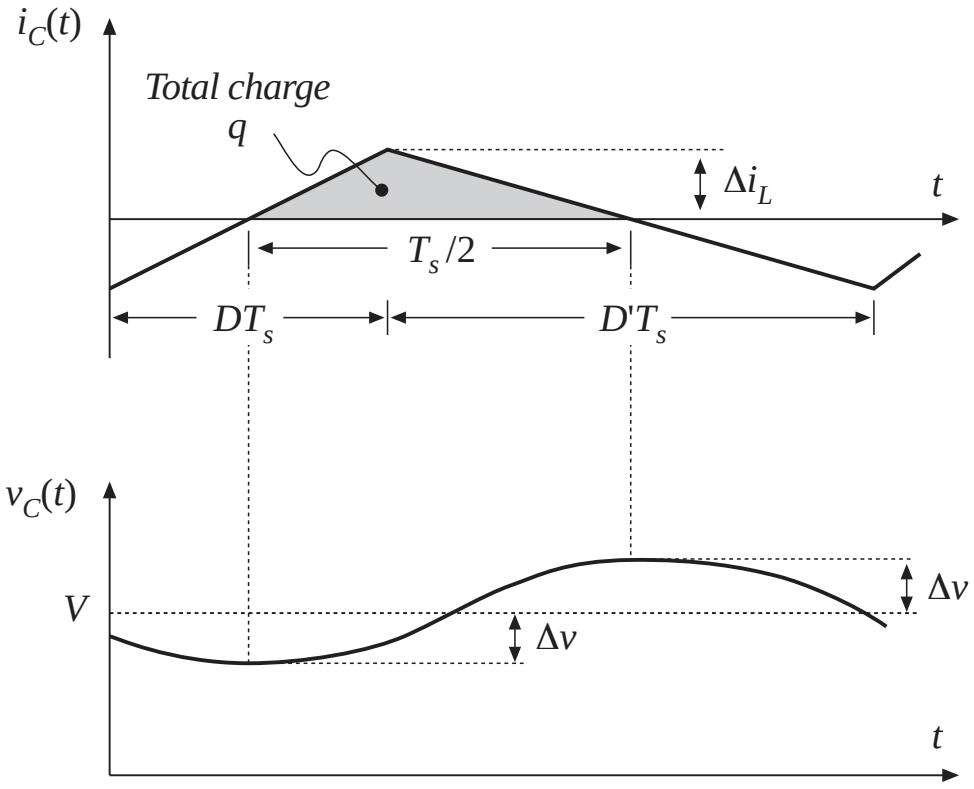


Current $i_C(t)$ is positive for half of the switching period. This positive current causes the capacitor voltage $v_C(t)$ to increase between its minimum and maximum extrema. During this time, the total charge q is deposited on the capacitor plates, where

$$q = C\,(2\Delta v)$$

(*change in charge*) =
C (*change in voltage*)

Estimating capacitor voltage ripple Δv



The total charge q is the area of the triangle, as shown:

$$q = \tfrac{1}{2} \Delta i_L \frac{T_s}{2}$$

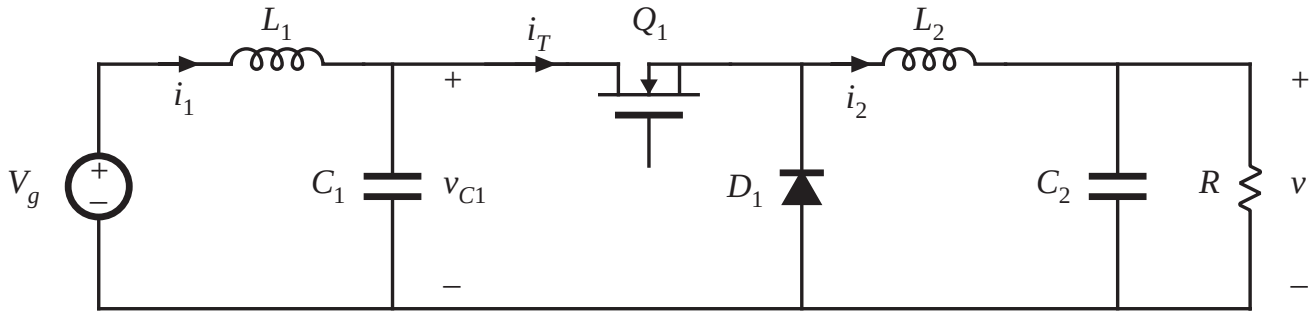
Eliminate q and solve for Δv:

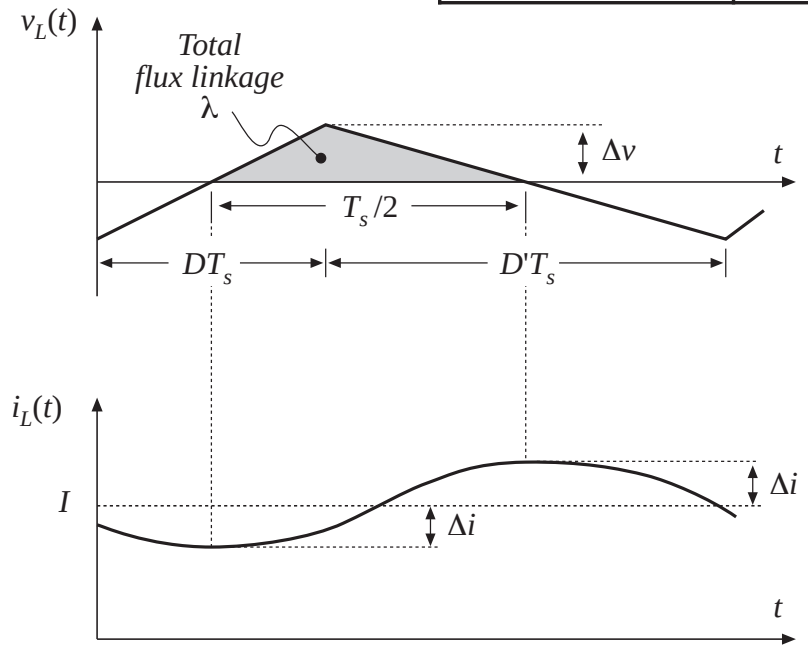
$$\Delta v = \frac{\Delta i_L \, T_s}{8 \, C}$$

Note: in practice, capacitor equivalent series resistance (esr) further increases Δv.

Inductor current ripple in two-pole filters

Example:
problem 2.9





can use similar arguments, with

$$\lambda = L\,(2\Delta i)$$

λ = inductor flux linkages

= inductor volt-seconds

2.6 Summary of Key Points

1. The dc component of a converter waveform is given by its average value, or the integral over one switching period, divided by the switching period. Solution of a dc-dc converter to find its dc, or steady-state, voltages and currents therefore involves averaging the waveforms.
2. The linear ripple approximation greatly simplifies the analysis. In a well-designed converter, the switching ripples in the inductor currents and capacitor voltages are small compared to the respective dc components, and can be neglected.
3. The principle of inductor volt-second balance allows determination of the dc voltage components in any switching converter. In steady-state, the average voltage applied to an inductor must be zero.

Summary of Chapter 2

4. The principle of capacitor charge balance allows determination of the dc components of the inductor currents in a switching converter. In steady-state, the average current applied to a capacitor must be zero.
5. By knowledge of the slopes of the inductor current and capacitor voltage waveforms, the ac switching ripple magnitudes may be computed. Inductance and capacitance values can then be chosen to obtain desired ripple magnitudes.
6. In converters containing multiple-pole filters, continuous (nonpulsating) voltages and currents are applied to one or more of the inductors or capacitors. Computation of the ac switching ripple in these elements can be done using capacitor charge and/or inductor flux-linkage arguments, without use of the small-ripple approximation.
7. Converters capable of increasing (boost), decreasing (buck), and inverting the voltage polarity (buck-boost and Cuk) have been described. Converter circuits are explored more fully in a later chapter.

Chapter 3. Steady-State Equivalent Circuit Modeling, Losses, and Efficiency

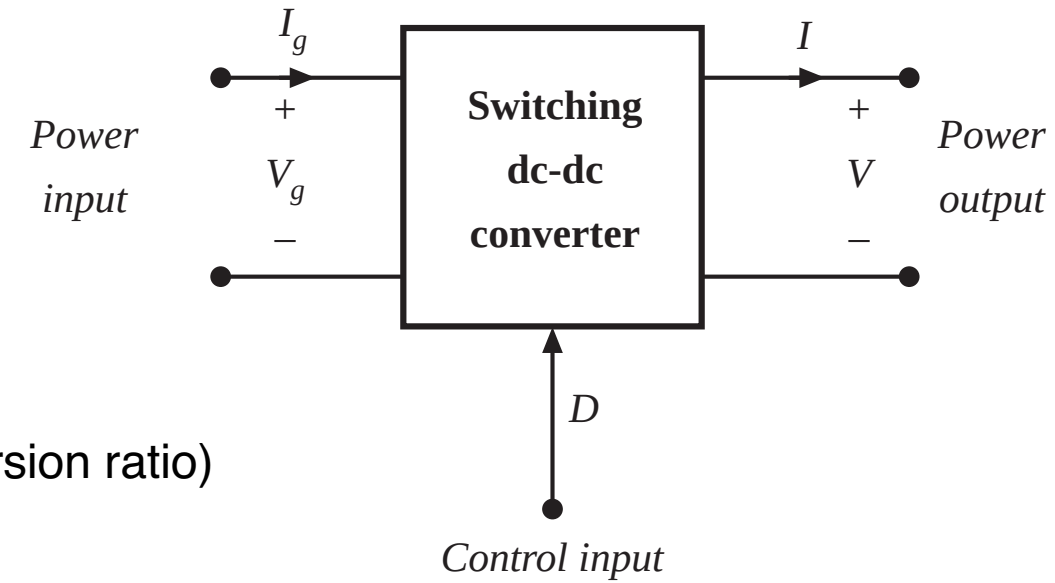
3.1. The dc transformer model

Basic equations of an ideal dc-dc converter:

$$P_{in} = P_{out}$$

$$V_g I_g = V I$$

(η = 100%)



$$V = M(D)\, V_g$$

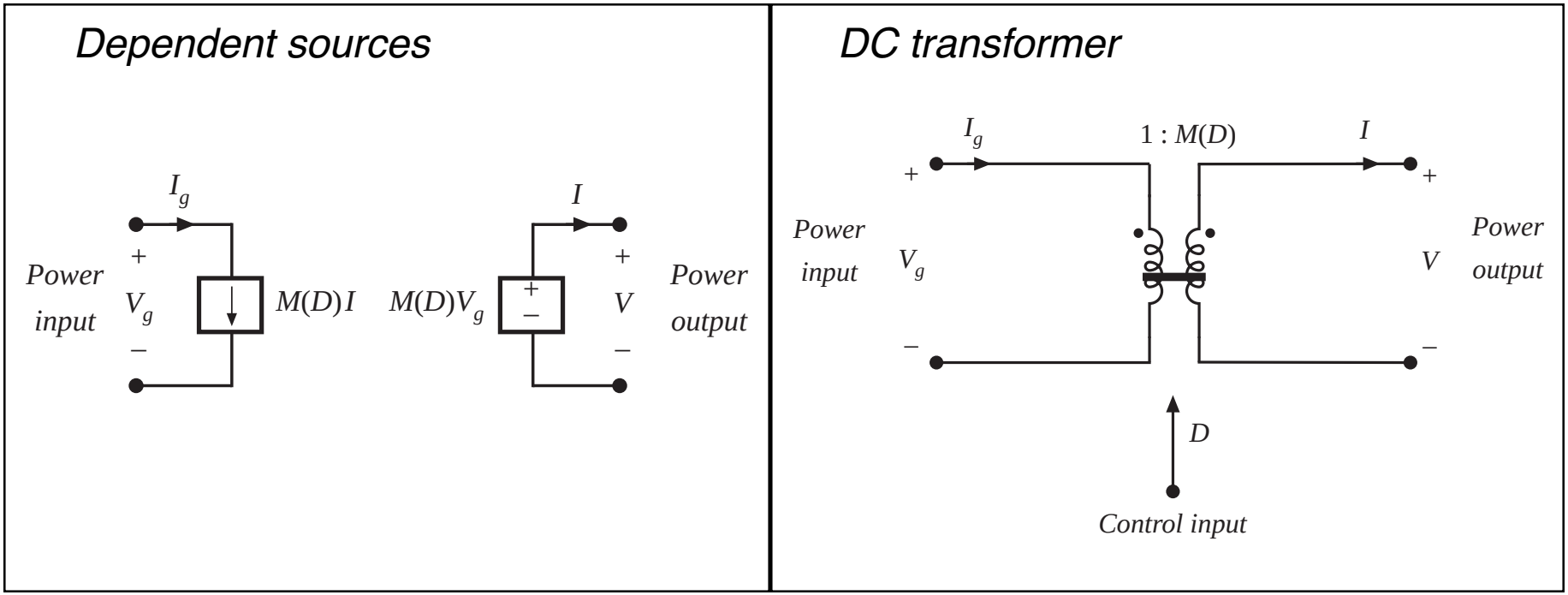
$$I_g = M(D)\, I$$

(ideal conversion ratio)

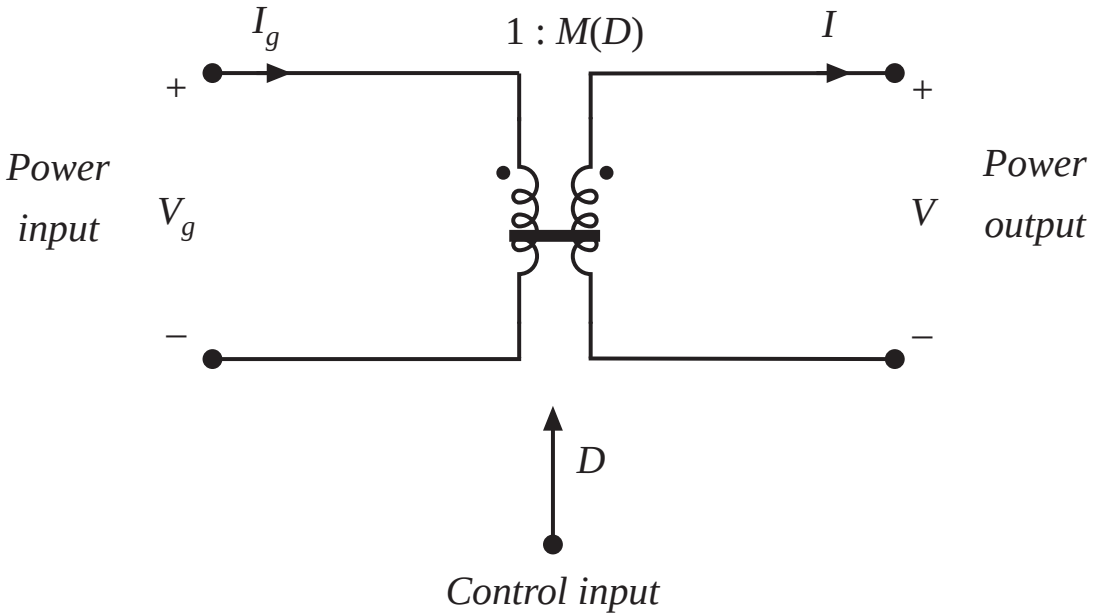
These equations are valid in steady-state. During transients, energy storage within filter elements may cause $P_{in} \neq P_{out}$

Equivalent circuits corresponding to ideal dc-dc converter equations

$$P_{in} = P_{out} \qquad V_g I_g = V I \qquad V = M(D)\, V_g \qquad I_g = M(D)\, I$$



The DC transformer model



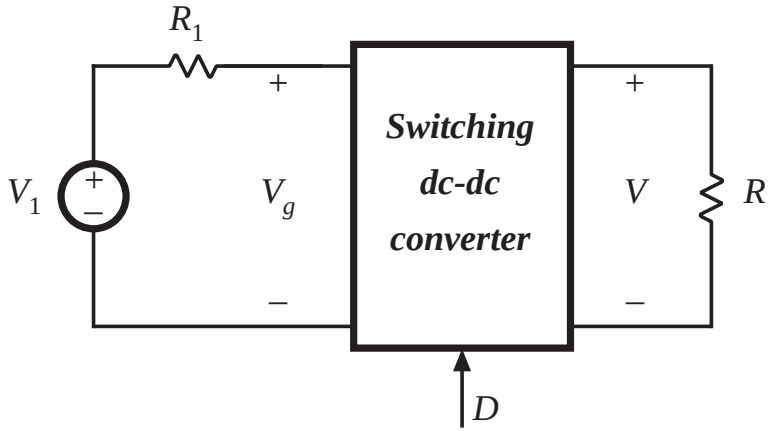
Models basic properties of ideal dc-dc converter:

- conversion of dc voltages and currents, ideally with 100% efficiency
- conversion ratio M controllable via duty cycle

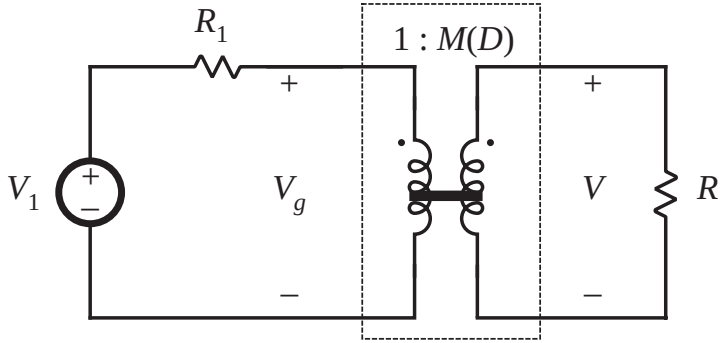
- Solid line denotes ideal transformer model, capable of passing dc voltages and currents
- Time-invariant model (no switching) which can be solved to find dc components of converter waveforms

Example: use of the DC transformer model

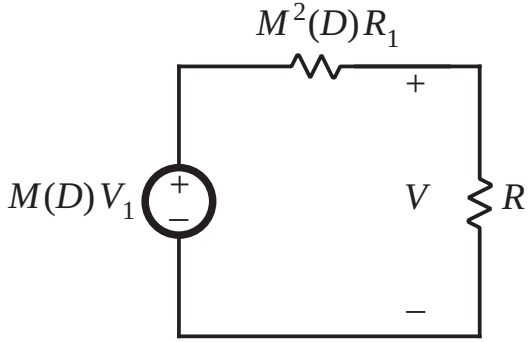
1. Original system



2. Insert dc transformer model



3. Push source through transformer



4. Solve circuit

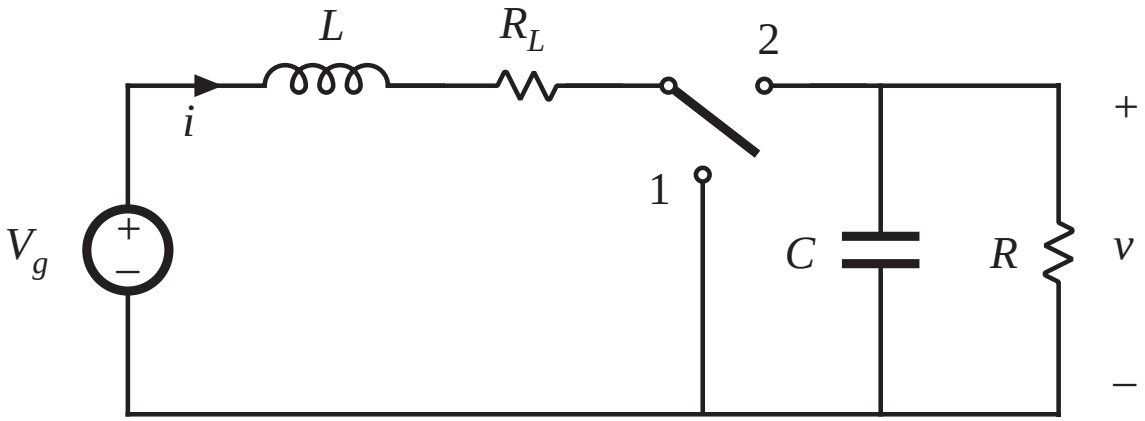
$$V = M(D)\, V_1 \, \frac{R}{R + M^2(D)\, R_1}$$

3.2. Inclusion of inductor copper loss

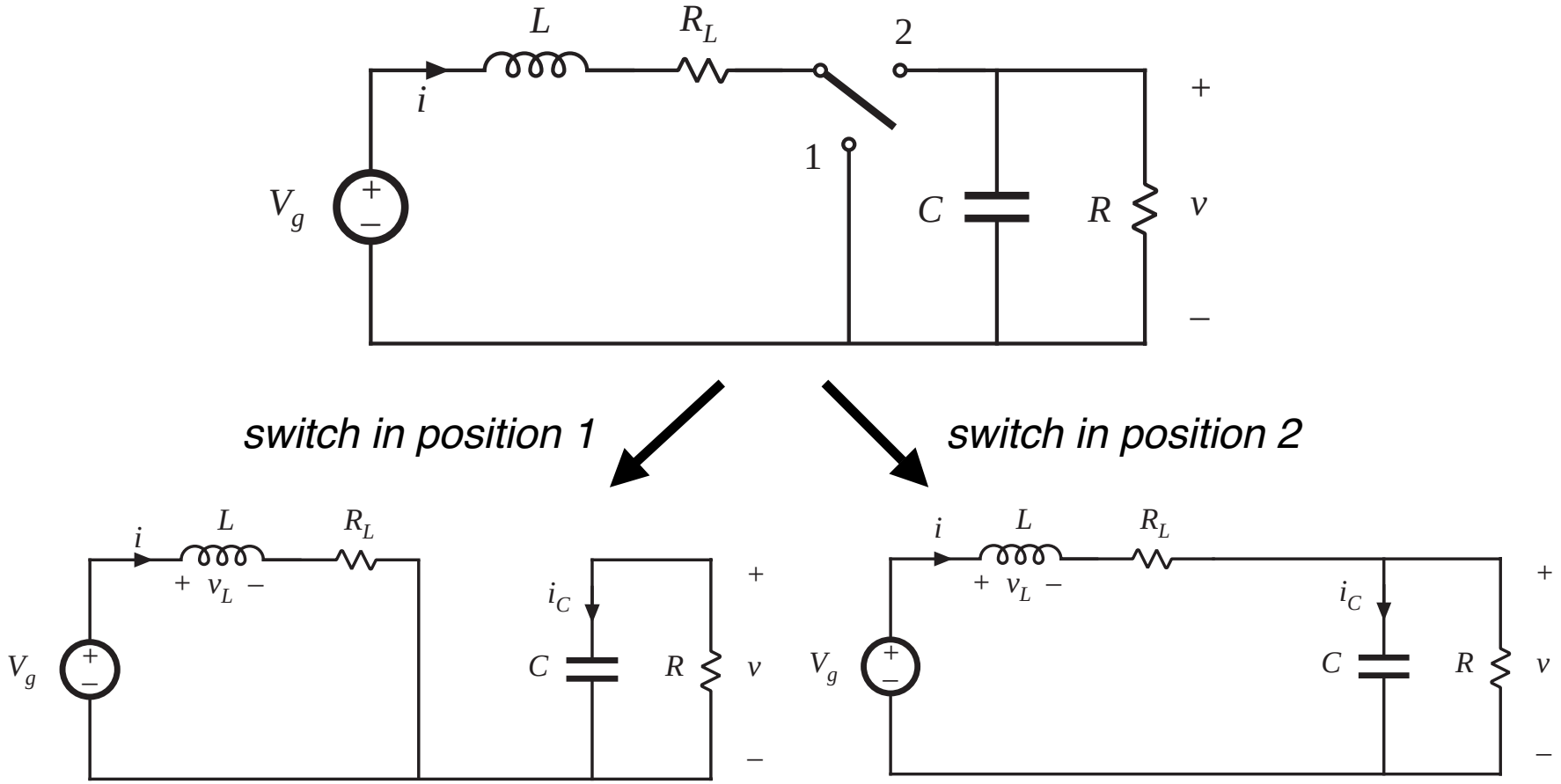
Dc transformer model can be extended, to include converter nonidealities.

Example: inductor copper loss (resistance of winding):

Insert this inductor model into boost converter circuit:



Analysis of nonideal boost converter

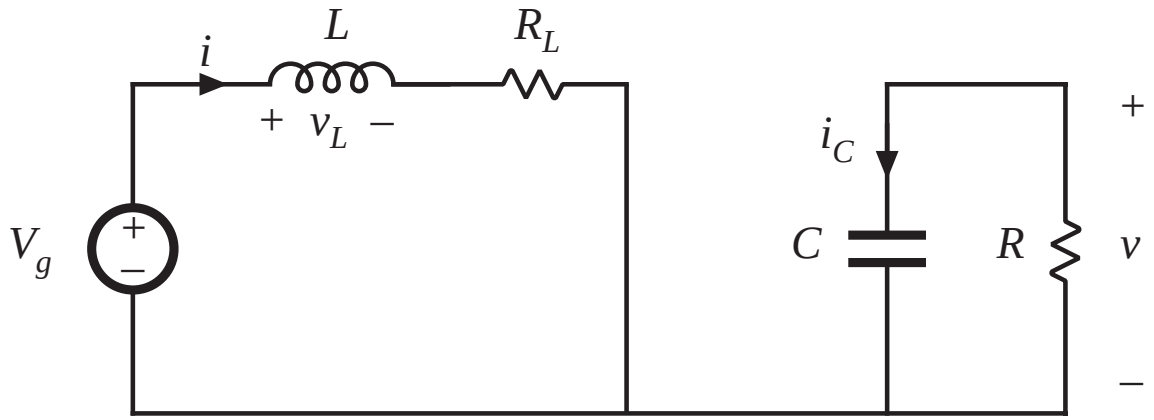


Circuit equations, switch in position 1

Inductor current and capacitor voltage:

$$v_L(t) = V_g - i(t)\, R_L$$

$$i_C(t) = -v(t) / R$$

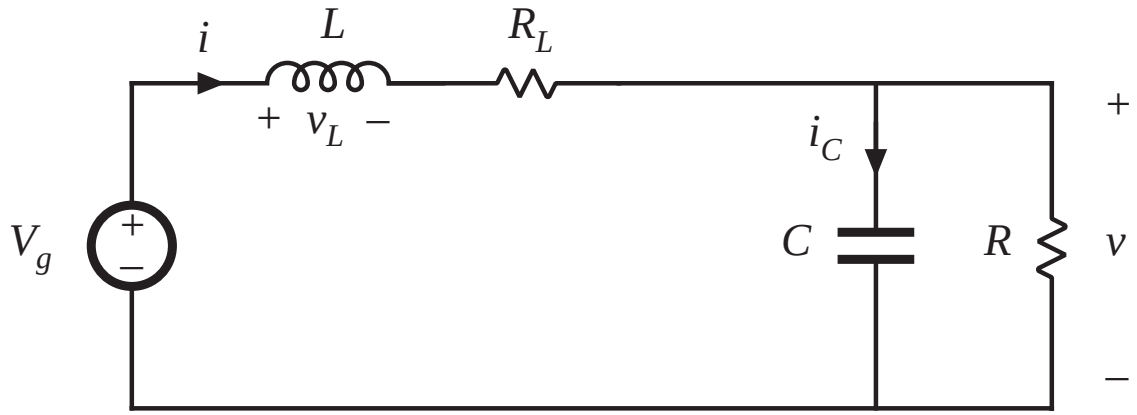


Small ripple approximation:

$$v_L(t) = V_g - I\, R_L$$

$$i_C(t) = -V / R$$

Circuit equations, switch in position 2



$$v_L(t) = V_g - i(t)\,R_L - v(t) \approx V_g - I\,R_L - V$$
$$i_C(t) = i(t) - v(t) / R \approx I - V / R$$

Inductor voltage and capacitor current waveforms

Average inductor voltage:

$$\left\langle v_L(t) \right\rangle = \frac{1}{T_s} \int_0^{T_s} v_L(t) dt$$

$$= D(V_g - I\,R_L) + D'(V_g - I\,R_L - V)$$

Inductor volt-second balance:

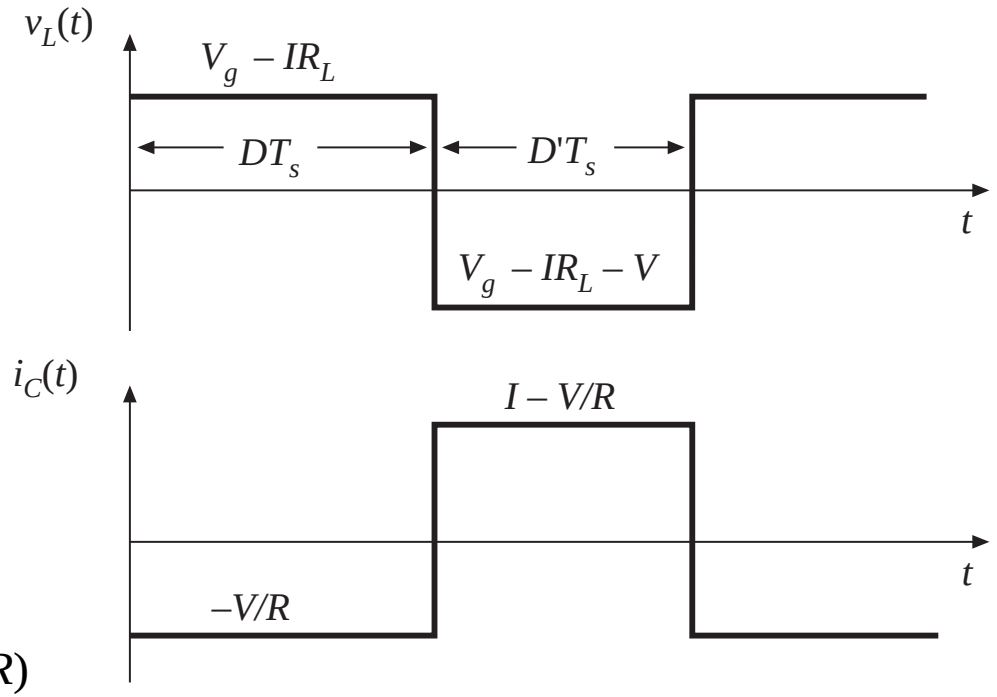
$$0 = V_g - I\,R_L - D'V$$

Average capacitor current:

$$\left\langle i_C(t) \right\rangle = D\,(-V/R) + D'\,(I - V/R)$$

Capacitor charge balance:

$$0 = D'I - V/R$$



Solution for output voltage

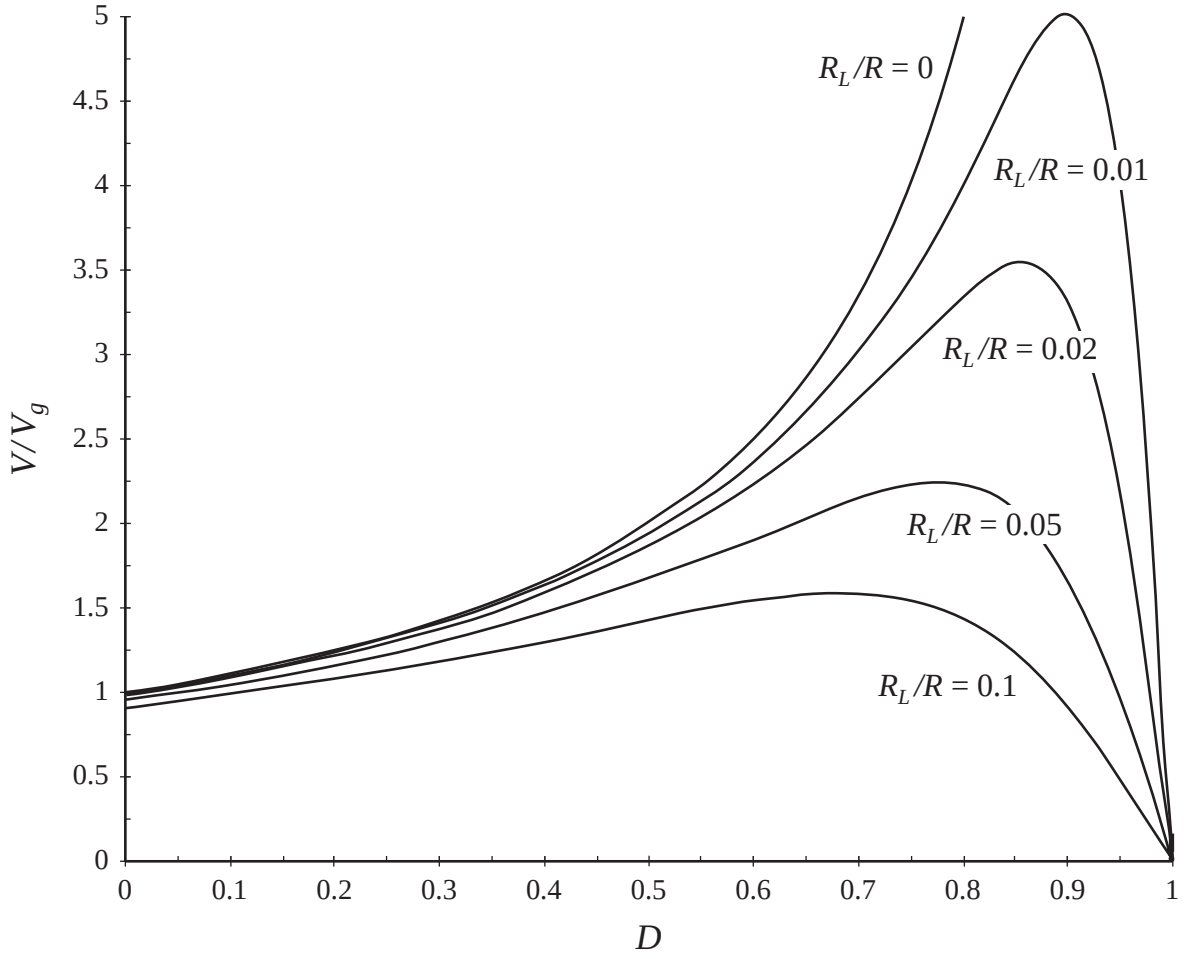
We now have two equations and two unknowns:

$$0 = V_g - I\,R_L - D'V$$

$$0 = D'I - V / R$$

Eliminate I and solve for V:

$$\frac{V}{V_g} = \frac{1}{D'}\,\frac{1}{(1 + R_L / D'^2 R)}$$



3.3. Construction of equivalent circuit model

Results of previous section (derived via inductor volt-sec balance and capacitor charge balance):

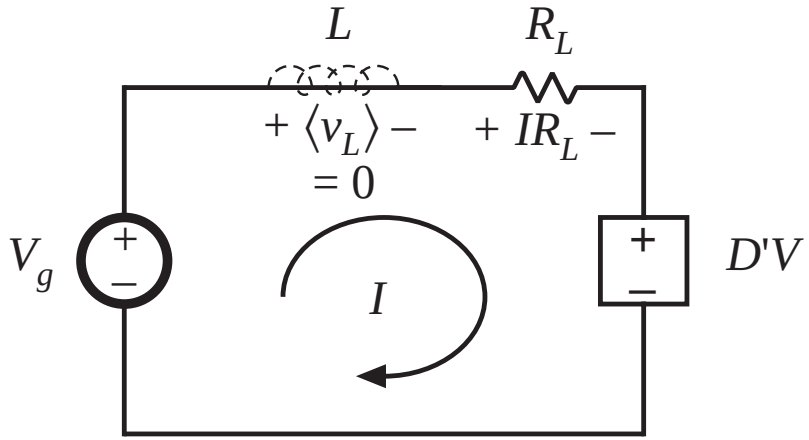
$$\langle v_L \rangle = 0 = V_g - I\,R_L - D'V$$
$$\langle i_C \rangle = 0 = D'I - V / R$$

View these as loop and node equations of the equivalent circuit.
Reconstruct an equivalent circuit satisfying these equations

Inductor voltage equation

$$\langle v_L \rangle = 0 = V_g - I\,R_L - D'V$$

- Derived via Kirchhoff's voltage law, to find the inductor voltage during each subinterval
- Average inductor voltage then set to zero
- This is a loop equation: the dc components of voltage around a loop containing the inductor sum to zero

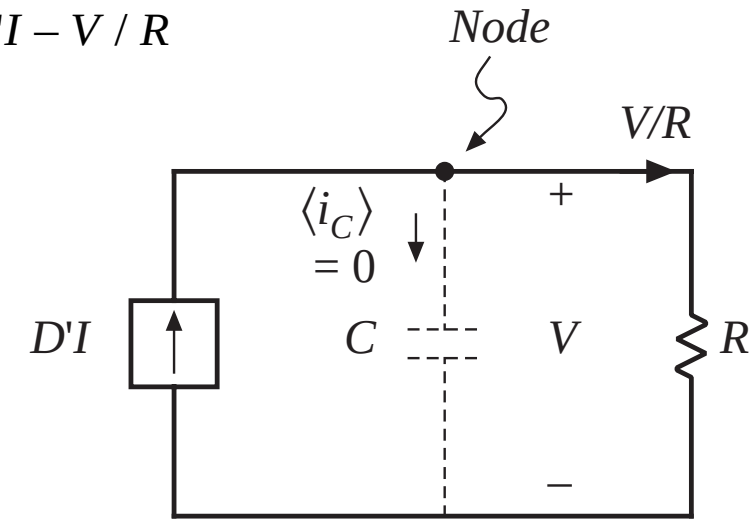


- IR_L term: voltage across resistor of value R_L having current I
- $D'V$ term: for now, leave as dependent source

Capacitor current equation

$$\langle i_C \rangle = 0 = D'I - V / R$$

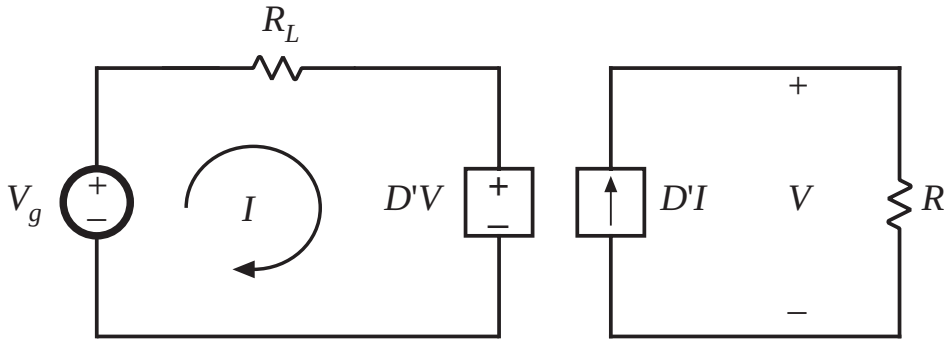
- Derived via Kirchoff's current law, to find the capacitor current during each subinterval
- Average capacitor current then set to zero
- This is a node equation: the dc components of current flowing into a node connected to the capacitor sum to zero



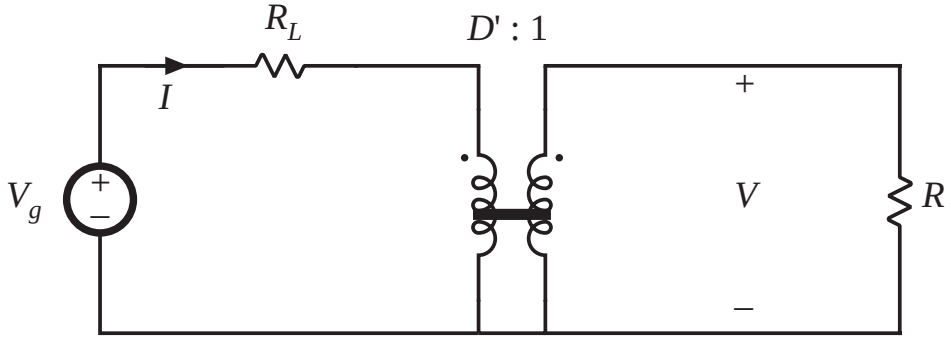
- *V/R* term: current through load resistor of value *R* having voltage *V*
- *D'I* term: for now, leave as dependent source

Complete equivalent circuit

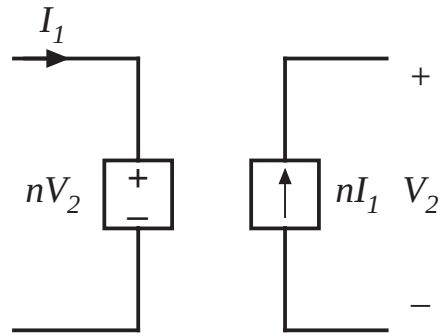
The two circuits, drawn together:

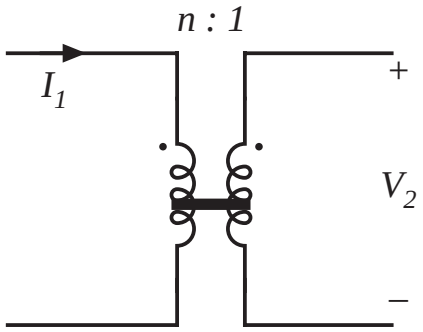


The dependent sources are equivalent to a D' : 1 transformer:



Dependent sources and transformers

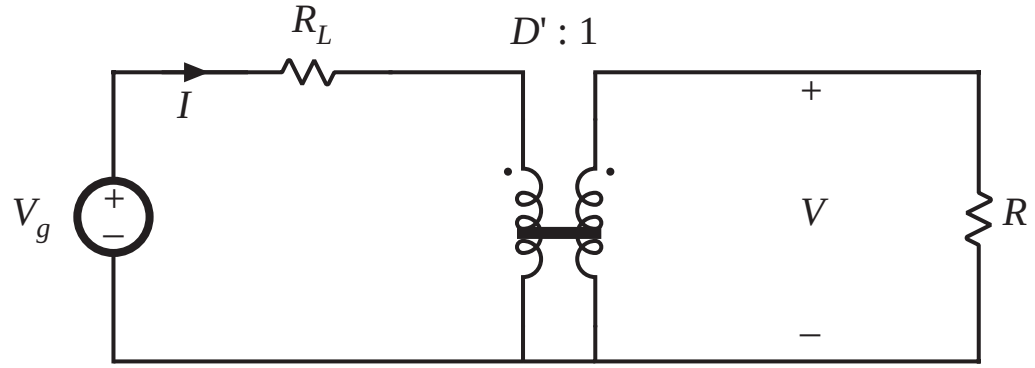




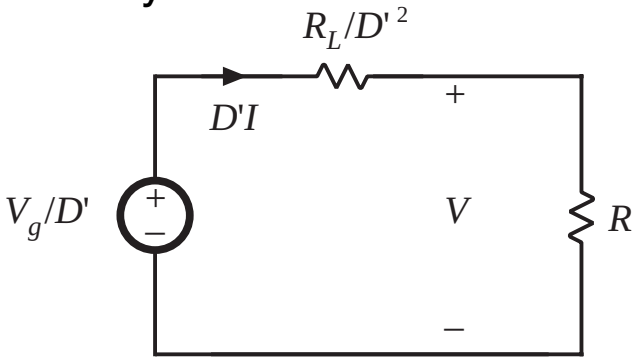
- *sources have same coefficient*
- *reciprocal voltage/current dependence*

Solution of equivalent circuit

Converter equivalent circuit



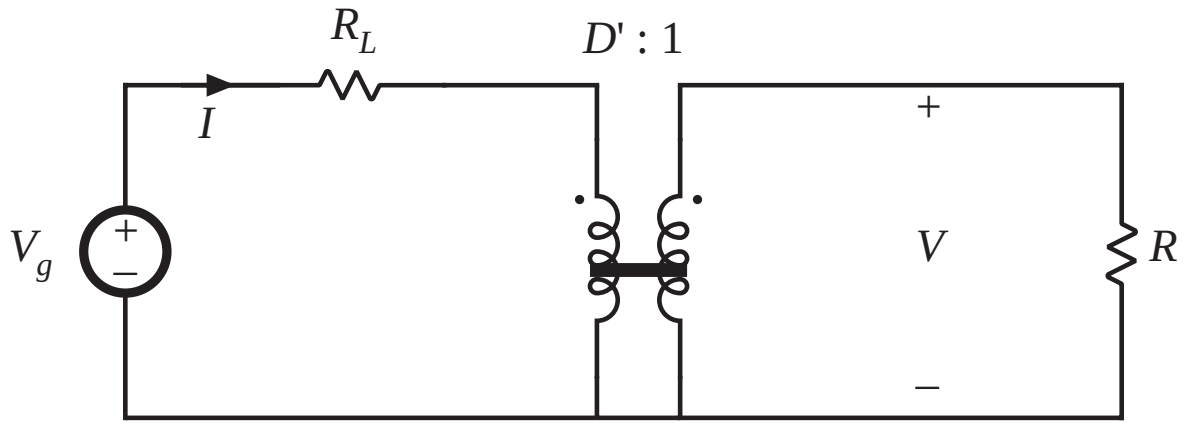
Refer all elements to transformer secondary:



Solution for output voltage using voltage divider formula:

$$V = \frac{V_g}{D'} \frac{R}{R + \frac{R_L}{D'^2}} = \frac{V_g}{D'} \frac{1}{1 + \frac{R_L}{D'^2 R}}$$

Solution for input (inductor) current

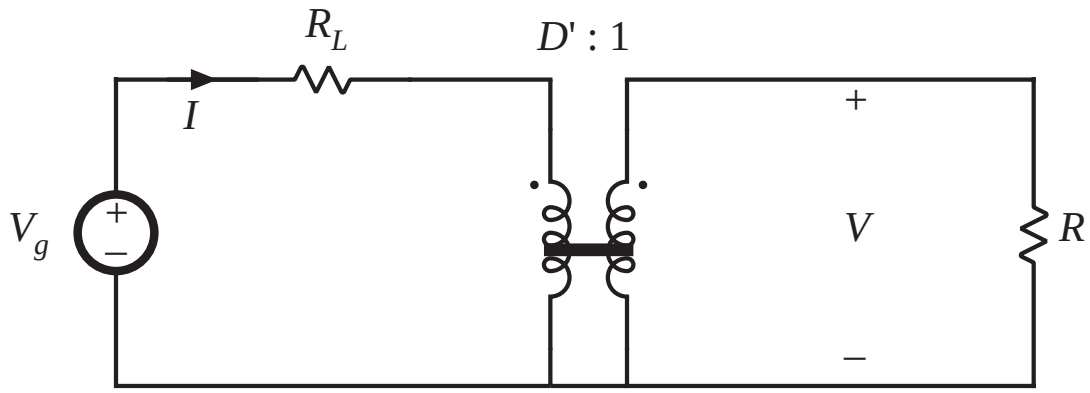


$$I = \frac{V_g}{D'^2 R + R_L} = \frac{V_g}{D'^2} \frac{1}{1 + \frac{R_L}{D'^2 R}}$$

Solution for converter efficiency

$$P_{in} = (V_g)\,(I)$$

$$P_{out} = (V)\,(D'I)$$

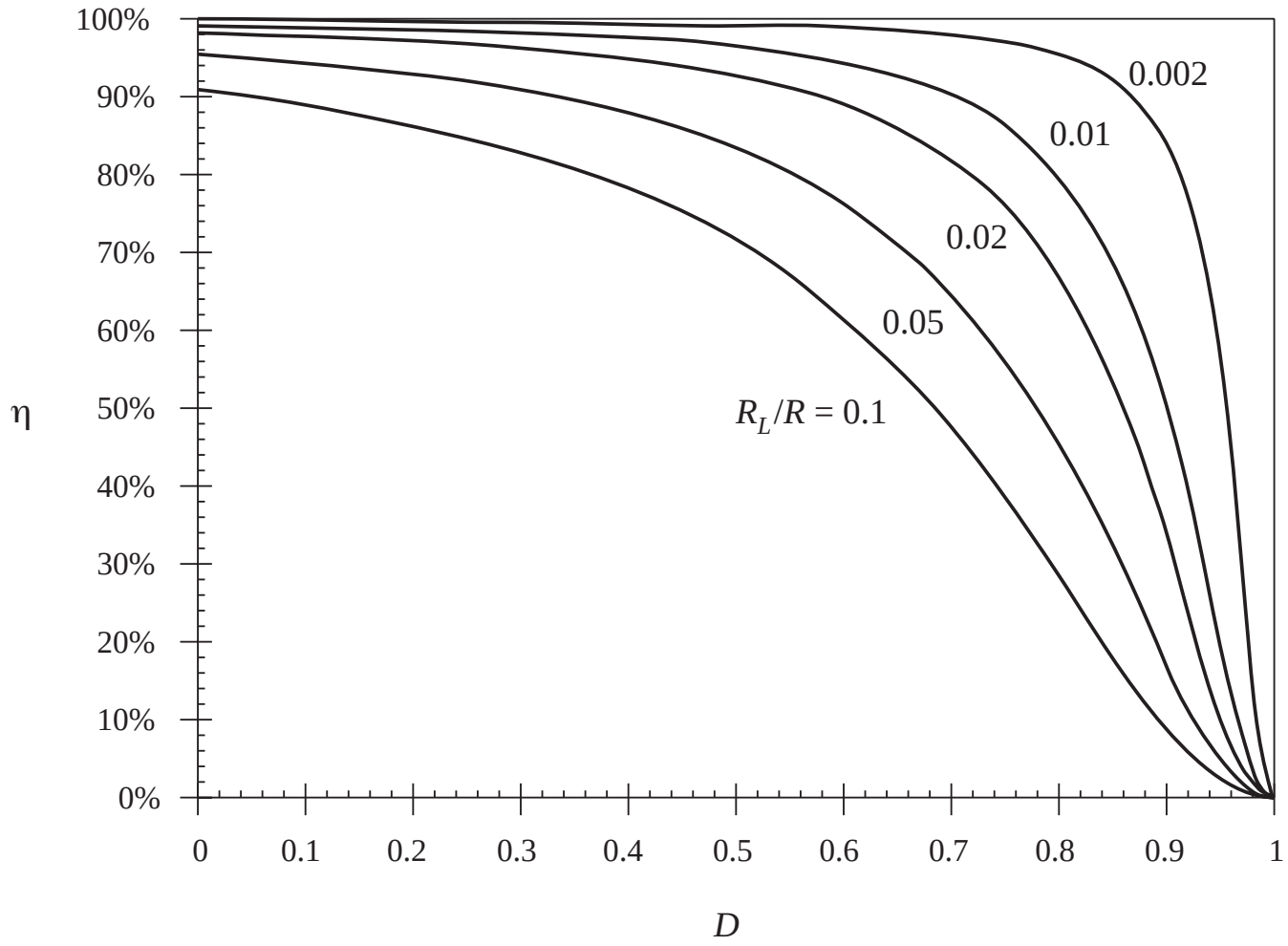


$$\eta = \frac{P_{out}}{P_{in}} = \frac{(V)\,(D'I)}{(V_g)\,(I)} = \frac{V}{V_g}\,D'$$

$$\eta = \frac{1}{1 + \dfrac{R_L}{D'^2\,R}}$$

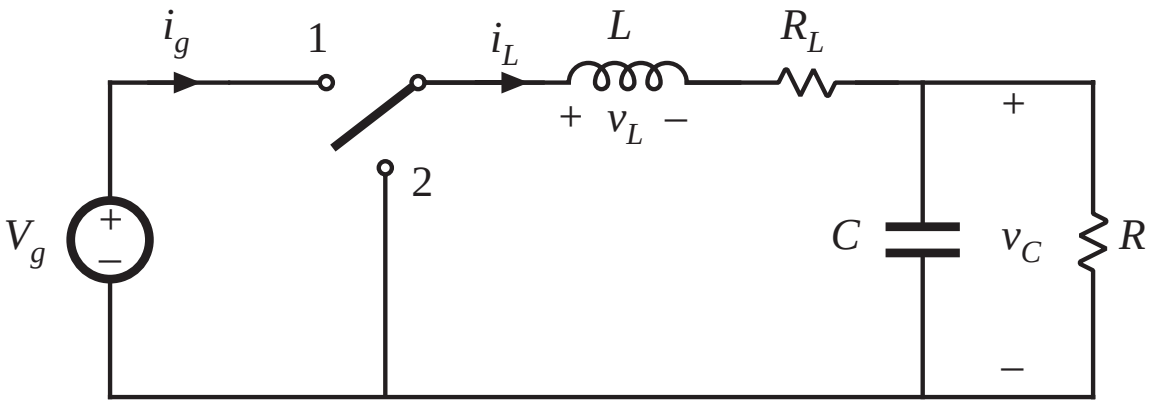
Efficiency, for various values of R_L

$$\eta = \frac{1}{1 + \frac{R_L}{D'^2 R}}$$



3.4. How to obtain the input port of the model

Buck converter example —use procedure of previous section to derive equivalent circuit

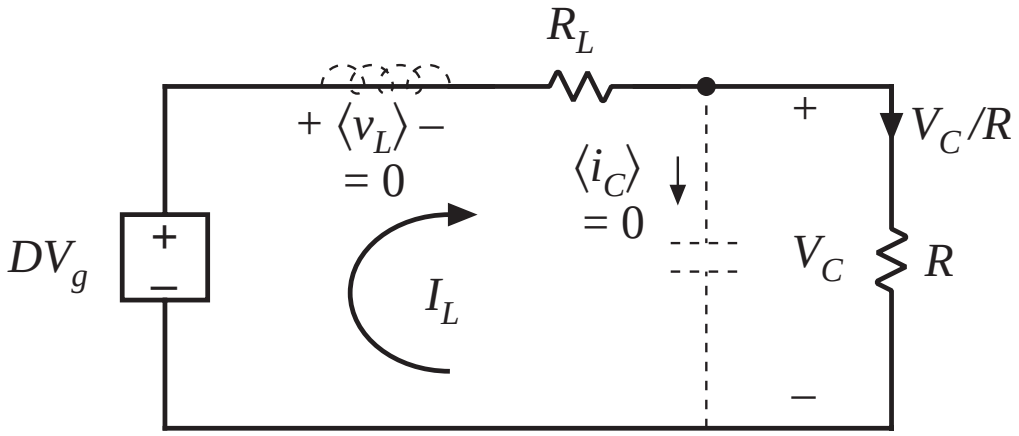


Average inductor voltage and capacitor current:

$$\langle v_L \rangle = 0 = DV_g - I_L R_L - V_C \qquad \langle i_C \rangle = 0 = I_L - V_C/R$$

Construct equivalent circuit as usual

$$\langle v_L \rangle = 0 = DV_g - I_L R_L - V_C \qquad \langle i_C \rangle = 0 = I_L - V_C/R$$

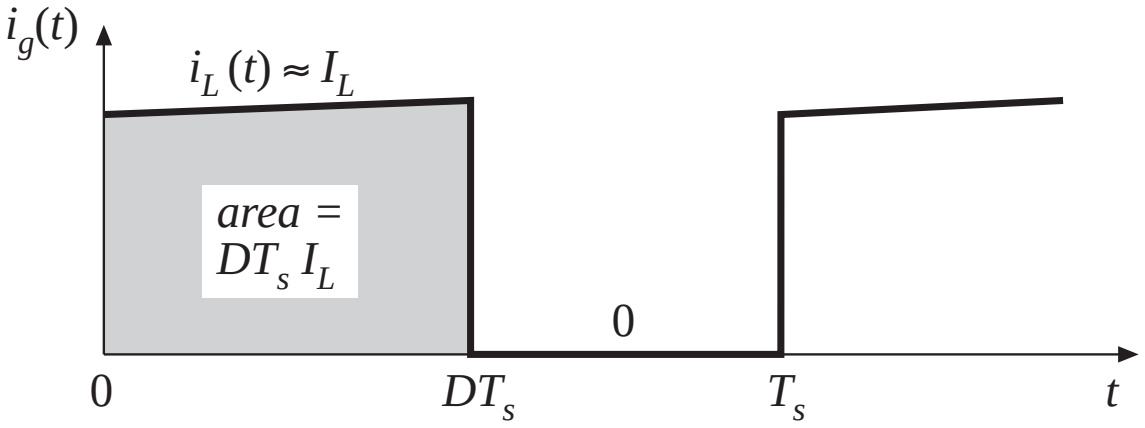


What happened to the transformer?

- Need another equation

Modeling the converter input port

Input current waveform $i_g(t)$:

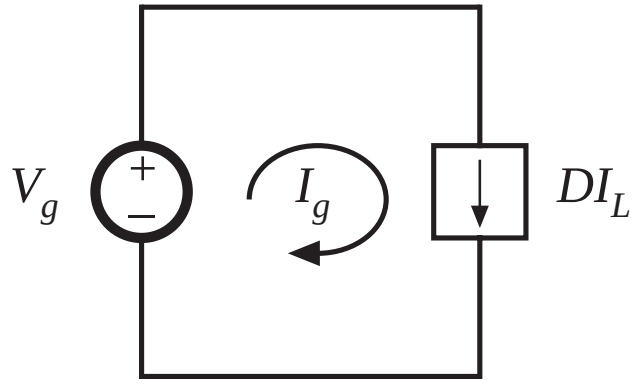


Dc component (average value) of $i_g(t)$ is

$$I_g = \frac{1}{T_s} \int_0^{T_s} i_g(t)\, dt = DI_L$$

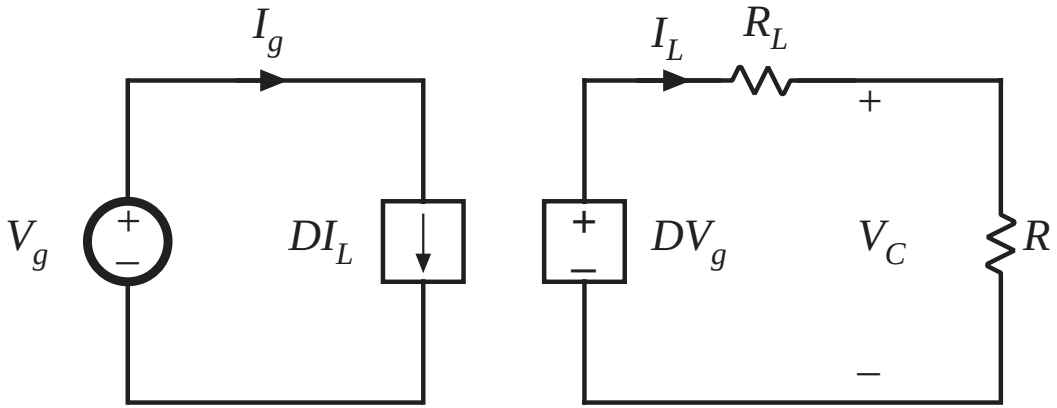
Input port equivalent circuit

$$I_g = \frac{1}{T_s} \int_0^{T_s} i_g(t)\, dt = DI_L$$

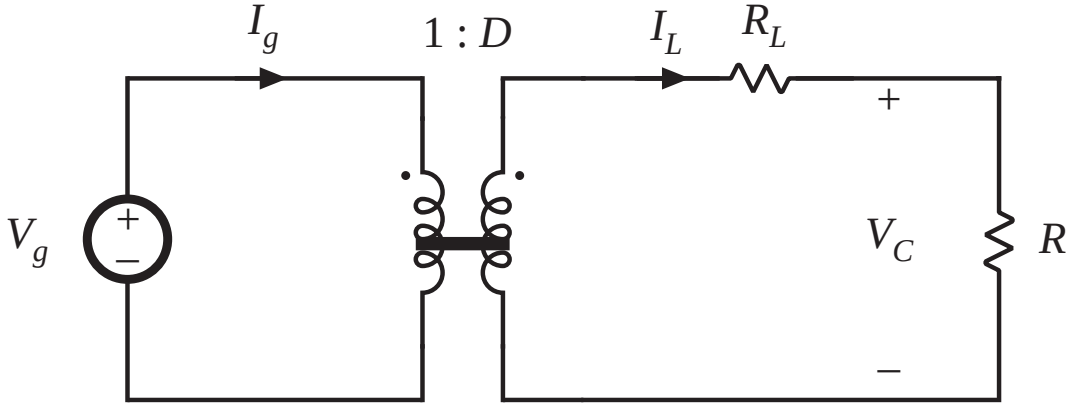


Complete equivalent circuit, buck converter

Input and output port equivalent circuits, drawn together:

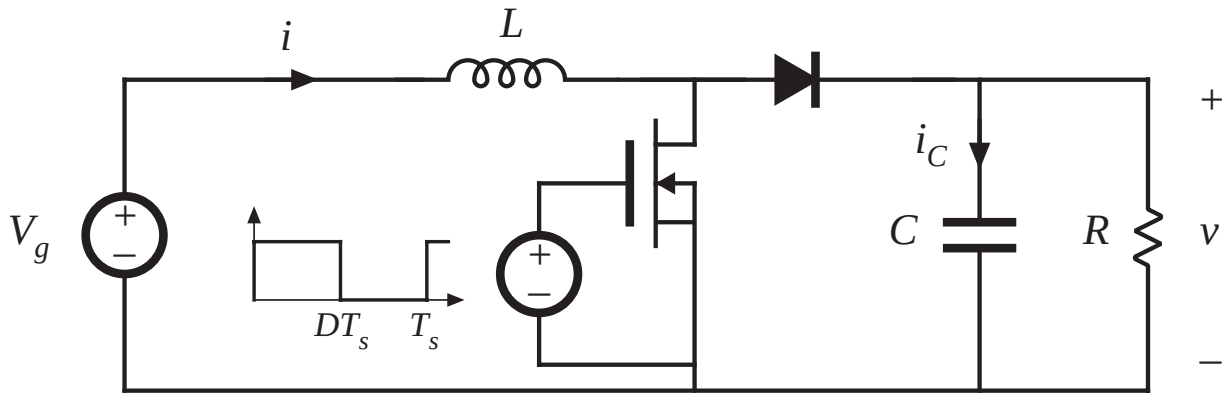


Replace dependent sources with equivalent dc transformer:



3.5. Example: inclusion of semiconductor conduction losses in the boost converter model

Boost converter example



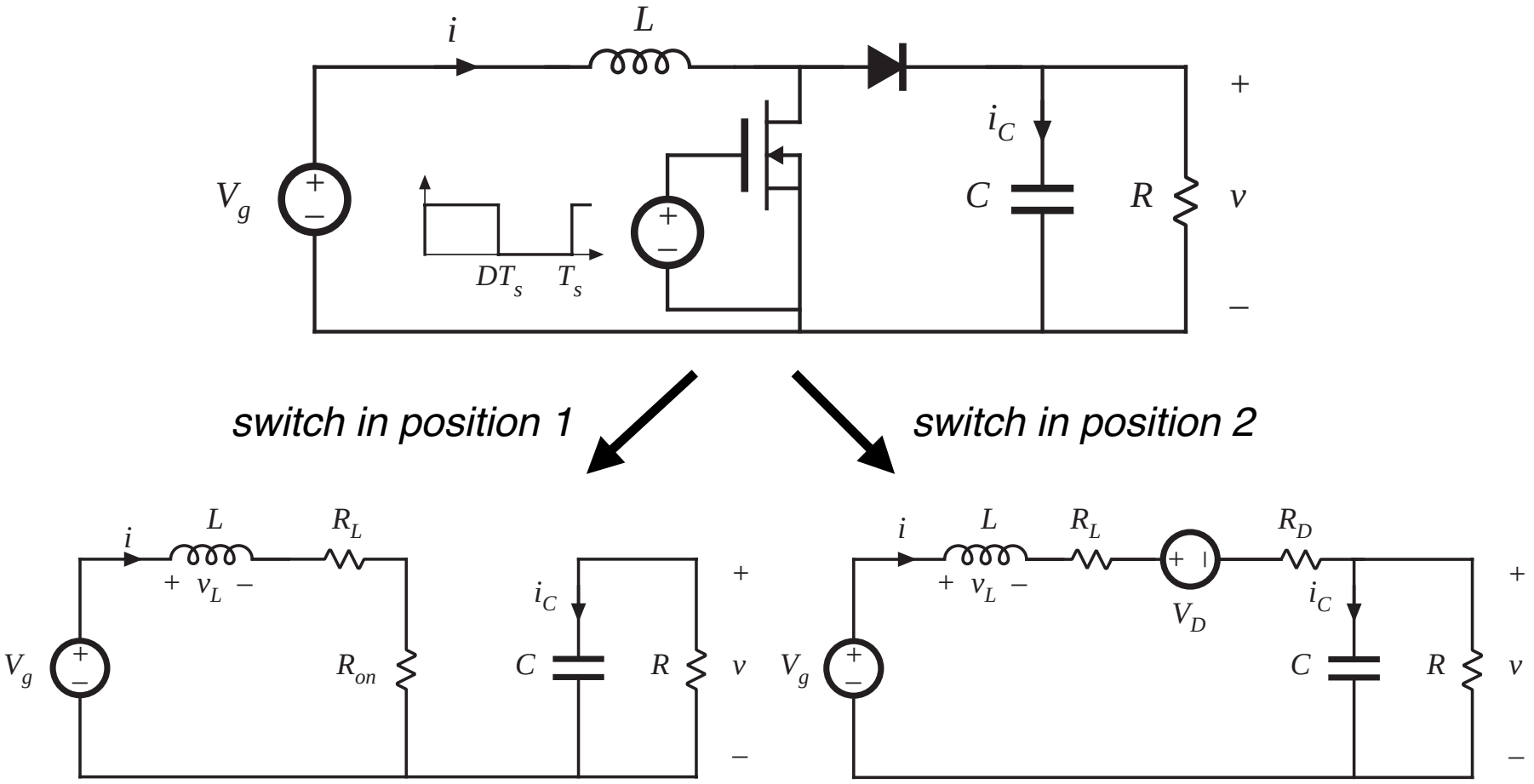
Models of on-state semiconductor devices:

MOSFET: on-resistance R_{on}

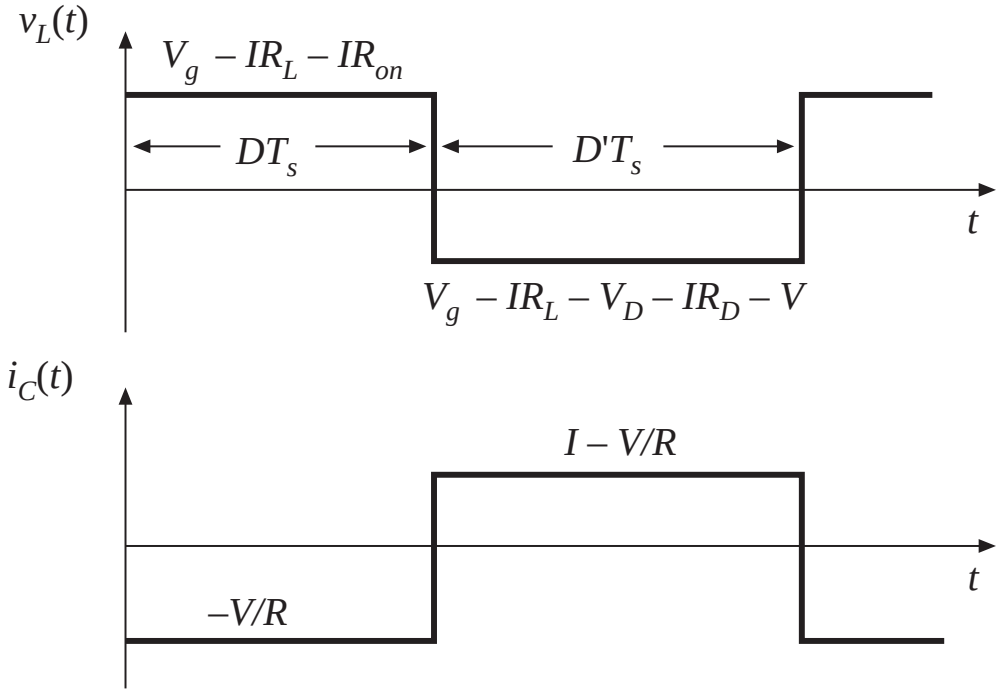
Diode: constant forward voltage V_D plus on-resistance R_D

Insert these models into subinterval circuits

Boost converter example: circuits during subintervals 1 and 2



Average inductor voltage and capacitor current

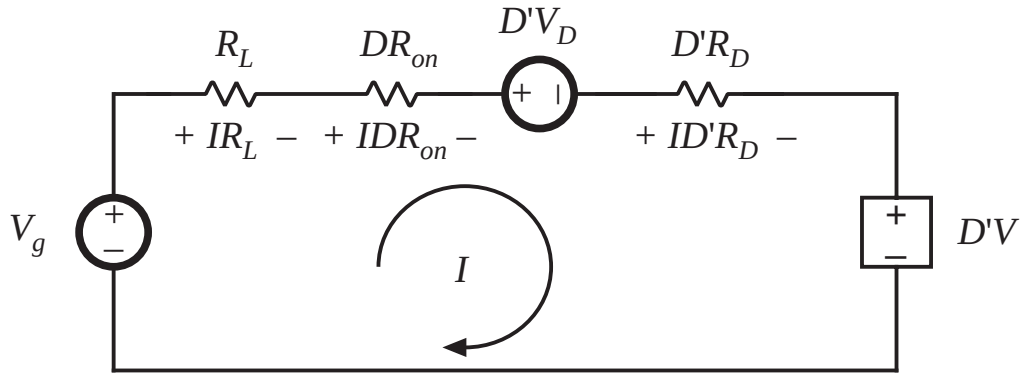


$$\langle v_L \rangle = D(V_g - IR_L - IR_{on}) + D'(V_g - IR_L - V_D - IR_D - V) = 0$$

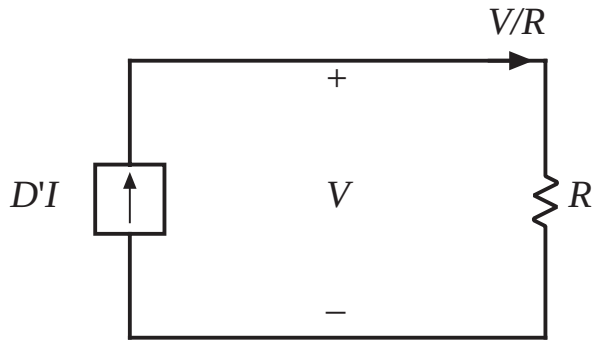
$$\langle i_C \rangle = D(-V/R) + D'(I - V/R) = 0$$

Construction of equivalent circuits

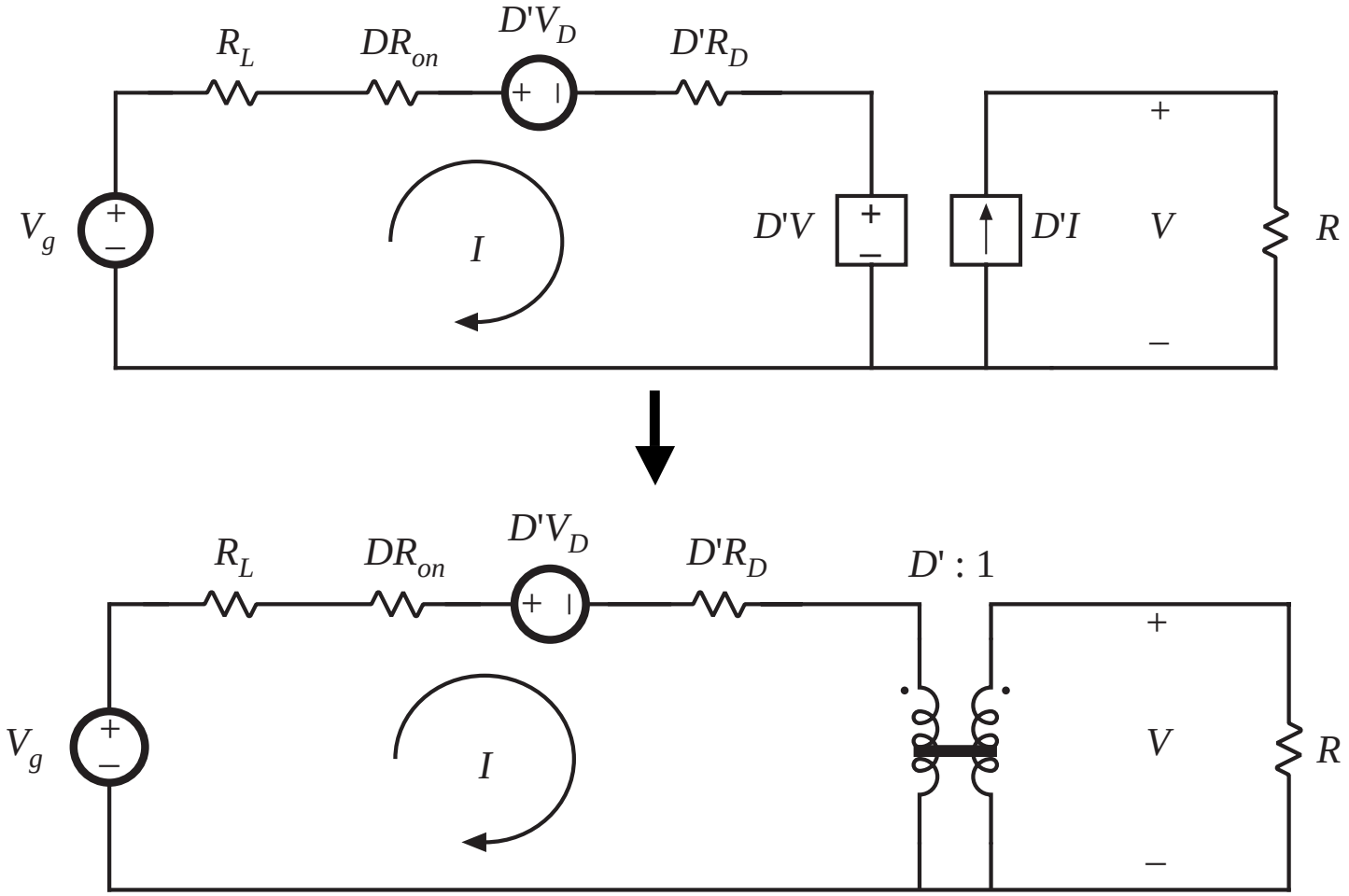
$$V_g - IR_L - IDR_{on} - D'V_D - ID'R_D - D'V = 0$$



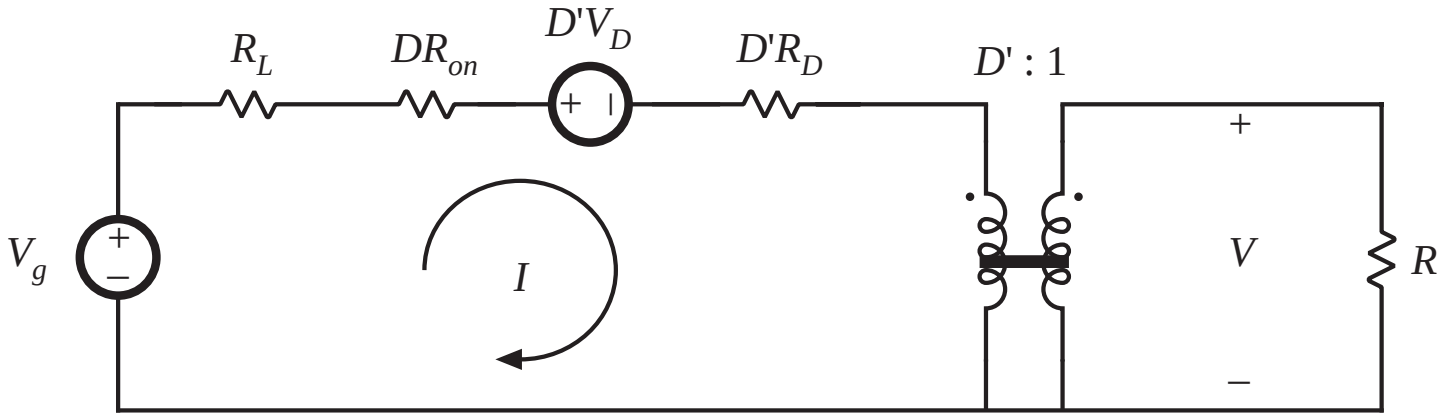
$$D'I - V/R = 0$$



Complete equivalent circuit



Solution for output voltage



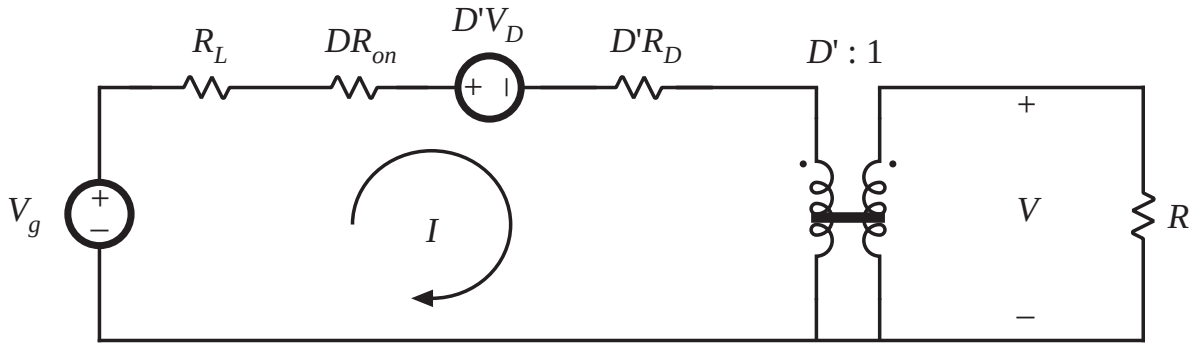
$$V = \left(\frac{1}{D'}\right)\left(V_g - D'V_D\right)\left(\frac{D'^2 R}{D'^2 R + R_L + DR_{on} + D'R_D}\right)$$

$$\frac{V}{V_g} = \left(\frac{1}{D'}\right)\left(1 - \frac{D'V_D}{V_g}\right)\left(\frac{1}{1 + \dfrac{R_L + DR_{on} + D'R_D}{D'^2 R}}\right)$$

Solution for converter efficiency

$$P_{in} = (V_g)\,(I)$$

$$P_{out} = (V)\,(D'I)$$



$$\eta = D'\,\frac{V}{V_g} = \frac{\left(1 - \dfrac{D'V_D}{V_g}\right)}{\left(1 + \dfrac{R_L + DR_{on} + D'R_D}{D'^2 R}\right)}$$

Conditions for high efficiency:

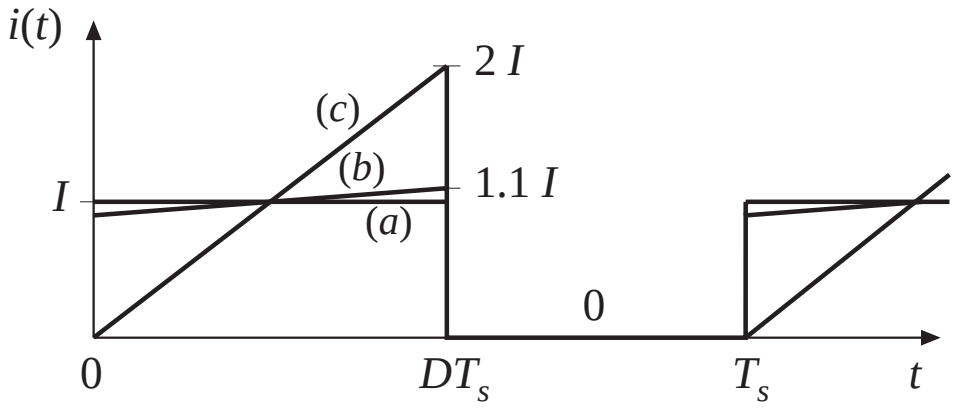
$$V_g/D' \gg V_D$$

$$D'^2 R \gg R_L + DR_{on} + D'R_D$$

Accuracy of the averaged equivalent circuit in prediction of losses

- Model uses average currents and voltages
- To correctly predict power loss in a resistor, use rms values
- Result is the same, provided ripple is small

MOSFET current waveforms, for various ripple magnitudes:



Inductor current ripple	*MOSFET rms current*	*Average power loss in* R_{on}
(a) $\Delta i = 0$	$I\sqrt{D}$	$D\,I^2\,R_{on}$
(b) $\Delta i = 0.1\,I$	$(1.00167)\,I\sqrt{D}$	$(1.0033)\,D\,I^2\,R_{on}$
(c) $\Delta i = I$	$(1.155)\,I\sqrt{D}$	$(1.3333)\,D\,I^2\,R_{on}$

Summary of chapter 3

1. The dc transformer model represents the primary functions of any dc-dc converter: transformation of dc voltage and current levels, ideally with 100% efficiency, and control of the conversion ratio M via the duty cycle D. This model can be easily manipulated and solved using familiar techniques of conventional circuit analysis.
2. The model can be refined to account for loss elements such as inductor winding resistance and semiconductor on-resistances and forward voltage drops. The refined model predicts the voltages, currents, and efficiency of practical nonideal converters.
3. In general, the dc equivalent circuit for a converter can be derived from the inductor volt-second balance and capacitor charge balance equations. Equivalent circuits are constructed whose loop and node equations coincide with the volt-second and charge balance equations. In converters having a pulsating input current, an additional equation is needed to model the converter input port; this equation may be obtained by averaging the converter input current.

Chapter 4. Switch Realization

4.1. Switch applications

Single-, two-, and four-quadrant switches. Synchronous rectifiers

4.2. A brief survey of power semiconductor devices

Power diodes, MOSFETs, BJTs, IGBTs, and thyristors

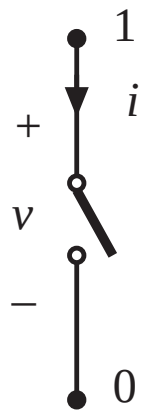
4.3. Switching loss

Transistor switching with clamped inductive load. Diode recovered charge. Stray capacitances and inductances, and ringing. Efficiency vs. switching frequency.

4.4. Summary of key points

SPST (single-pole single-throw) switches

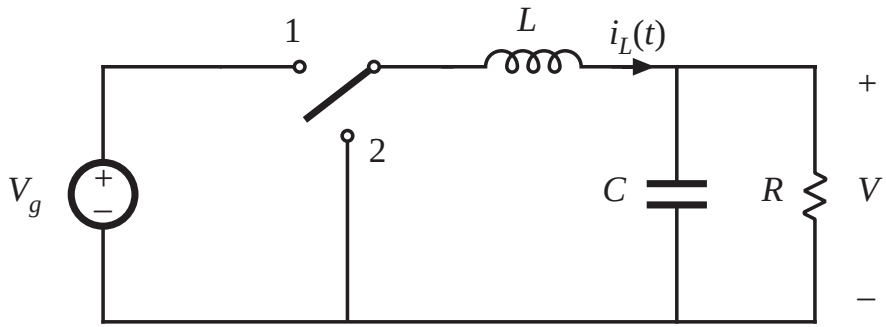
SPST switch, with voltage and current polarities defined



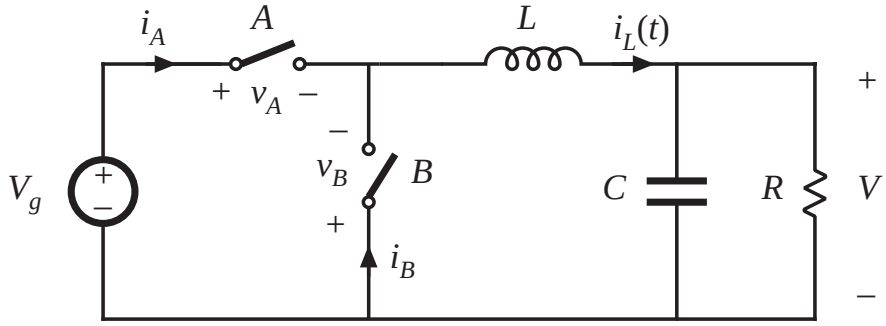
All power semiconductor devices function as SPST switches.

Buck converter

with SPDT switch:



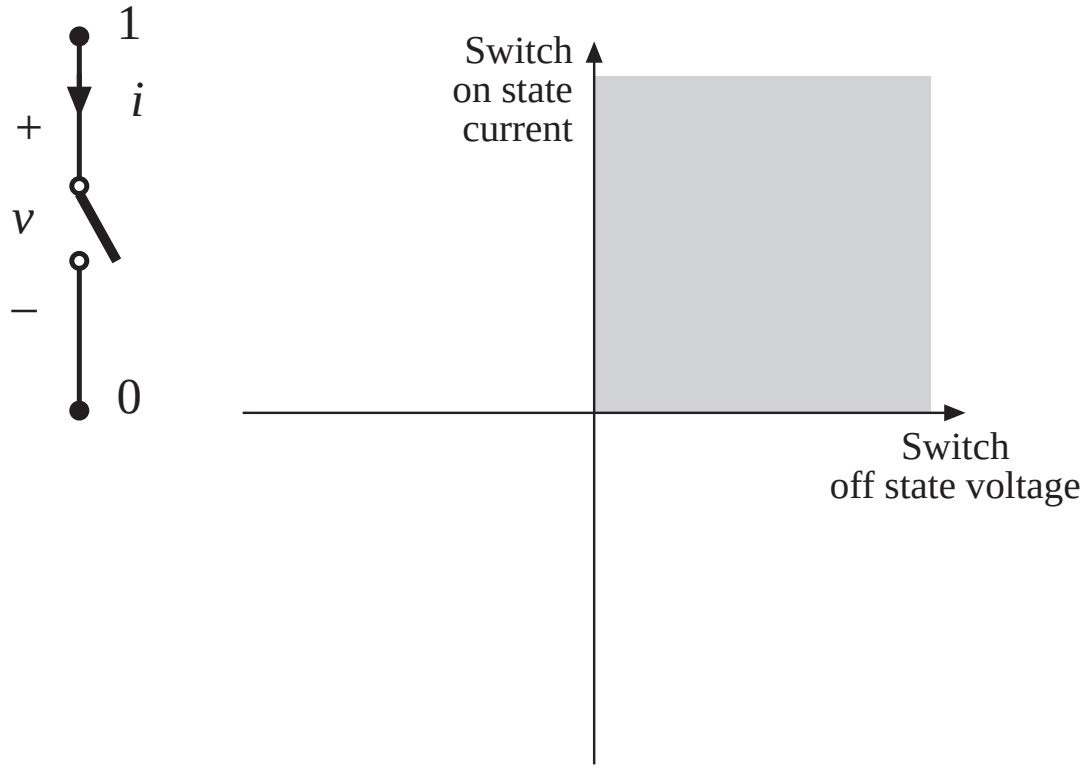
with two SPST switches:



Realization of SPDT switch using two SPST switches

- A nontrivial step: two SPST switches are not exactly equivalent to one SPDT switch
- It is possible for both SPST switches to be simultaneously ON or OFF
- Behavior of converter is then significantly modified —discontinuous conduction modes (chapter 5)
- Conducting state of SPST switch may depend on applied voltage or current —for example: diode

Quadrants of SPST switch operation



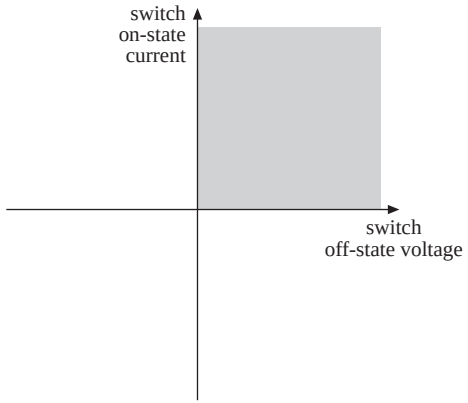
A single-quadrant switch example:

ON-state: $i > 0$

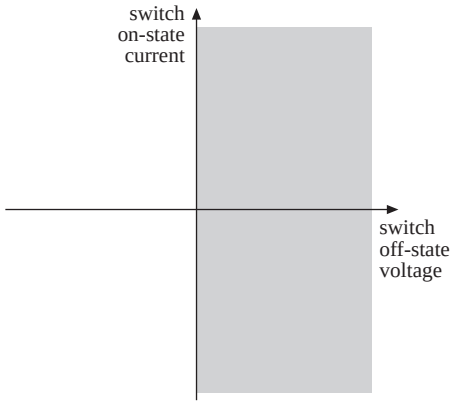
OFF-state: $v > 0$

Some basic switch applications

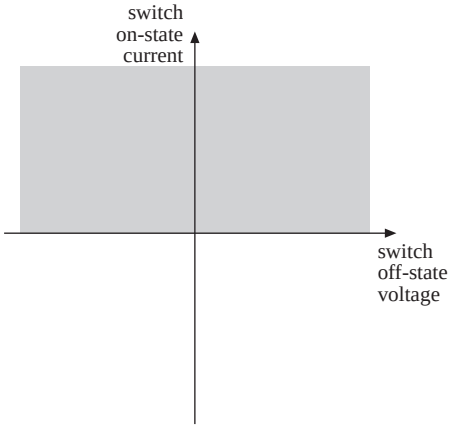
Single-quadrant switch



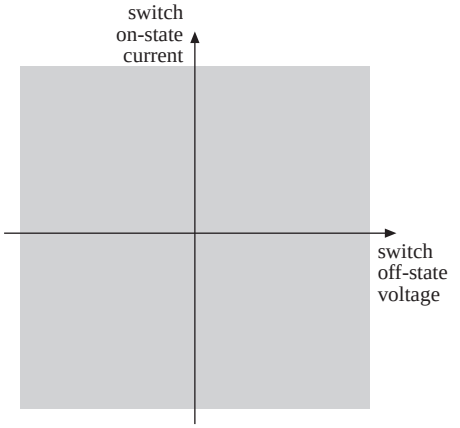
Current-bidirectional two-quadrant switch



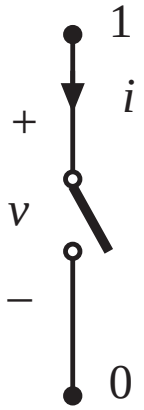
Voltage-bidirectional two-quadrant switch



Four-quadrant switch



4.1.1. Single-quadrant switches



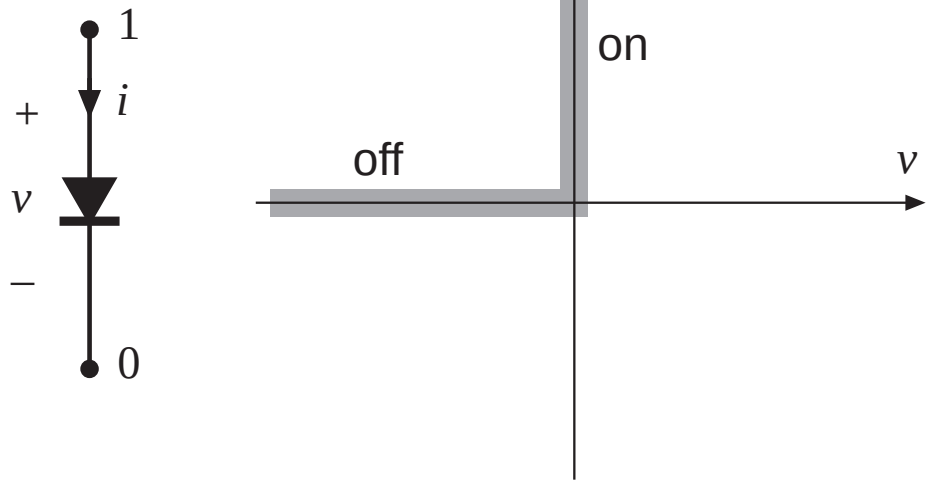
Active switch: Switch state is controlled exclusively by a third terminal (control terminal).

Passive switch: Switch state is controlled by the applied current and/or voltage at terminals 1 and 2.

SCR: A special case — turn-on transition is active, while turn-off transition is passive.

Single-quadrant switch: on-state $i(t)$ and off-state $v(t)$ are unipolar.

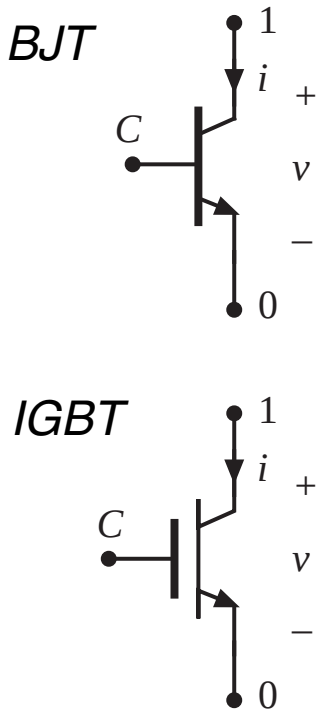
The diode

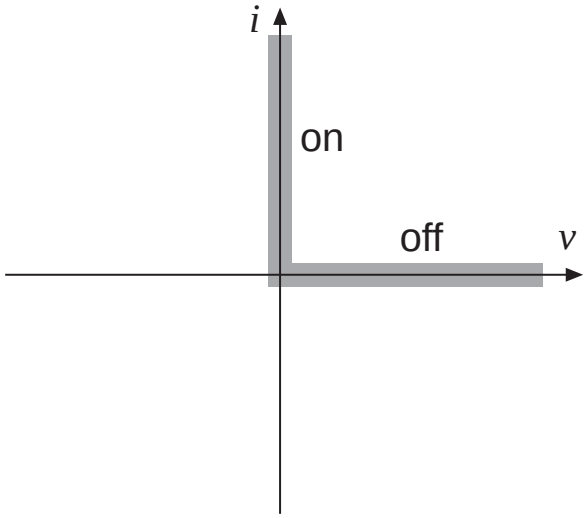


Symbol *instantaneous i-v characteristic*

- *A passive switch*
- *Single-quadrant switch:*
- *can conduct positive on-state current*
- *can block negative off-state voltage*
- *provided that the intended on-state and off-state operating points lie on the diode i-v characteristic, then switch can be realized using a diode*

The Bipolar Junction Transistor (BJT) and the Insulated Gate Bipolar Transistor (IGBT)

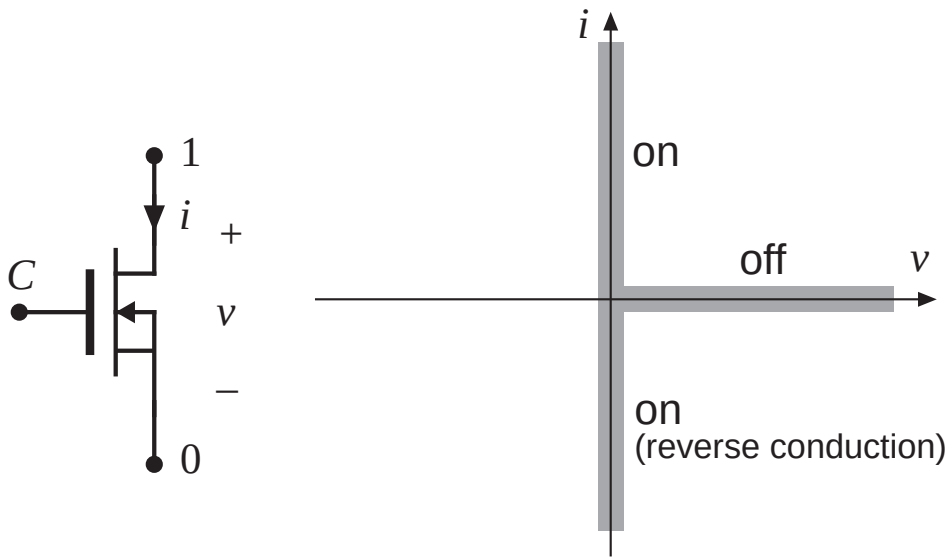




instantaneous i-v characteristic

- *An active switch, controlled by terminal C*
- *Single-quadrant switch:*
- *can conduct positive on-state current*
- *can block positive off-state voltage*
- *provided that the intended on-state and off-state operating points lie on the transistor i-v characteristic, then switch can be realized using a BJT or IGBT*

The Metal-Oxide Semiconductor Field Effect Transistor (MOSFET)

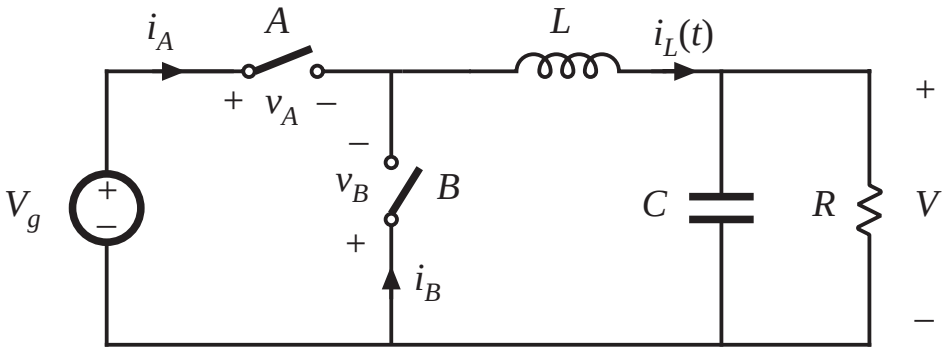


Symbol *instantaneous i-v characteristic*

- *An active switch, controlled by terminal C*
- *Normally operated as single-quadrant switch:*
- *can conduct positive on-state current (can also conduct negative current in some circumstances)*
- *can block positive off-state voltage*
- *provided that the intended on-state and off-state operating points lie on the MOSFET i-v characteristic, then switch can be realized using a MOSFET*

Realization of switch using transistors and diodes

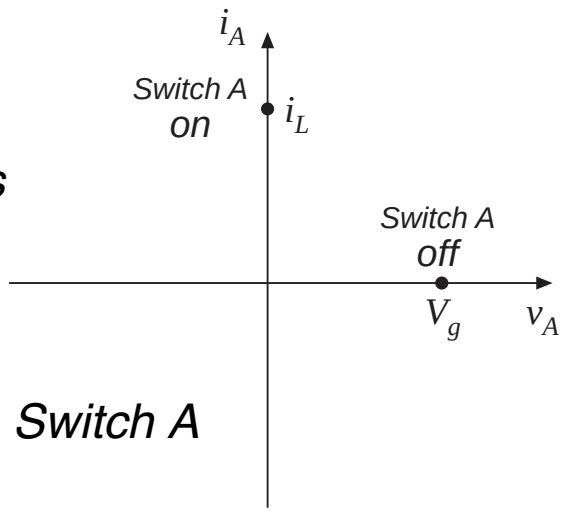
Buck converter example



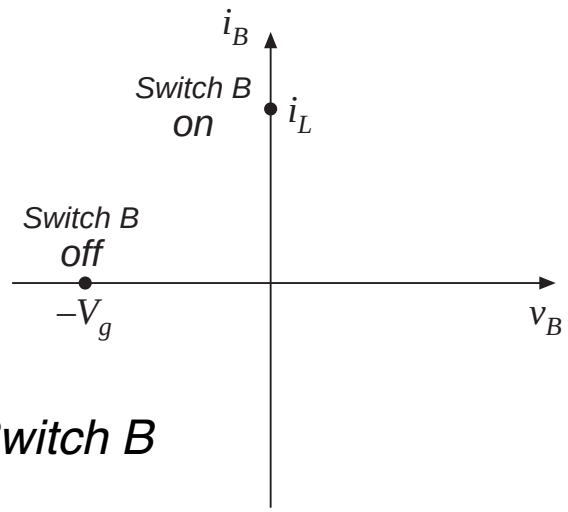
Switch A: transistor

Switch B: diode

SPST switch operating points

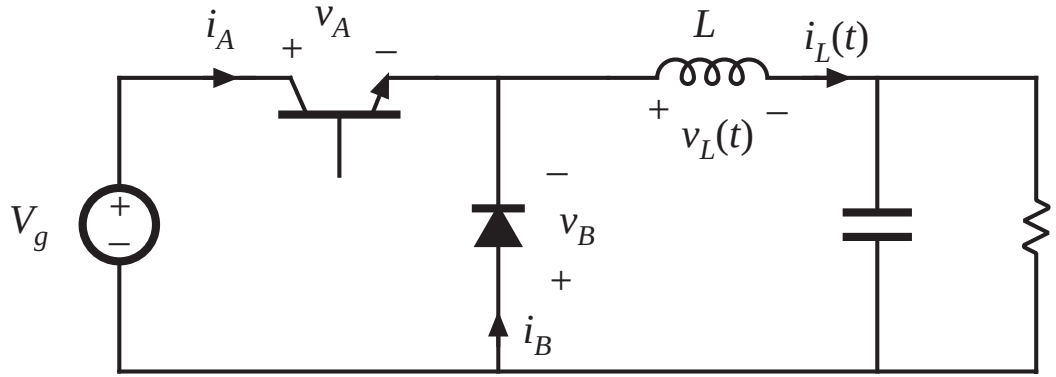


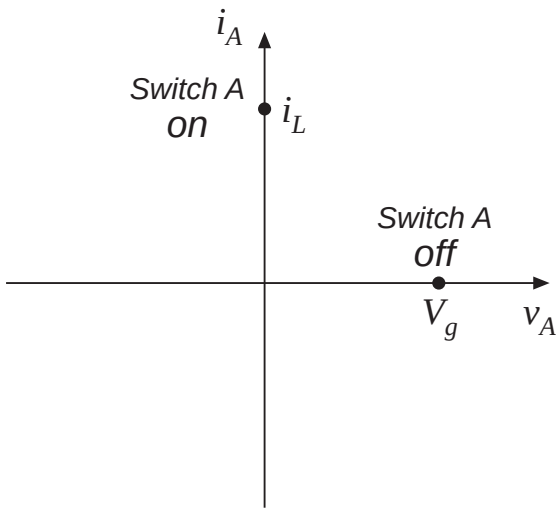
Switch A

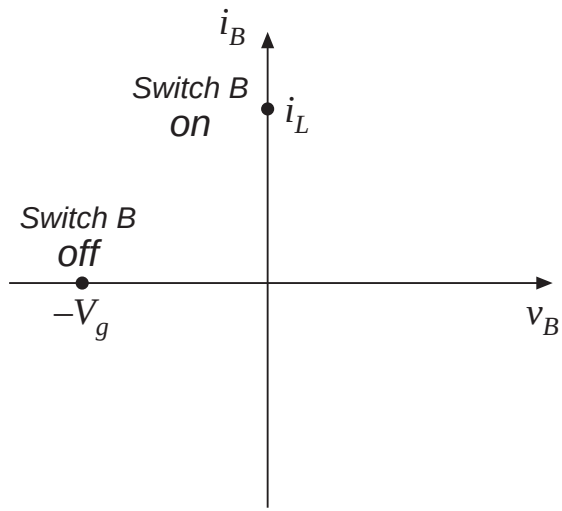


Switch B

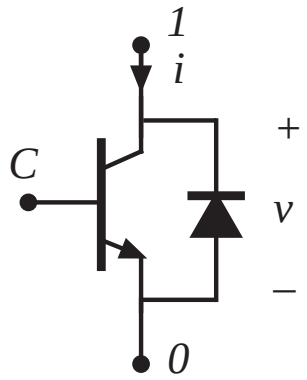
Realization of buck converter using single-quadrant switches



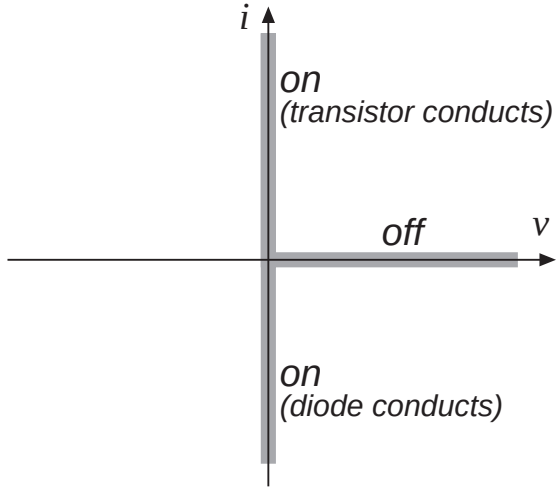




4.1.2. Current-bidirectional two-quadrant switches



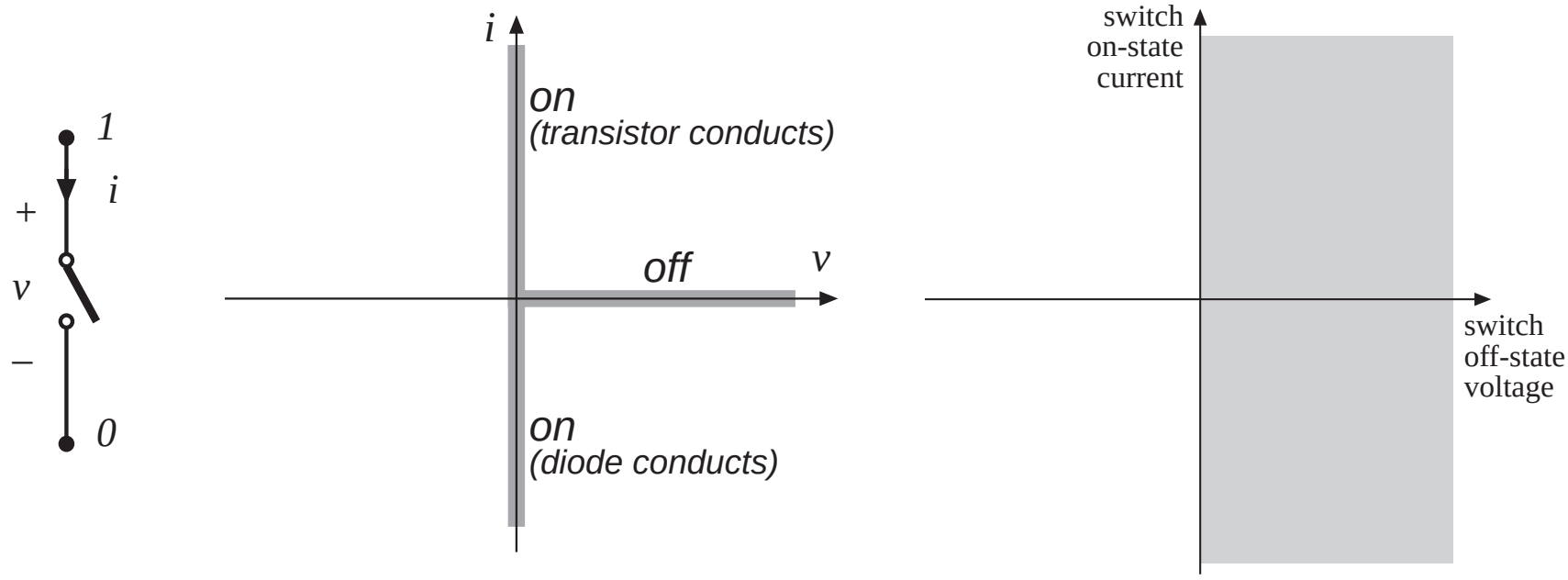
BJT / anti-parallel diode realization



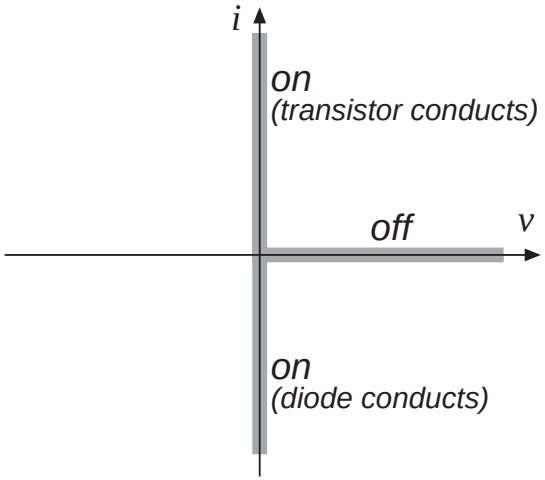
instantaneous i-v characteristic

- *Usually an active switch, controlled by terminal C*
- *Normally operated as two-quadrant switch:*
- *can conduct positive or negative on-state current*
- *can block positive off-state voltage*
- *provided that the intended on-state and off-state operating points lie on the composite i-v characteristic, then switch can be realized as shown*

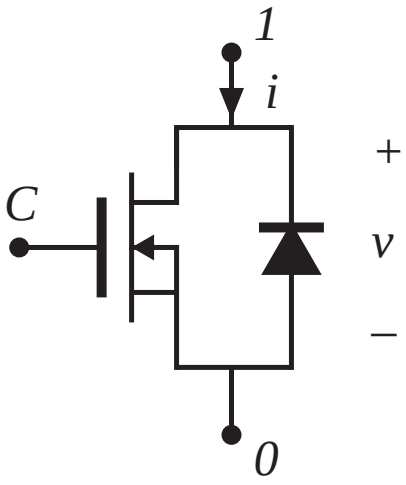
Two quadrant switches



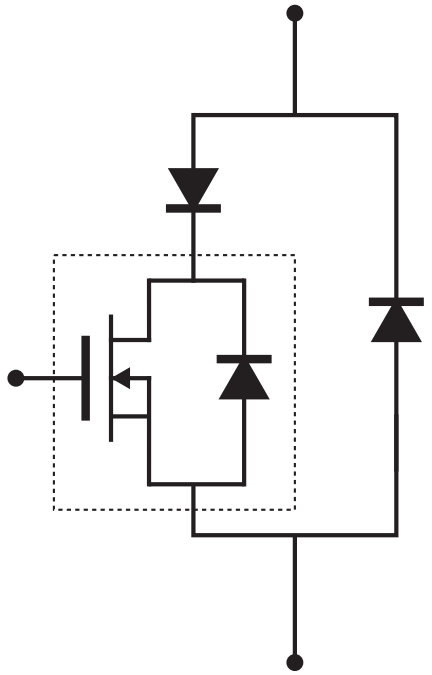
MOSFET body diode



Power MOSFET characteristics

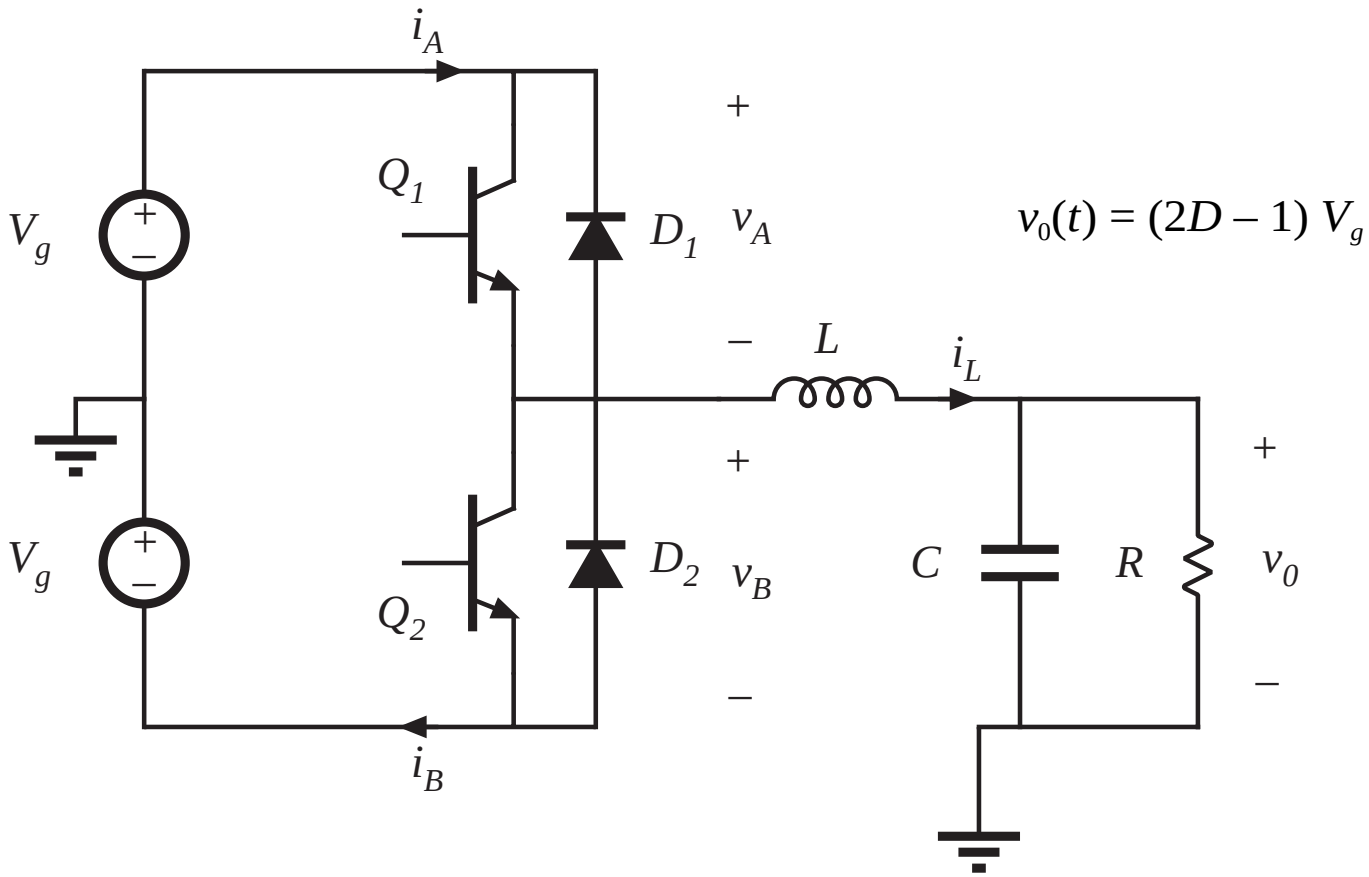


Power MOSFET, and its integral body diode



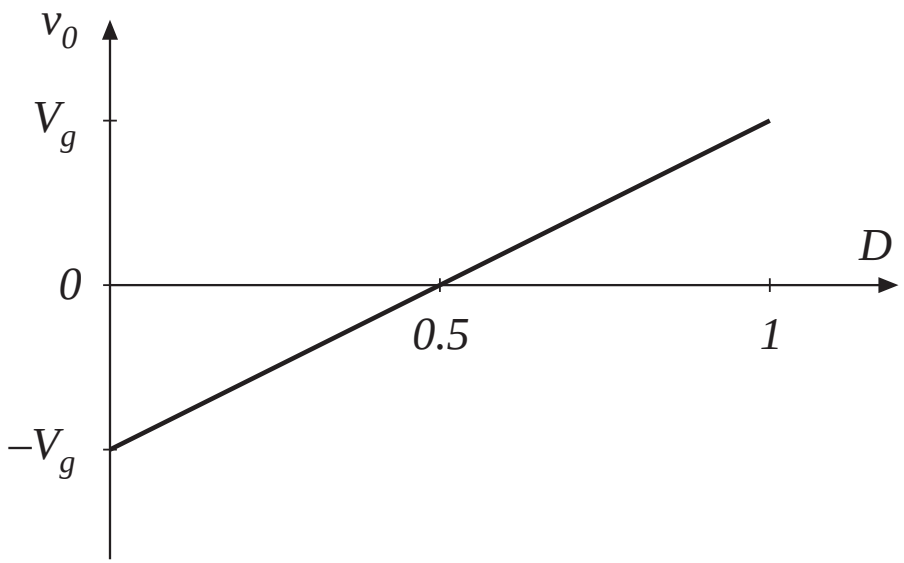
Use of external diodes to prevent conduction of body diode

A simple inverter



Inverter: sinusoidal modulation of D

$$v_0(t) = (2D - 1)\, V_g$$



Sinusoidal modulation to produce ac output:

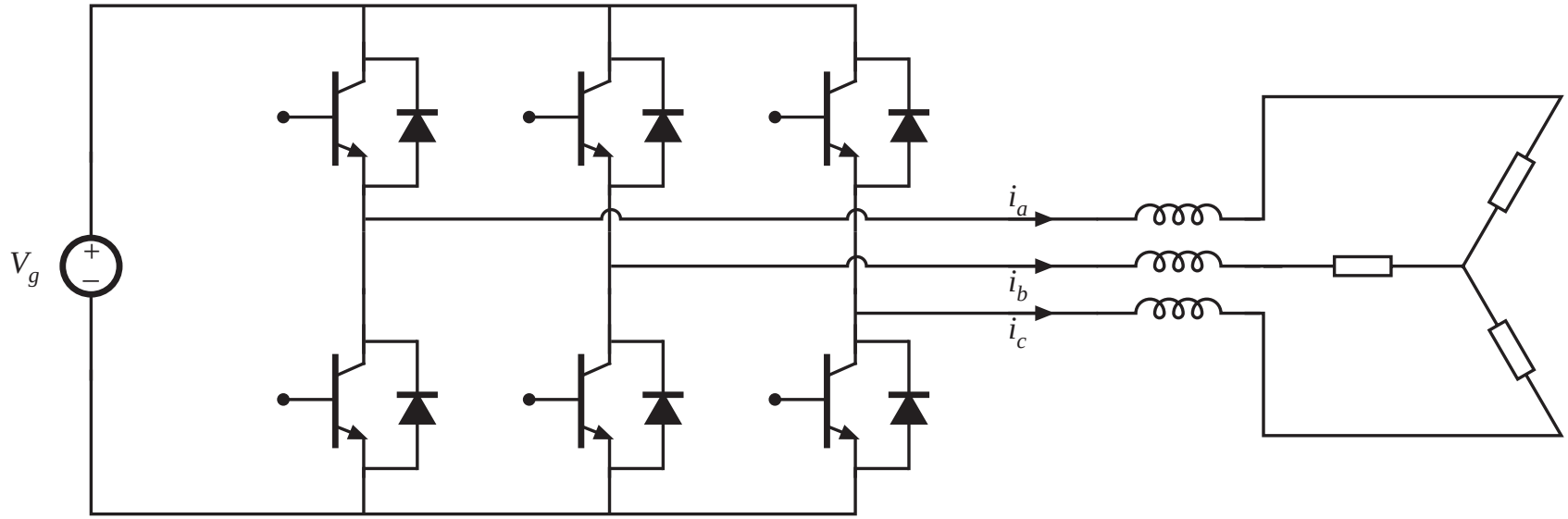
$$D(t) = 0.5 + D_m \sin(\omega t)$$

The resulting inductor current variation is also sinusoidal:

$$i_L(t) = \frac{v_0(t)}{R} = (2D - 1)\, \frac{V_g}{R}$$

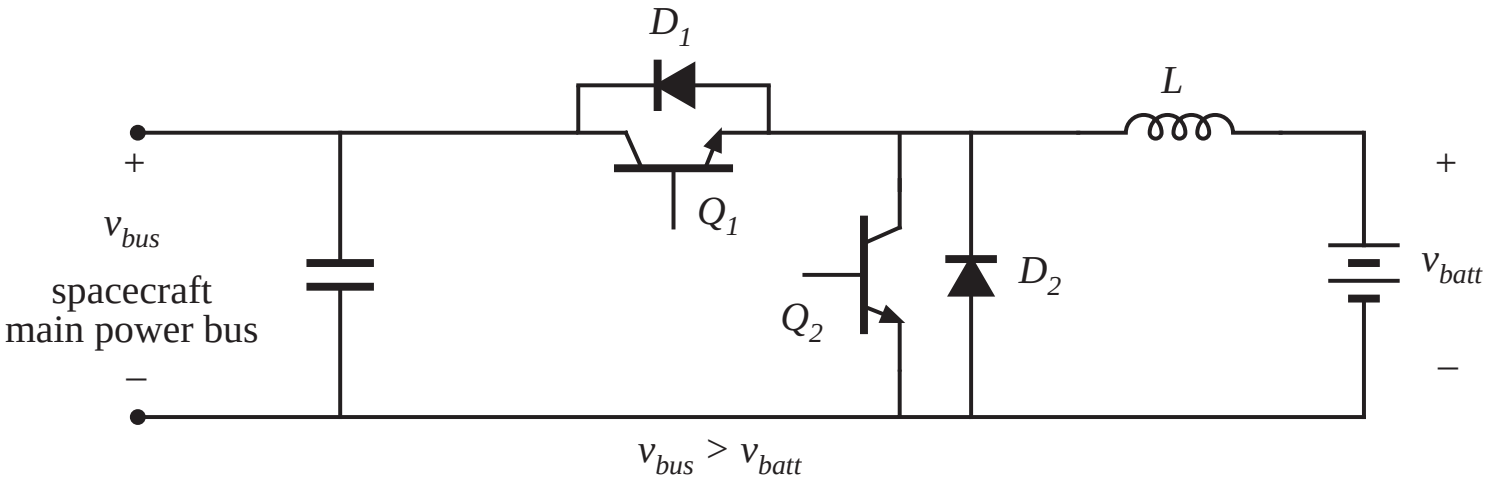
Hence, current-bidirectional two-quadrant switches are required.

The dc-3øac voltage source inverter (VSI)



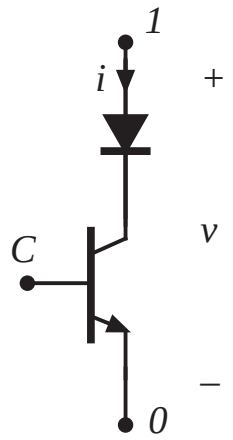
Switches must block dc input voltage, and conduct ac load current.

Bidirectional battery charger/discharger

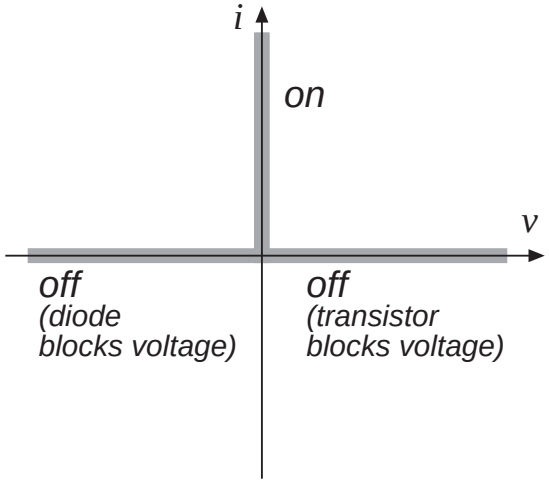


A dc-dc converter with bidirectional power flow.

4.1.3. Voltage-bidirectional two-quadrant switches



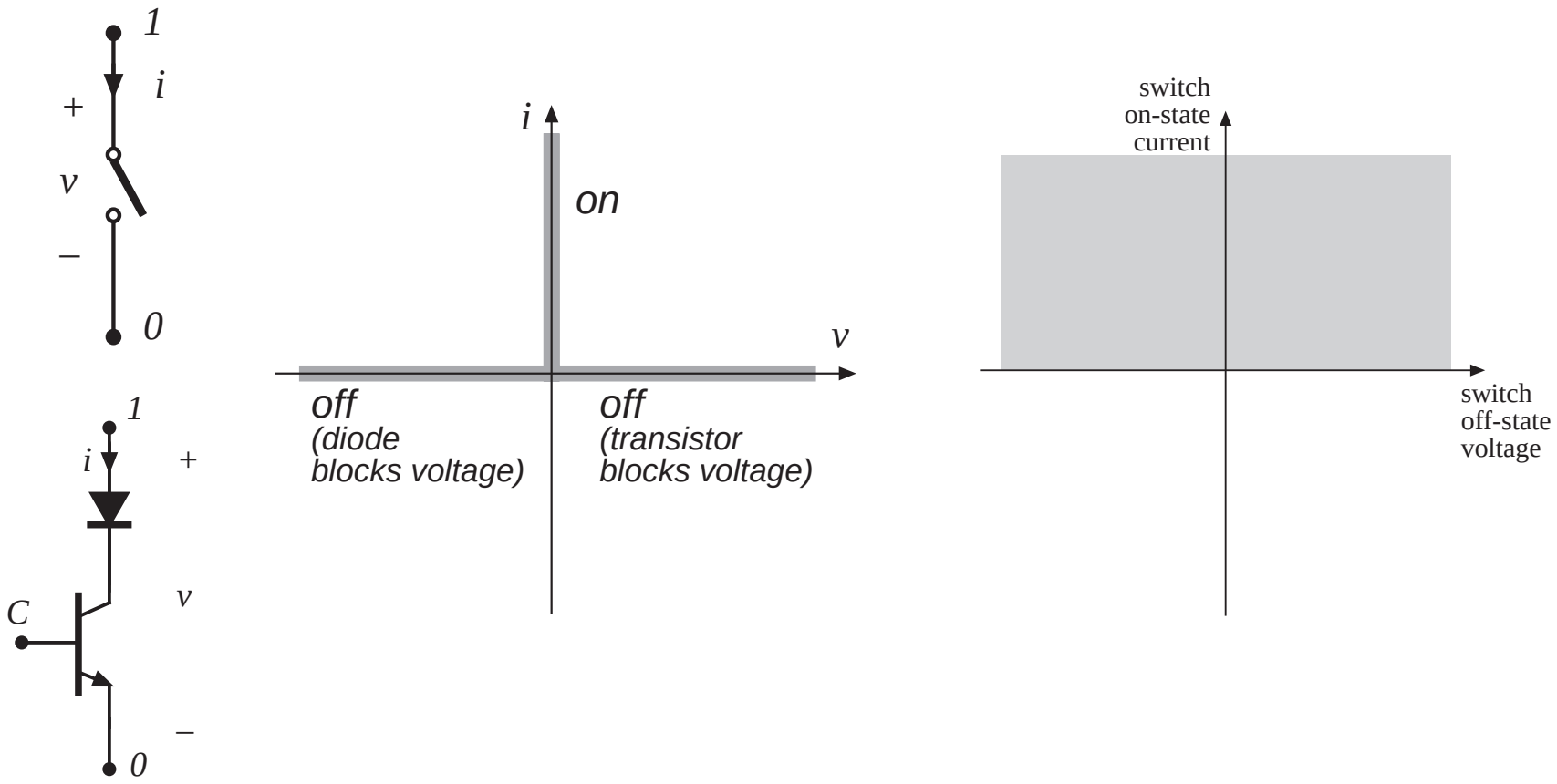
BJT / series diode realization



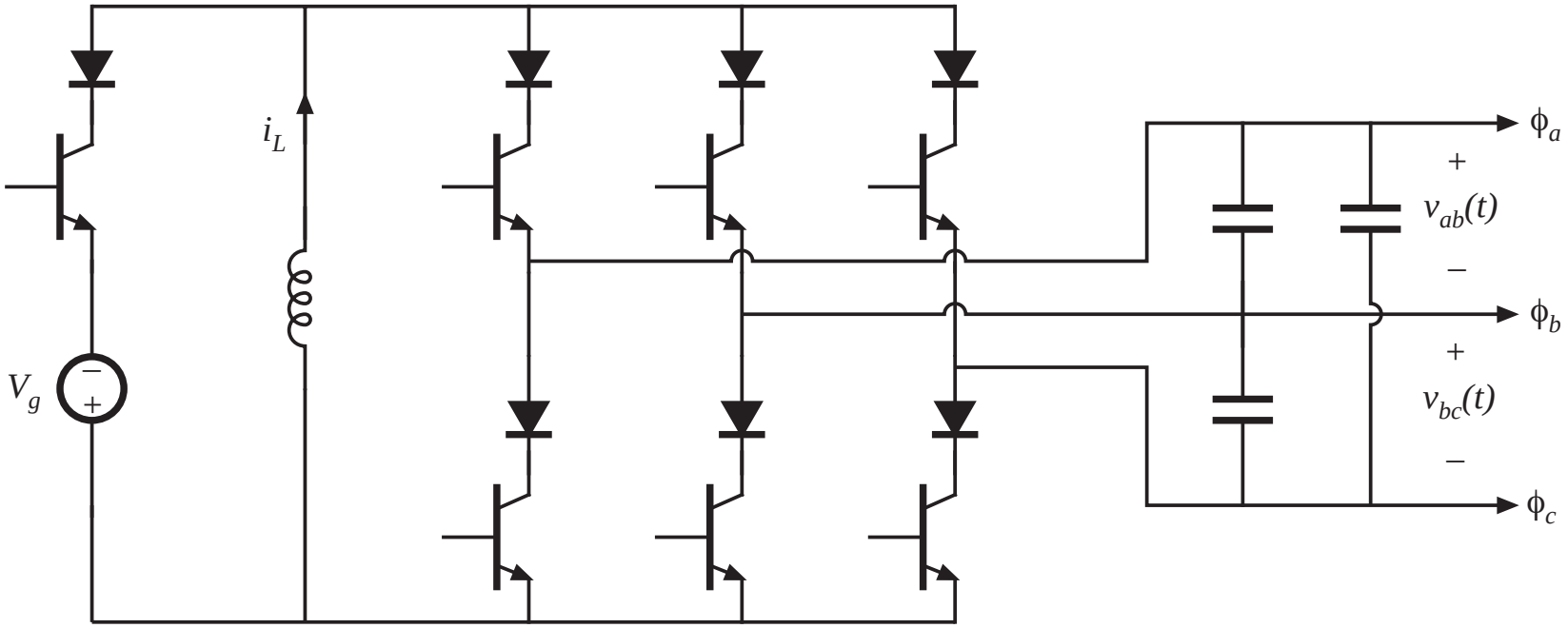
instantaneous i-v characteristic

- *Usually an active switch, controlled by terminal C*
- *Normally operated as two-quadrant switch:*
- *can conduct positive on-state current*
- *can block positive or negative off-state voltage*
- *provided that the intended on-state and off-state operating points lie on the composite i-v characteristic, then switch can be realized as shown*
- *The SCR is such a device, without controlled turn-off*

Two-quadrant switches



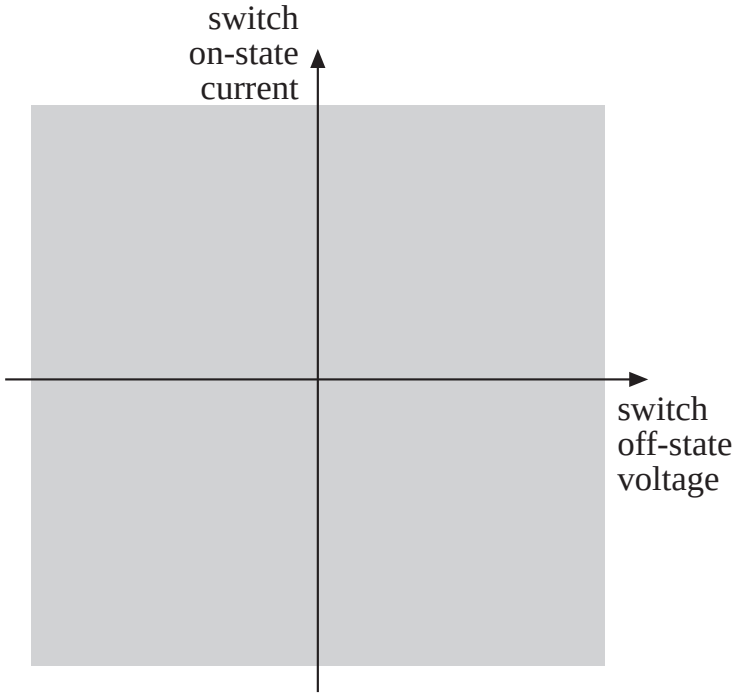
A dc-3øac buck-boost inverter



Requires voltage-bidirectional two-quadrant switches.

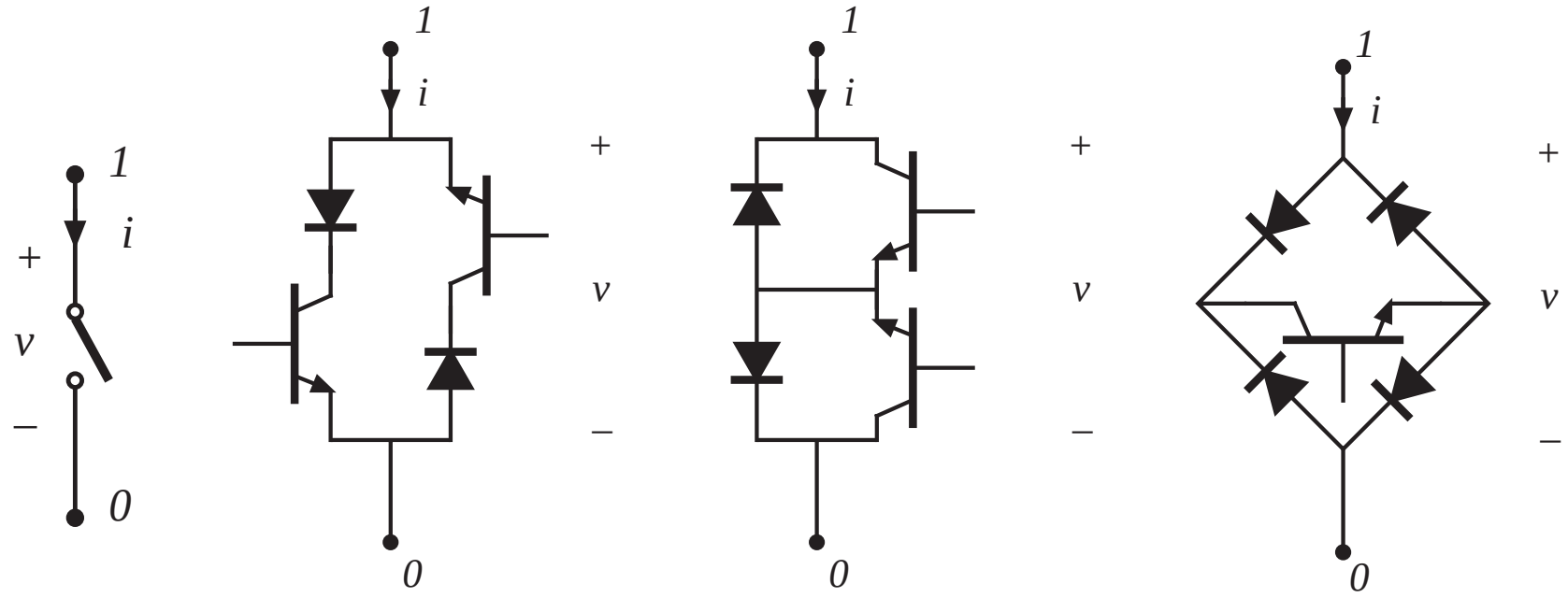
Another example: boost-type inverter, or current-source inverter (CSI).

4.1.4. Four-quadrant switches

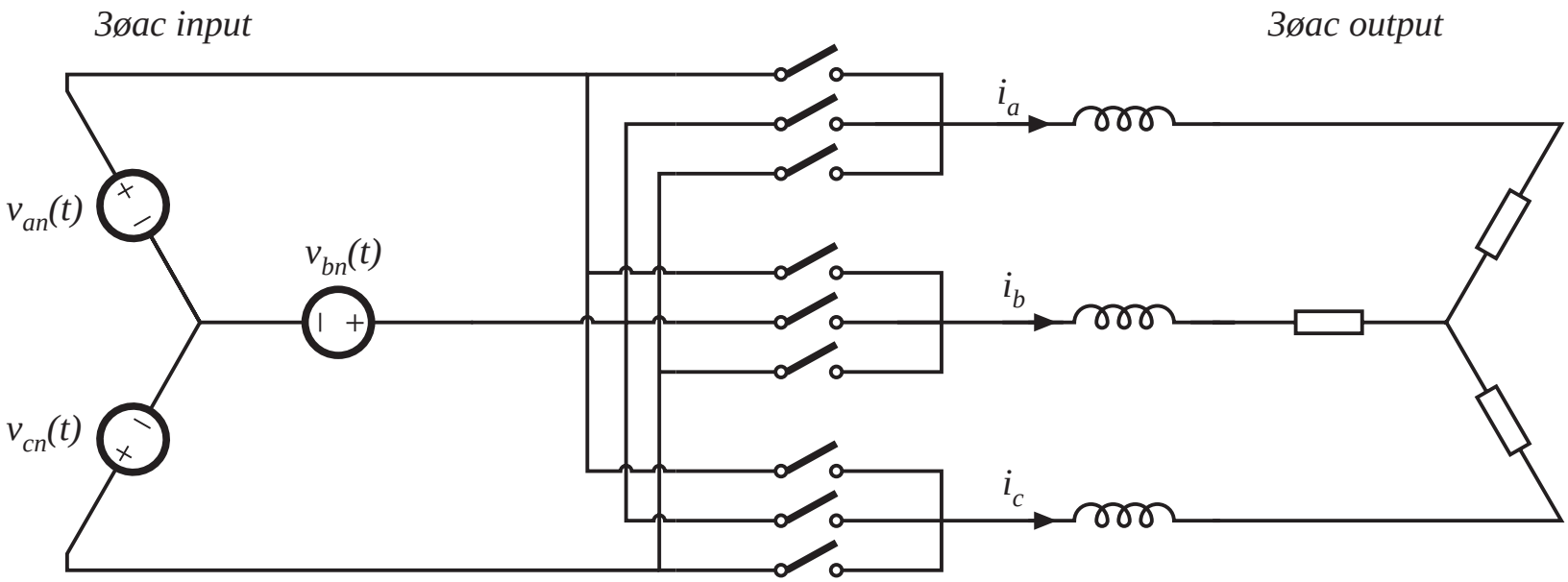


- *Usually an active switch, controlled by terminal C*
- *can conduct positive or negative on-state current*
- *can block positive or negative off-state voltage*

Three ways to realize a four-quadrant switch



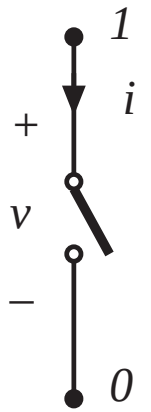
A 3øac-3øac matrix converter



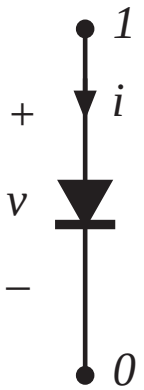
- All voltages and currents are ac; hence, four-quadrant switches are required.
- Requires nine four-quadrant switches

4.1.5. Synchronous rectifiers

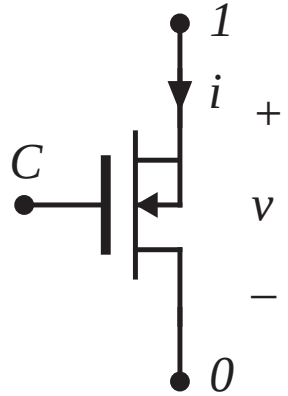
Replacement of diode with a backwards-connected MOSFET,
to obtain reduced conduction loss



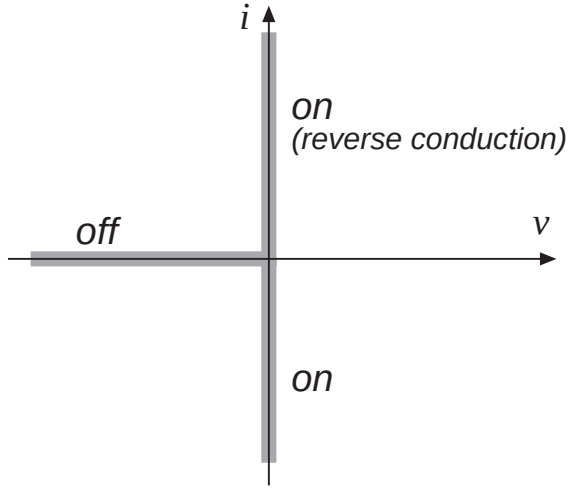
ideal switch



conventional diode rectifier

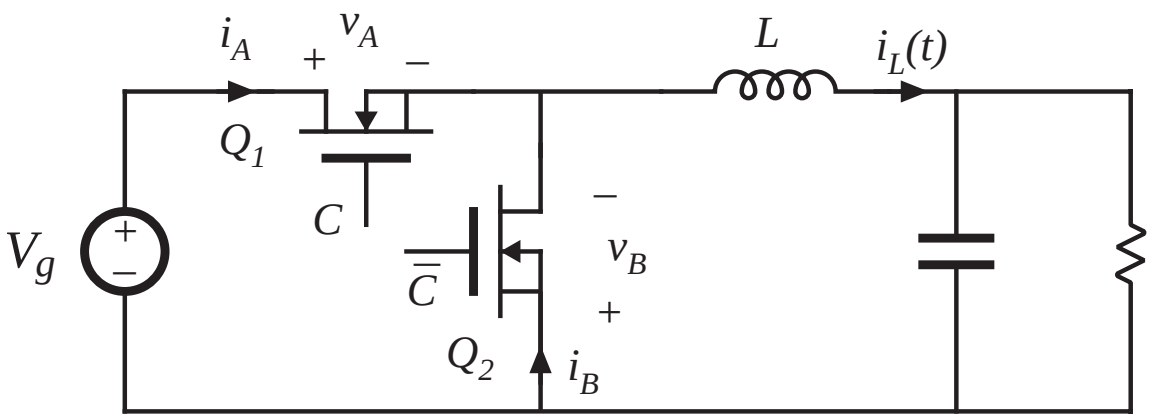


MOSFET as synchronous rectifier



instantaneous i-v characteristic

Buck converter with synchronous rectifier



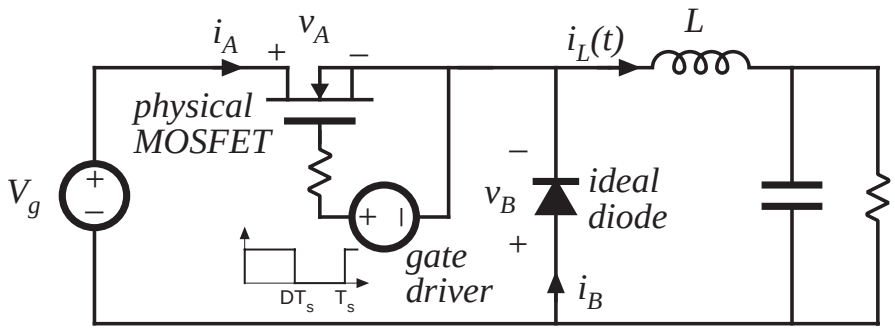
- MOSFET Q_2 is controlled to turn on when diode would normally conduct
- Semiconductor conduction loss can be made arbitrarily small, by reduction of MOSFET on-resistances
- Useful in low-voltage high-current applications

4.2. A brief survey of power semiconductor devices

- Power diodes
- Power MOSFETs
- Bipolar Junction Transistors (BJTs)
- Insulated Gate Bipolar Transistors (IGBTs)
- Thyristors (SCR, GTO, MCT)

- On resistance vs. breakdown voltage vs. switching times
- Minority carrier and majority carrier devices

4.3.1. Transistor switching with clamped inductive load

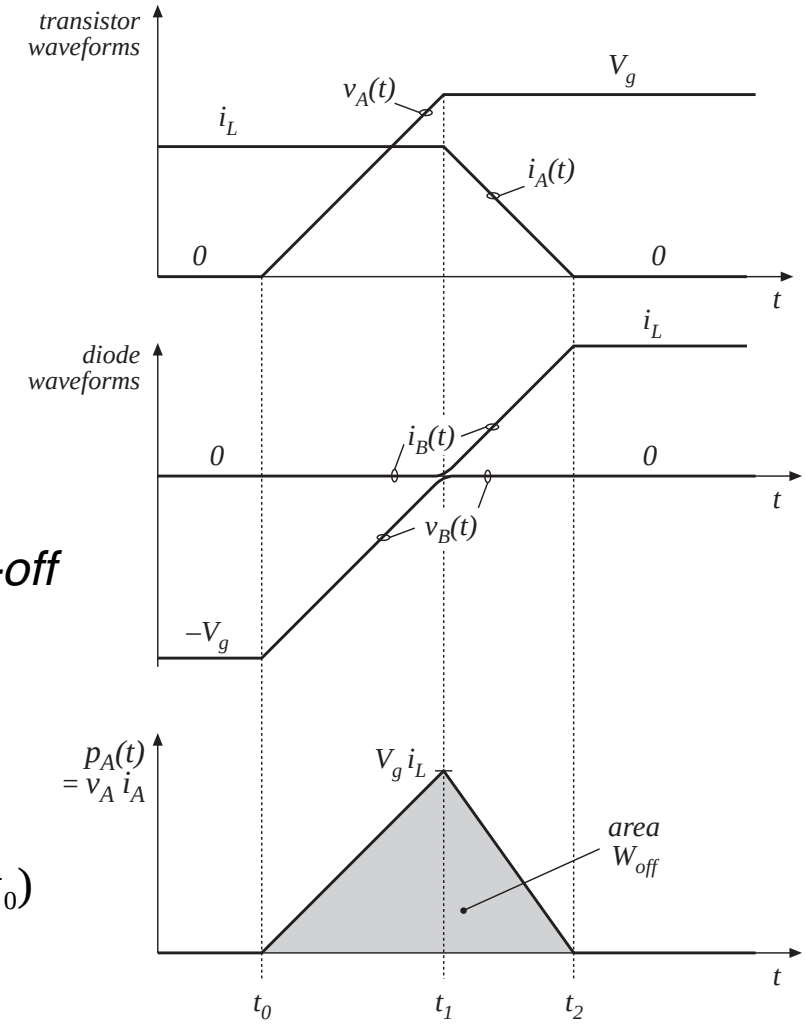


Buck converter example

$$v_B(t) = v_A(t) - V_g$$

$$i_A(t) + i_B(t) = i_L$$

transistor turn-off transition



$$W_{off} = \frac{1}{2}\, V_g i_L\, (t_2 - t_0)$$

Switching loss induced by transistor turn-off transition

Energy lost during transistor turn-off transition:

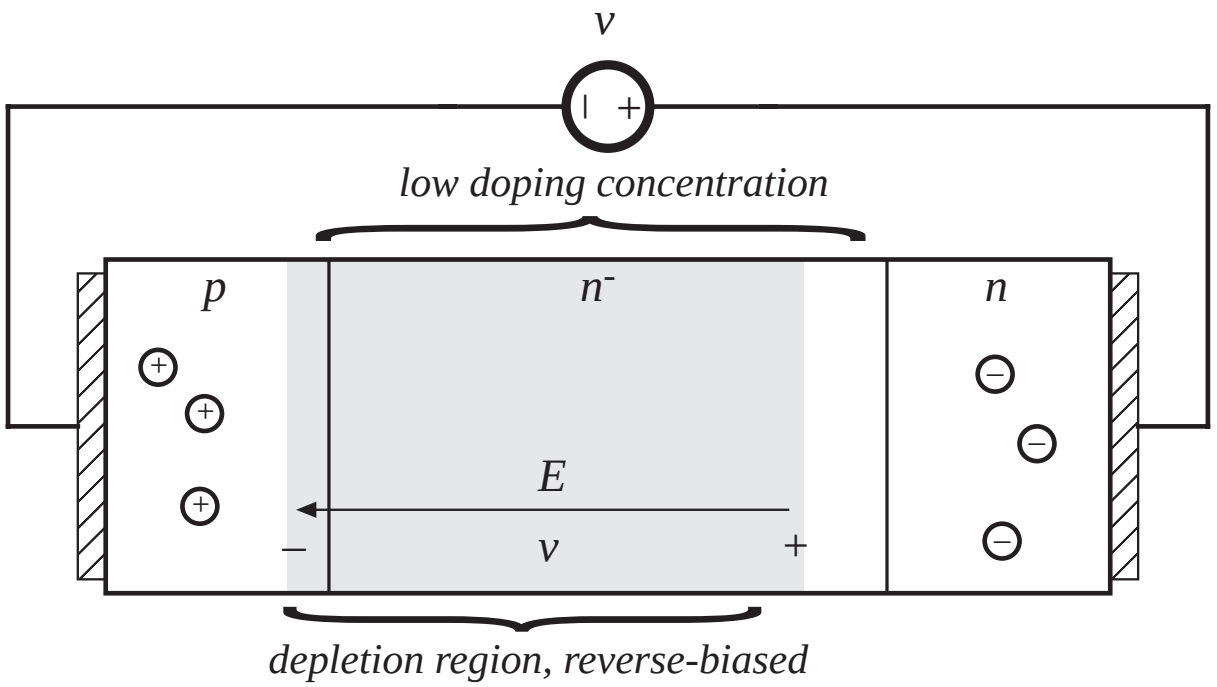
$$W_{off} = \frac{1}{2} V_g i_L (t_2 - t_0)$$

Similar result during transistor turn-on transition.
Average power loss:

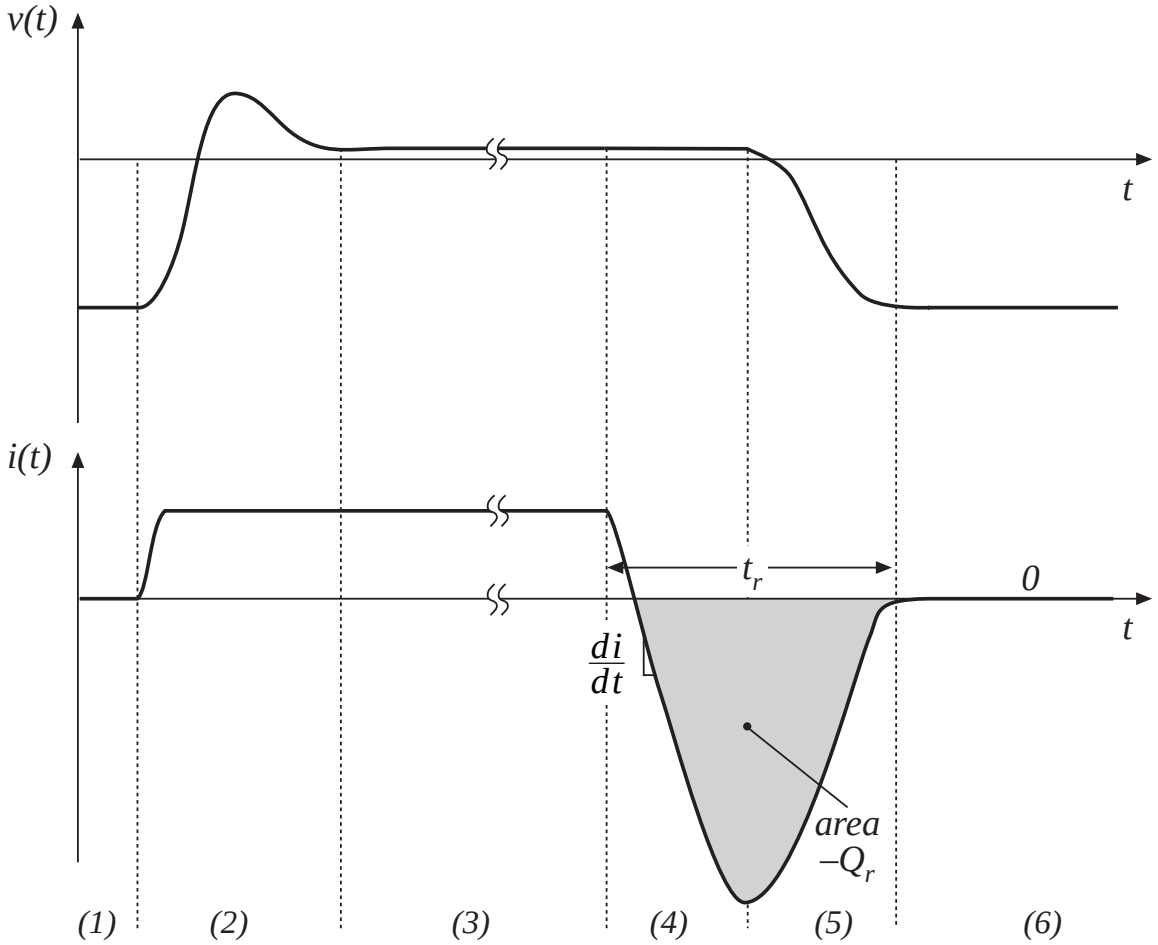
$$P_{sw} = \frac{1}{T_s} \int_{\substack{switching \\ transitions}} p_A(t)\, dt = (W_{on} + W_{off})\, f_s$$

4.2.1. Power diodes

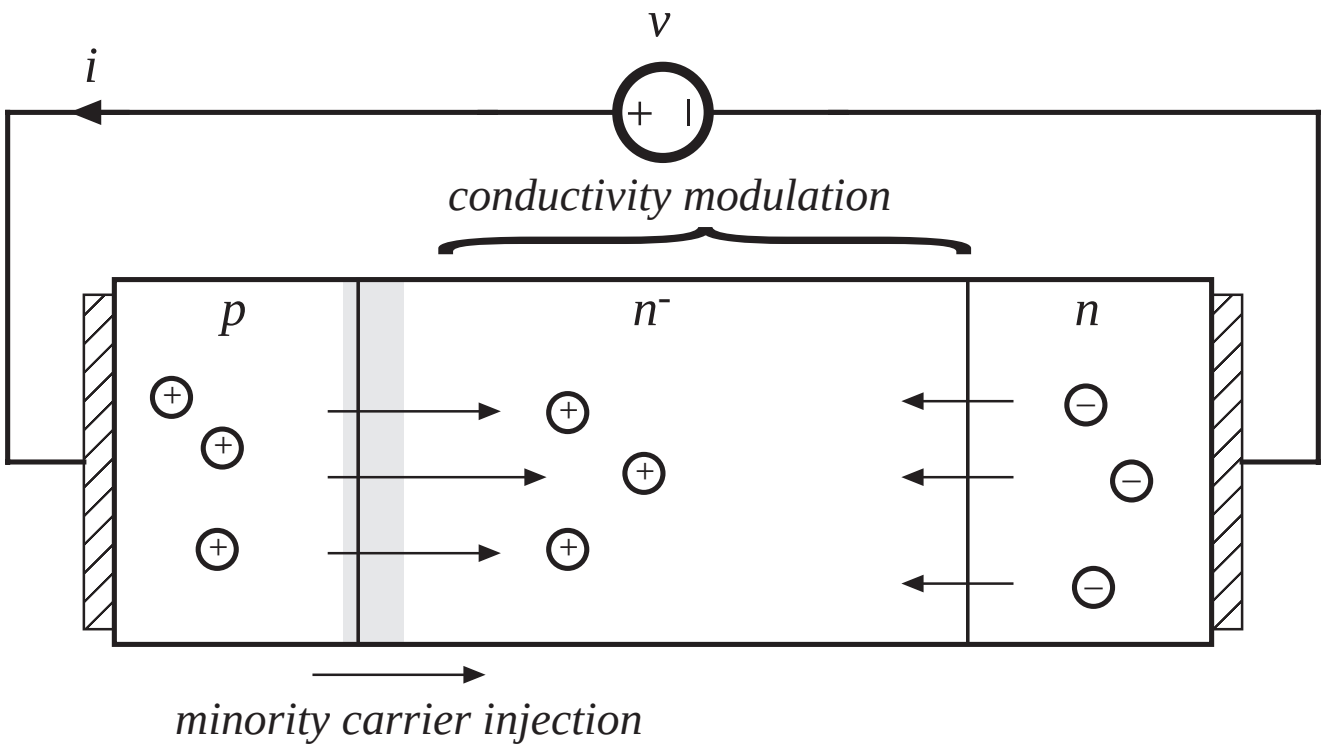
A power diode, under reverse-biased conditions:



Typical diode switching waveforms



Forward-biased power diode



Charge-controlled behavior of the diode

The diode equation:

$$q(t) = Q_0\left(e^{\lambda v(t)} - 1\right)$$

Charge control equation:

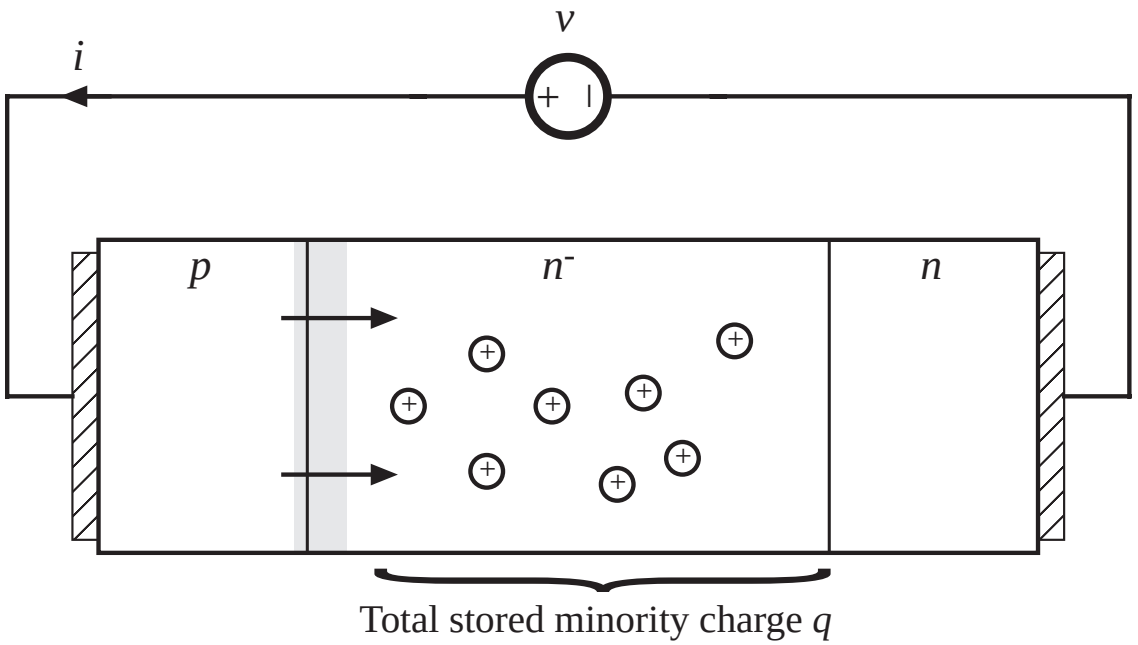
$$\frac{dq(t)}{dt} = i(t) - \frac{q(t)}{\tau_L}$$

With:

λ= 1/(26 mV) at 300 K

τ_L = minority carrier lifetime

(above equations don't include current that charges depletion region capacitance)



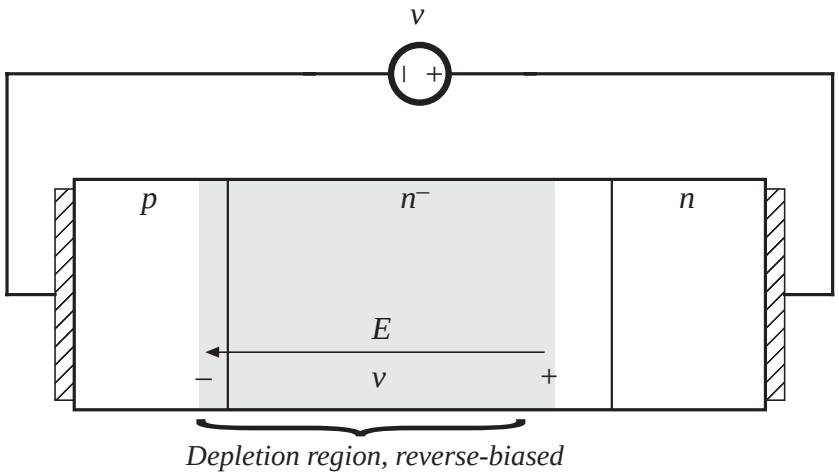
In equilibrium: $dq/dt = 0$, and hence

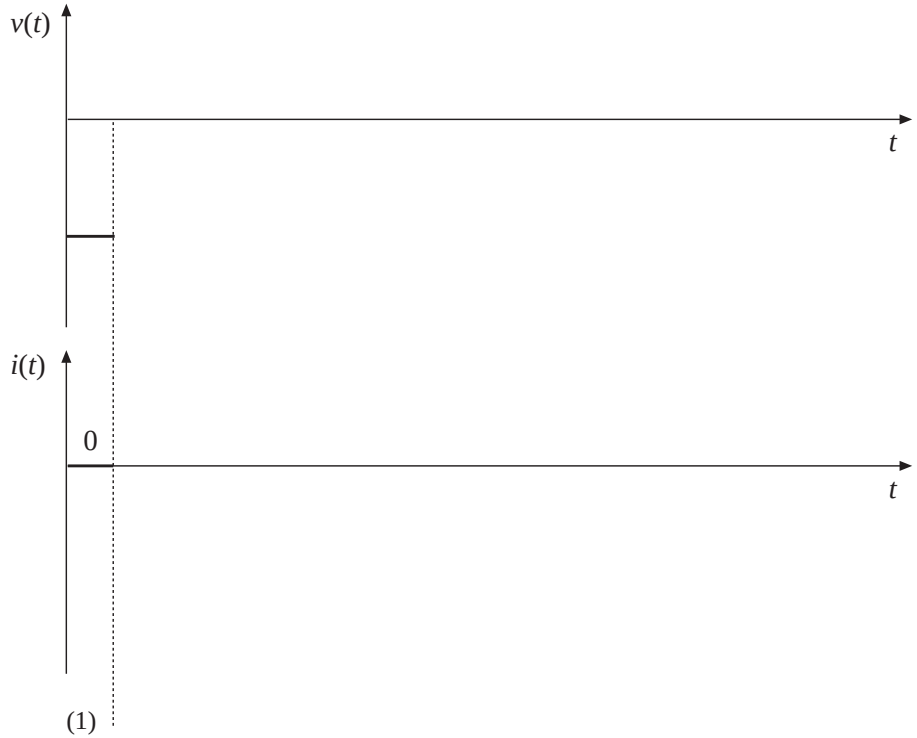
$$i(t) = \frac{q(t)}{\tau_L} = \frac{Q_0}{\tau_L}\left(e^{\lambda v(t)} - 1\right) = I_0\left(e^{\lambda v(t)} - 1\right)$$

Charge-control in the diode: Discussion

- The familiar i–v curve of the diode is an equilibrium relationship that can be violated during transient conditions
- During the turn-on and turn-off switching transients, the current deviates substantially from the equilibrium i–v curve, because of change in the stored charge and change in the charge within the reverse-bias depletion region
- Under forward-biased conditions, the stored minority charge causes “conductivity modulation” of the resistance of the lightly-doped n^- region, reducing the device on-resistance

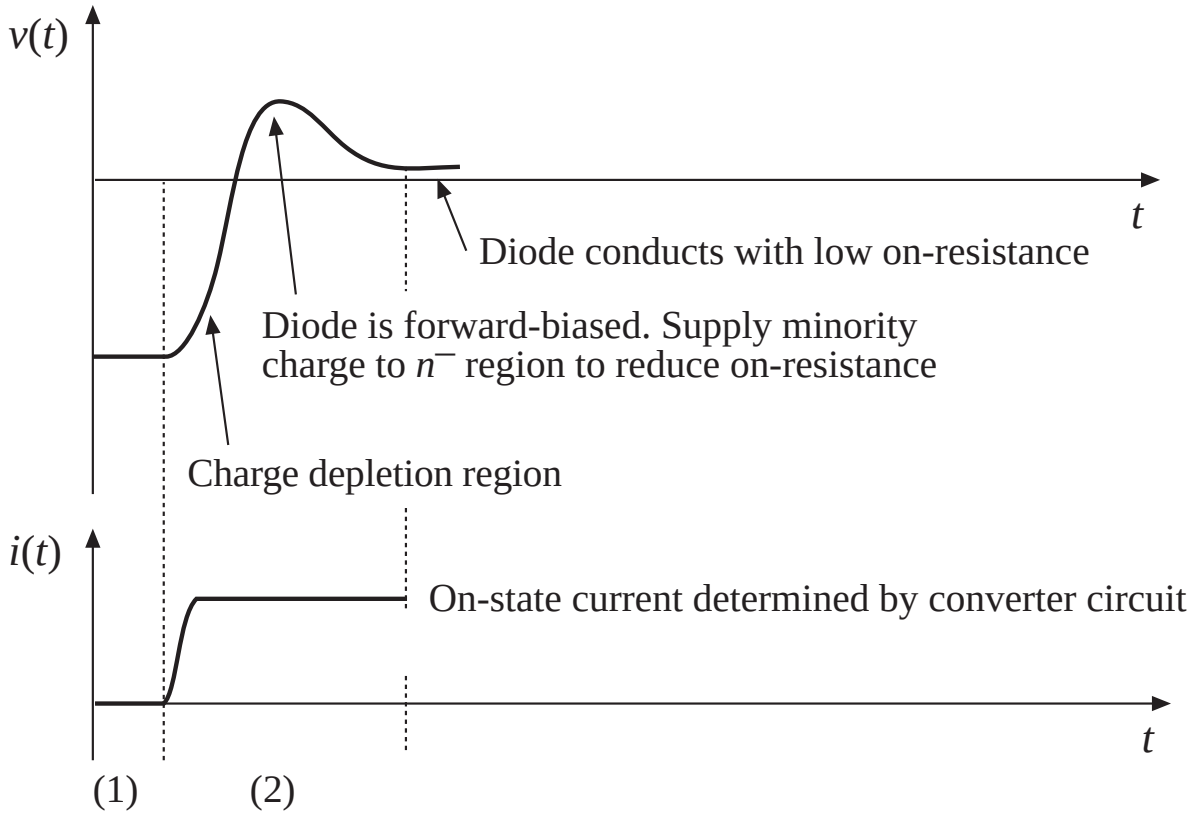
Diode in OFF state: reversed-biased, blocking voltage





- Diode is reverse-biased
- No stored minority charge: $q = 0$
- Depletion region blocks applied reverse voltage; charge is stored in capacitance of depletion region

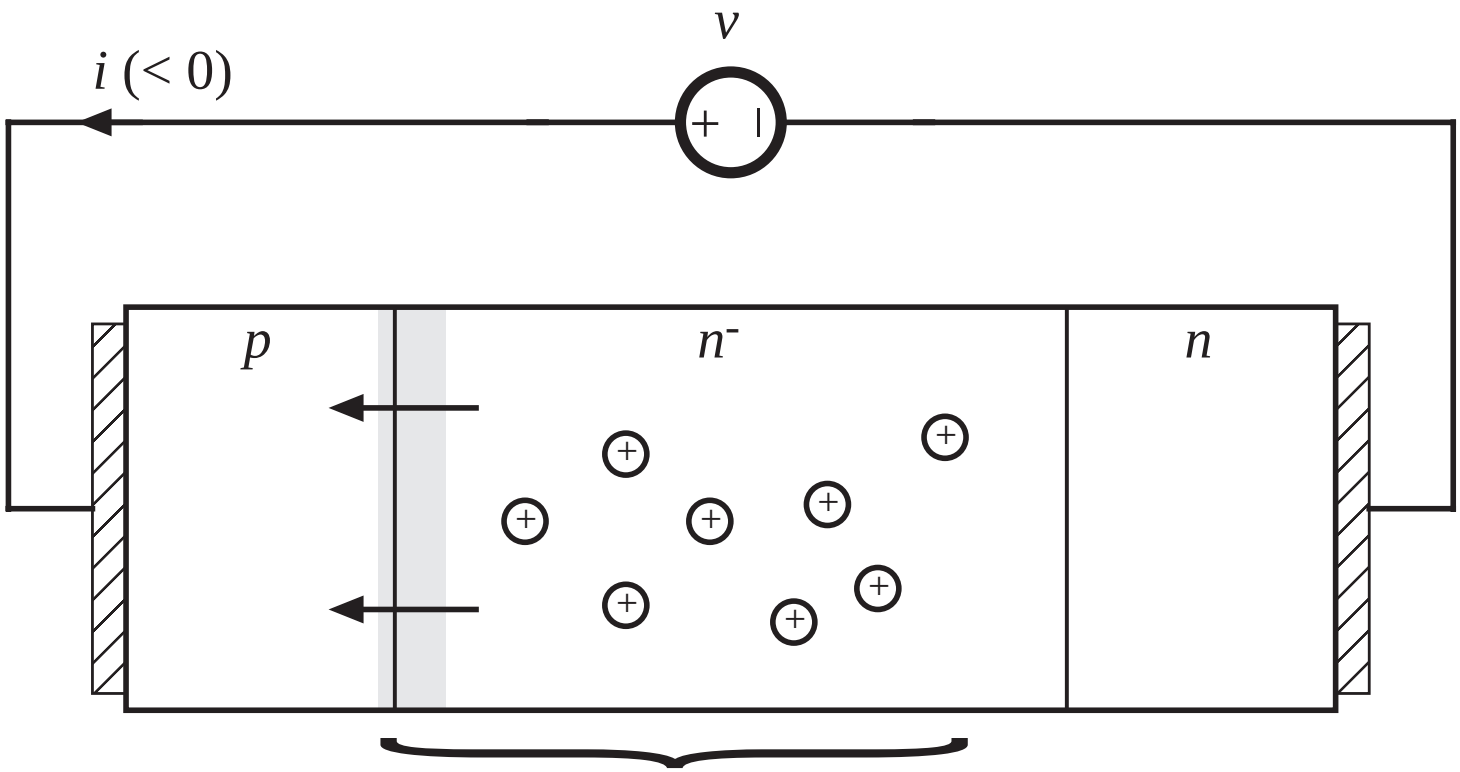
Turn-on transient



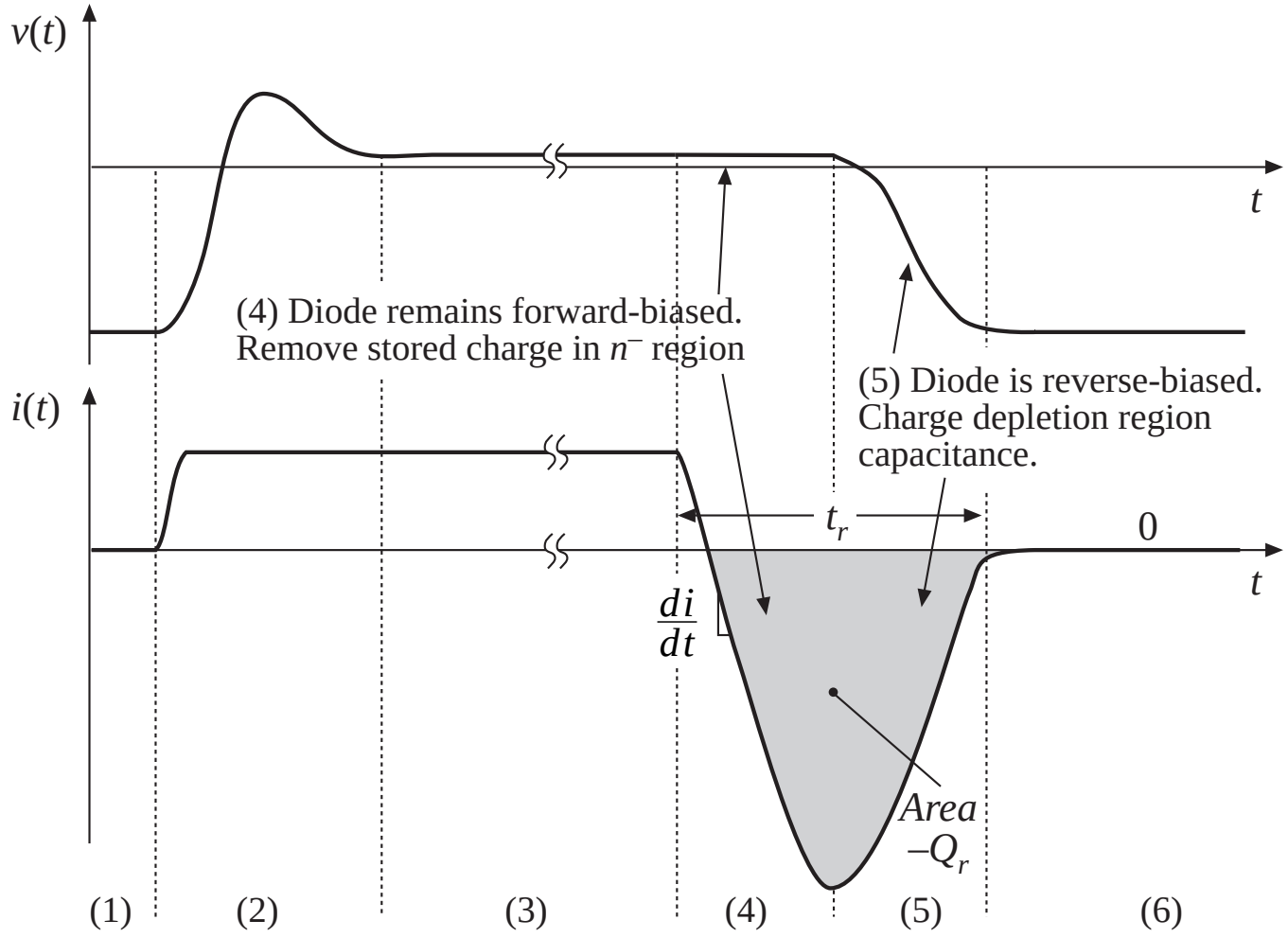
The current $i(t)$ is determined by the converter circuit. This current supplies:

- charge to increase voltage across depletion region
- charge needed to support the on-state current
- charge to reduce on-resistance of n^- region

Turn-off transient

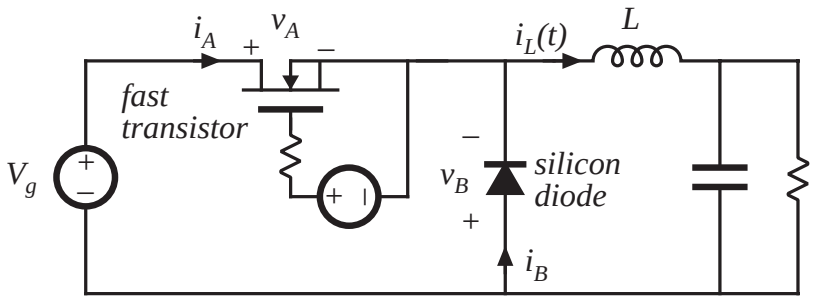


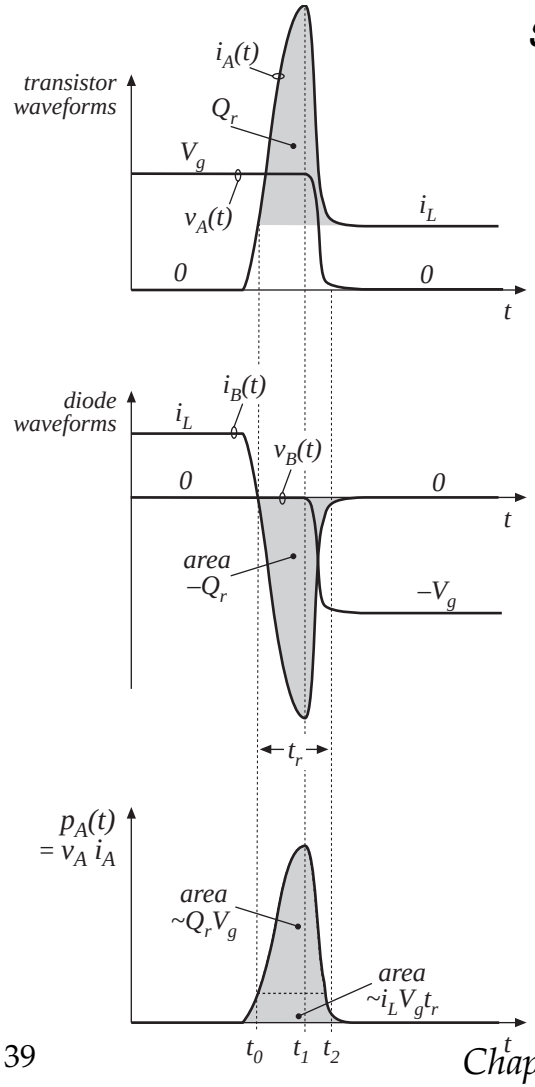
Diode turn-off transient
continued



The diode switching transients induce switching loss in the transistor

see Section 4.3.2





- Diode recovered stored charge Q_r flows through transistor during transistor turn-on transition, inducing switching loss
- Q_r depends on diode on-state forward current, and on the rate-of-change of diode current during diode turn-off transition

Switching loss calculation

Energy lost in transistor:

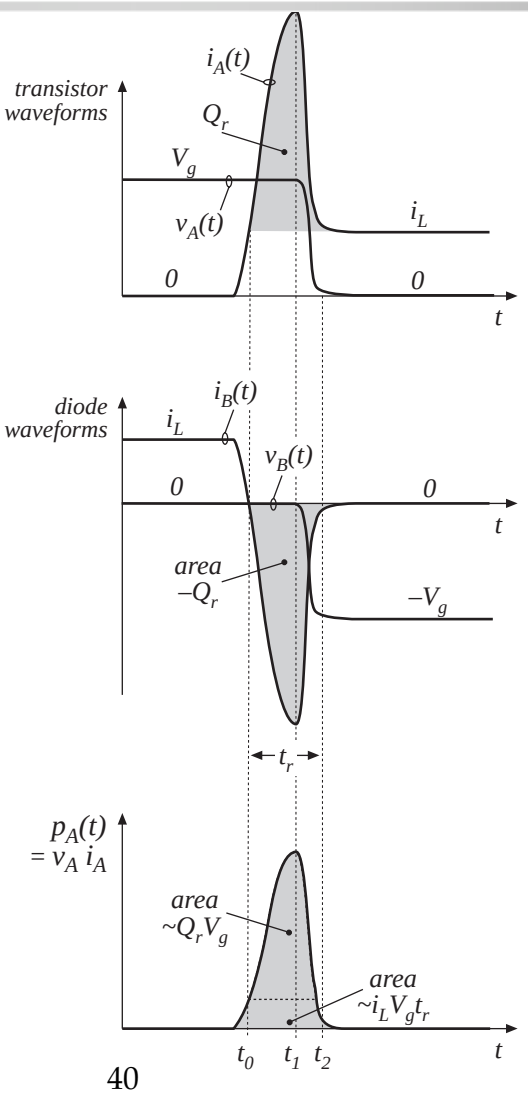
$$W_D = \int_{\substack{\text{switching} \\ \text{transition}}} v_A(t)\, i_A(t)\, dt$$

With abrupt-recovery diode:

$$W_D \approx \int_{\substack{\text{switching} \\ \text{transition}}} V_g\, (i_L - i_B(t))\, dt$$

$$= V_g\, i_L\, t_r + V_g\, Q_r$$

- *Often, this is the largest component of switching loss*



Soft-recovery diode:

$(t_2 - t_1) >> (t_1 - t_0)$

Abrupt-recovery diode:

$(t_2 - t_1) << (t_1 - t_0)$

Types of power diodes

Standard recovery

- Reverse recovery time not specified, intended for 50/60Hz

Fast recovery and ultra-fast recovery

- Reverse recovery time and recovered charge specified
- Intended for converter applications

Schottky diode

- A majority carrier device
- Essentially no recovered charge
- Model with equilibrium i-v characteristic, in parallel with depletion region capacitance
- Restricted to low voltage (few devices can block 100V or more)

Characteristics of several commercial power rectifier diodes

Part number	*Rated max voltage*	*Rated avg current*	V_F *(typical)*	t_r *(max)*
Fast recovery rectifiers				
1N3913	400V	30A	1.1V	400ns
SD453N25S20PC	2500V	400A	2.2V	2μs
Ultra-fast recovery rectifiers				
MUR815	150V	8A	0.975V	35ns
MUR1560	600V	15A	1.2V	60ns
RHRU100120	1200V	100A	2.6V	60ns
Schottky rectifiers				
MBR6030L	30V	60A	0.48V	
444CNQ045	45V	440A	0.69V	
30CPQ150	150V	30A	1.19V	

Paralleling diodes

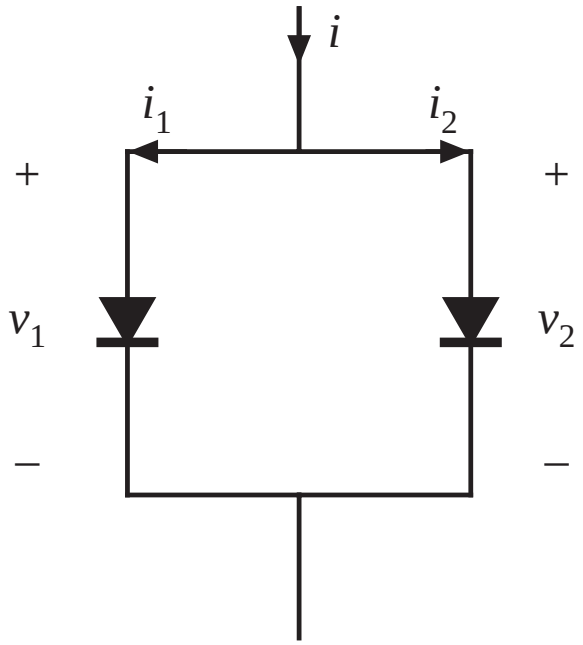
Attempts to parallel diodes, and share the current so that $i_1 = i_2 = i/2$, generally don't work.

Reason: thermal instability caused by temperature dependence of the diode equation.

Increased temperature leads to increased current, or reduced voltage.

One diode will hog the current.

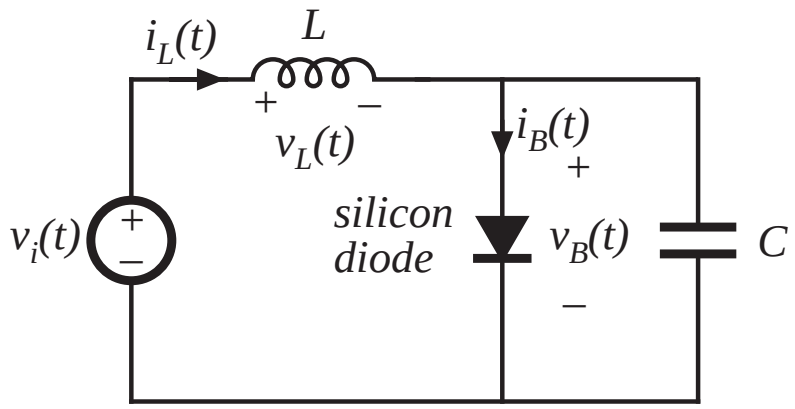
To get the diodes to share the current, heroic measures are required:

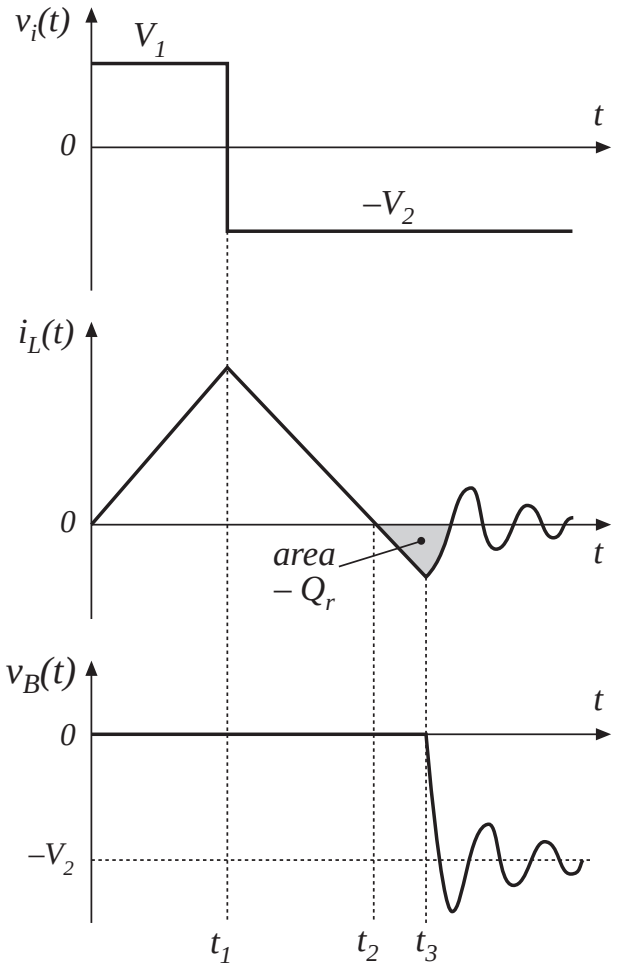


- Select matched devices
- Package on common thermal substrate
- Build external circuitry that forces the currents to balance

Ringing induced by diode stored charge

see Section 4.3.3





- Diode is forward-biased while $i_L(t) > 0$
- Negative inductor current removes diode stored charge Q_r
- When diode becomes reverse-biased, negative inductor current flows through capacitor C.
- Ringing of L-C network is damped by parasitic losses. Ringing energy is lost.

Energy associated with ringing

Recovered charge is $Q_r = -\int_{t_2}^{t_3} i_L(t)\, dt$

Energy stored in inductor during interval $t_2 \le t \le t_3$:

$$W_L = \int_{t_2}^{t_3} v_L(t)\, i_L(t)\, dt$$

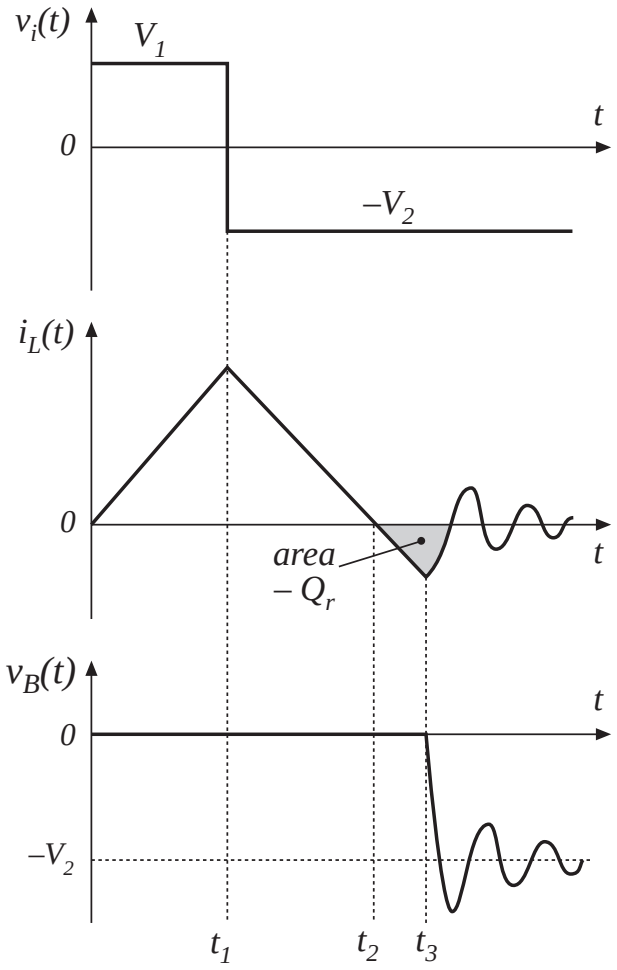
Applied inductor voltage during interval $t_2 \le t \le t_3$:

$$v_L(t) = L\, \frac{d i_L(t)}{dt} = -V_2$$

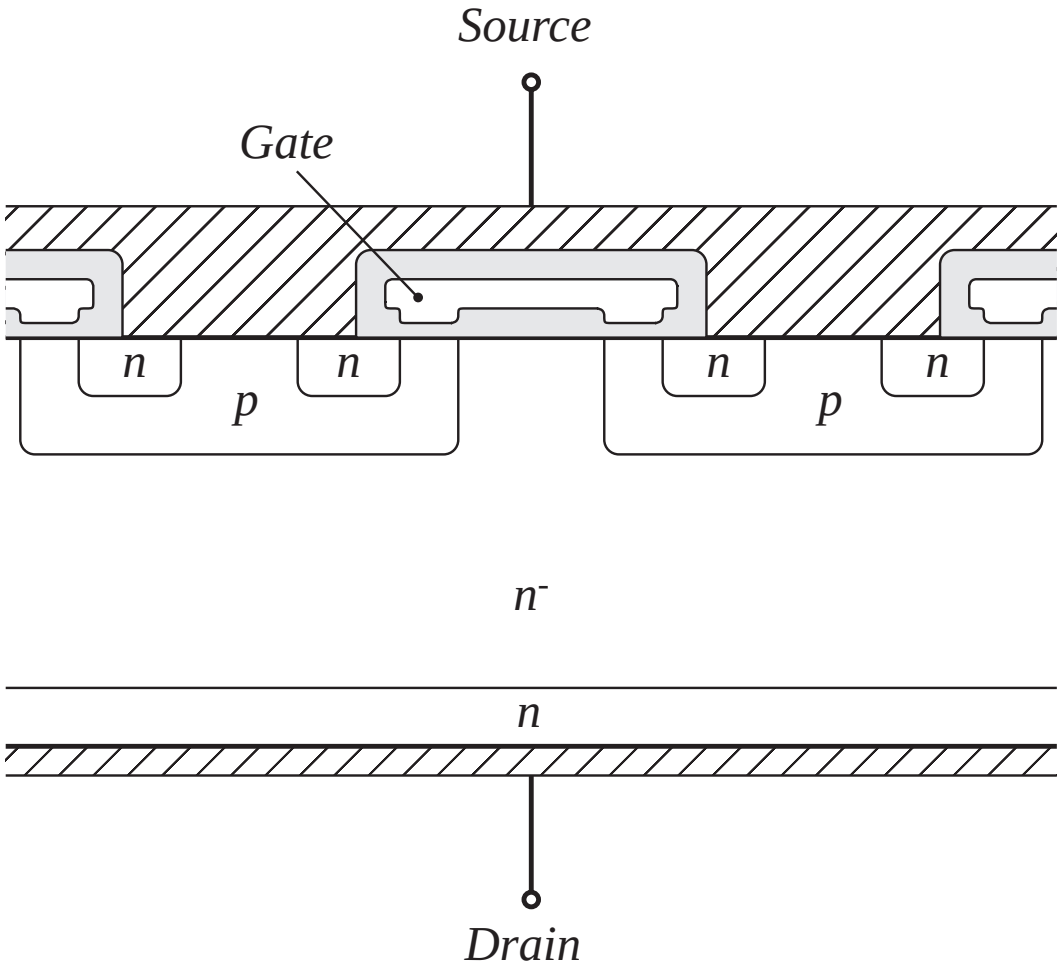
Hence,

$$W_L = \int_{t_2}^{t_3} L\, \frac{d i_L(t)}{dt}\, i_L(t)\, dt = \int_{t_2}^{t_3} (-V_2)\, i_L(t)\, dt$$

$$W_L = \tfrac{1}{2} L\, i_L^2(t_3) = V_2\, Q_r$$

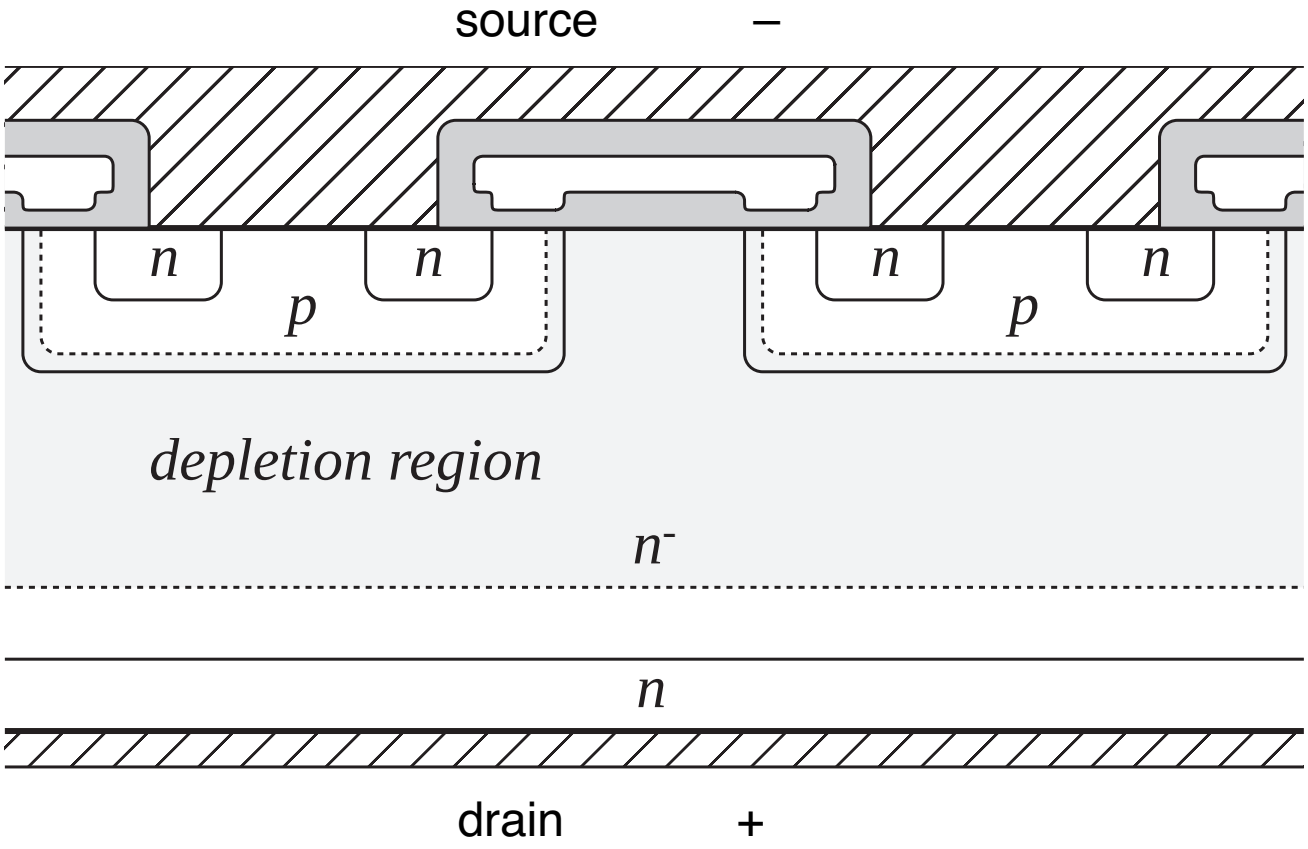


4.2.2. The Power MOSFET



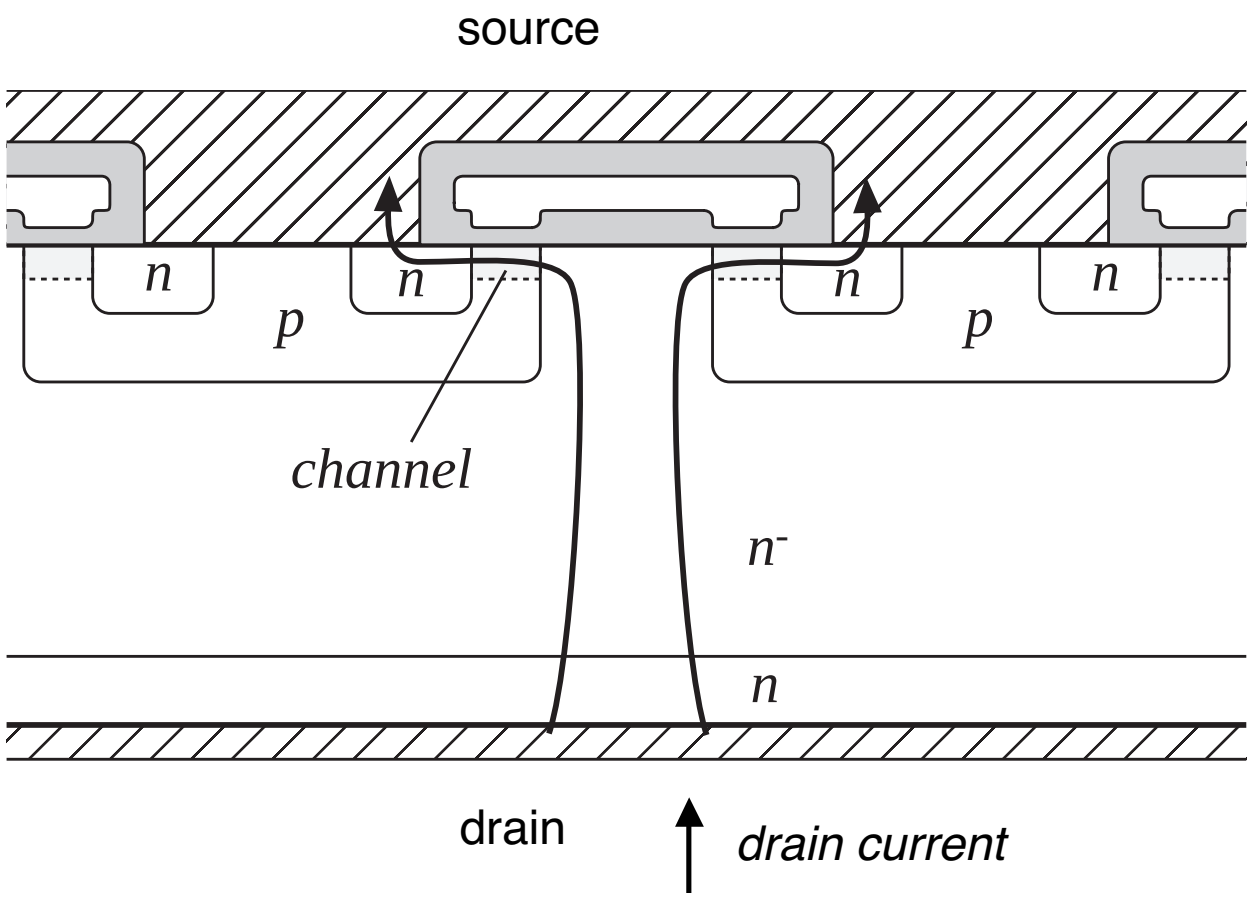
- Gate lengths approaching one micron
- Consists of many small enhancement-mode parallel-connected MOSFET cells, covering the surface of the silicon wafer
- Vertical current flow
- n-channel device is shown

MOSFET: Off state



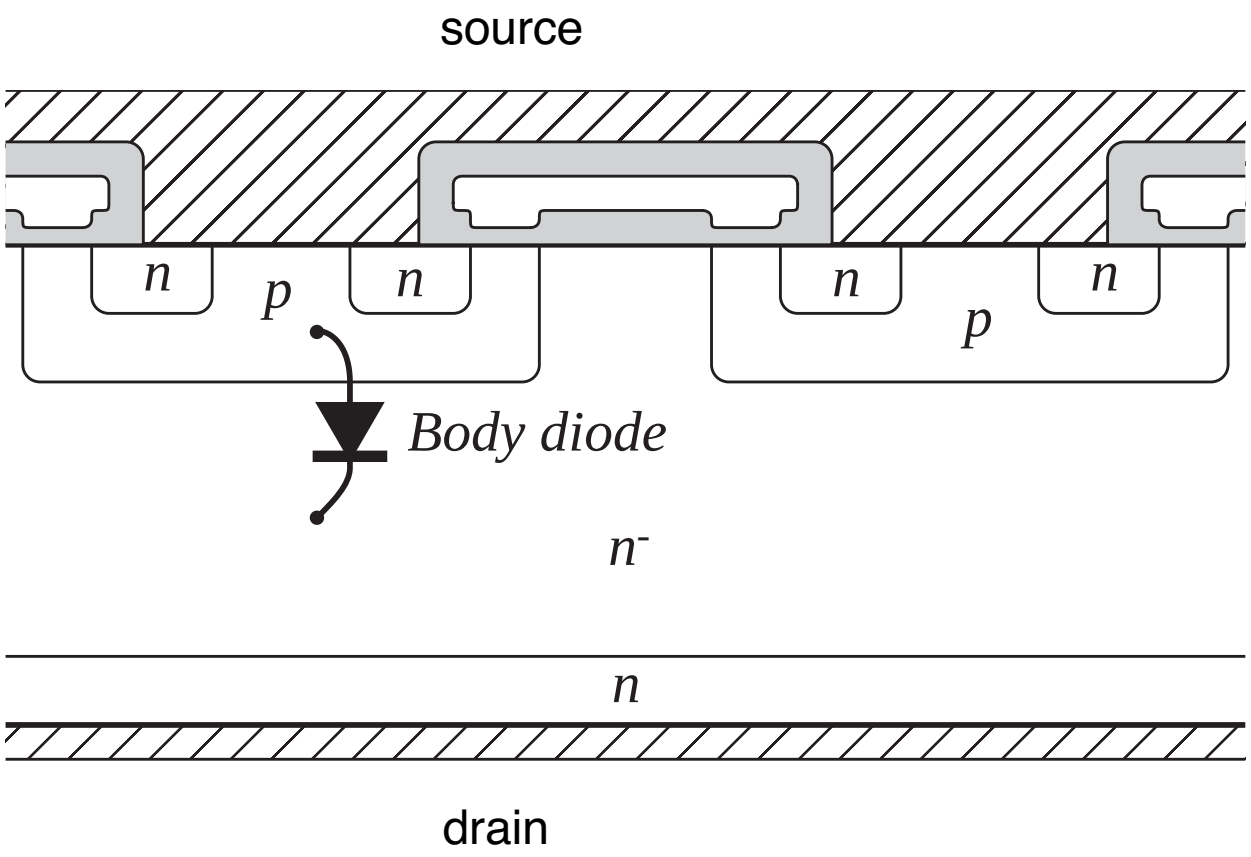
- p-n^- junction is reverse-biased
- off-state voltage appears across n^- region

MOSFET: on state



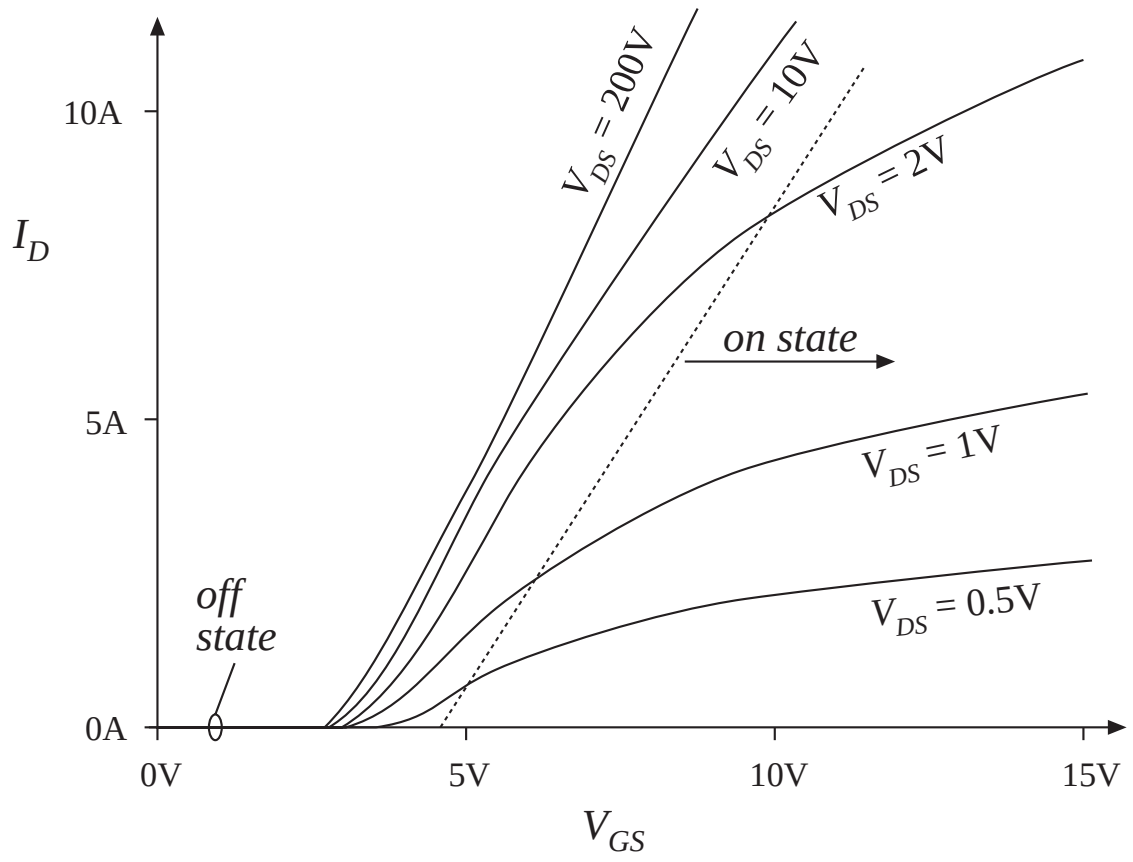
- p-n^- junction is slightly reverse-biased
- positive gate voltage induces conducting channel
- drain current flows through n^- region and conducting channel
- on resistance = total resistances of n^- region, conducting channel, source and drain contacts, etc.

MOSFET body diode



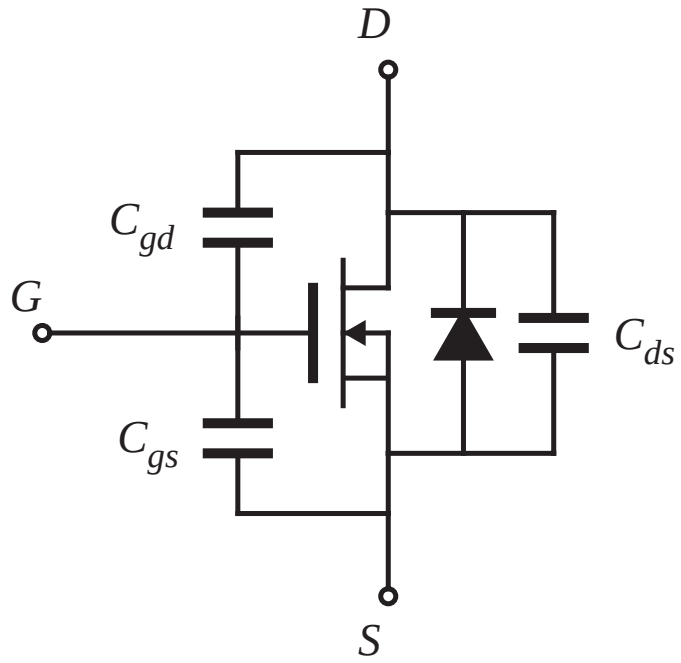
- p-n^- junction forms an effective diode, in parallel with the channel
- negative drain-to-source voltage can forward-bias the body diode
- diode can conduct the full MOSFET rated current
- diode switching speed not optimized —body diode is slow, Q_r is large

Typical MOSFET characteristics



- Off state: $V_{GS} < V_{th}$
- On state: $V_{GS} >> V_{th}$
- MOSFET can conduct peak currents well in excess of average current rating —characteristics are unchanged
- on-resistance has positive temperature coefficient, hence easy to parallel

A simple MOSFET equivalent circuit



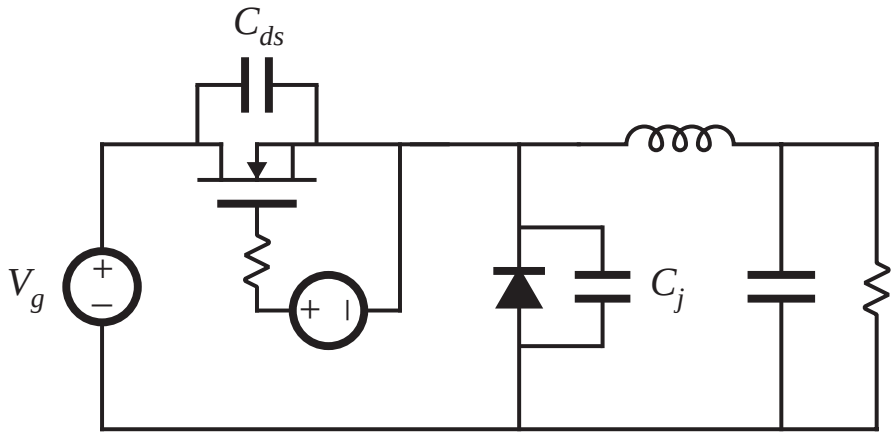
- C_{gs} : large, essentially constant
- C_{gd} : small, highly nonlinear
- C_{ds} : intermediate in value, highly nonlinear
- switching times determined by rate at which gate driver charges/discharges C_{gs} and C_{gd}

$$C_{ds}(v_{ds}) = \frac{C_0}{\sqrt{1 + \frac{v_{ds}}{V_0}}}$$

$$C_{ds}(v_{ds}) \approx C_0 \sqrt{\frac{V_0}{v_{ds}}} = \frac{C_0'}{\sqrt{v_{ds}}}$$

Switching loss caused by semiconductor output capacitances

Buck converter example



Energy lost during MOSFET turn-on transition (assuming linear capacitances):

$$W_C = \tfrac{1}{2} (C_{ds} + C_j) V_g^2$$

MOSFET nonlinear C_{ds}

Approximate dependence of incremental C_{ds} on v_{ds} :

$$C_{ds}(v_{ds}) \approx C_0 \sqrt{\frac{V_0}{v_{ds}}} = \frac{C_0^{'}}{\sqrt{v_{ds}}}$$

Energy stored in C_{ds} at $v_{ds} = V_{DS}$:

$$W_{Cds} = \int v_{ds}\, i_C\, dt = \int_0^{V_{DS}} v_{ds}\, C_{ds}(v_{ds})\, dv_{ds}$$

$$W_{Cds} = \int_0^{V_{DS}} C_0^{'}(v_{ds})\, \sqrt{v_{ds}}\, dv_{ds} = \frac{2}{3}\, C_{ds}(V_{DS})\, V_{DS}^2$$

— same energy loss as linear capacitor having value $\frac{4}{3}\, C_{ds}(V_{DS})$

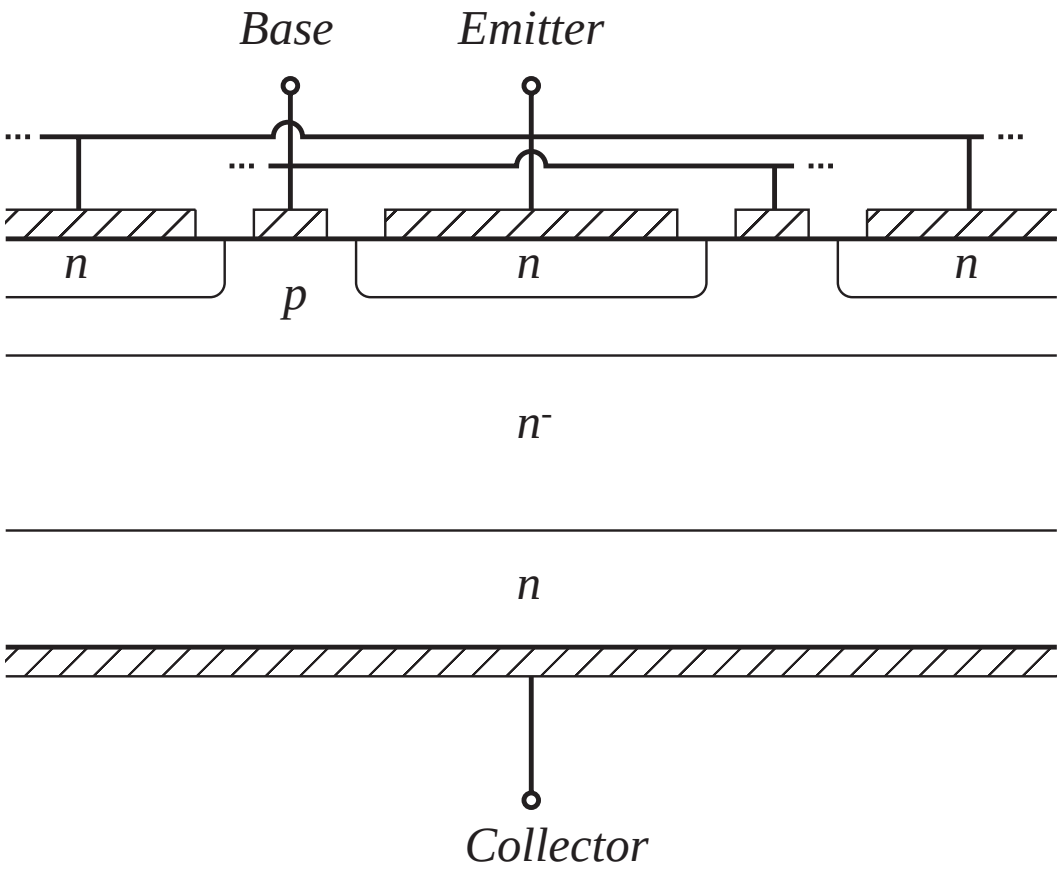
Characteristics of several commercial power MOSFETs

Part number	*Rated max voltage*	*Rated avg current*	R_{on}	Q_g *(typical)*
IRFZ48	60V	50A	0.018Ω	110nC
IRF510	100V	5.6A	0.54Ω	8.3nC
IRF540	100V	28A	0.077Ω	72nC
APT10M25BNR	100V	75A	0.025Ω	171nC
IRF740	400V	10A	0.55Ω	63nC
MTM15N40E	400V	15A	0.3Ω	110nC
APT5025BN	500V	23A	0.25Ω	83nC
APT1001RBNR	1000V	11A	1.0Ω	150nC

MOSFET: conclusions

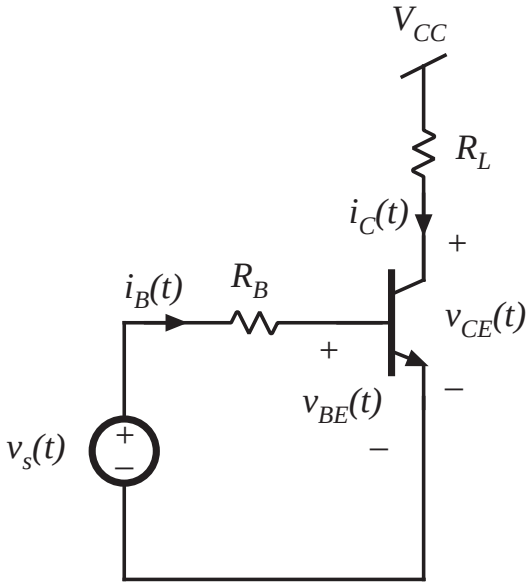
- A majority-carrier device: fast switching speed
- Typical switching frequencies: tens and hundreds of kHz
- On-resistance increases rapidly with rated blocking voltage
- Easy to drive
- The device of choice for blocking voltages less than 500V
- 1000V devices are available, but are useful only at low power levels (100W)
- Part number is selected on the basis of on-resistance rather than current rating

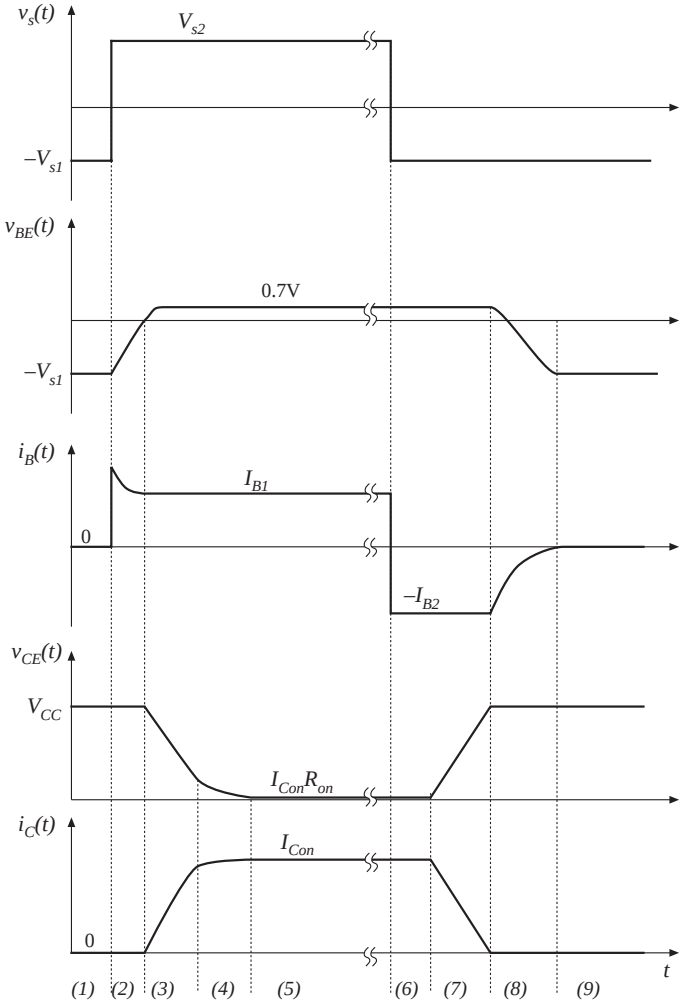
4.2.3. Bipolar Junction Transistor (BJT)



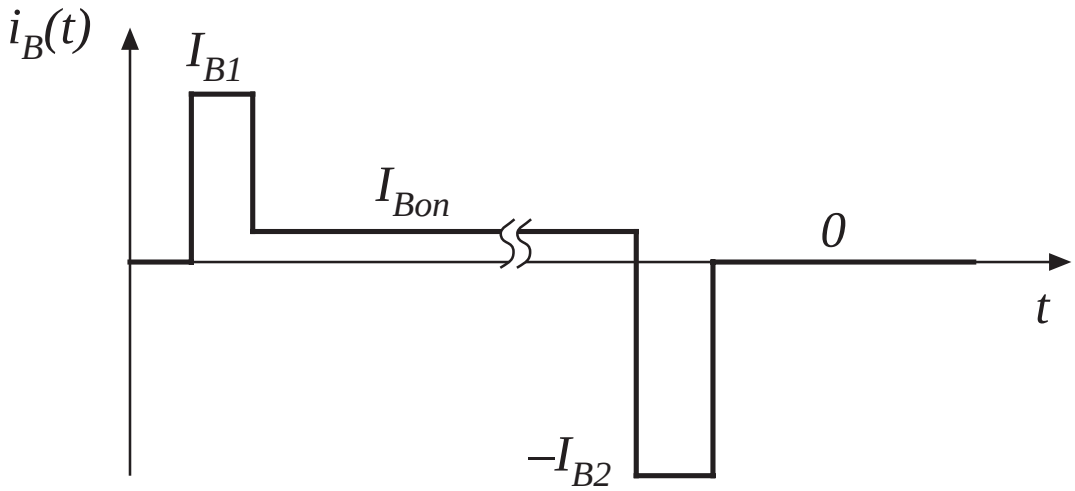
- Interdigitated base and emitter contacts
- Vertical current flow
- npn device is shown
- minority carrier device
- on-state: base-emitter and collector-base junctions are both forward-biased
- on-state: substantial minority charge in p and n^- regions, conductivity modulation

BJT switching times

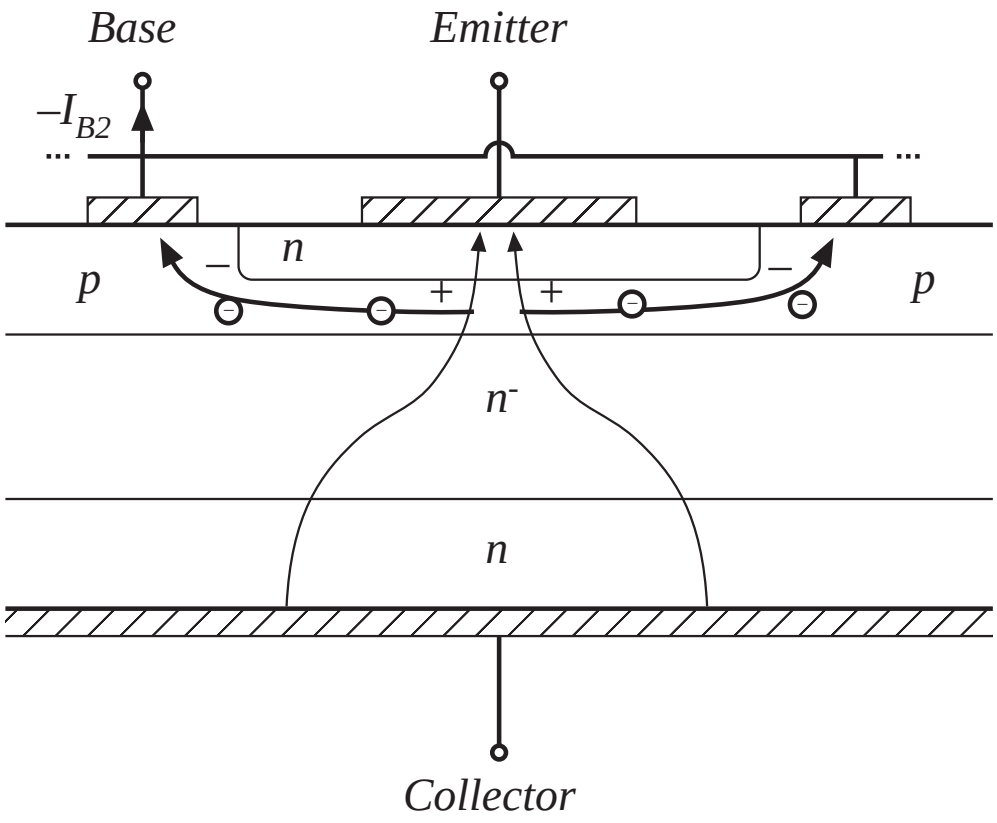




Ideal base current waveform

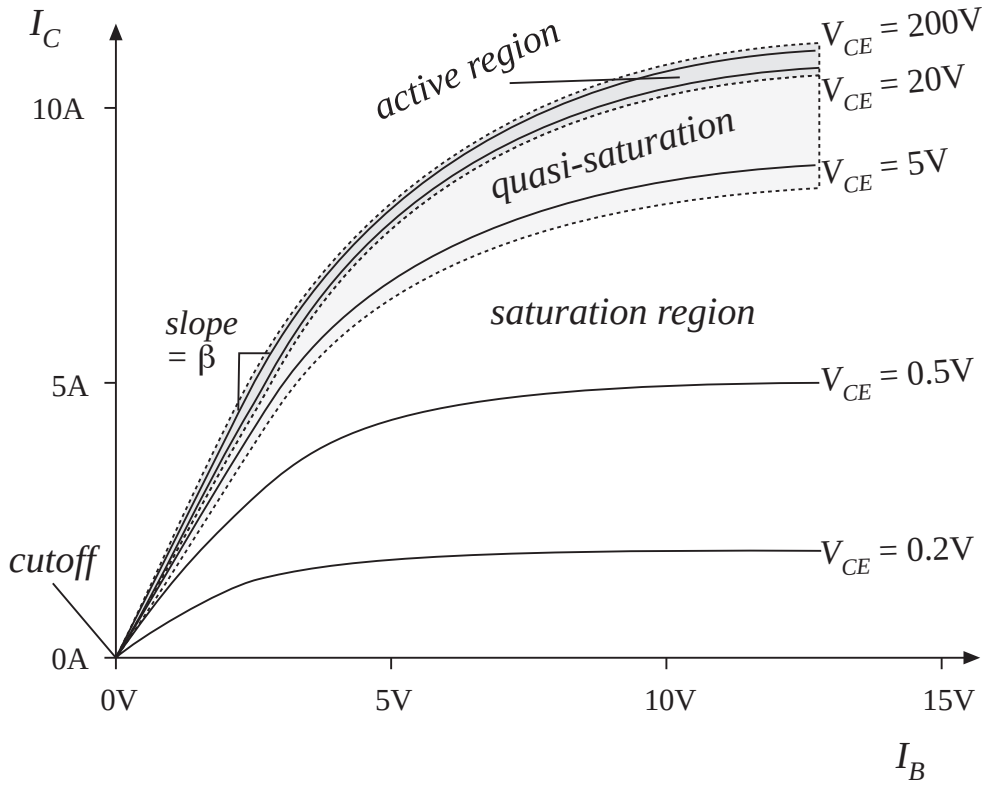


Current crowding due to excessive I_{B2}



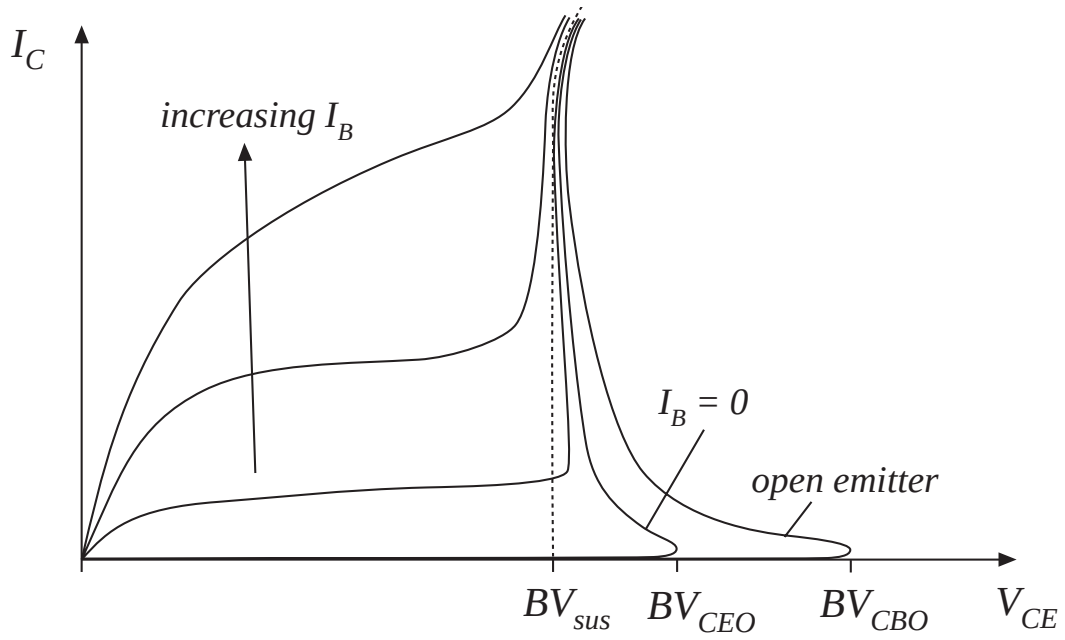
can lead to formation of hot spots and device failure

BJT characteristics



- Off state: $I_B = 0$
- On state: $I_B > I_C / \beta$
- Current gain β decreases rapidly at high current. Device should not be operated at instantaneous currents exceeding the rated value

Breakdown voltages



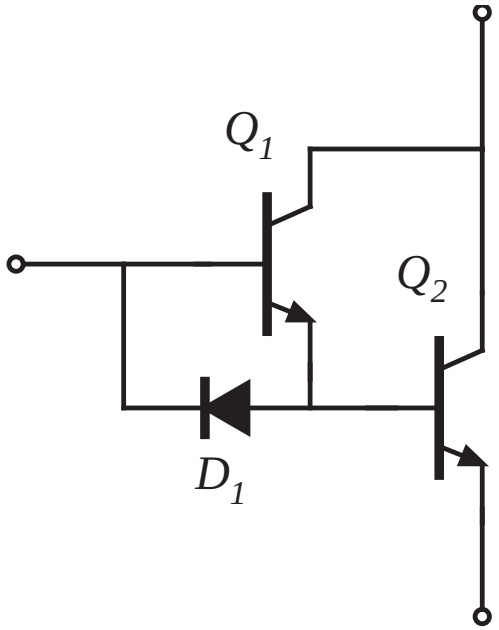
BV_{CBO}: avalanche breakdown voltage of base-collector junction, with the emitter open-circuited

BV_{CEO}: collector-emitter breakdown voltage with zero base current

BV_{sus}: breakdown voltage observed with positive base current

In most applications, the off-state transistor voltage must not exceed BV_{CEO}.

Darlington-connected BJT

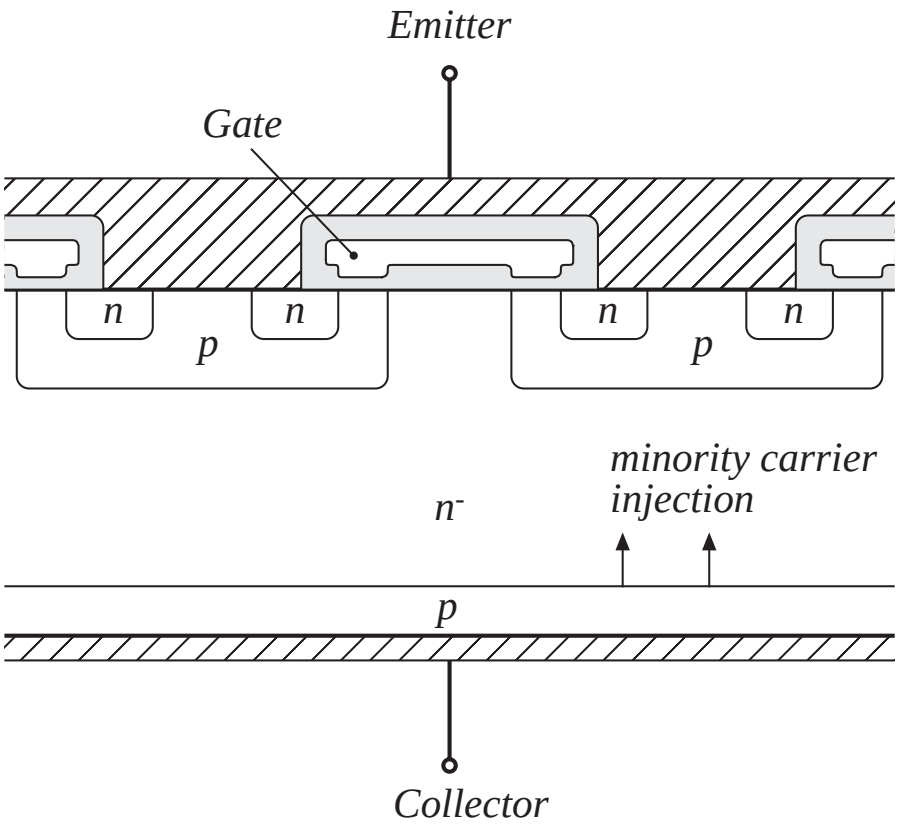


- Increased current gain, for high-voltage applications
- In a monolithic Darlington device, transistors Q_1 and Q_2 are integrated on the same silicon wafer
- Diode D_1 speeds up the turn-off process, by allowing the base driver to actively remove the stored charge of both Q_1 and Q_2 during the turn-off transition

Conclusions: BJT

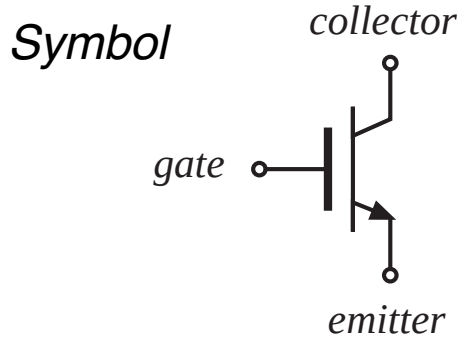
- BJT has been replaced by MOSFET in low-voltage (<500V) applications
- BJT is being replaced by IGBT in applications at voltages above 500V
- A minority-carrier device: compared with MOSFET, the BJT exhibits slower switching, but lower on-resistance at high voltages

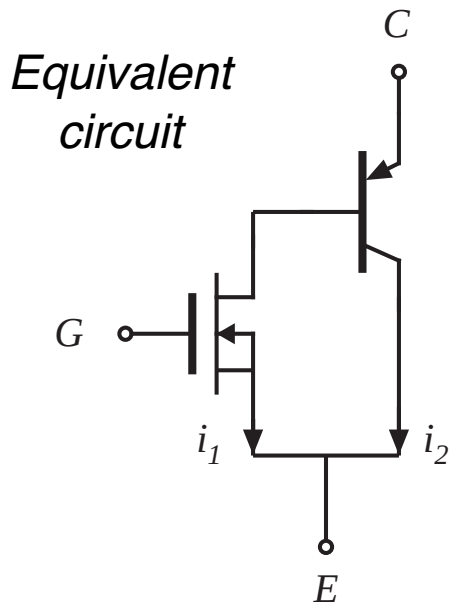
4.2.4. The Insulated Gate Bipolar Transistor (IGBT)

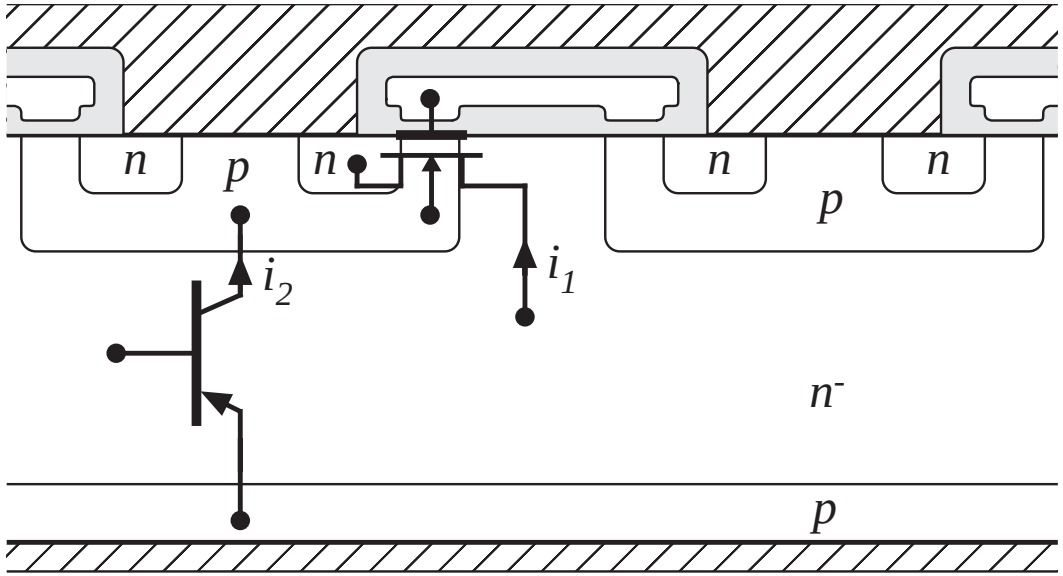


- A four-layer device
- Similar in construction to MOSFET, except extra p region
- On-state: minority carriers are injected into n^- region, leading to conductivity modulation
- compared with MOSFET: slower switching times, lower on-resistance, useful at higher voltages (up to 1700V)

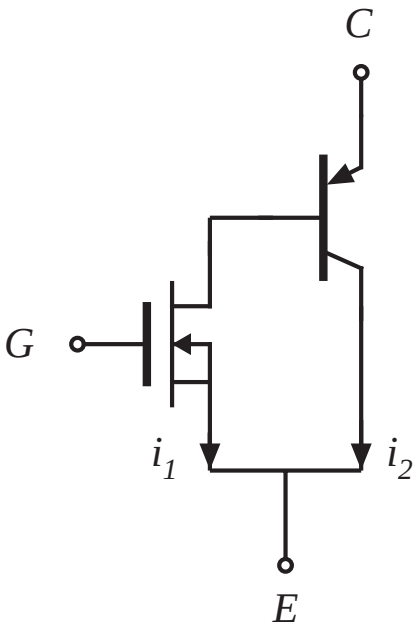
The IGBT

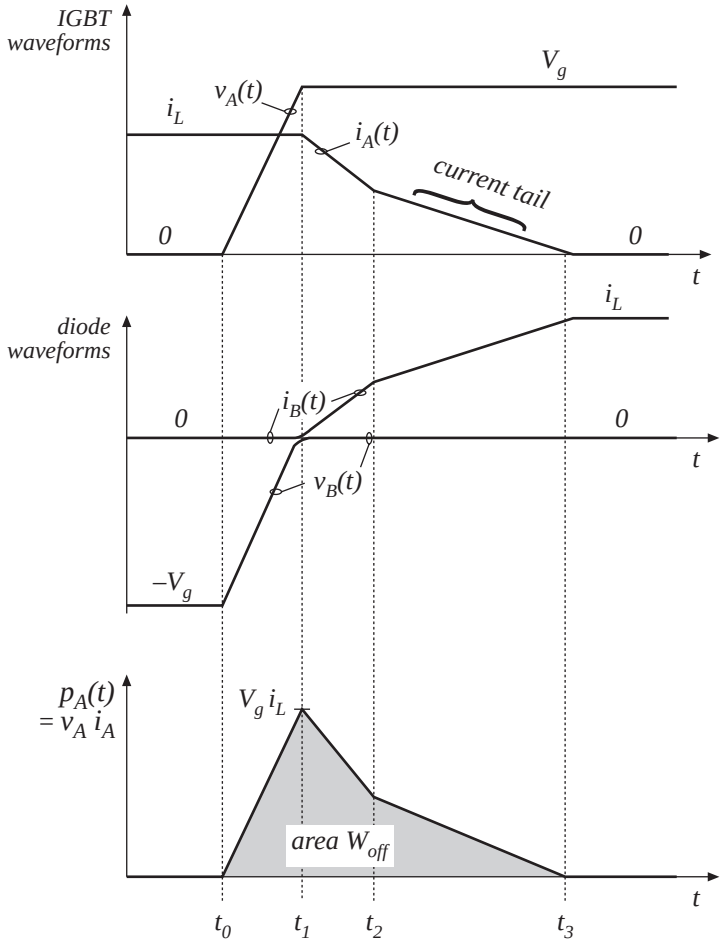

Symbol
collector
gate
emitter


Equivalent circuit
C
G
i_1
i_2
E

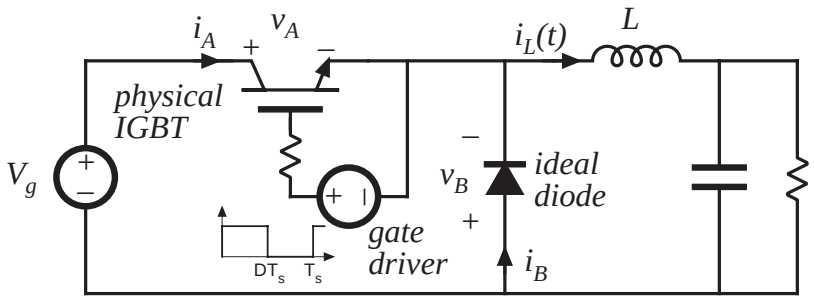

Location of equivalent devices
n
p
n
n
n
p
i_2
i_1
n^-
p

Current tailing in IGBTs

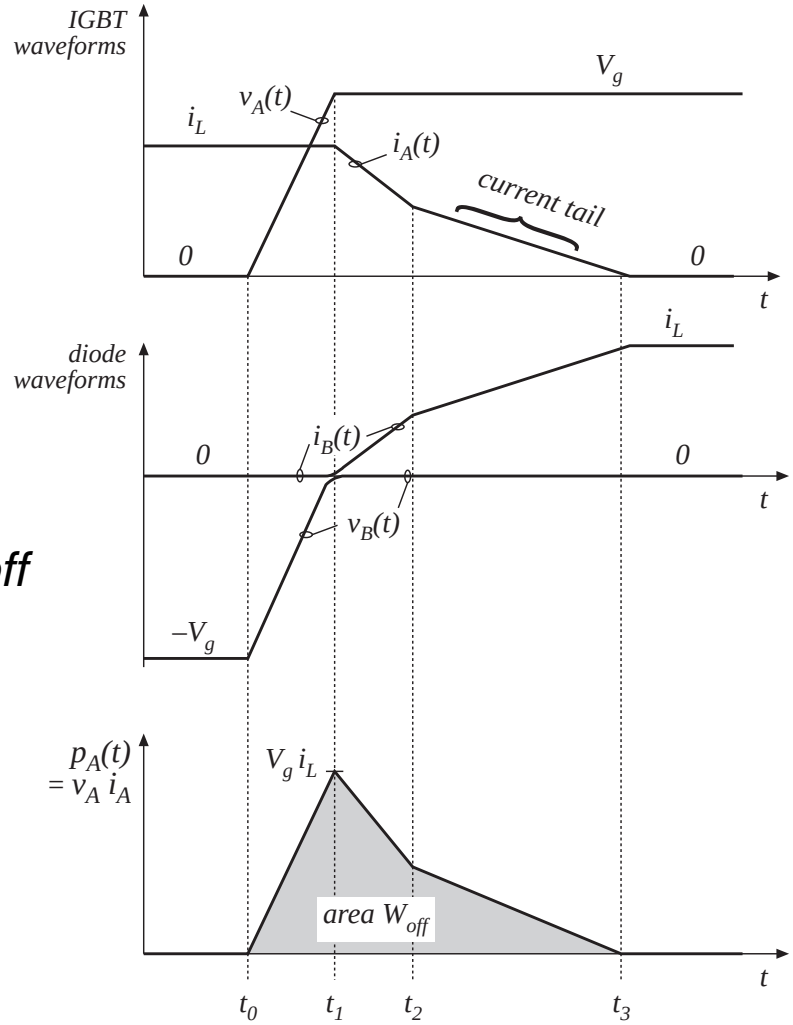




Switching loss due to current-tailing in IGBT



Example: buck converter with IGBT



transistor turn-off transition

$$P_{sw} = \frac{1}{T_s} \int_{\substack{\text{switching} \\ \text{transitions}}} p_A(t)\, dt = (W_{on} + W_{off})\, f_s$$

Characteristics of several commercial devices

Part number	*Rated max voltage*	*Rated avg current*	V_F *(typical)*	t_f *(typical)*
Single-chip devices				
HGTG32N60E2	600V	32A	2.4V	0.62μs
HGTG30N120D2	1200V	30A	3.2A	0.58μs
Multiple-chip power modules				
CM400HA-12E	600V	400A	2.7V	0.3μs
CM300HA-24E	1200V	300A	2.7V	0.3μs

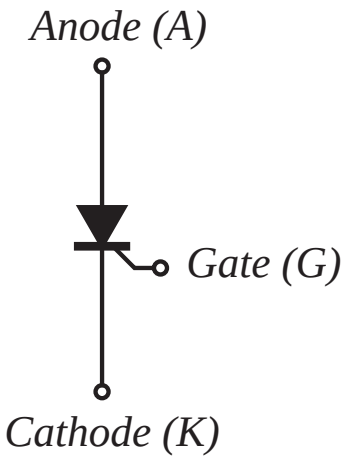
Conclusions: IGBT

- Becoming the device of choice in 500 to 1700V+ applications, at power levels of 1-1000kW
- Positive temperature coefficient at high current —easy to parallel and construct modules
- Forward voltage drop: diode in series with on-resistance. 2-4V typical
- Easy to drive —similar to MOSFET
- Slower than MOSFET, but faster than Darlington, GTO, SCR
- Typical switching frequencies: 3-30kHz
- IGBT technology is rapidly advancing:
  - 3300 V devices: HVIGBTs
  - 150 kHz switching frequencies in 600 V devices

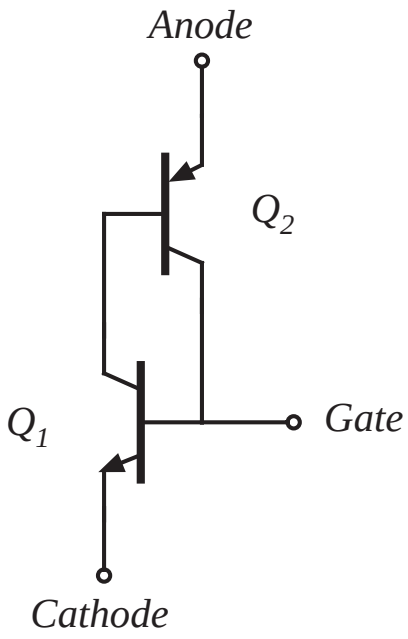
4.2.5. Thyristors (SCR, GTO, MCT)

The SCR

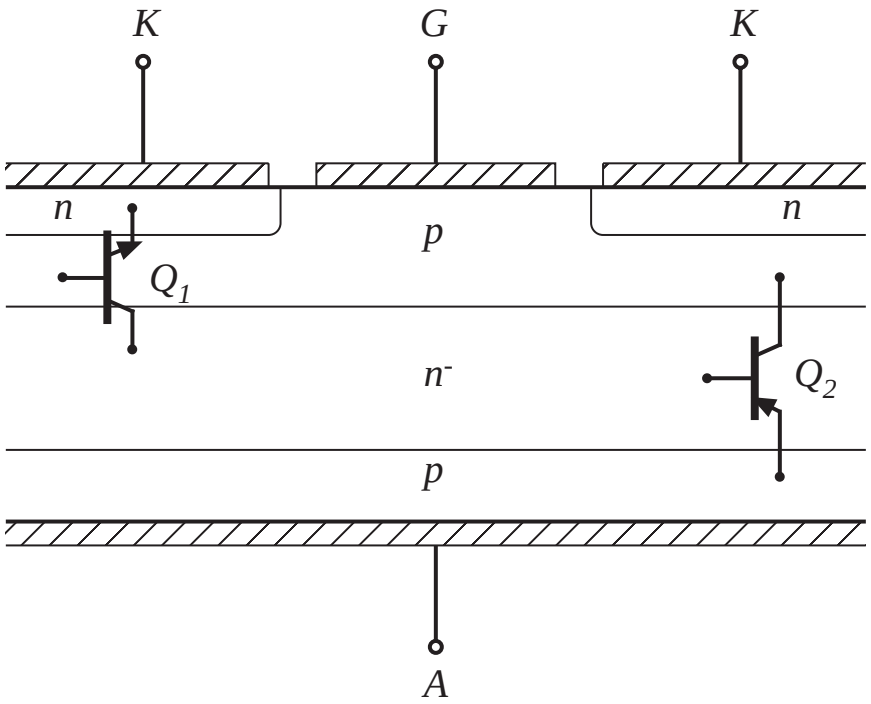
symbol



equiv circuit

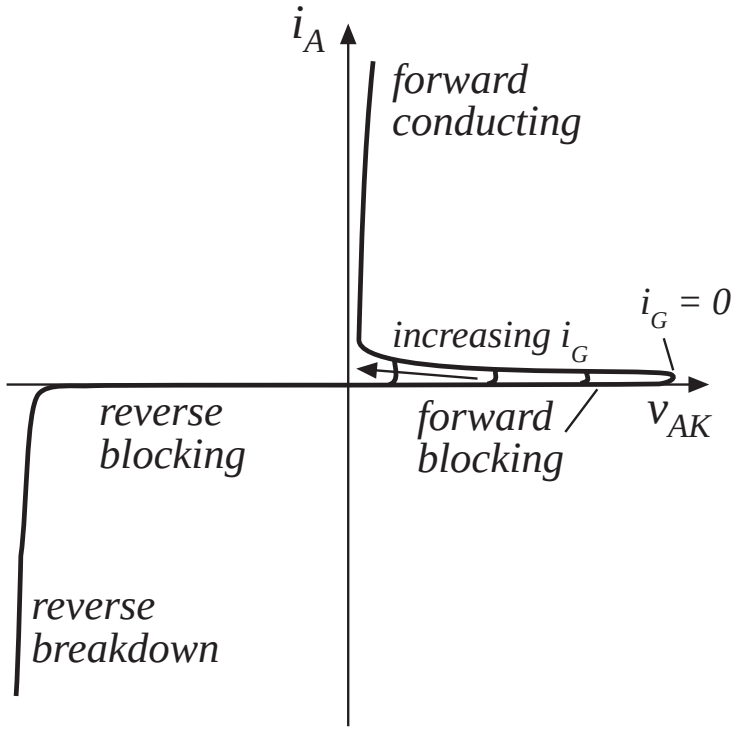


construction



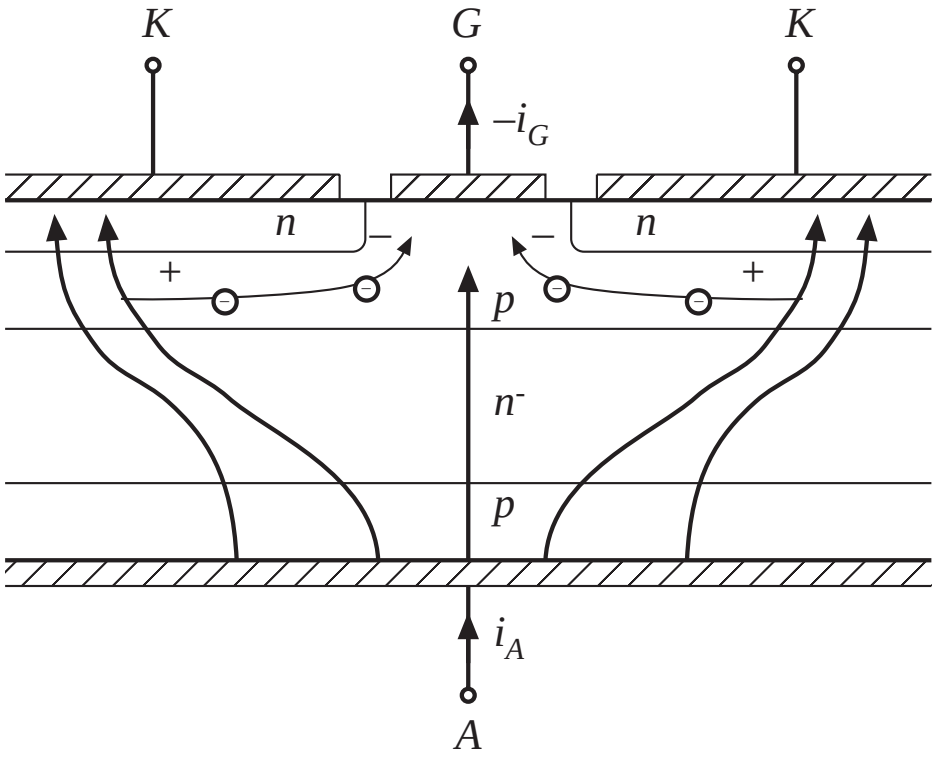
The Silicon Controlled Rectifier (SCR)

- Positive feedback —a latching device
- A minority carrier device
- Double injection leads to very low on-resistance, hence low forward voltage drops attainable in very high voltage devices
- Simple construction, with large feature size
- Cannot be actively turned off
- A voltage-bidirectional two-quadrant switch
- 5000-6000V, 1000-2000A devices



Why the conventional SCR cannot be turned off via gate control

- Large feature size
- Negative gate current induces lateral voltage drop along gate-cathode junction
- Gate-cathode junction becomes reverse-biased only in vicinity of gate contact



The Gate Turn-Off Thyristor (GTO)

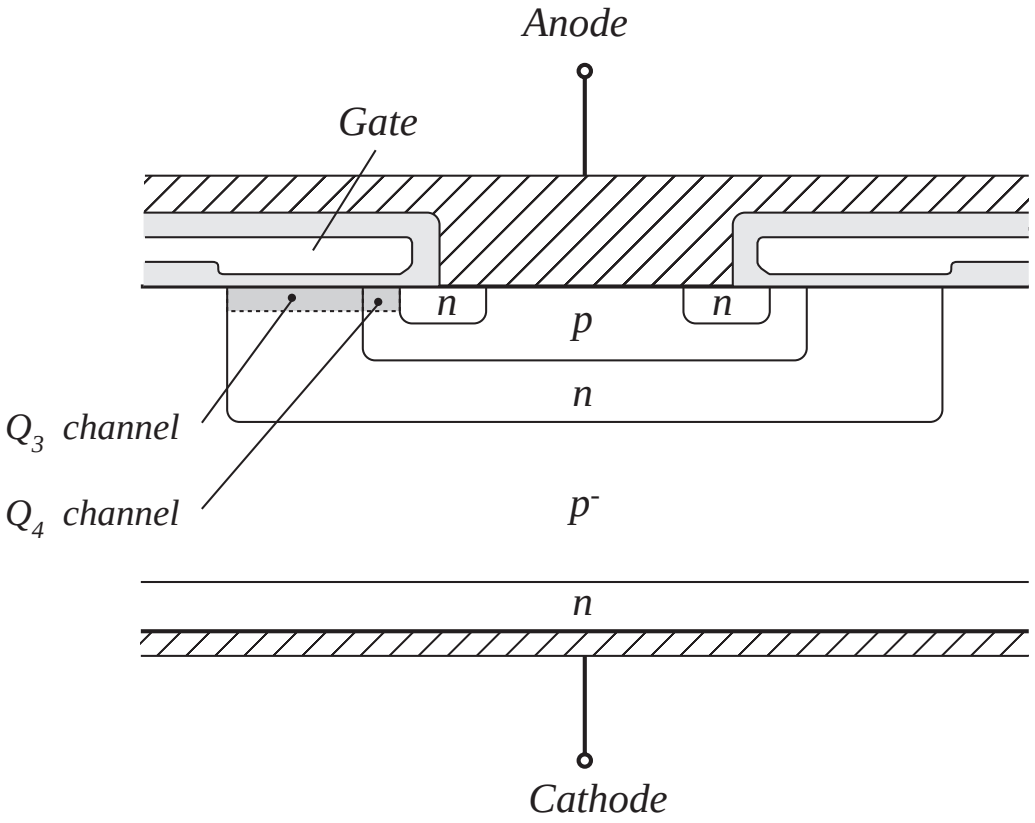
- An SCR fabricated using modern techniques —small feature size
- Gate and cathode contacts are highly interdigitated
- Negative gate current is able to completely reverse-bias the gate-cathode junction

Turn-off transition:

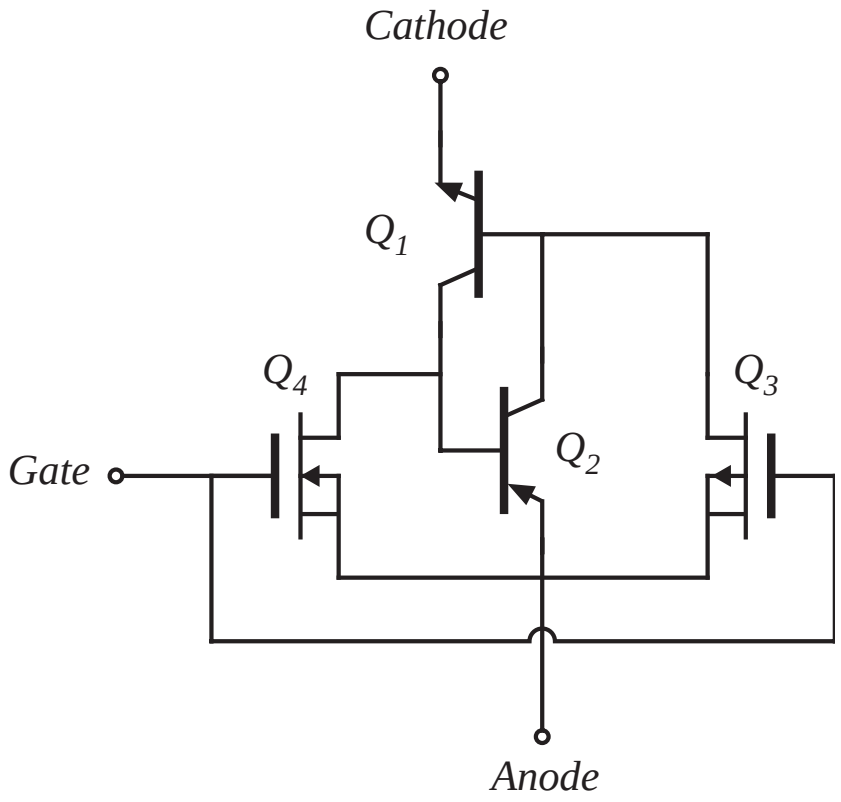
- Turn-off current gain: typically 2-5
- Maximum controllable on-state current: maximum anode current that can be turned off via gate control. GTO can conduct peak currents well in excess of average current rating, but cannot switch off

The MOS-Controlled Thyristor (MCT)

- Still an emerging device, but some devices are commercially available
- p-type device
- A latching SCR, with added built-in MOSFETs to assist the turn-on and turn-off processes
- Small feature size, highly interdigitated, modern fabrication



The MCT: equivalent circuit



- Negative gate-anode voltage turns p-channel MOSFET Q_3 on, causing Q_1 and Q_2 to latch ON
- Positive gate-anode voltage turns n-channel MOSFET Q_4 on, reverse-biasing the base-emitter junction of Q_2 and turning off the device
- Maximum current that can be interrupted is limited by the on-resistance of Q_4

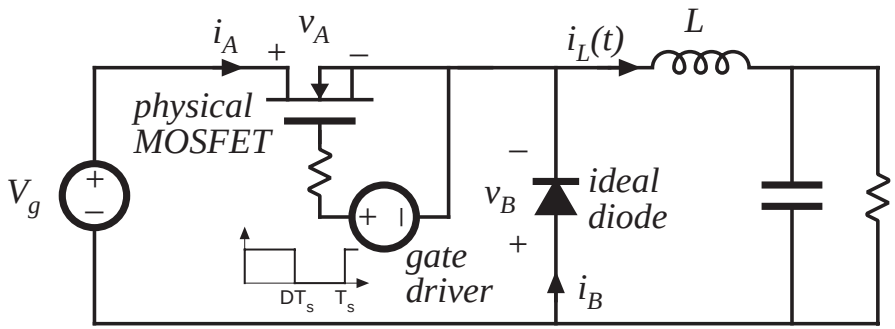
Summary: Thyristors

- The thyristor family: double injection yields lowest forward voltage drop in high voltage devices. More difficult to parallel than MOSFETs and IGBTs
- The SCR: highest voltage and current ratings, low cost, passive turn-off transition
- The GTO: intermediate ratings (less than SCR, somewhat more than IGBT). Slower than IGBT. Slower than MCT. Difficult to drive.
- The MCT: So far, ratings lower than IGBT. Slower than IGBT. Easy to drive. Second breakdown problems? Still an emerging device.

4.3. Switching loss

- Energy is lost during the semiconductor switching transitions, via several mechanisms:
  - Transistor switching times
  - Diode stored charge
  - Energy stored in device capacitances and parasitic inductances
- Semiconductor devices are *charge controlled*
- Time required to insert or remove the controlling charge determines switching times

4.3.1. Transistor switching with clamped inductive load

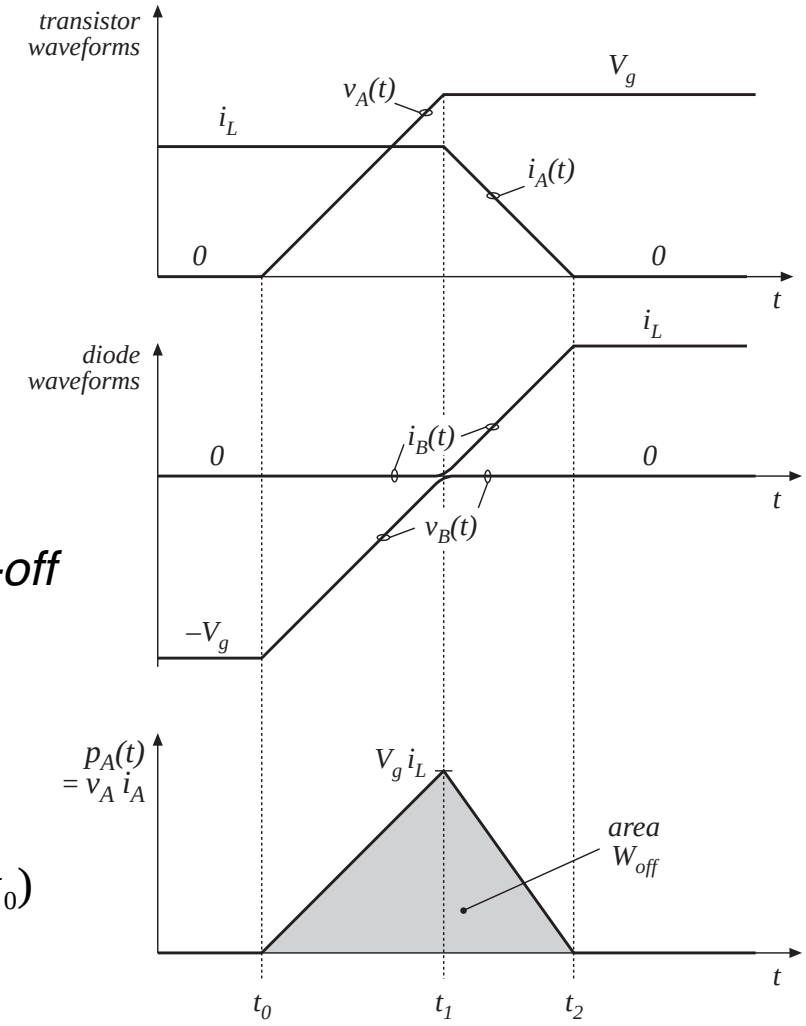


Buck converter example

$$v_B(t) = v_A(t) - V_g$$

$$i_A(t) + i_B(t) = i_L$$

transistor turn-off transition



$$W_{off} = \frac{1}{2}\, V_g i_L\, (t_2 - t_0)$$

Switching loss induced by transistor turn-off transition

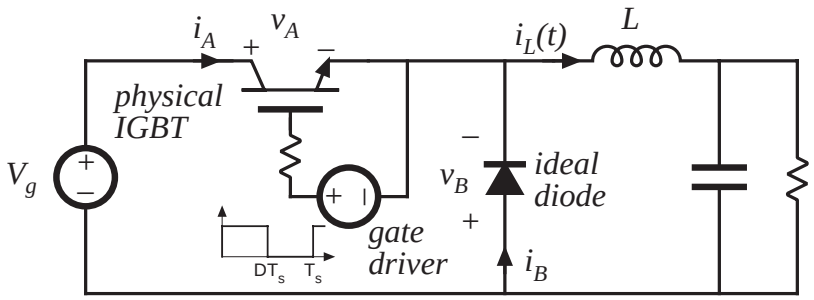
Energy lost during transistor turn-off transition:

$$W_{off} = \frac{1}{2} V_g i_L (t_2 - t_0)$$

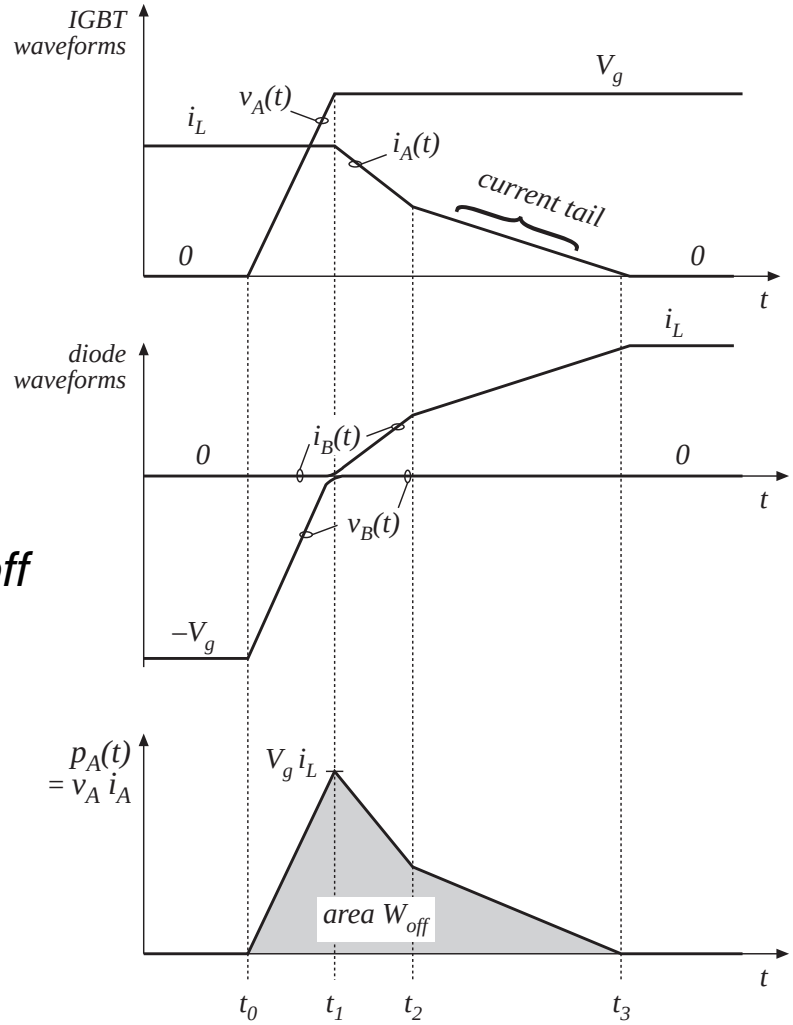
Similar result during transistor turn-on transition.
Average power loss:

$$P_{sw} = \frac{1}{T_s} \int_{\substack{switching \\ transitions}} p_A(t)\, dt = (W_{on} + W_{off})\, f_s$$

Switching loss due to current-tailing in IGBT



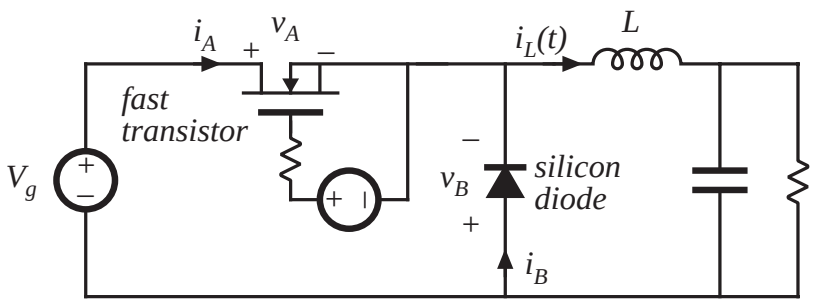
Example: buck converter with IGBT

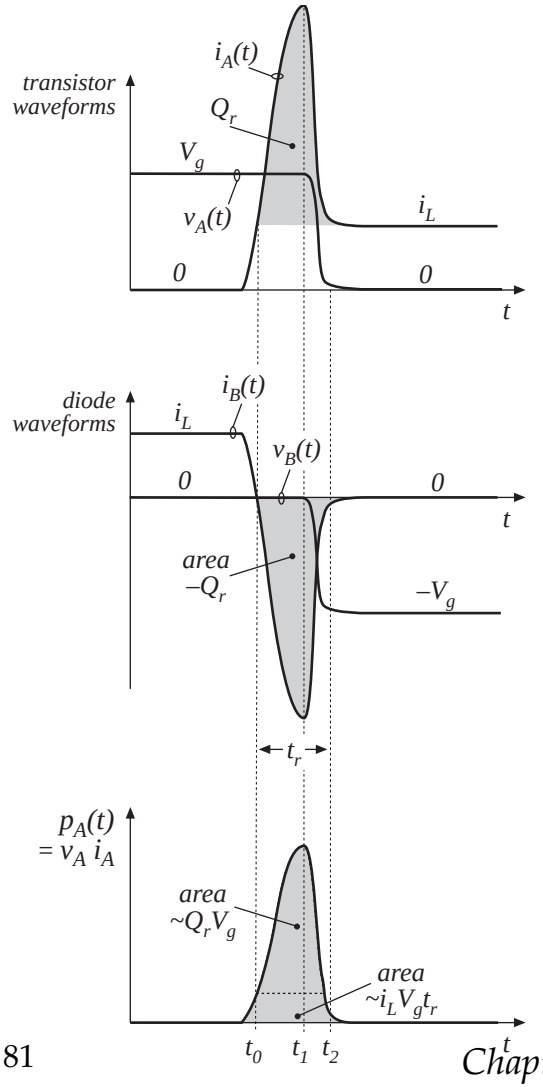


transistor turn-off transition

$$P_{sw} = \frac{1}{T_s} \int_{\substack{\text{switching} \\ \text{transitions}}} p_A(t)\, dt = (W_{on} + W_{off})\, f_s$$

4.3.2. Diode recovered charge





- Diode recovered stored charge Q_r flows through transistor during transistor turn-on transition, inducing switching loss
- Q_r depends on diode on-state forward current, and on the rate-of-change of diode current during diode turn-off transition

Switching loss calculation

Energy lost in transistor:

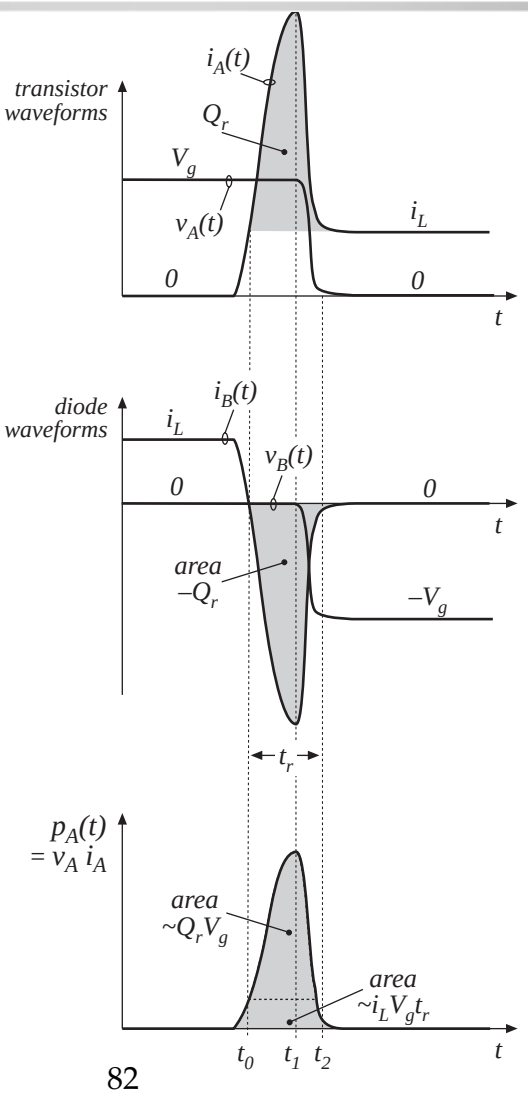
$$W_D = \int_{\substack{\text{switching} \\ \text{transition}}} v_A(t)\, i_A(t)\, dt$$

With abrupt-recovery diode:

$$W_D \approx \int_{\substack{\text{switching} \\ \text{transition}}} V_g\, (i_L - i_B(t))\, dt$$

$$= V_g\, i_L\, t_r + V_g\, Q_r$$

- *Often, this is the largest component of switching loss*



Soft-recovery diode:

$(t_2 - t_1) >> (t_1 - t_0)$

Abrupt-recovery diode:

$(t_2 - t_1) << (t_1 - t_0)$

4.3.3. Device capacitances, and leakage, package, and stray inductances

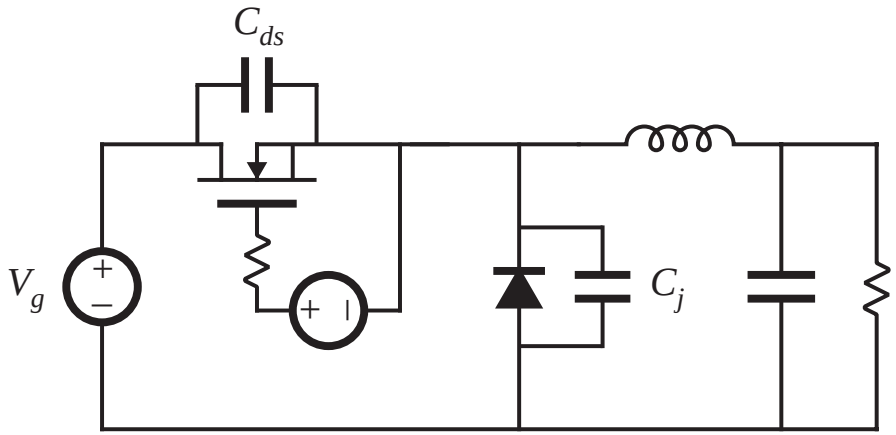
- Capacitances that appear effectively in parallel with switch elements are shorted when the switch turns on. Their stored energy is lost during the switch turn-on transition.
- Inductances that appear effectively in series with switch elements are open-circuited when the switch turns off. Their stored energy is lost during the switch turn-off transition.

Total energy stored in linear capacitive and inductive elements:

$$W_C = \sum_{\substack{\text{capacitive} \\ \text{elements}}} \frac{1}{2} C_i V_i^2 \qquad W_L = \sum_{\substack{\text{inductive} \\ \text{elements}}} \frac{1}{2} L_j I_j^2$$

Example: semiconductor output capacitances

Buck converter example



Energy lost during MOSFET turn-on transition (assuming linear capacitances):

$$W_C = \tfrac{1}{2} (C_{ds} + C_j) V_g^2$$

MOSFET nonlinear C_{ds}

Approximate dependence of incremental C_{ds} on v_{ds} :

$$C_{ds}(v_{ds}) \approx C_0 \sqrt{\frac{V_0}{v_{ds}}} = \frac{C_0^{'}}{\sqrt{v_{ds}}}$$

Energy stored in C_{ds} at $v_{ds} = V_{DS}$:

$$W_{Cds} = \int v_{ds}\, i_C\, dt = \int_0^{V_{DS}} v_{ds}\, C_{ds}(v_{ds})\, dv_{ds}$$

$$W_{Cds} = \int_0^{V_{DS}} C_0^{'}(v_{ds})\, \sqrt{v_{ds}}\, dv_{ds} = \frac{2}{3}\, C_{ds}(V_{DS})\, V_{DS}^2$$

— same energy loss as linear capacitor having value $\frac{4}{3}\, C_{ds}(V_{DS})$

Some other sources of this type of switching loss

Schottky diode

- Essentially no stored charge
- Significant reverse-biased junction capacitance

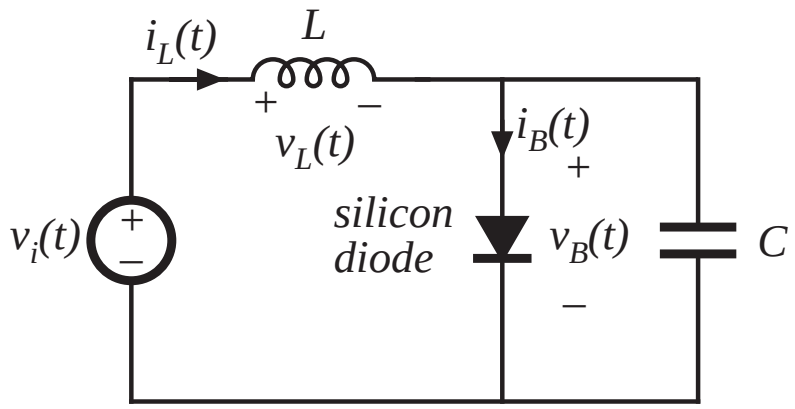
Transformer leakage inductance

- Effective inductances in series with windings
- A significant loss when windings are not tightly coupled

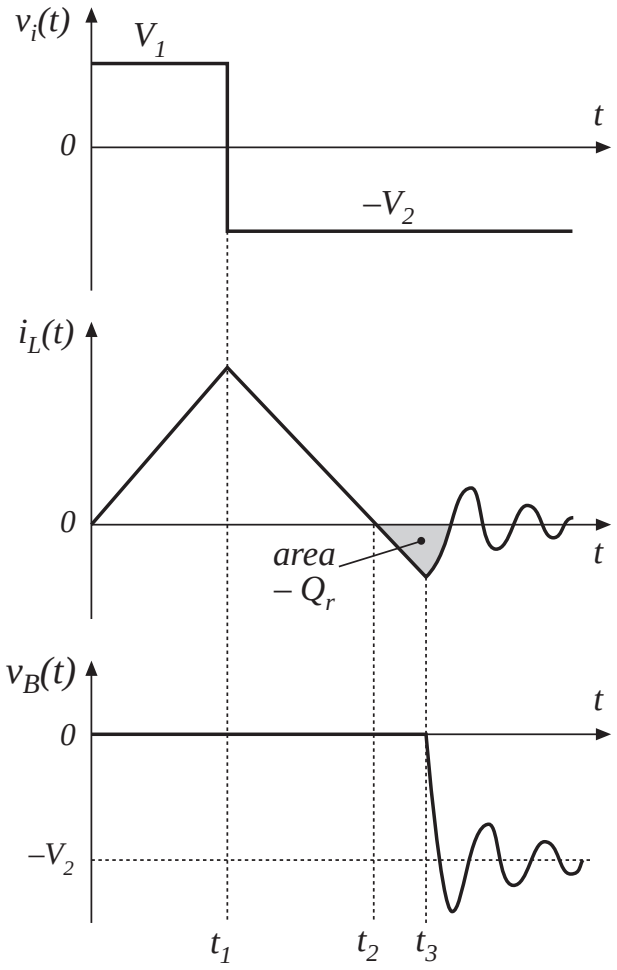
Interconnection and package inductances

- Diodes
- Transistors
- A significant loss in high current applications

Ringing induced by diode stored charge



- Diode is forward-biased while $i_L(t) > 0$
- Negative inductor current removes diode stored charge Q_r
- When diode becomes reverse-biased, negative inductor current flows through capacitor C.
- Ringing of L-C network is damped by parasitic losses. Ringing energy is lost.



Energy associated with ringing

Recovered charge is $Q_r = -\int_{t_2}^{t_3} i_L(t)\, dt$

Energy stored in inductor during interval $t_2 \le t \le t_3$:

$$W_L = \int_{t_2}^{t_3} v_L(t)\, i_L(t)\, dt$$

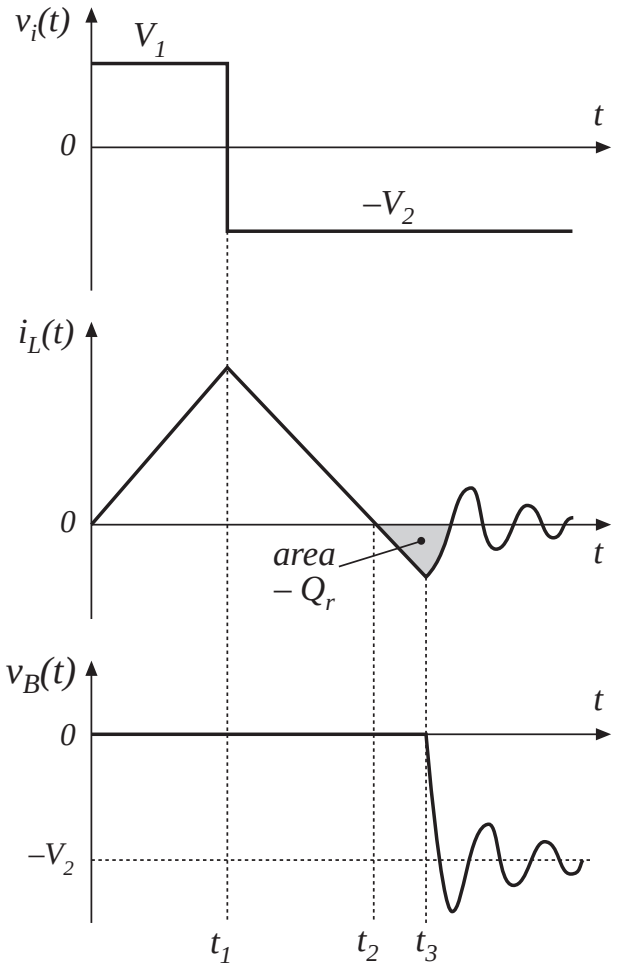
Applied inductor voltage during interval $t_2 \le t \le t_3$:

$$v_L(t) = L\, \frac{d i_L(t)}{dt} = -V_2$$

Hence,

$$W_L = \int_{t_2}^{t_3} L\, \frac{d i_L(t)}{dt}\, i_L(t)\, dt = \int_{t_2}^{t_3} (-V_2)\, i_L(t)\, dt$$

$$W_L = \tfrac{1}{2} L\, i_L^2(t_3) = V_2\, Q_r$$



4.3.4. Efficiency vs. switching frequency

Add up all of the energies lost during the switching transitions of one switching period:

$$W_{tot} = W_{on} + W_{off} + W_D + W_C + W_L + \ldots$$

Average switching power loss is

$$P_{sw} = W_{tot}\ f_{sw}$$

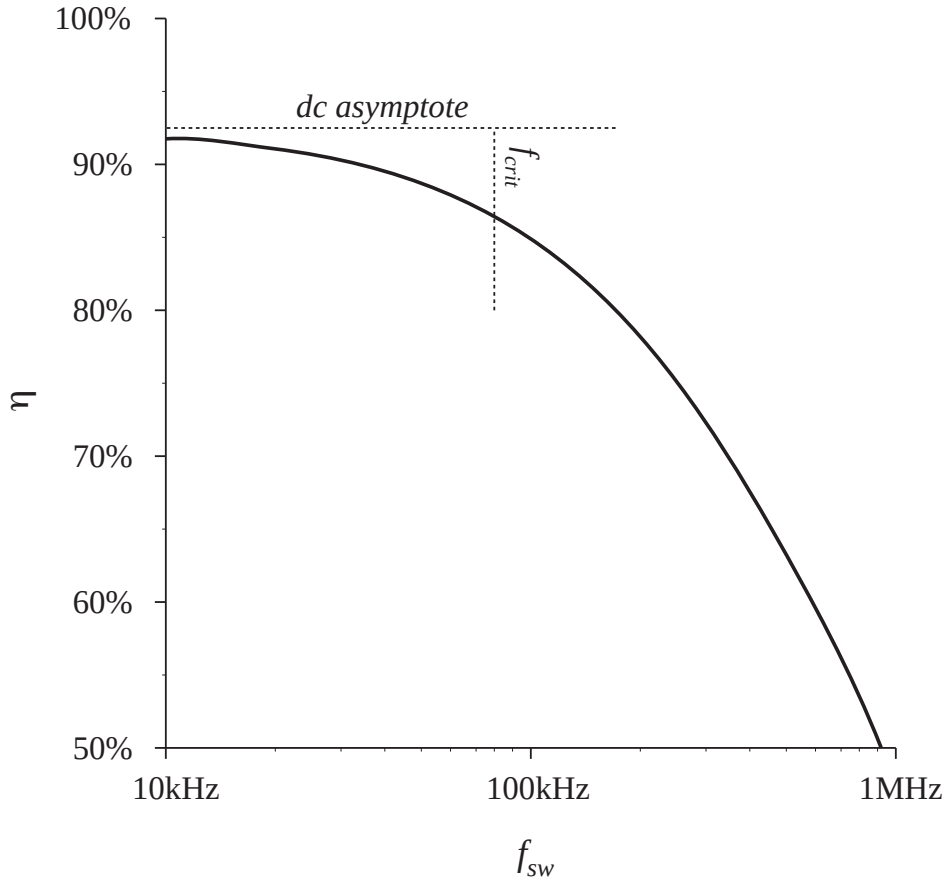
Total converter loss can be expressed as

$$P_{loss} = P_{cond} + P_{fixed} + W_{tot}\ f_{sw}$$

where P_{fixed} = fixed losses (independent of load and f_{sw})
P_{cond} = conduction losses

Efficiency vs. switching frequency

$$P_{loss} = P_{cond} + P_{fixed} + W_{tot}\ f_{sw}$$



Switching losses are equal to the other converter losses at the critical frequency

$$f_{crit} = \frac{P_{cond} + P_{fixed}}{W_{tot}}$$

This can be taken as a rough upper limit on the switching frequency of a practical converter. For $f_{sw} > f_{crit}$, the efficiency decreases rapidly with frequency.

Summary of chapter 4

1. How an SPST ideal switch can be realized using semiconductor devices depends on the polarity of the voltage which the devices must block in the off-state, and on the polarity of the current which the devices must conduct in the on-state.
2. Single-quadrant SPST switches can be realized using a single transistor or a single diode, depending on the relative polarities of the off-state voltage and on-state current.
3. Two-quadrant SPST switches can be realized using a transistor and diode, connected in series (bidirectional-voltage) or in anti-parallel (bidirectional-current). Several four-quadrant schemes are also listed here.
4. A “synchronous rectifier” is a MOSFET connected to conduct reverse current, with gate drive control as necessary. This device can be used where a diode would otherwise be required. If a MOSFET with sufficiently low R_{on} is used, reduced conduction loss is obtained.

Summary of chapter 4

5. Majority carrier devices, including the MOSFET and Schottky diode, exhibit very fast switching times, controlled essentially by the charging of the device capacitances. However, the forward voltage drops of these devices increases quickly with increasing breakdown voltage.
6. Minority carrier devices, including the BJT, IGBT, and thyristor family, can exhibit high breakdown voltages with relatively low forward voltage drop. However, the switching times of these devices are longer, and are controlled by the times needed to insert or remove stored minority charge.
7. Energy is lost during switching transitions, due to a variety of mechanisms. The resulting average power loss, or switching loss, is equal to this energy loss multiplied by the switching frequency. Switching loss imposes an upper limit on the switching frequencies of practical converters.

Summary of chapter 4

8. The diode and inductor present a “clamped inductive load” to the transistor. When a transistor drives such a load, it experiences high instantaneous power loss during the switching transitions. An example where this leads to significant switching loss is the IGBT and the “current tail” observed during its turn-off transition.
9. Other significant sources of switching loss include diode stored charge and energy stored in certain parasitic capacitances and inductances. Parasitic ringing also indicates the presence of switching loss.

Chapter 5. The Discontinuous Conduction Mode

5.1. Origin of the discontinuous conduction mode, and mode boundary

5.2. Analysis of the conversion ratio $M(D,K)$

5.3. Boost converter example

5.4. Summary of results and key points

Introduction to Discontinuous Conduction Mode (DCM)

- Occurs because switching ripple in inductor current or capacitor voltage causes polarity of applied switch current or voltage to reverse, such that the current- or voltage-unidirectional assumptions made in realizing the switch are violated.
- Commonly occurs in dc-dc converters and rectifiers, having single-quadrant switches. May also occur in converters having two-quadrant switches.
- Typical example: dc-dc converter operating at light load (small load current). Sometimes, dc-dc converters and rectifiers are purposely designed to operate in DCM at all loads.
- Properties of converters change radically when DCM is entered:

  M becomes load-dependent

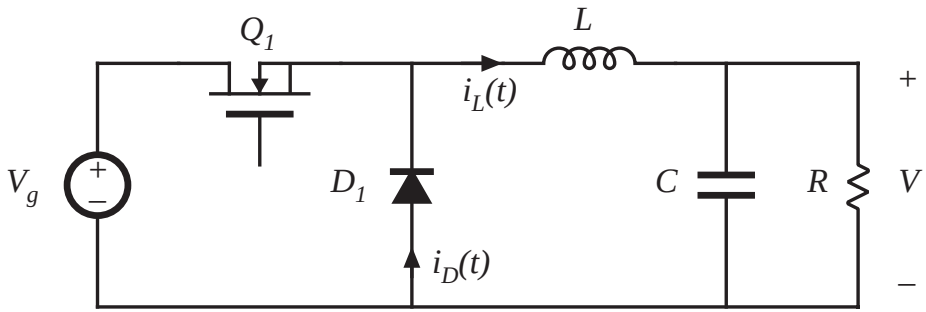
  Output impedance is increased

  Dynamics are altered

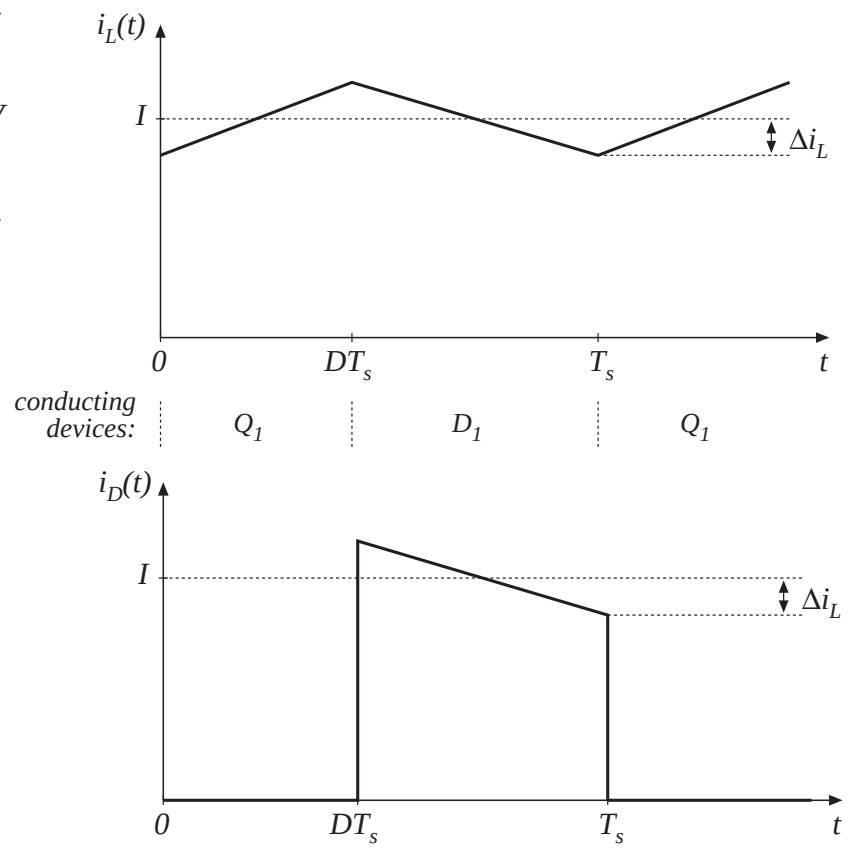
  Control of output voltage may be lost when load is removed

5.1. Origin of the discontinuous conduction mode, and mode boundary

Buck converter example, with single-quadrant switches



continuous conduction mode (CCM)



Minimum diode current is $(I - \Delta i_L)$

Dc component $I = V/R$

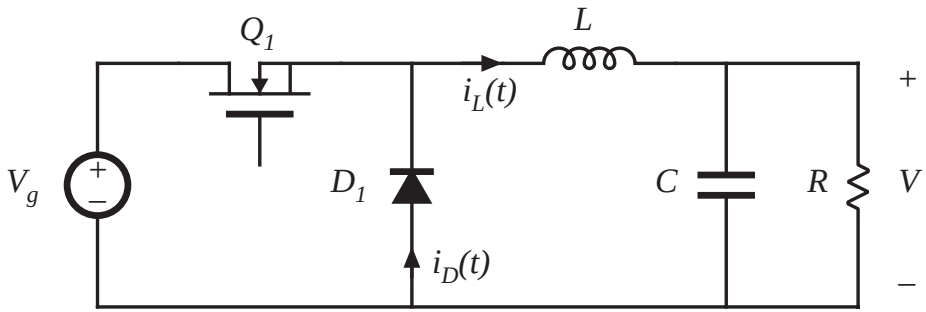
Current ripple is

$$\Delta i_L = \frac{(V_g - V)}{2L} DT_s = \frac{V_g DD'T_s}{2L}$$

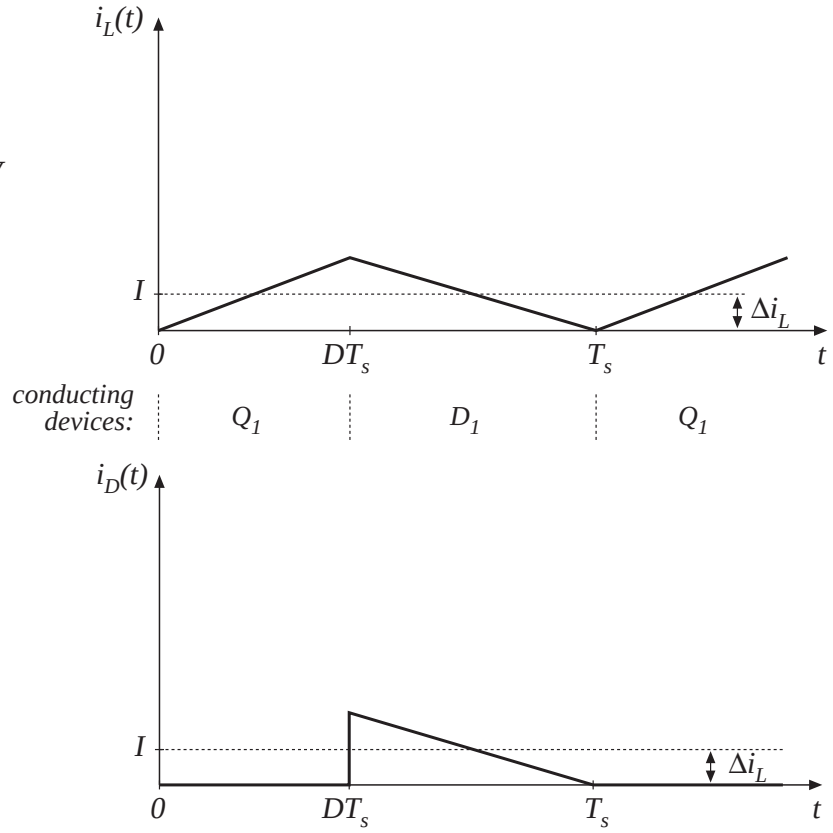
Note that I depends on load, but Δi_L does not.

Reduction of load current

Increase R, until $I = \Delta i_L$



CCM-DCM boundary



Minimum diode current is $(I - \Delta i_L)$

Dc component $I = V/R$

Current ripple is

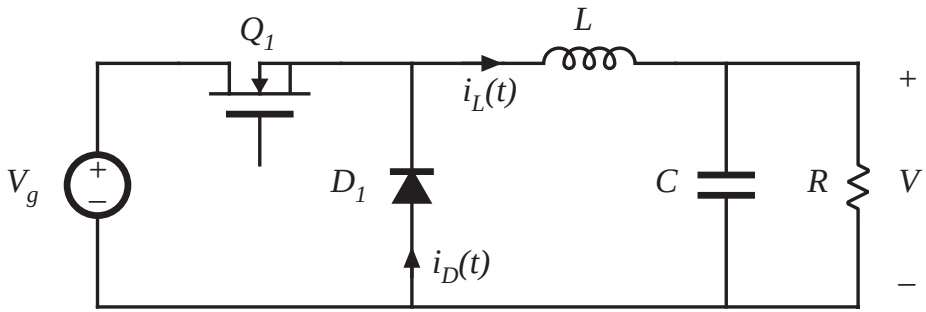
$$\Delta i_L = \frac{(V_g - V)}{2L} DT_s = \frac{V_g DD'T_s}{2L}$$

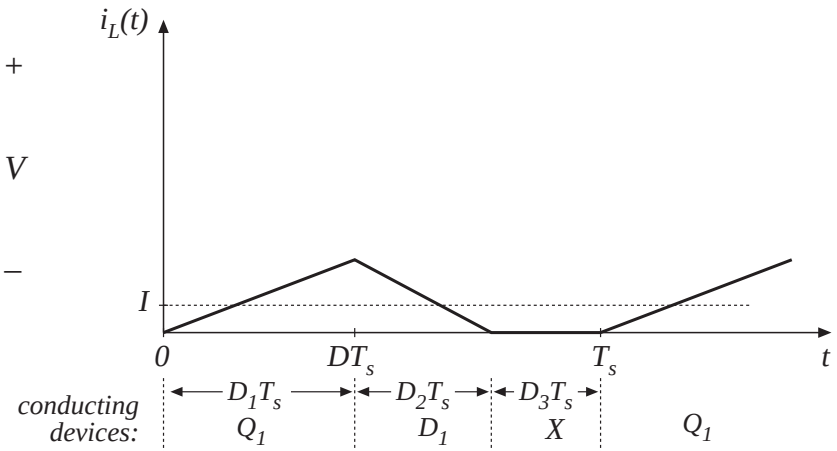
Note that I depends on load, but Δi_L does not.

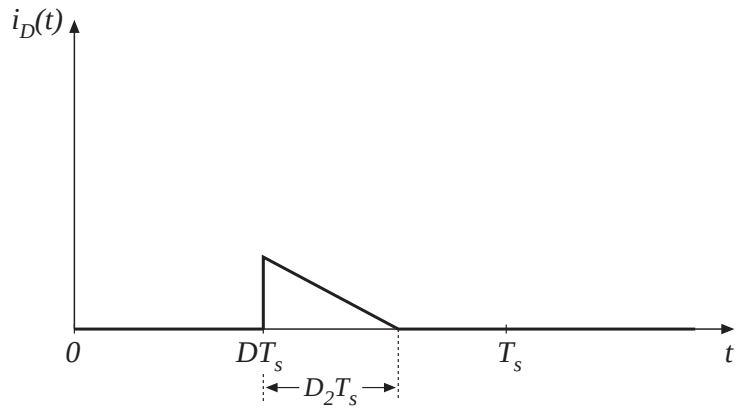
Further reduce load current

Increase R some more, such that $I < \Delta i_L$

Discontinuous conduction mode







Minimum diode current is $(I - \Delta i_L)$

Dc component $I = V/R$

Current ripple is

$$\Delta i_L = \frac{(V_g - V)}{2L} DT_s = \frac{V_g DD'T_s}{2L}$$

Note that I depends on load, but Δi_L does not.

The load current continues to be positive and non-zero.

Mode boundary

$$I > \Delta i_L \quad \textit{for CCM}$$
$$I < \Delta i_L \quad \textit{for DCM}$$

Insert buck converter expressions for I and Δi_L :

$$\frac{DV_g}{R} < \frac{DD'T_sV_g}{2L}$$

Simplify:

$$\frac{2L}{RT_s} < D'$$

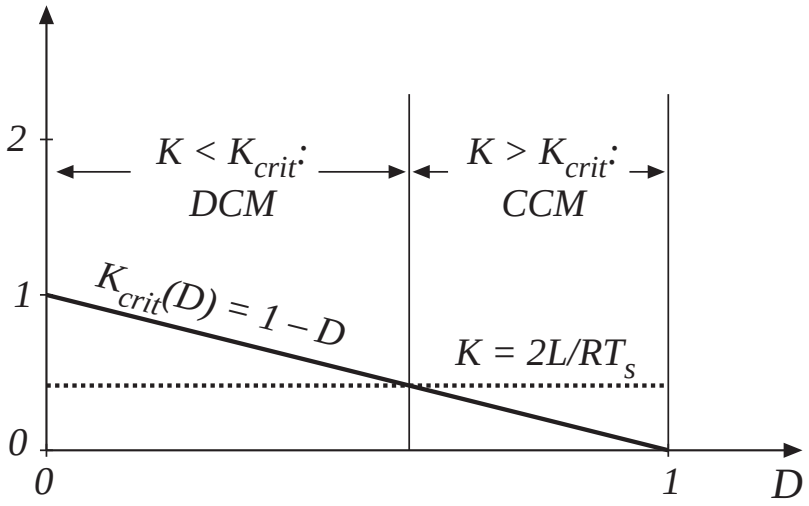
This expression is of the form

$$K < K_{crit}(D) \qquad \textit{for DCM}$$

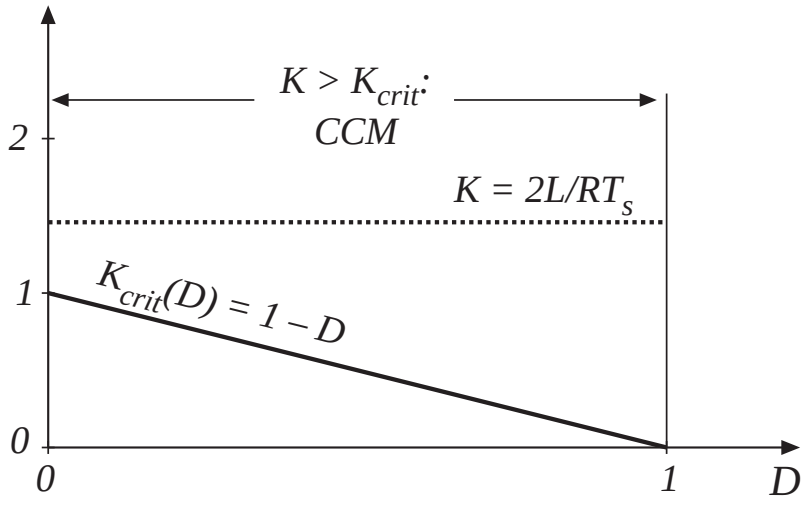
where $\quad K = \frac{2L}{RT_s} \quad \textit{and} \quad K_{crit}(D) = D'$

K and K_{crit} vs. D

for $K < 1$:



for $K > 1$:



Critical load resistance R_{crit}

Solve K_{crit} equation for load resistance R:

$$R < R_{crit}(D) \qquad \textit{for CCM}$$

$$R > R_{crit}(D) \qquad \textit{for DCM}$$

where $$R_{crit}(D) = \frac{2L}{D'T_s}$$

Summary: mode boundary

$$K > K_{crit}(D) \quad \textit{or} \quad R < R_{crit}(D) \quad \textit{for CCM}$$
$$K < K_{crit}(D) \quad \textit{or} \quad R > R_{crit}(D) \quad \textit{for DCM}$$

Table 5.1. CCM-DCM mode boundaries for the buck, boost, and buck-boost converters

Converter	$K_{crit}(D)$	$\max_{0 \le D \le 1}(K_{crit})$	$R_{crit}(D)$	$\min_{0 \le D \le 1}(R_{crit})$
Buck	$(1 - D)$	1	$\frac{2L}{(1-D)T_s}$	$2\frac{L}{T_s}$
Boost	$D(1 - D)^2$	$\frac{4}{27}$	$\frac{2L}{D(1-D)^2 T_s}$	$\frac{27}{2}\frac{L}{T_s}$
Buck-boost	$(1 - D)^2$	1	$\frac{2L}{(1-D)^2 T_s}$	$2\frac{L}{T_s}$

5.2. Analysis of the conversion ratio *M(D,K)*

Analysis techniques for the discontinuous conduction mode:

Inductor volt-second balance

$$\left\langle v_L \right\rangle = \frac{1}{T_s} \int_0^{T_s} v_L(t)\, dt = 0$$

Capacitor charge balance

$$\left\langle i_C \right\rangle = \frac{1}{T_s} \int_0^{T_s} i_C(t)\, dt = 0$$

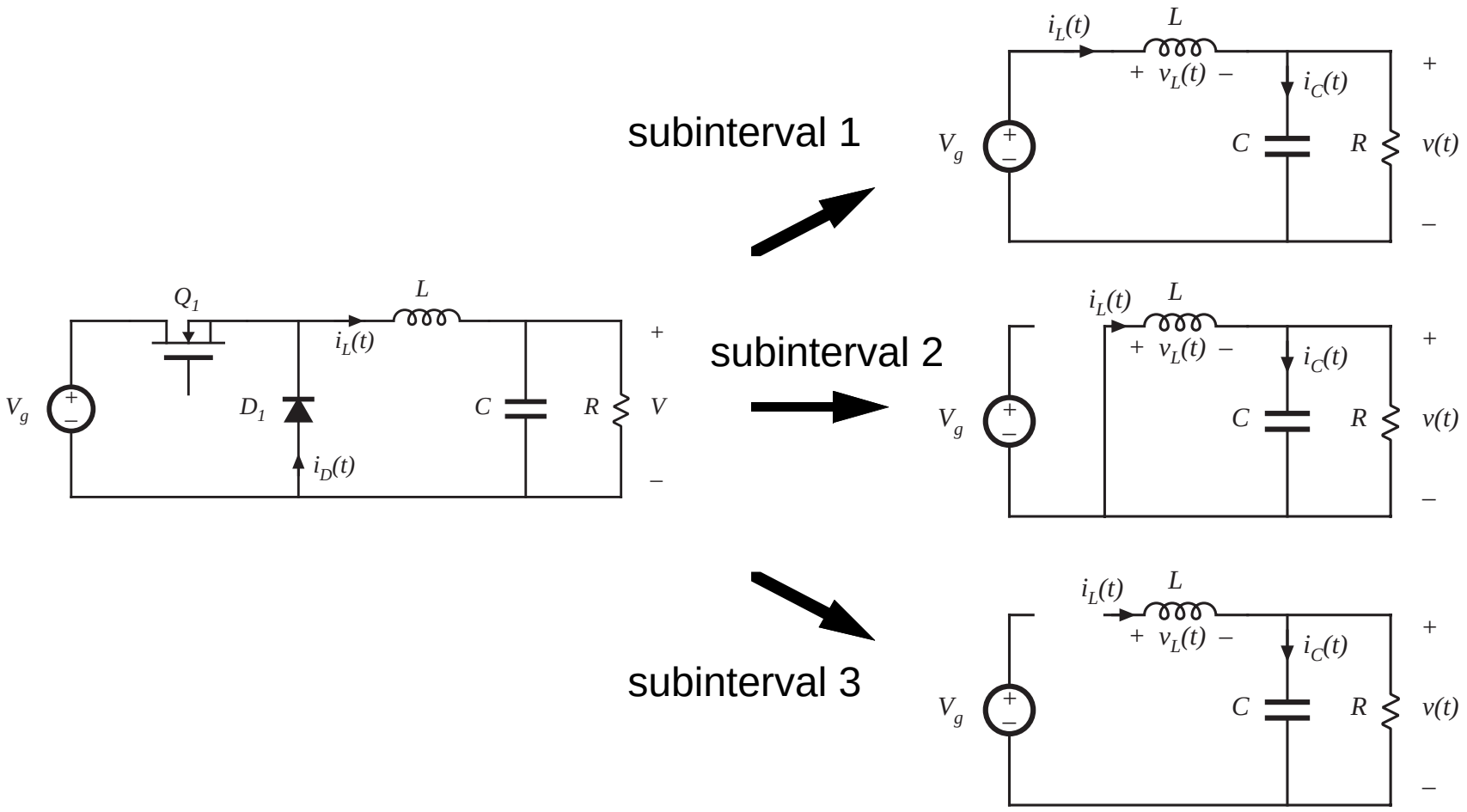
Small ripple approximation sometimes applies:

$v(t) \approx V$ because $\Delta v << V$

$i(t) \approx I$ is a poor approximation when $\Delta i > I$

Converter steady-state equations obtained via charge balance on each capacitor and volt-second balance on each inductor. Use care in applying small ripple approximation.

Example: Analysis of DCM buck converter *M(D,K)*

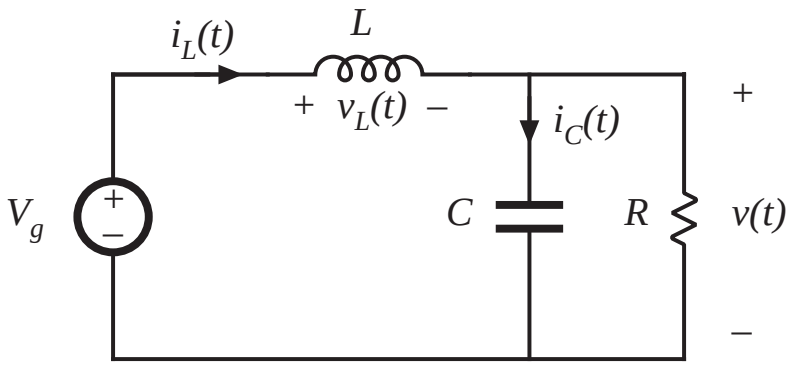


Subinterval 1

$$v_L(t) = V_g - v(t)$$
$$i_C(t) = i_L(t) - v(t) / R$$

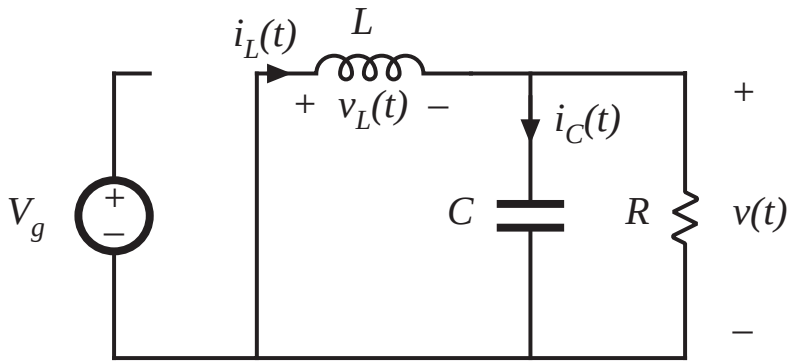
Small ripple approximation for *v(t)* (but not for *i(t)*!):

$$v_L(t) \approx V_g - V$$
$$i_C(t) \approx i_L(t) - V / R$$



Subinterval 2

$$v_L(t) = -\,v(t)$$
$$i_C(t) = i_L(t) - v(t) / R$$



Small ripple approximation for *v(t)* but not for *i(t)*:

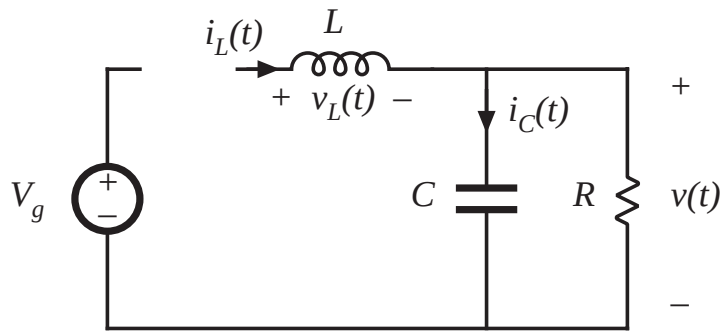
$$v_L(t) \approx -\,V$$
$$i_C(t) \approx i_L(t) - V / R$$

Subinterval 3

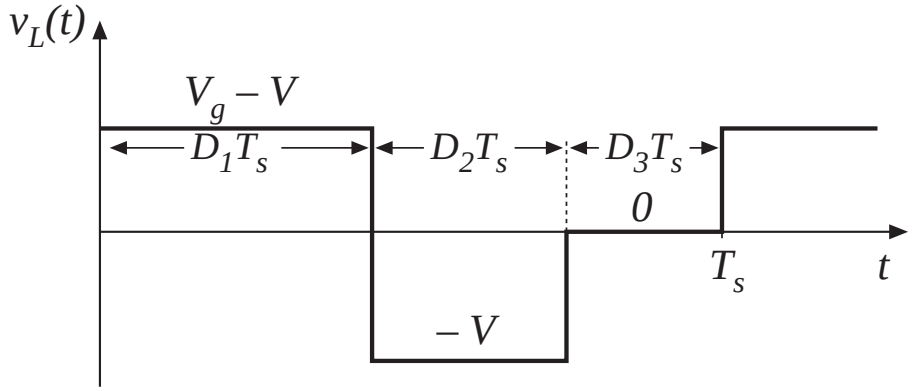
$$v_L = 0, \quad i_L = 0$$
$$i_C(t) = i_L(t) - v(t) / R$$

Small ripple approximation:

$$v_L(t) = 0$$
$$i_C(t) = -V / R$$



Inductor volt-second balance



Volt-second balance:

$$\left\langle v_L(t) \right\rangle = D_1(V_g - V) + D_2(-V) + D_3(0) = 0$$

Solve for V:

$$V = V_g \frac{D_1}{D_1 + D_2}$$

note that D_2 is unknown

Capacitor charge balance

node equation:

$$i_L(t) = i_C(t) + V / R$$

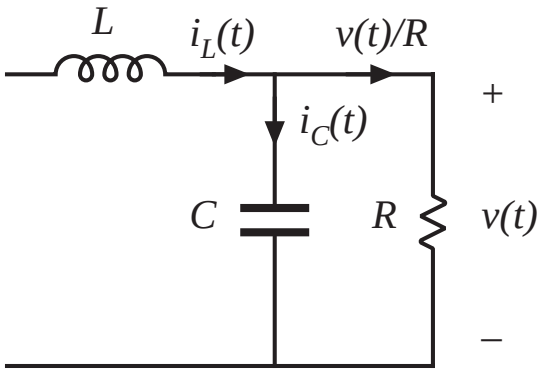
capacitor charge balance:

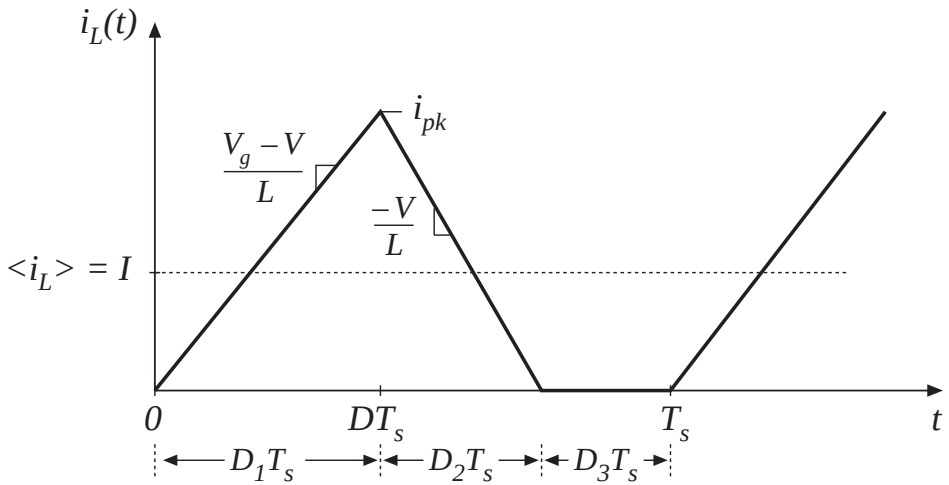
$$\langle i_C \rangle = 0$$

hence

$$\langle i_L \rangle = V / R$$

must compute dc component of inductor current and equate to load current (for this buck converter example)





Inductor current waveform

peak current:

$$i_L(D_1 T_s) = i_{pk} = \frac{V_g - V}{L} D_1 T_s$$

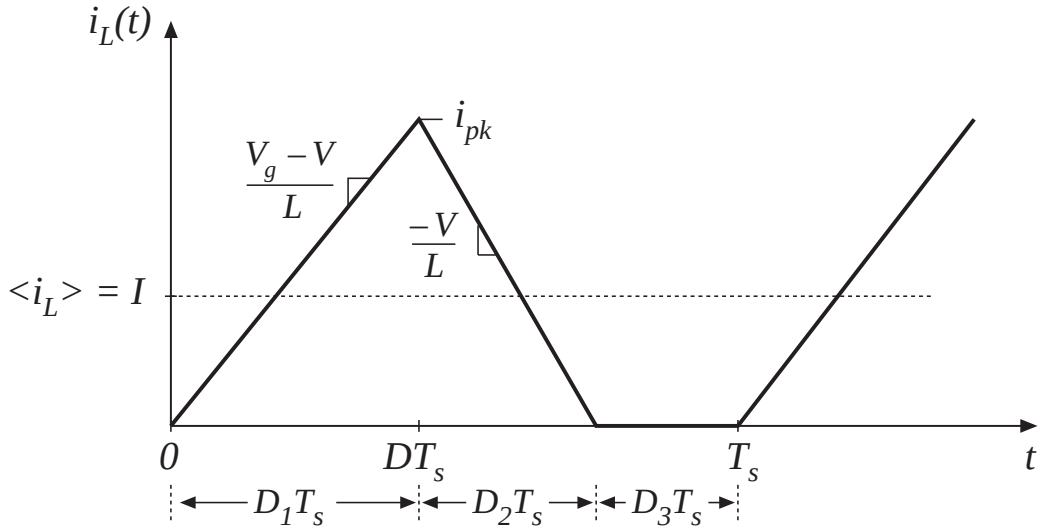
average current:

$$\left\langle i_L \right\rangle = \frac{1}{T_s} \int_0^{T_s} i_L(t)\, dt$$

triangle area formula:

$$\int_0^{T_s} i_L(t)\, dt = \frac{1}{2}\, i_{pk}\, (D_1 + D_2) T_s$$

$$\left\langle i_L \right\rangle = (V_g - V) \frac{D_1 T_s}{2L} (D_1 + D_2)$$



equate dc component to dc load current:

$$\frac{V}{R} = \frac{D_1 T_s}{2L} (D_1 + D_2) (V_g - V)$$

Solution for V

Two equations and two unknowns (V and D_2):

$$V = V_g \frac{D_1}{D_1 + D_2}$$ (from inductor volt-second balance)

$$\frac{V}{R} = \frac{D_1 T_s}{2L} (D_1 + D_2) (V_g - V)$$ (from capacitor charge balance)

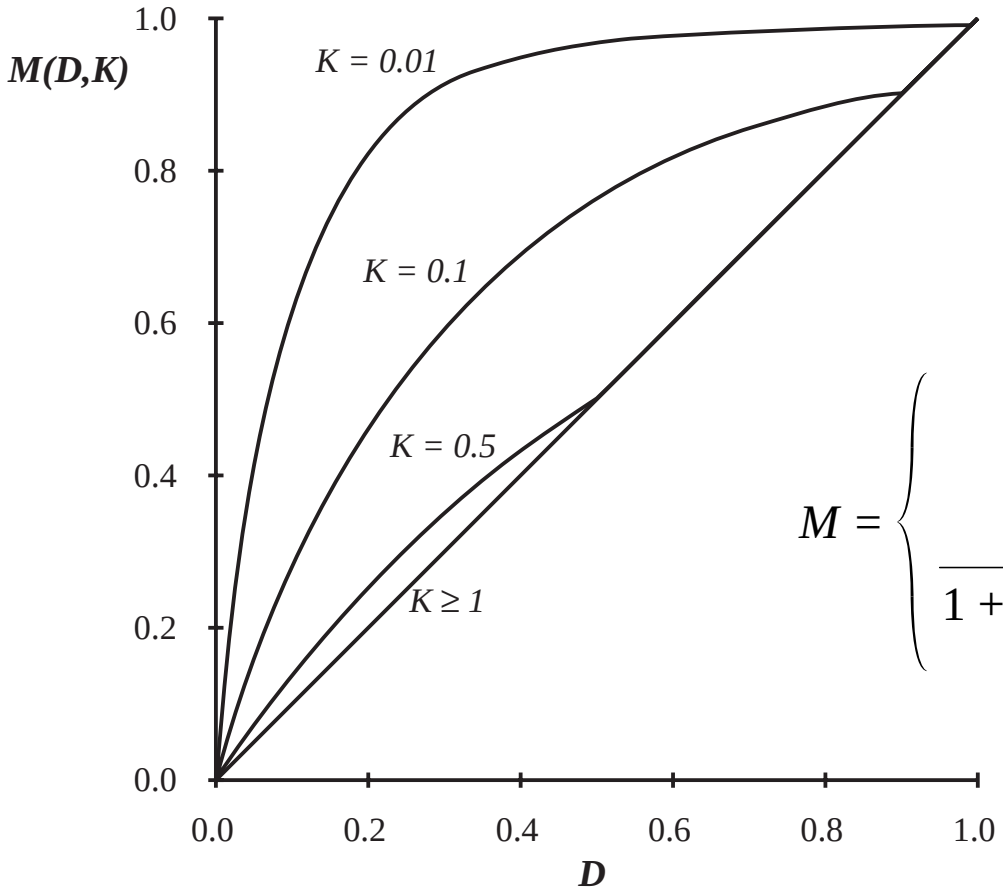
Eliminate D_2 , solve for V :

$$\frac{V}{V_g} = \frac{2}{1 + \sqrt{1 + 4K / D_1^2}}$$

where $K = 2L / RT_s$

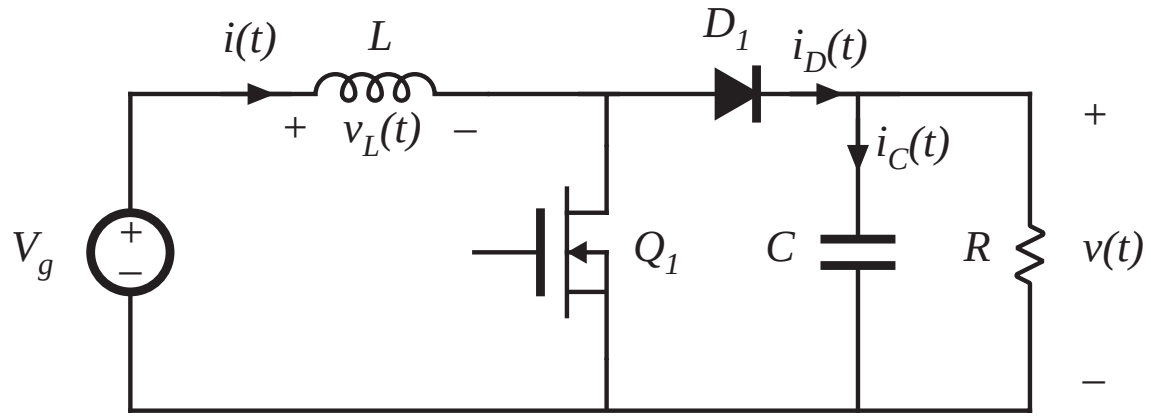
valid for $K < K_{crit}$

Buck converter *M(D,K)*



$$M = \begin{cases} D & \text{for } K > K_{crit} \\ \dfrac{2}{1 + \sqrt{1 + 4K / D^2}} & \text{for } K < K_{crit} \end{cases}$$

5.3. Boost converter example



Mode boundary:

$I > \Delta i_L$ *for CCM*

$I < \Delta i_L$ *for DCM*

Previous CCM soln:

$$I = \frac{V_g}{D'^2 R} \qquad \Delta i_L = \frac{V_g}{2L} DT_s$$

Mode boundary

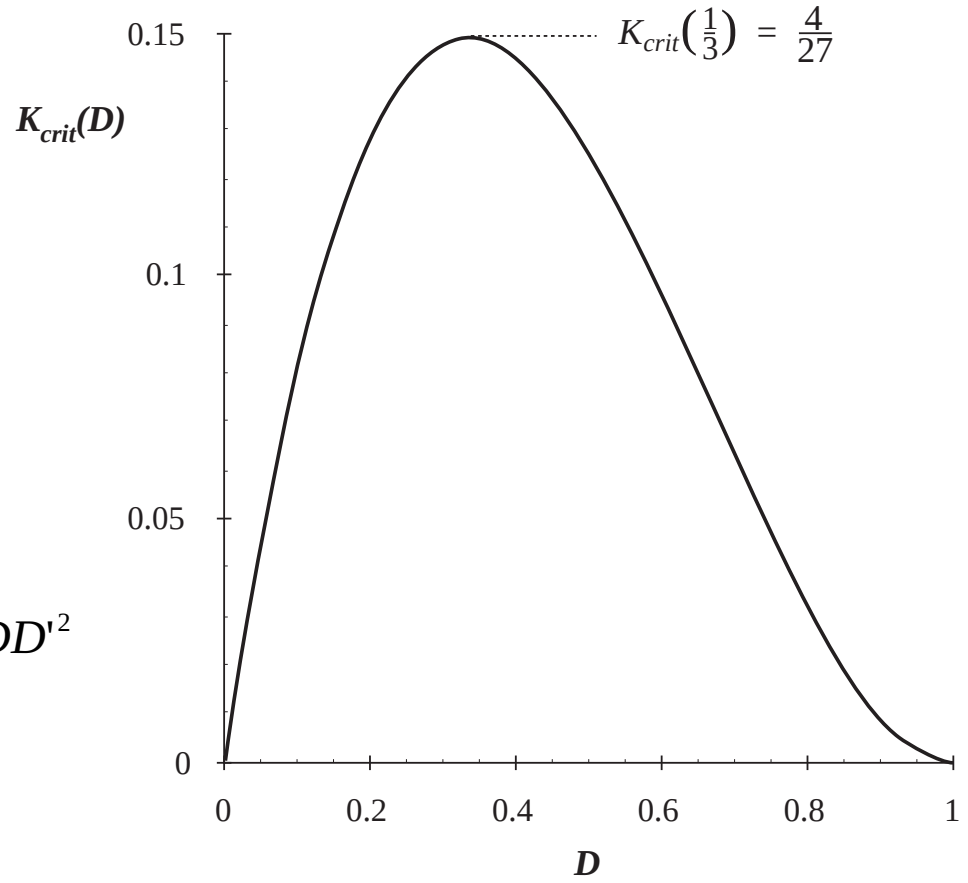
$$\frac{V_g}{D'^2 R} > \frac{DT_s V_g}{2L} \qquad \text{for CCM}$$

$$\frac{2L}{RT_s} > DD'^2 \qquad \text{for CCM}$$

$$K > K_{crit}(D) \qquad \text{for CCM}$$

$$K < K_{crit}(D) \qquad \text{for DCM}$$

where $K = \frac{2L}{RT_s}$ and $K_{crit}(D) = DD'^2$

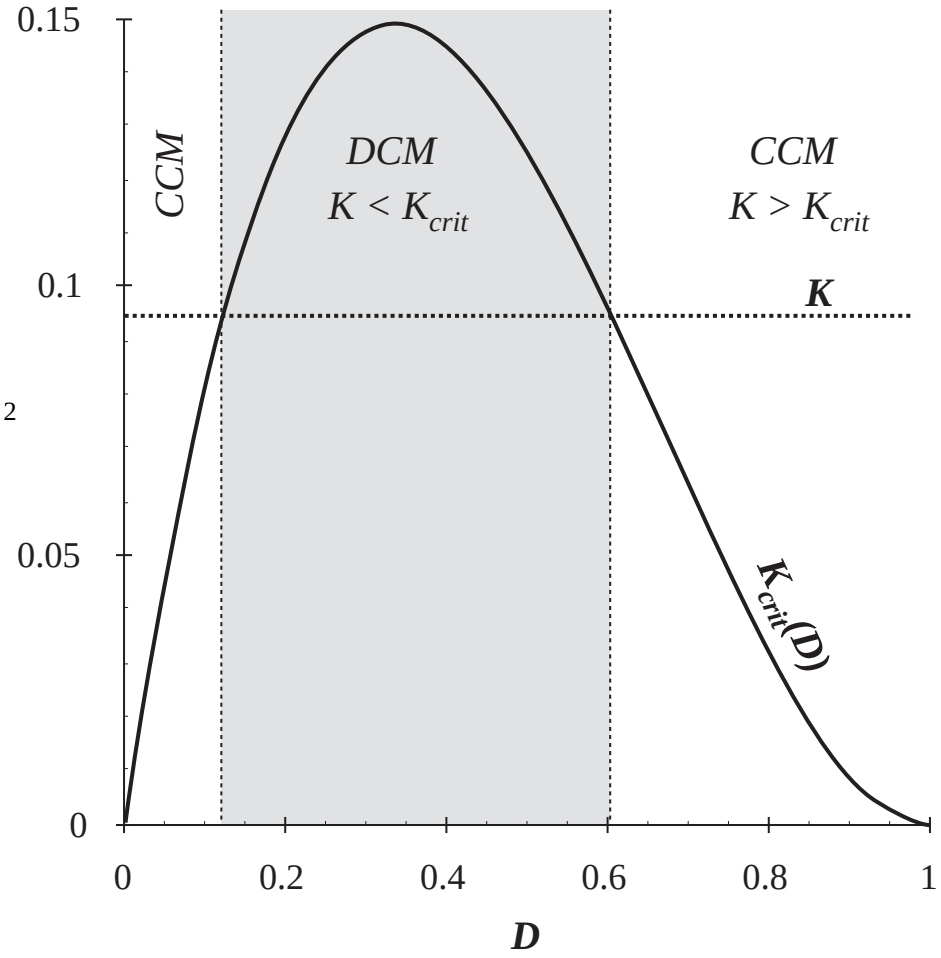


Mode boundary

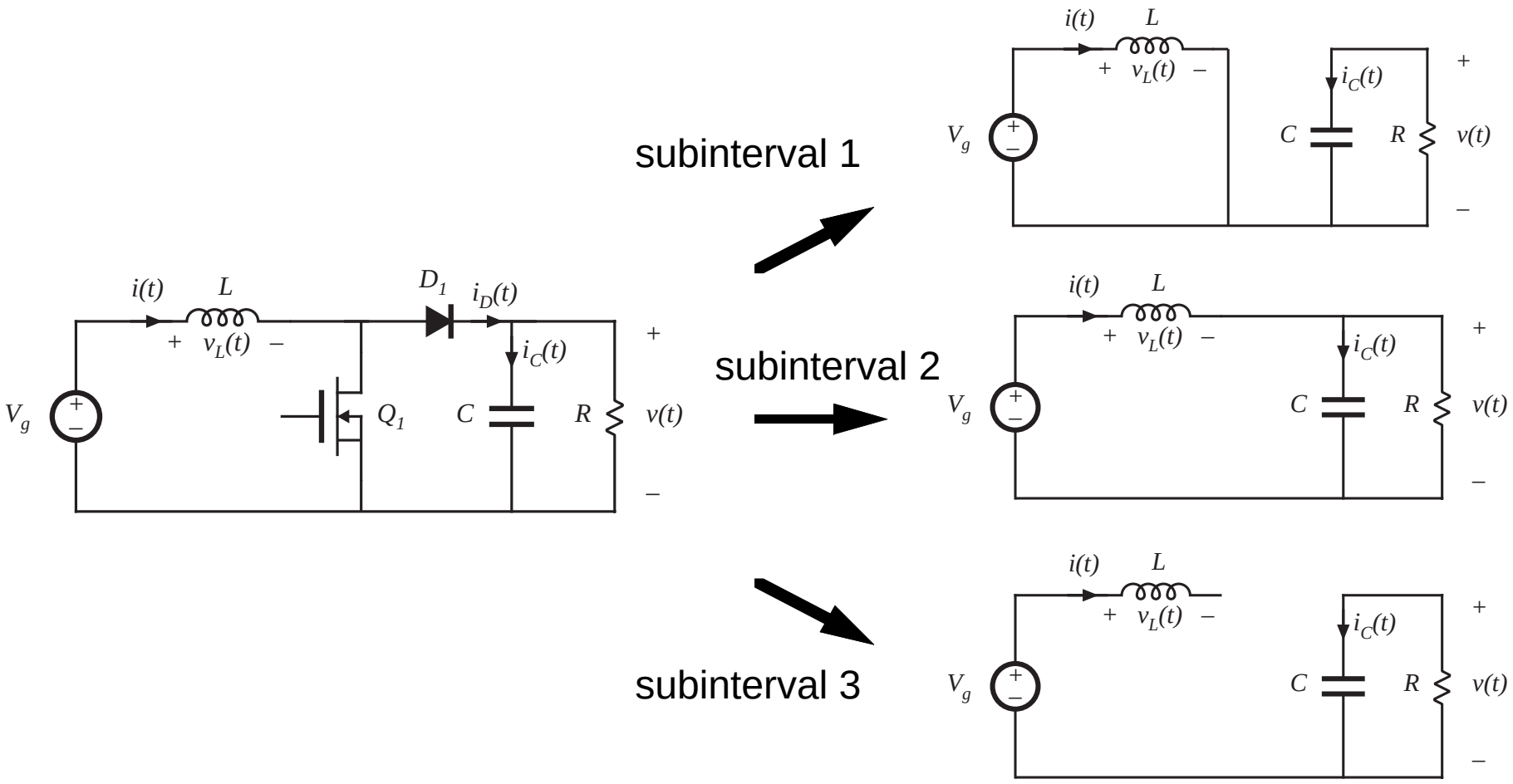
$K > K_{crit}(D)$ *for CCM*

$K < K_{crit}(D)$ *for DCM*

where $K = \frac{2L}{RT_s}$ *and* $K_{crit}(D) = DD'^2$



Conversion ratio: DCM boost

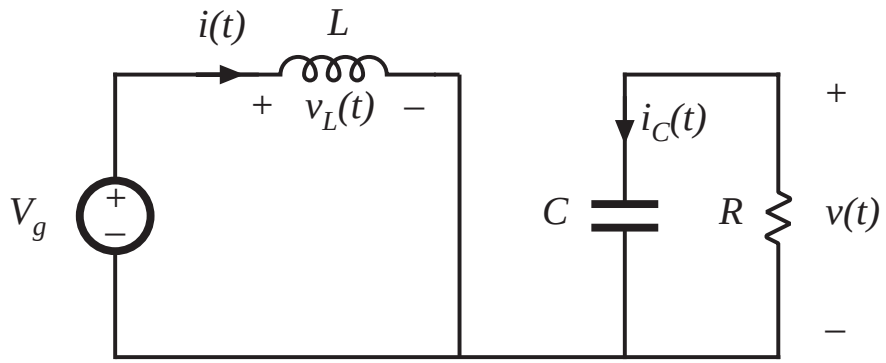


Subinterval 1

$$v_L(t) = V_g$$
$$i_C(t) = -v(t) / R$$

Small ripple approximation for *v(t)* (but not for *i(t)*!):

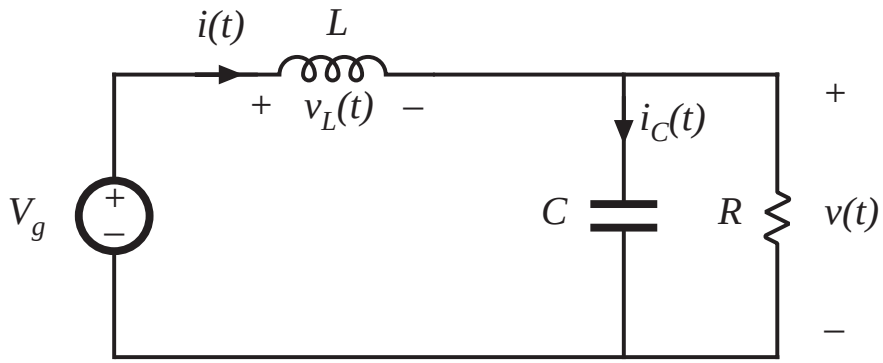
$$v_L(t) \approx V_g$$
$$i_C(t) \approx -V / R$$



$$0 < t < D_1 T_s$$

Subinterval 2

$$v_L(t) = V_g - v(t)$$
$$i_C(t) = i(t) - v(t) / R$$



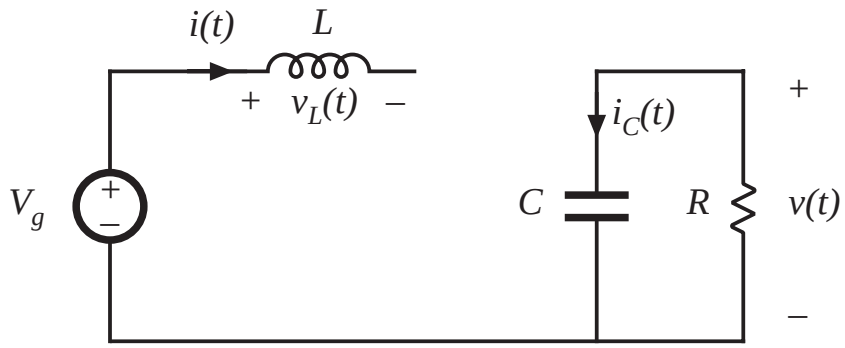
Small ripple approximation for *v(t)* but not for *i(t)*:

$$v_L(t) \approx V_g - V$$
$$i_C(t) \approx i(t) - V / R$$

$$D_1 T_s < t < (D_1 + D_2) T_s$$

Subinterval 3

$$v_L = 0, \quad i = 0$$
$$i_C(t) = -\, v(t) / R$$

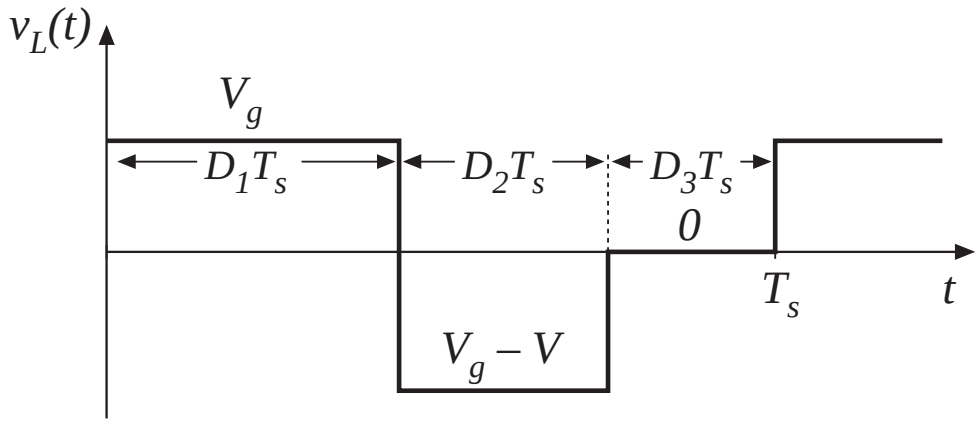


Small ripple approximation:

$$v_L(t) = 0$$
$$i_C(t) = -\, V / R$$

$$(D_1 + D_2)T_s < t < T_s$$

Inductor volt-second balance



Volt-second balance:

$$D_1 V_g + D_2(V_g - V) + D_3(0) = 0$$

Solve for V:

$$V = \frac{D_1 + D_2}{D_2} V_g$$

note that D_2 is unknown

Capacitor charge balance

node equation:

$$i_D(t) = i_C(t) + v(t) / R$$

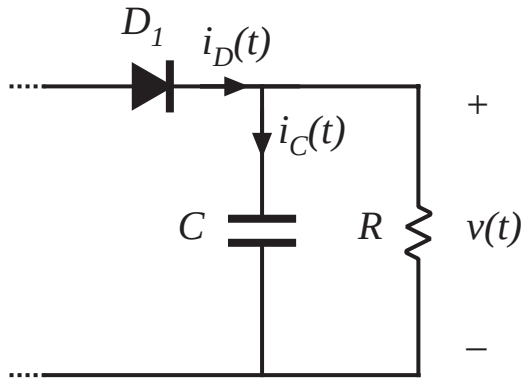
capacitor charge balance:

$$\langle i_C \rangle = 0$$

hence

$$\langle i_D \rangle = V / R$$

must compute dc component of diode current and equate to load current (for this boost converter example)



Inductor and diode current waveforms

peak current:

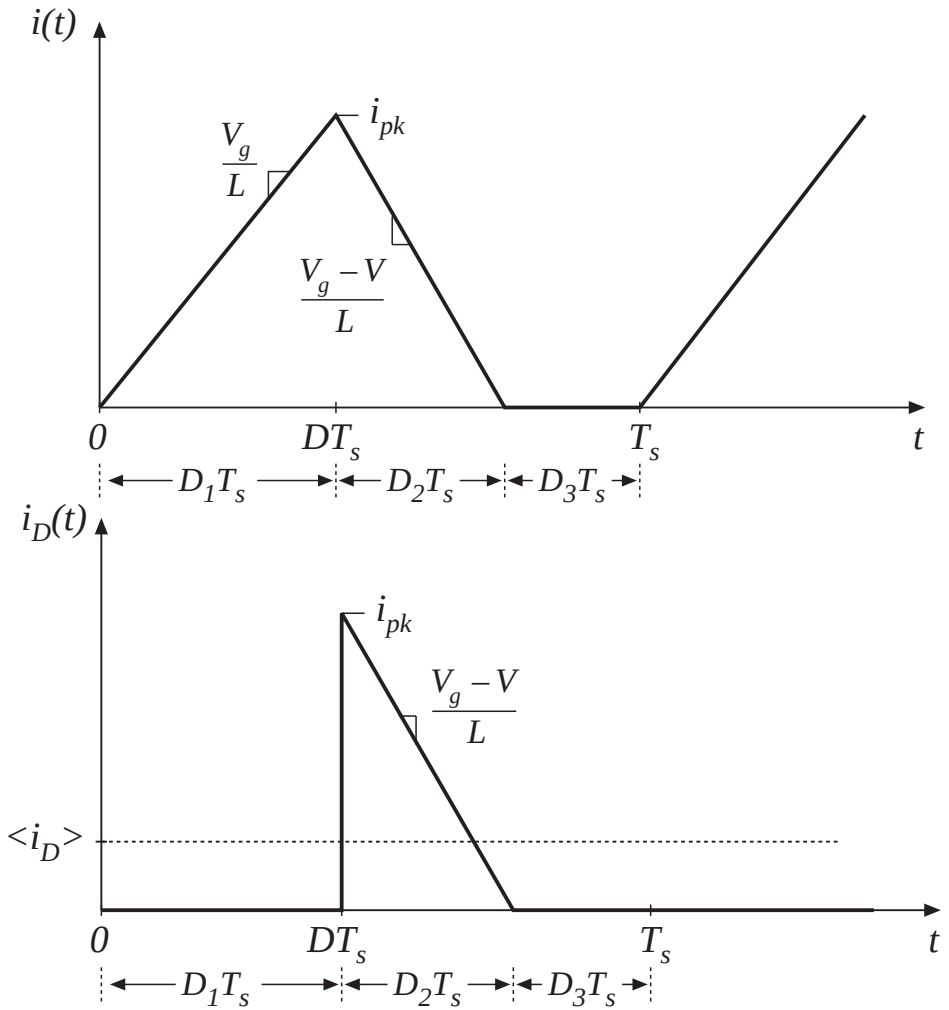
$$i_{pk} = \frac{V_g}{L} D_1 T_s$$

average diode current:

$$\left\langle i_D \right\rangle = \frac{1}{T_s} \int_0^{T_s} i_D(t)\, dt$$

triangle area formula:

$$\int_0^{T_s} i_D(t)\, dt = \frac{1}{2}\, i_{pk}\, D_2 T_s$$



Equate diode current to load current

average diode current:

$$\left\langle i_D \right\rangle = \frac{1}{T_s}\left(\frac{1}{2}\, i_{pk}\, D_2 T_s\right) = \frac{V_g D_1 D_2 T_s}{2L}$$

equate to dc load current:

$$\frac{V_g D_1 D_2 T_s}{2L} = \frac{V}{R}$$

Solution for V

Two equations and two unknowns (V and D_2):

$$V = \frac{D_1 + D_2}{D_2} V_g$$ (from inductor volt-second balance)

$$\frac{V_g D_1 D_2 T_s}{2L} = \frac{V}{R}$$ (from capacitor charge balance)

Eliminate D_2 , solve for V. From volt-sec balance eqn:

$$D_2 = D_1 \frac{V_g}{V - V_g}$$

Substitute into charge balance eqn, rearrange terms:

$$V^2 - V V_g - \frac{V_g^2 D_1^2}{K} = 0$$

Solution for V

$$V^2 - VV_g - \frac{V_g^2 D_1^2}{K} = 0$$

Use quadratic formula:

$$\frac{V}{V_g} = \frac{1 \pm \sqrt{1 + 4D_1^2 / K}}{2}$$

Note that one root leads to positive V, while other leads to negative V. Select positive root:

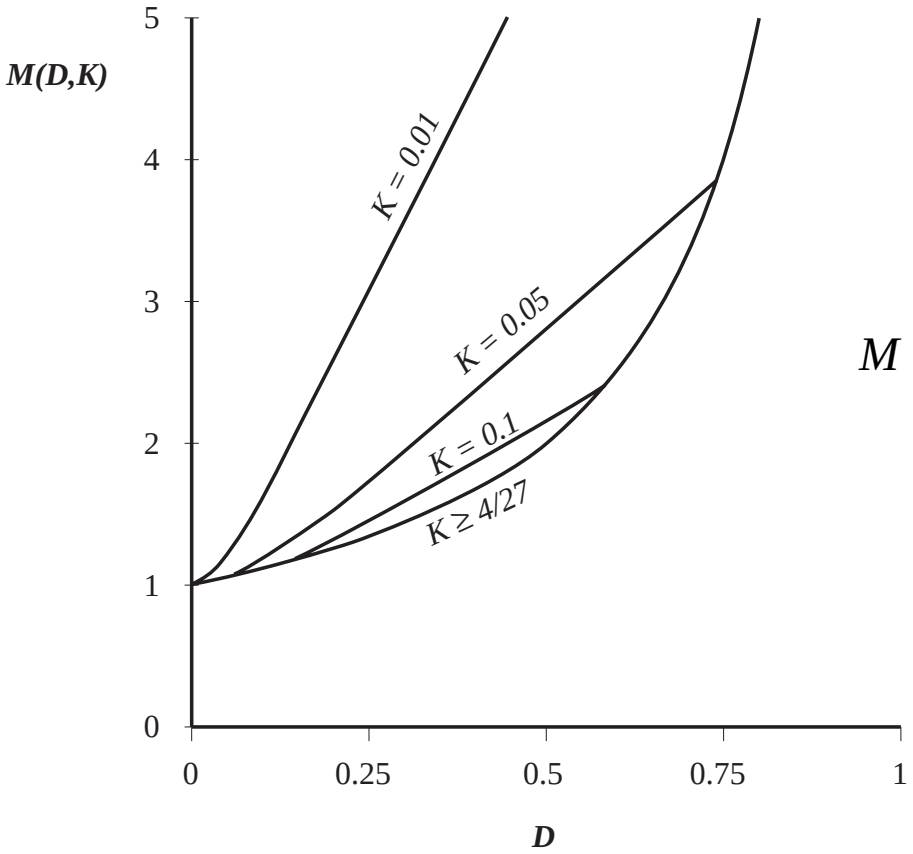
$$\frac{V}{V_g} = M(D_1, K) = \frac{1 + \sqrt{1 + 4D_1^2 / K}}{2}$$

where $K = 2L / RT_s$

valid for $K < K_{crit}(D)$

Transistor duty cycle D = interval *1* duty cycle D_1

Boost converter characteristics



$$M = \begin{cases} \dfrac{1}{1-D} & \text{for } K > K_{crit} \\ \dfrac{1+\sqrt{1+4D^2/K}}{2} & \text{for } K < K_{crit} \end{cases}$$

Approximate M in DCM:

$$M \approx \frac{1}{2} + \frac{D}{\sqrt{K}}$$

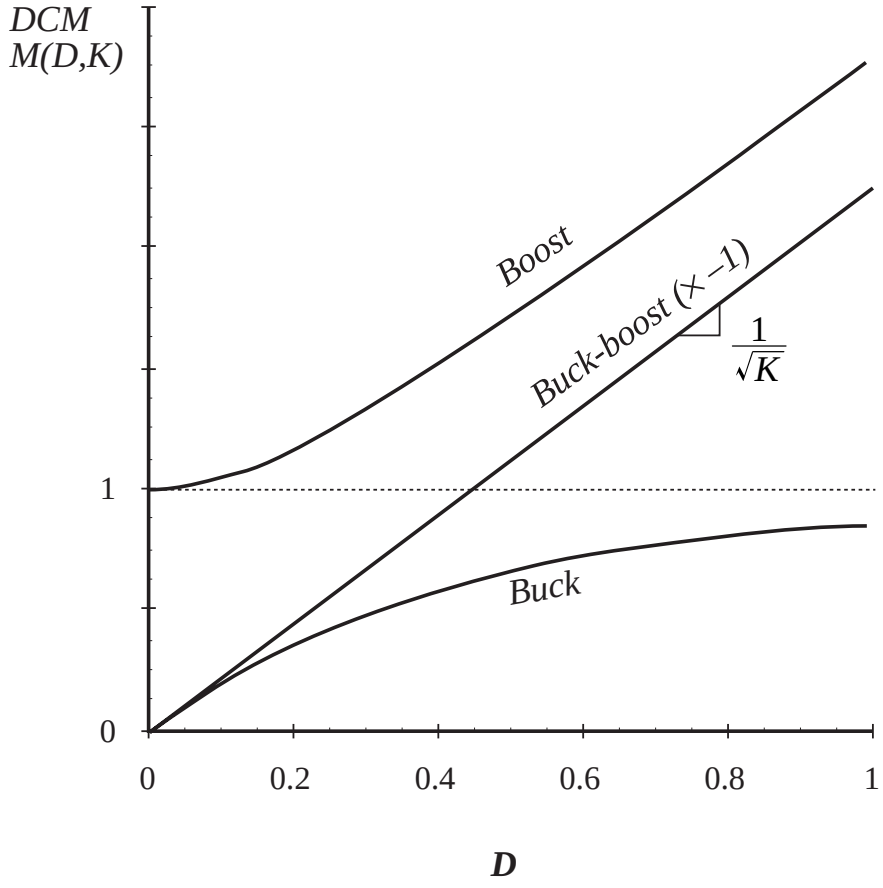
Summary of DCM characteristics

Table 5.2. Summary of CCM-DCM characteristics for the buck, boost, and buck-boost converters

Converter	$K_{crit}(D)$	*DCM* $M(D,K)$	*DCM* $D_2(D,K)$	*CCM* $M(D)$
Buck	$(1 - D)$	$\frac{2}{1 + \sqrt{1 + 4K / D^2}}$	$\frac{K}{D} M(D,K)$	D
Boost	$D (1 - D)^2$	$\frac{1 + \sqrt{1 + 4D^2 / K}}{2}$	$\frac{K}{D} M(D,K)$	$\frac{1}{1 - D}$
Buck-boost	$(1 - D)^2$	$-\frac{D}{\sqrt{K}}$	$\sqrt{K}$	$-\frac{D}{1 - D}$

with $K = 2L / RT_s$. *DCM occurs for* $K < K_{crit}$.

Summary of DCM characteristics



- DCM buck and boost characteristics are asymptotic to $M = 1$ and to the DCM buck-boost characteristic
- DCM buck-boost characteristic is linear
- CCM and DCM characteristics intersect at mode boundary. Actual M follows characteristic having larger magnitude
- DCM boost characteristic is nearly linear

Summary of key points

1. The discontinuous conduction mode occurs in converters containing current- or voltage-unidirectional switches, when the inductor current or capacitor voltage ripple is large enough to cause the switch current or voltage to reverse polarity.
2. Conditions for operation in the discontinuous conduction mode can be found by determining when the inductor current or capacitor voltage ripples and dc components cause the switch on-state current or off-state voltage to reverse polarity.
3. The dc conversion ratio M of converters operating in the discontinuous conduction mode can be found by application of the principles of inductor volt-second and capacitor charge balance.

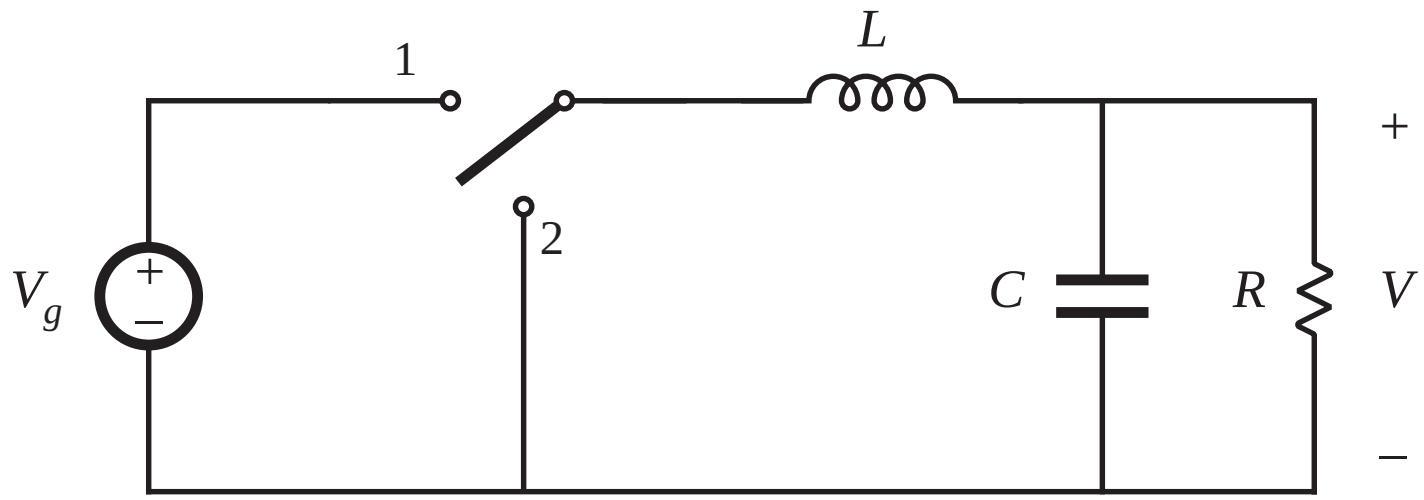
Summary of key points

4. Extra care is required when applying the small-ripple approximation. Some waveforms, such as the output voltage, should have small ripple which can be neglected. Other waveforms, such as one or more inductor currents, may have large ripple that cannot be ignored.
5. The characteristics of a converter changes significantly when the converter enters DCM. The output voltage becomes load-dependent, resulting in an increase in the converter output impedance.

Chapter 6. Converter Circuits

- Where do the boost, buck-boost, and other converters originate?
- How can we obtain a converter having given desired properties?
- What converters are possible?
- How can we obtain transformer isolation in a converter?
- For a given application, which converter is best?

6.1. Circuit Manipulations



Begin with buck converter: derived in Chapter 1 from first principles

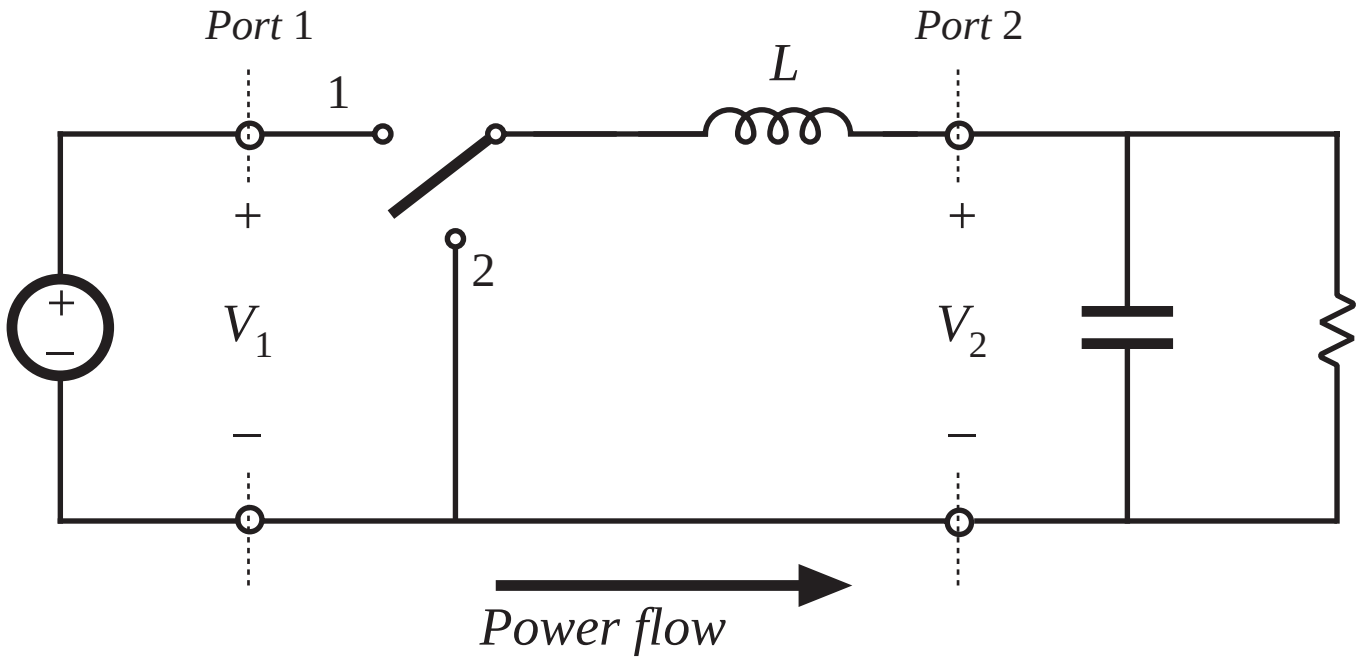
- Switch changes dc component, low-pass filter removes switching harmonics
- Conversion ratio is $M = D$

6.1.1. Inversion of source and load

Interchange power input and output ports of a converter

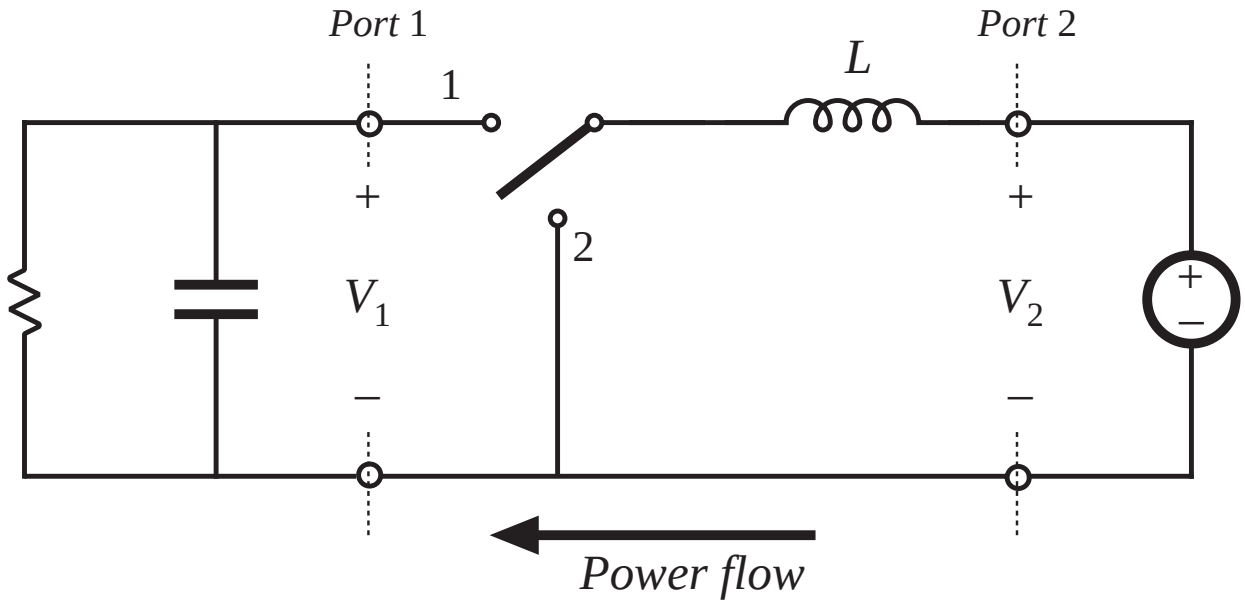
Buck converter example

$$V_2 = DV_1$$



Inversion of source and load

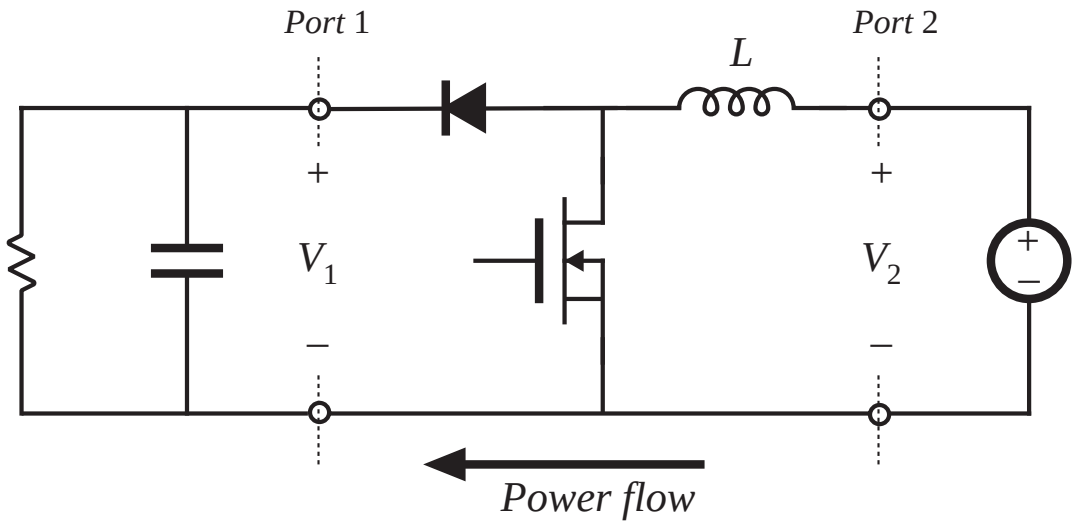
Interchange power source and load:



$$V_2 = DV_1 \qquad V_1 = \frac{1}{D} V_2$$

Realization of switches as in Chapter 4

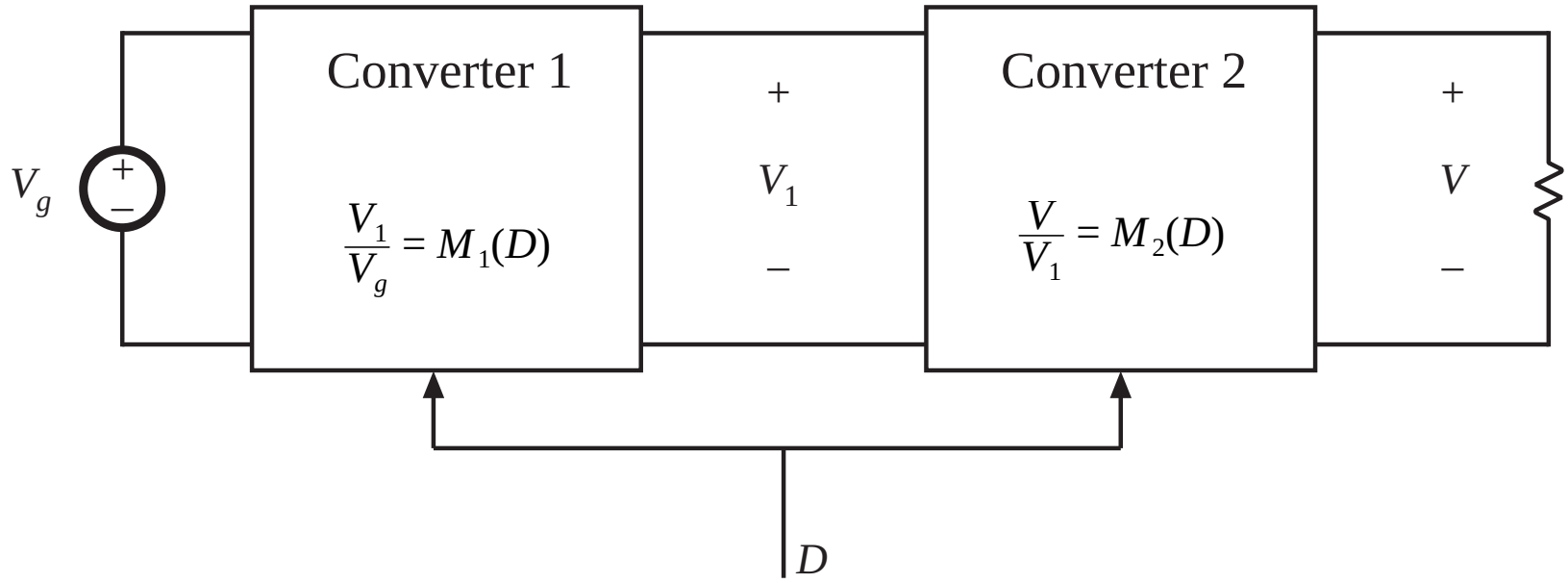
- Reversal of power flow requires new realization of switches
- Transistor conducts when switch is in position 2
- Interchange of D and D'



$$V_1 = \frac{1}{D'} V_2$$

Inversion of buck converter yields boost converter

6.1.2. Cascade connection of converters

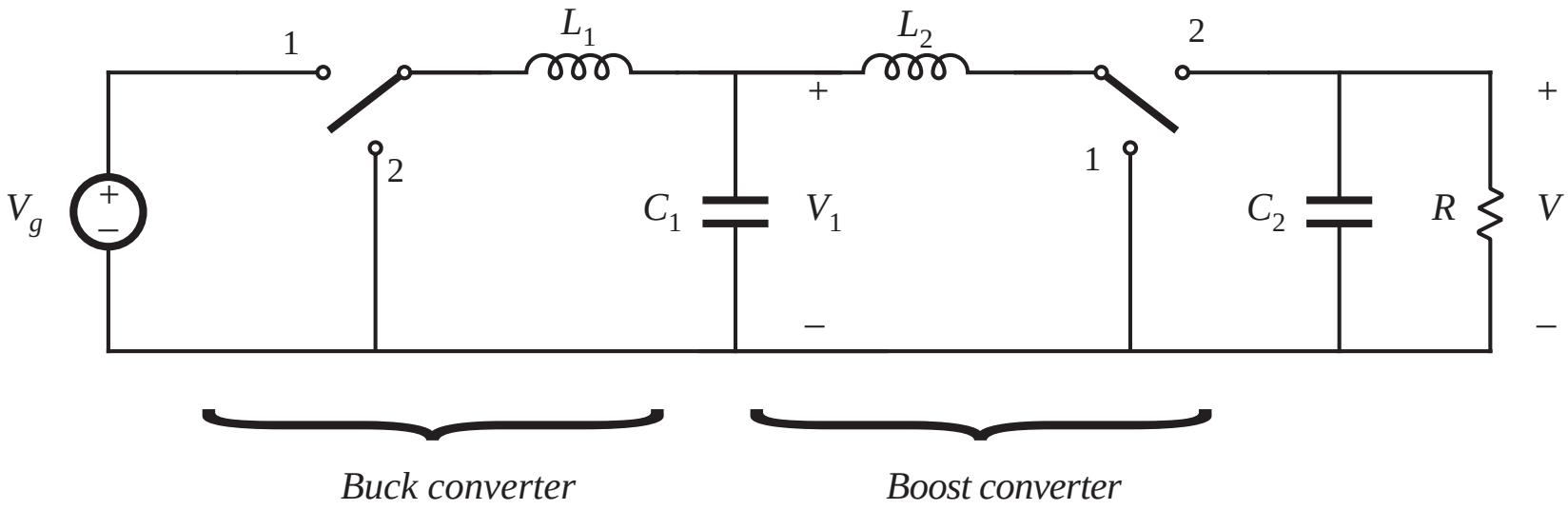


$$V_1 = M_1(D)V_g$$

$$V = M_2(D)V_1$$

$$\rightarrow \quad \frac{V}{V_g} = M(D) = M_1(D)M_2(D)$$

Example: buck cascaded by boost



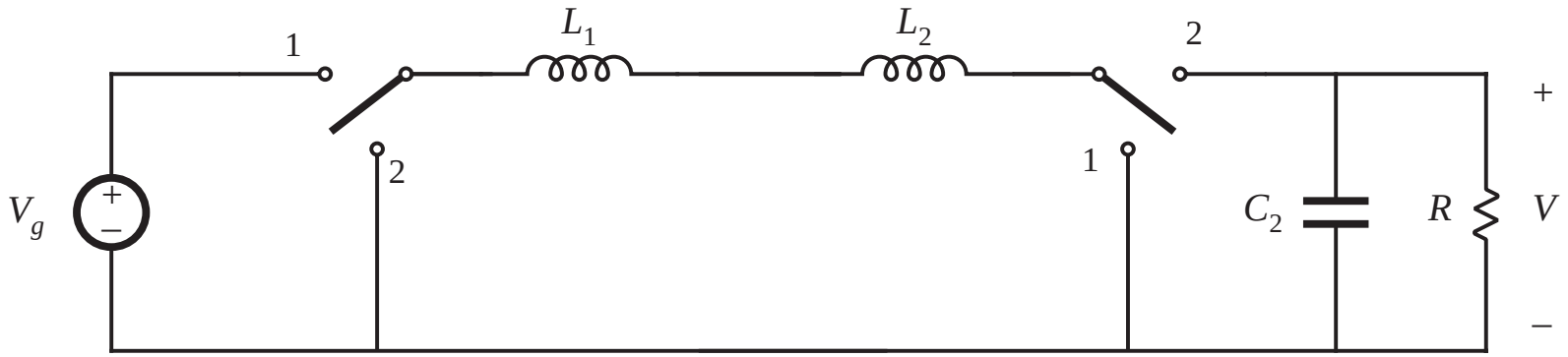
$$\frac{V_1}{V_g} = D$$

$$\frac{V}{V_1} = \frac{1}{1-D}$$

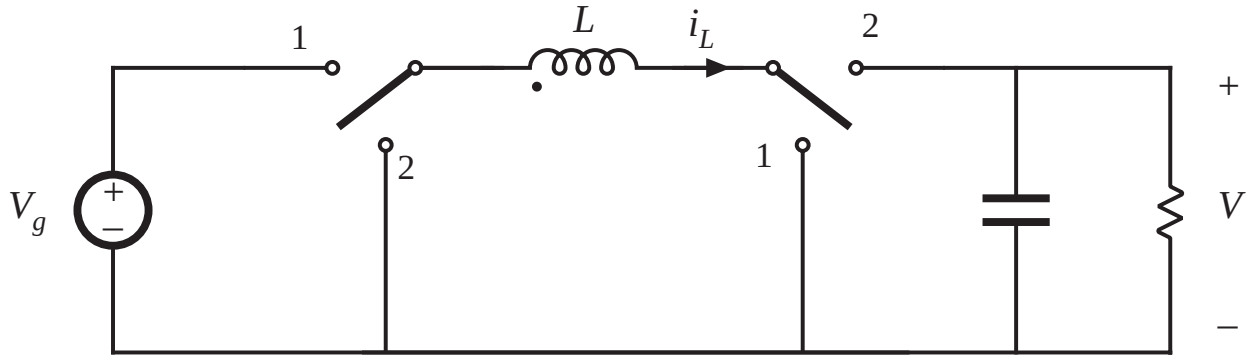
$$\longrightarrow \quad \frac{V}{V_g} = \frac{D}{1-D}$$

Buck cascaded by boost: simplification of internal filter

Remove capacitor C_1

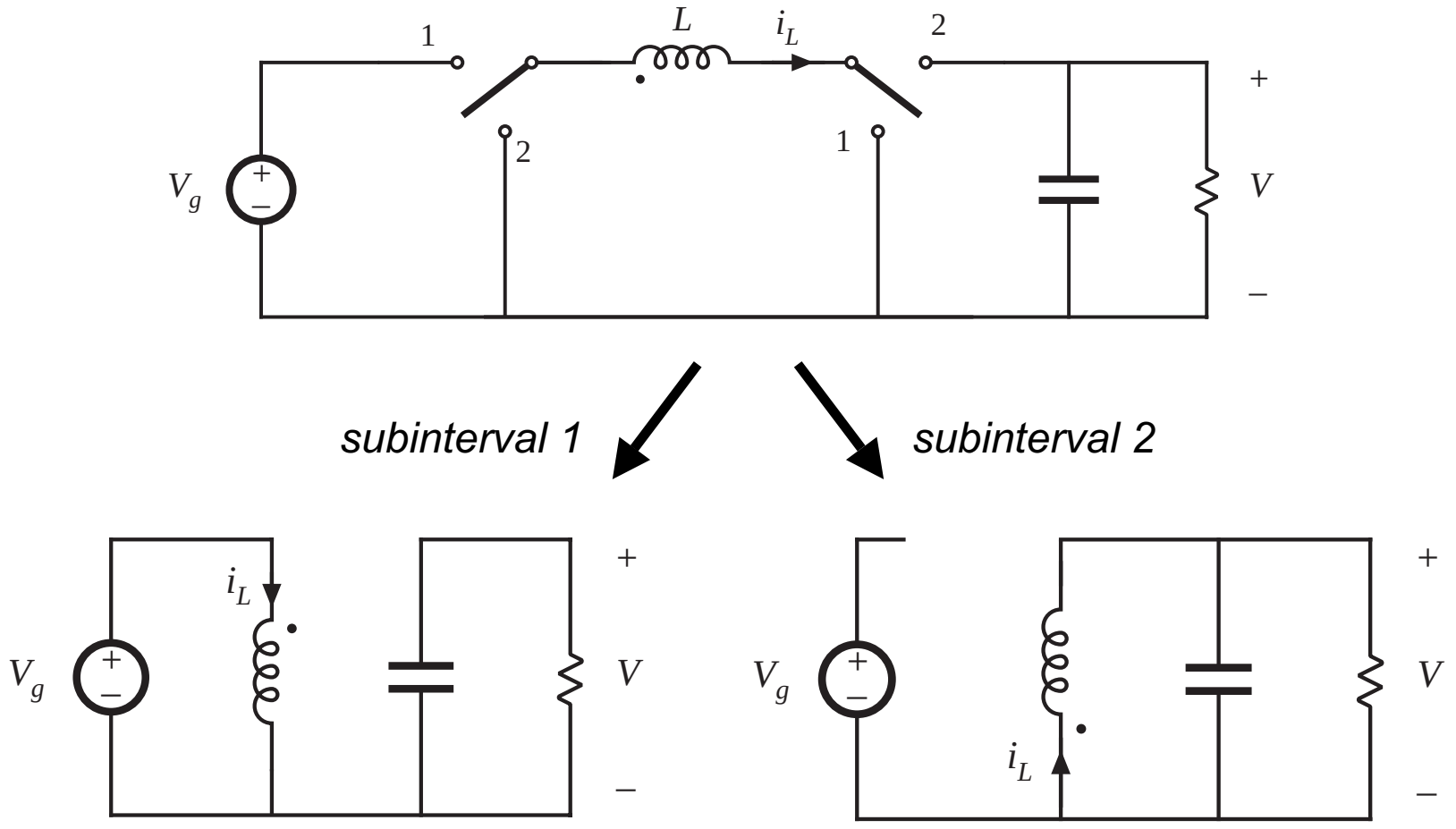


Combine inductors L_1 and L_2

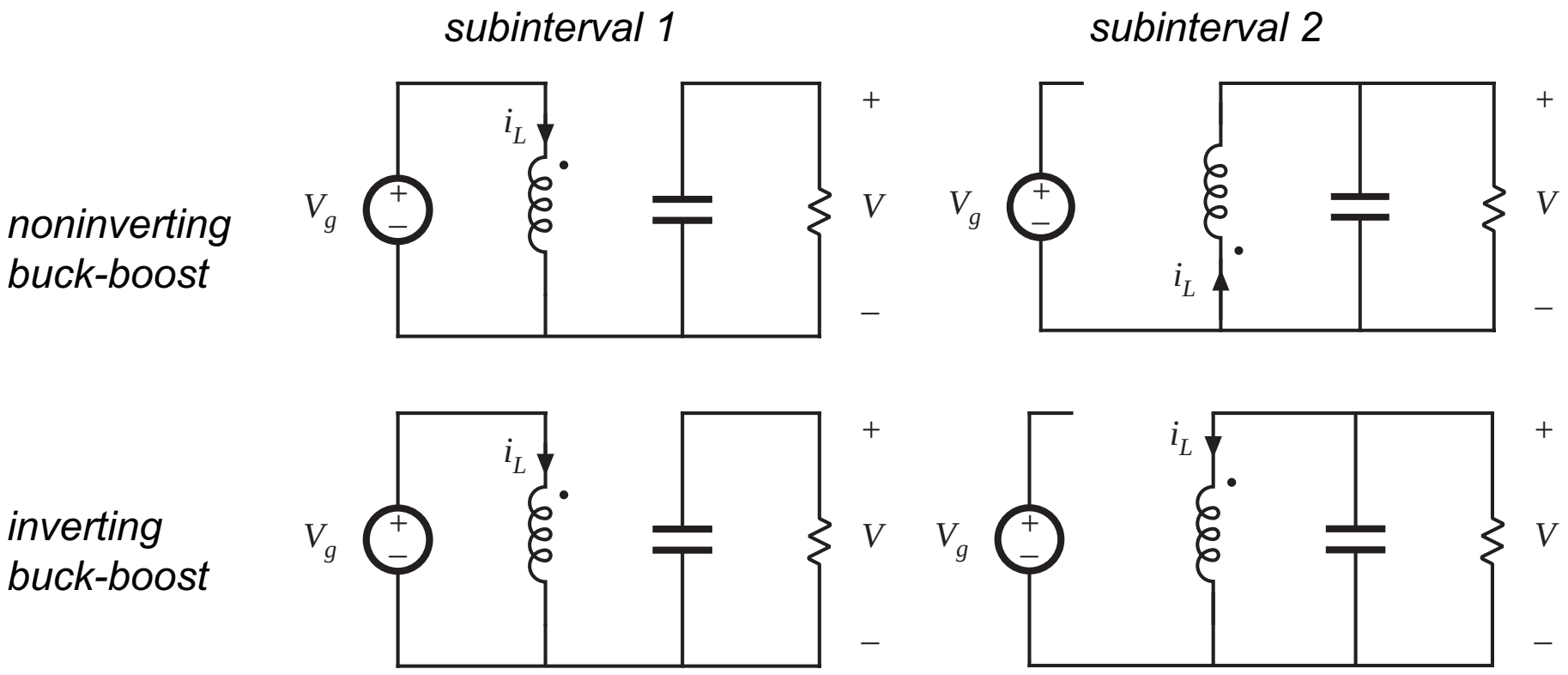


Noninverting buck-boost converter

Noninverting buck-boost converter

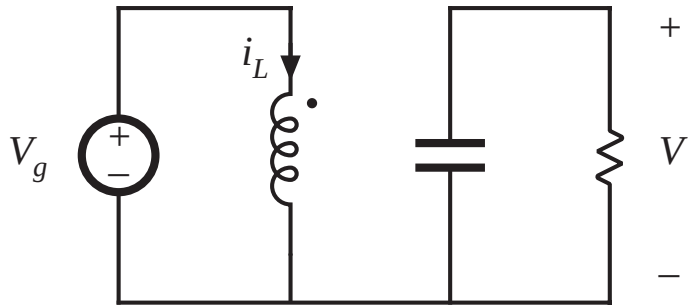


Reversal of output voltage polarity

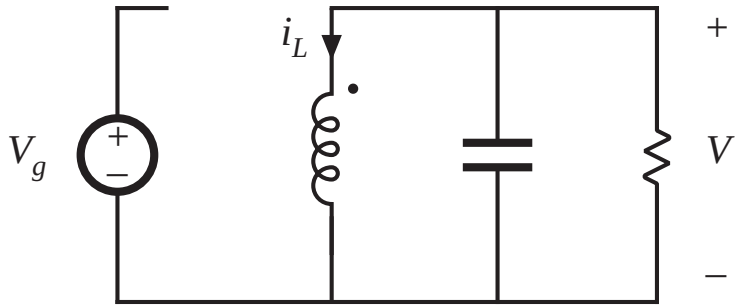


Reduction of number of switches: inverting buck-boost

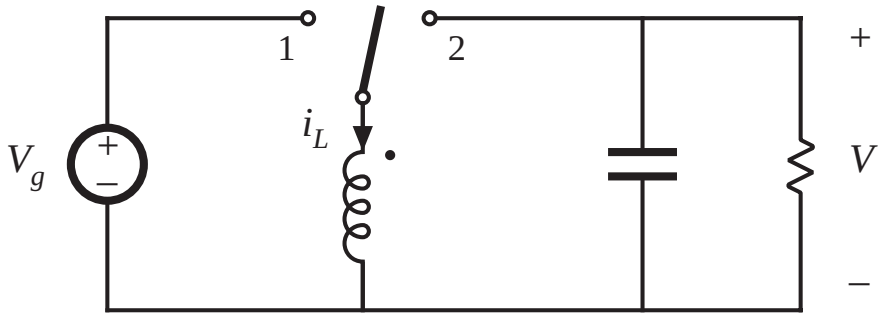
Subinterval 1



Subinterval 2



One side of inductor always connected to ground
— hence, only one SPDT switch needed:



$$\frac{V}{V_g} = -\frac{D}{1-D}$$

Discussion: cascade connections

- Properties of buck-boost converter follow from its derivation as buck cascaded by boost

  Equivalent circuit model: buck 1:D transformer cascaded by boost D':1 transformer

  Pulsating input current of buck converter

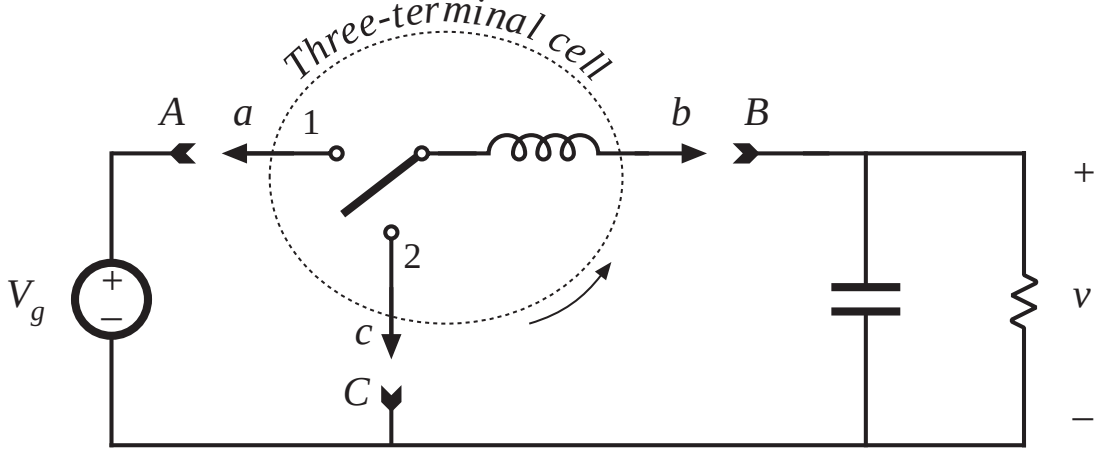
  Pulsating output current of boost converter

- Other cascade connections are possible

  Cuk converter: boost cascaded by buck

6.1.3. Rotation of three-terminal cell

Treat inductor and SPDT switch as three-terminal cell:

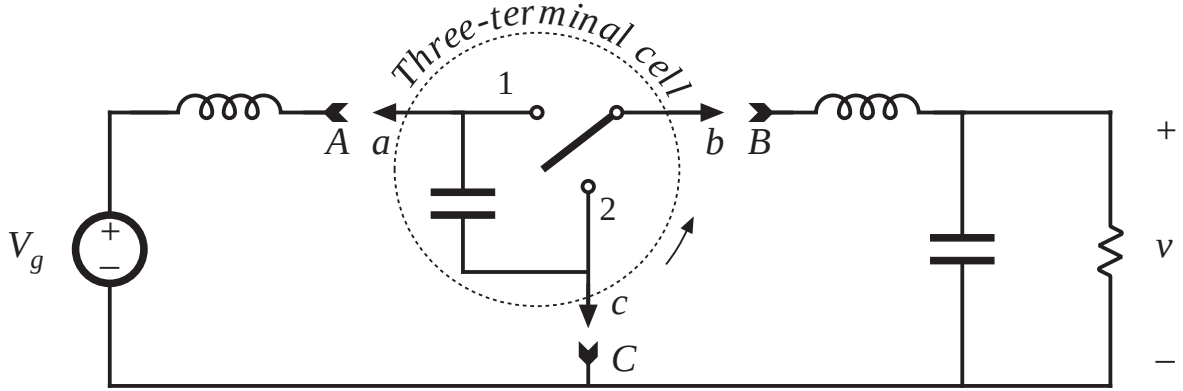


Three-terminal cell can be connected between source and load in three nontrivial distinct ways:

a-A b-B c-C	buck converter
a-C b-A c-B	boost converter
a-A b-C c-B	buck-boost converter

Rotation of a dual three-terminal network

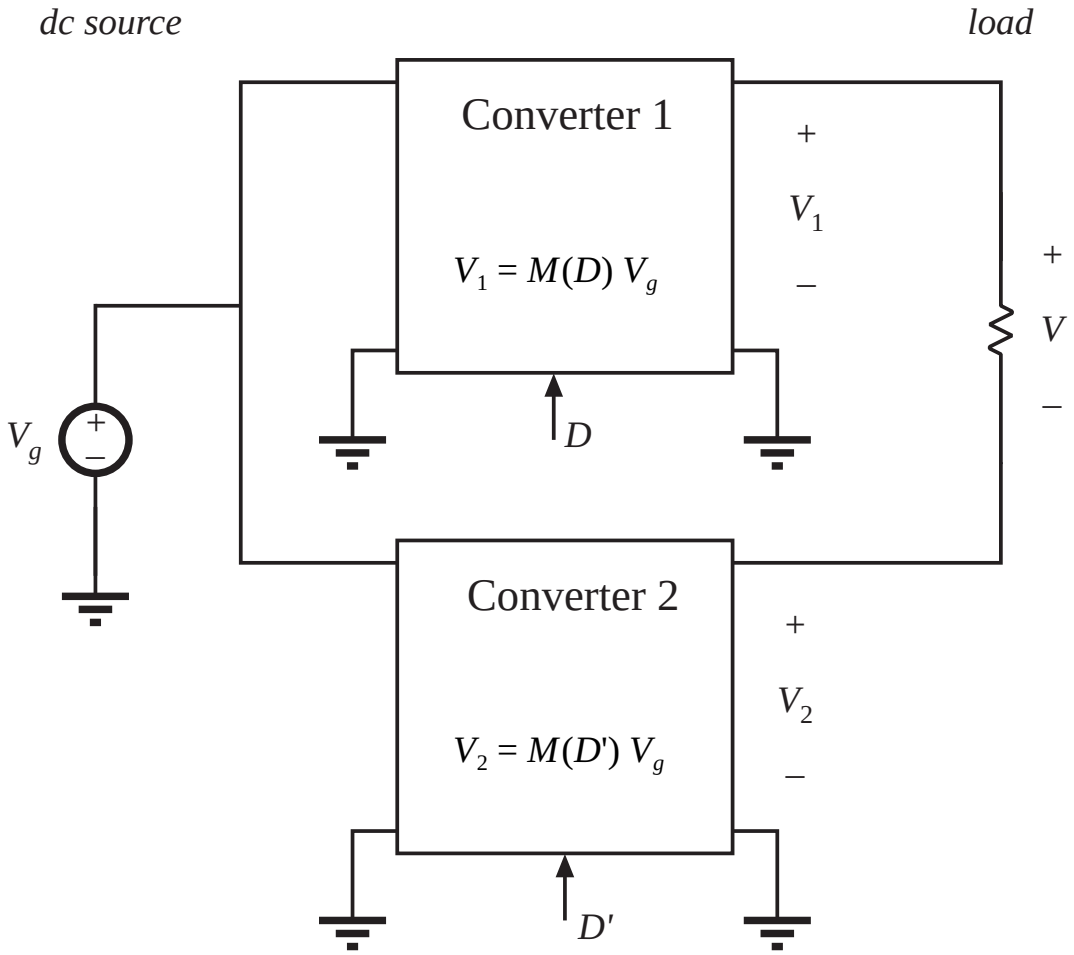
A capacitor and SPDT switch as a three-terminal cell:



Three-terminal cell can be connected between source and load in three nontrivial distinct ways:

a-A b-B c-C	buck converter with L-C input filter
a-C b-A c-B	boost converter with L-C output filter
a-A b-C c-B	Cuk converter

6.1.4. Differential connection of load to obtain bipolar output voltage

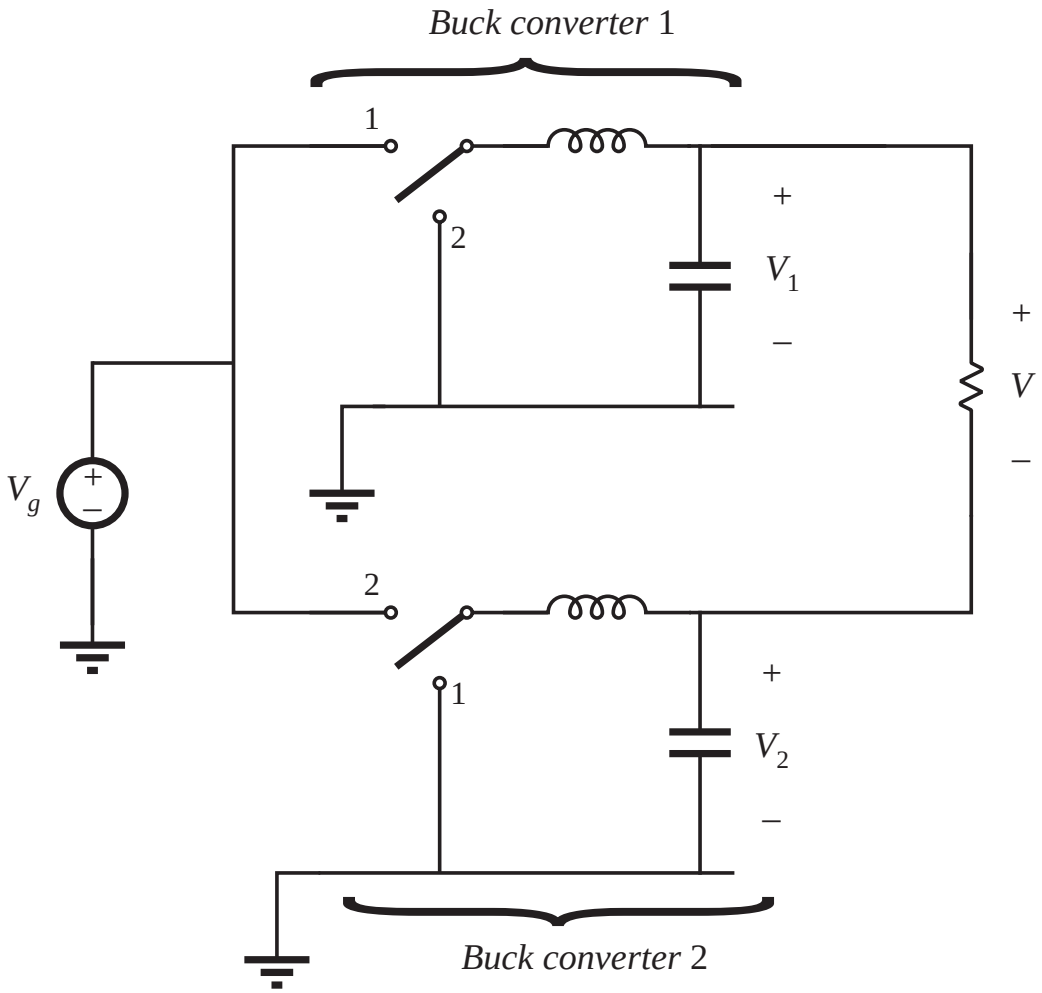


Differential load voltage is

$$V = V_1 - V_2$$

The outputs V_1 and V_2 may both be positive, but the differential output voltage V can be positive or negative.

Differential connection using two buck converters



Converter #1 transistor driven with duty cycle D

Converter #2 transistor driven with duty cycle complement D'

Differential load voltage is

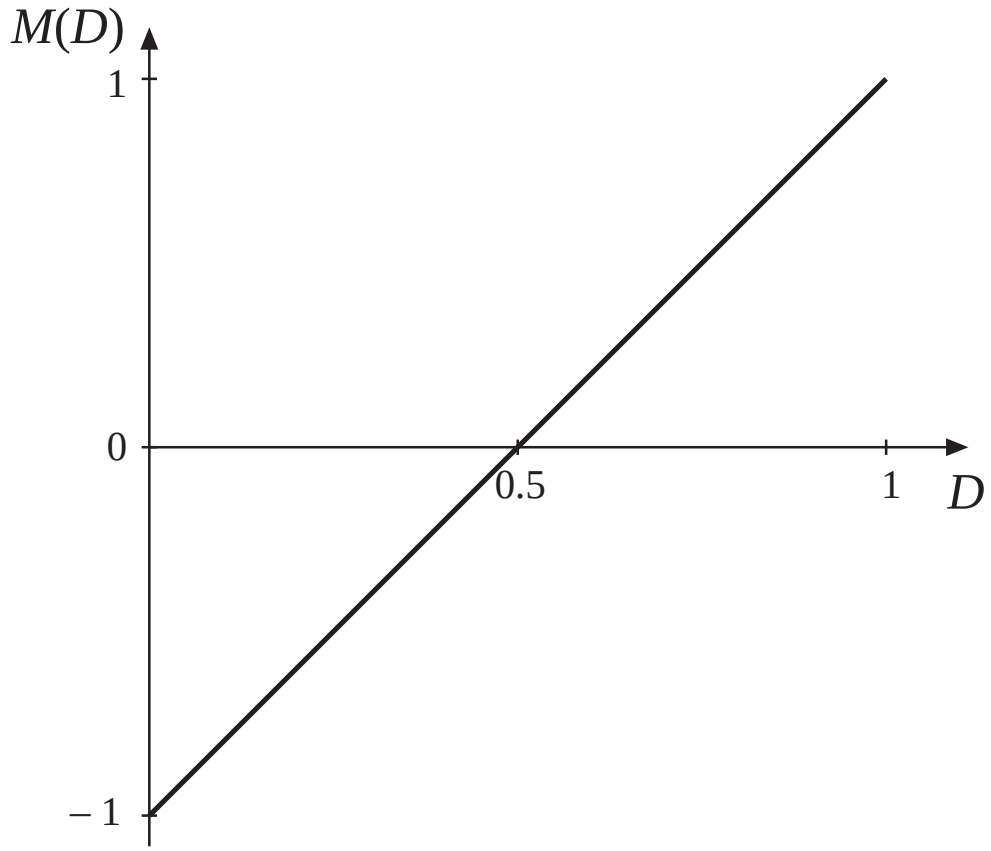
$$V = DV_g - D'V_g$$

Simplify:

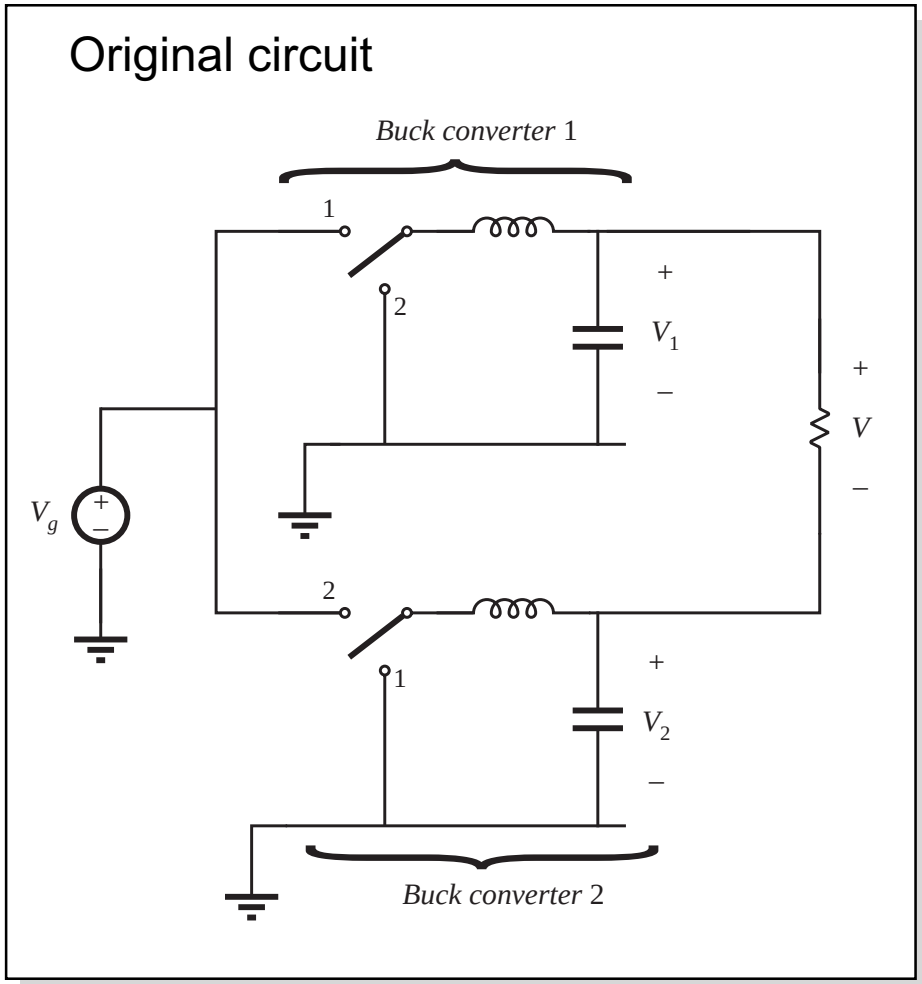
$$V = (2D - 1)V_g$$

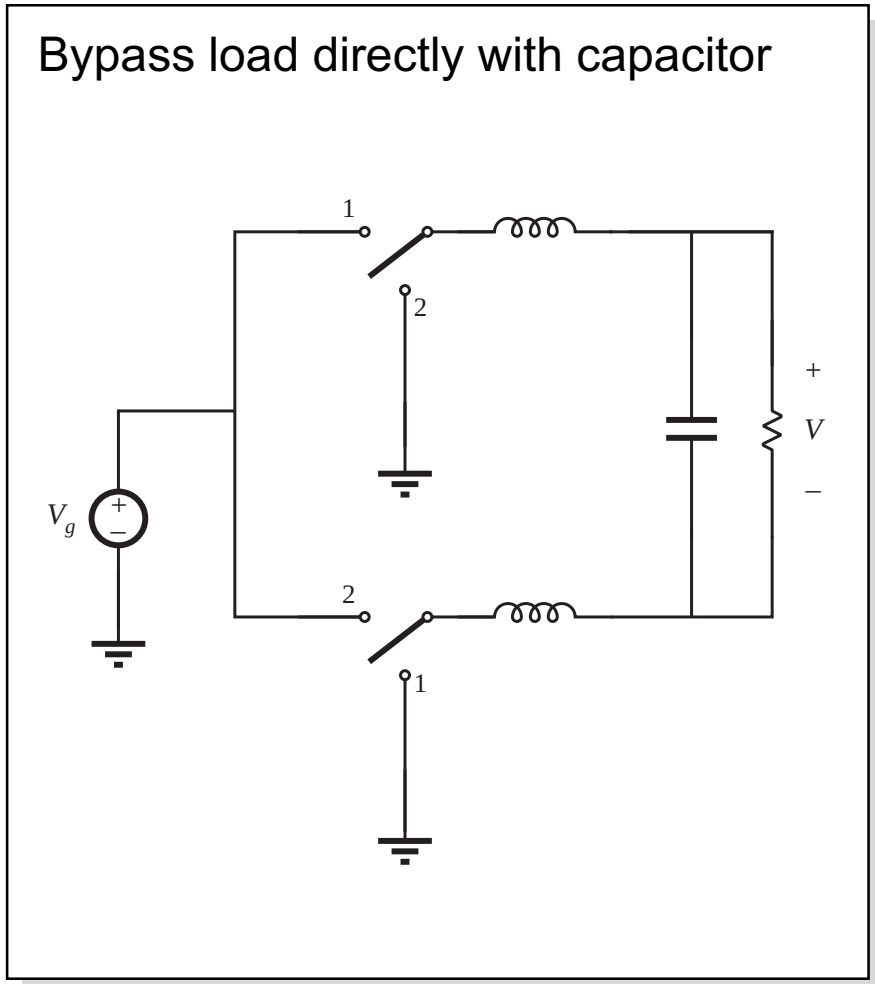
Conversion ratio $M(D)$, differentially-connected buck converters

$$V = (2D - 1)V_g$$



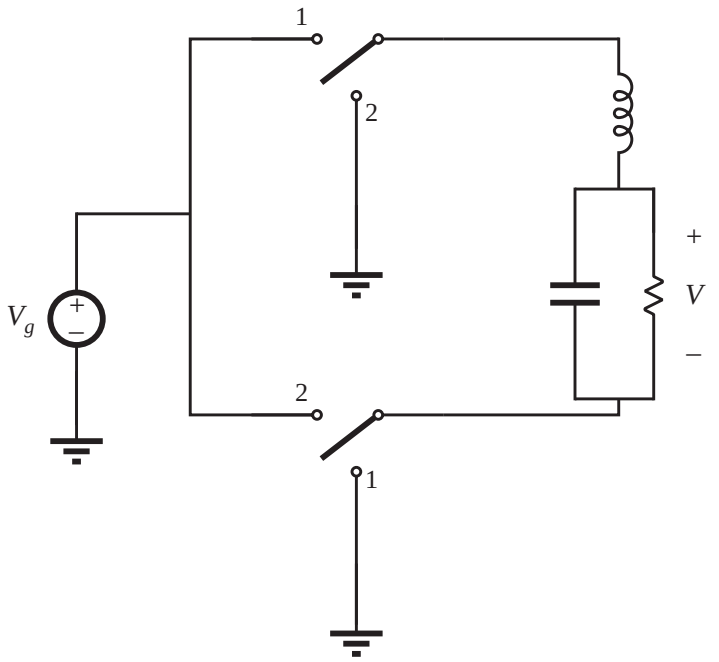
Simplification of filter circuit, differentially-connected buck converters



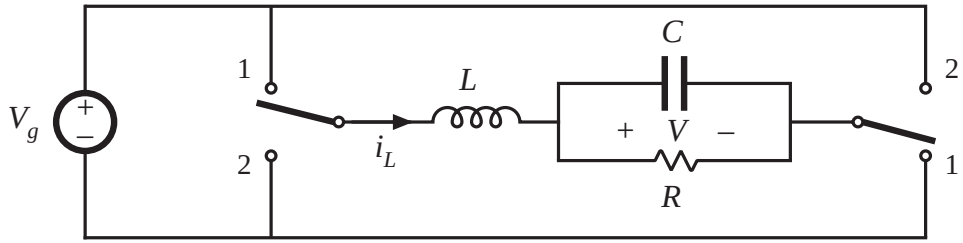


Simplification of filter circuit, differentially-connected buck converters

Combine series-connected inductors



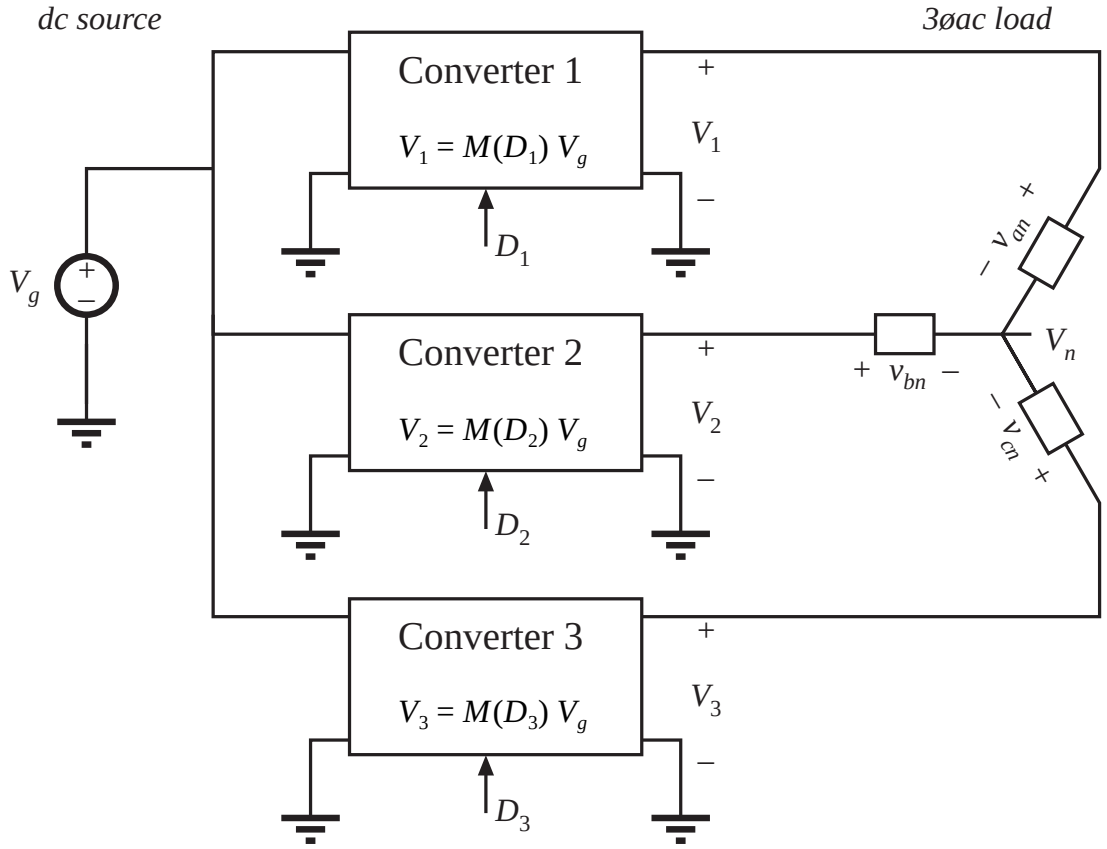
Re-draw for clarity



H-bridge, or bridge inverter

Commonly used in single-phase inverter applications and in servo amplifier applications

Differential connection to obtain 3ø inverter



With balanced 3ø load, neutral voltage is

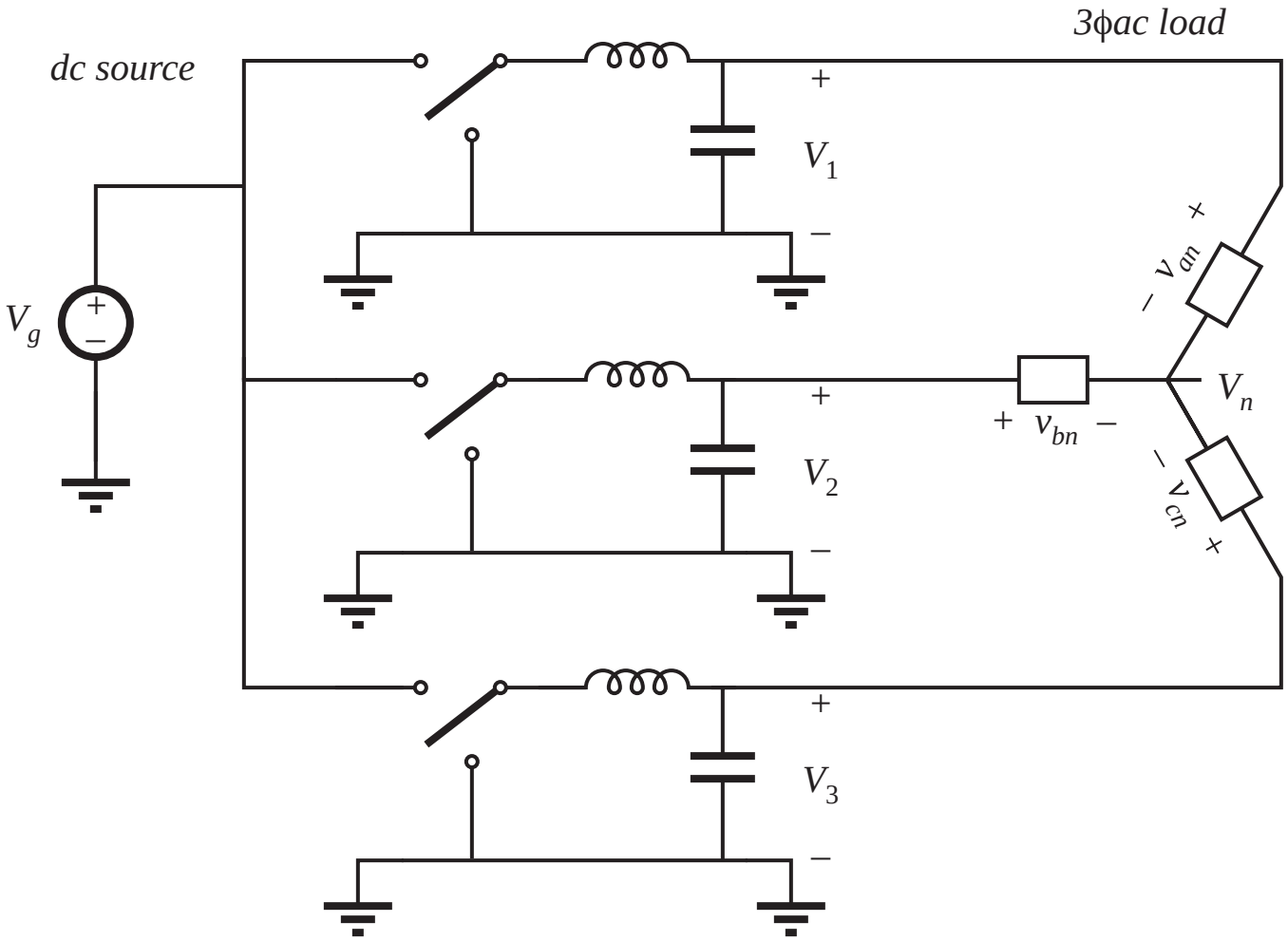
$$V_n = \frac{1}{3}\left(V_1 + V_2 + V_3\right)$$

Phase voltages are

$$V_{an} = V_1 - V_n$$
$$V_{bn} = V_2 - V_n$$
$$V_{cn} = V_3 - V_n$$

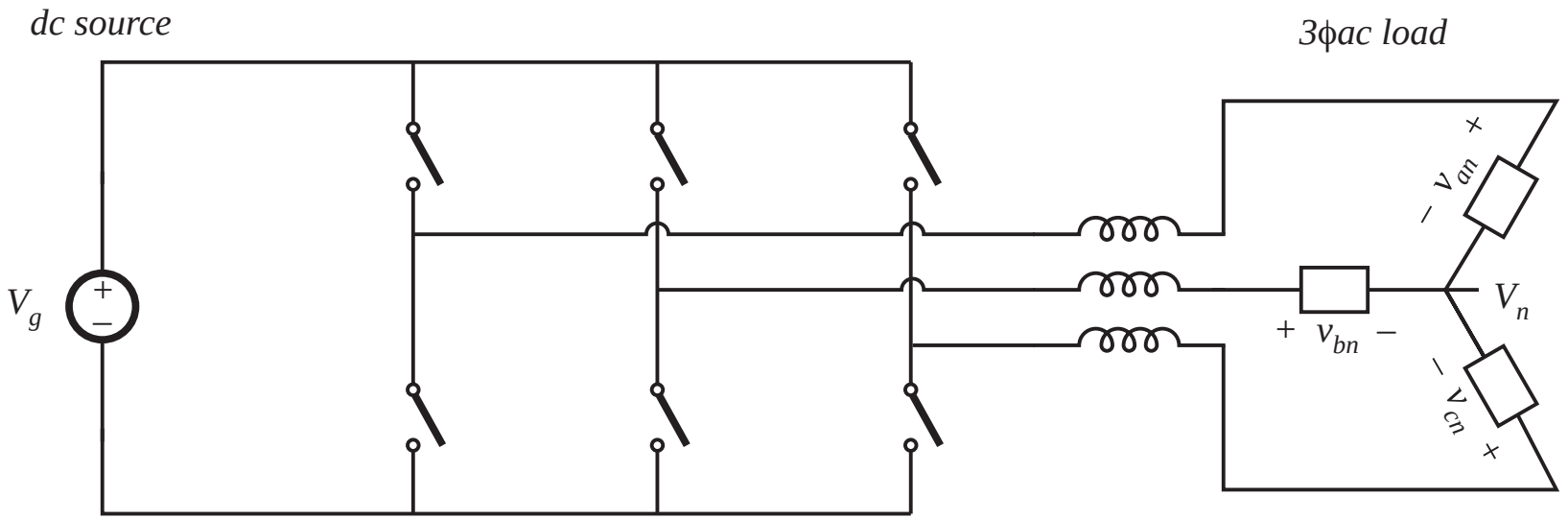
Control converters such that their output voltages contain the same dc biases. This dc bias will appear at the neutral point V_n. It then cancels out, so phase voltages contain no dc bias.

3ø differential connection of three buck converters



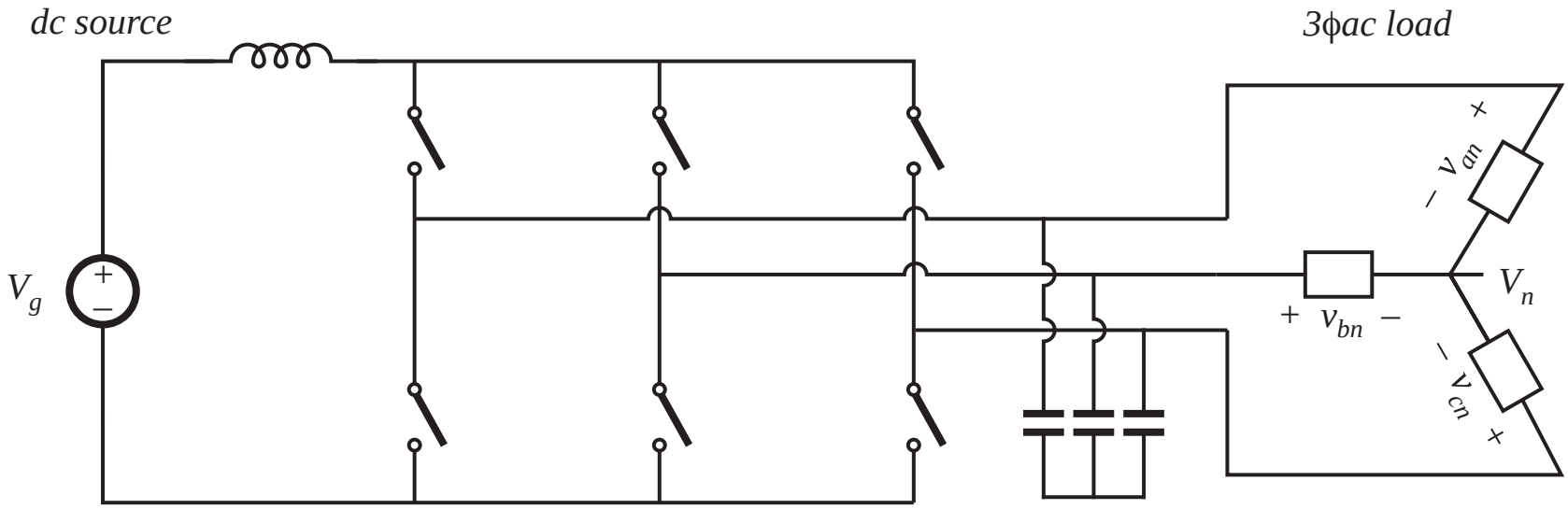
3ø differential connection of three buck converters

Re-draw for clarity:



"Voltage-source inverter" or buck-derived three-phase inverter

The 3ø current-source inverter



- Exhibits a boost-type conversion characteristic

6.2. A short list of converters

An infinite number of converters are possible, which contain switches embedded in a network of inductors and capacitors

Two simple classes of converters are listed here:

- Single-input single-output converters containing a single inductor. The switching period is divided into two subintervals. This class contains eight converters.
- Single-input single-output converters containing two inductors. The switching period is divided into two subintervals. Several of the more interesting members of this class are listed.

Single-input single-output converters containing one inductor

- Use switches to connect inductor between source and load, in one manner during first subinterval and in another during second subinterval
- There are a limited number of ways to do this, so all possible combinations can be found
- After elimination of degenerate and redundant cases, eight converters are found:

dc-dc converters

buck boost buck-boost noninverting buck-boost

dc-ac converters

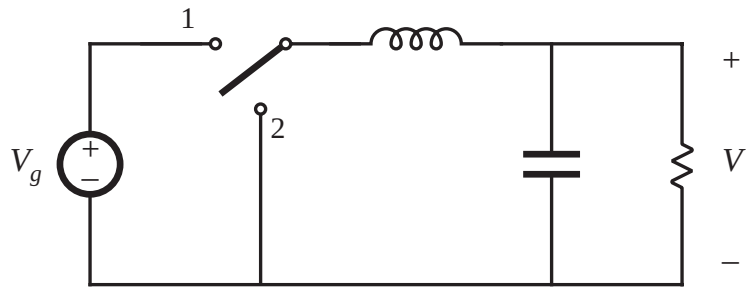
bridge Watkins-Johnson

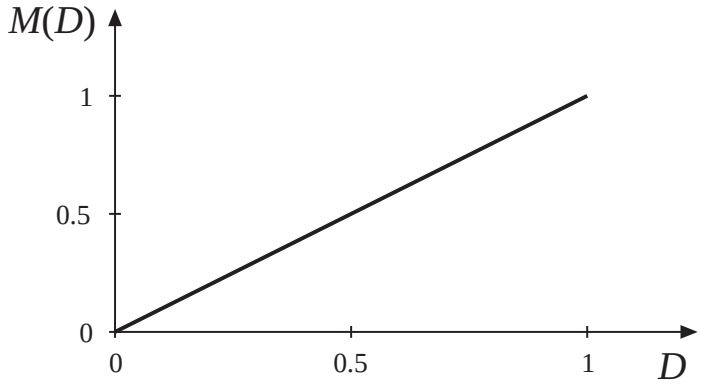
ac-dc converters

current-fed bridge inverse of Watkins-Johnson

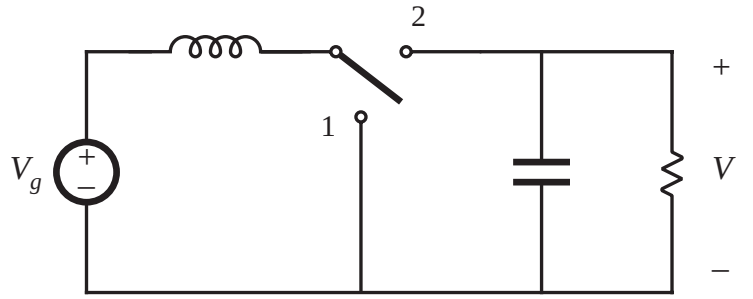
Converters producing a unipolar output voltage

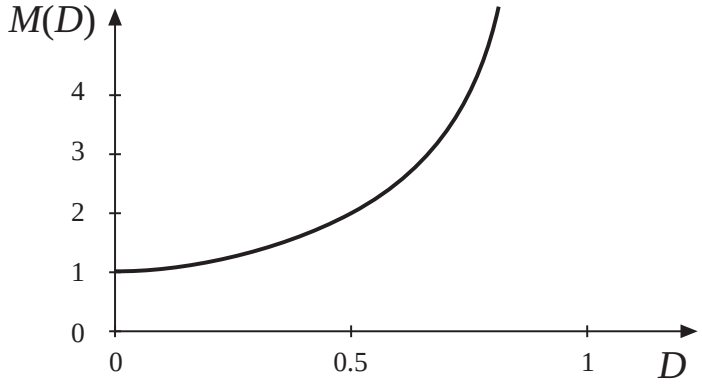
1. *Buck* $M(D) = D$





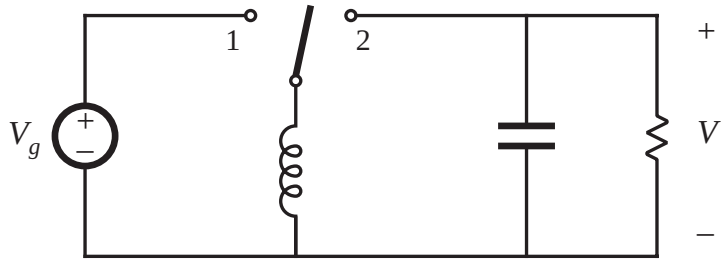
2. *Boost* $M(D) = \dfrac{1}{1 - D}$

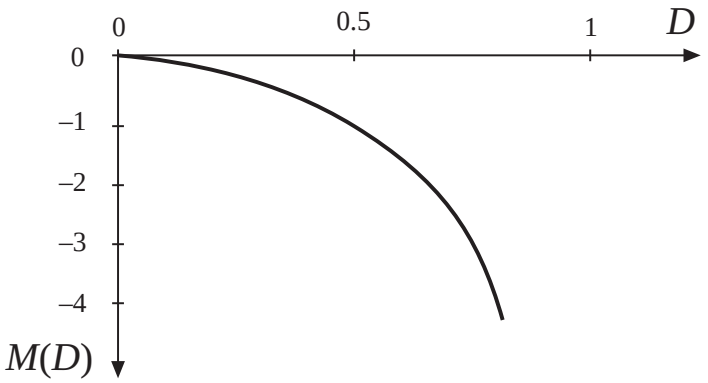




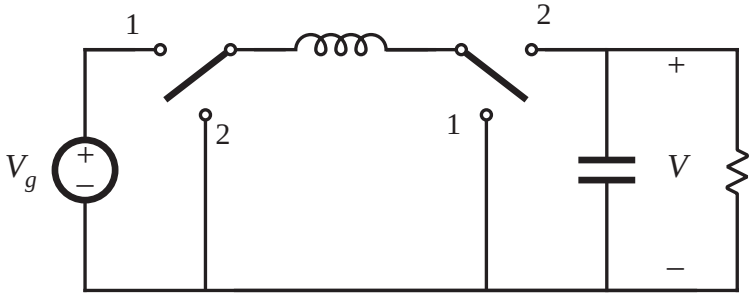
Converters producing a unipolar output voltage

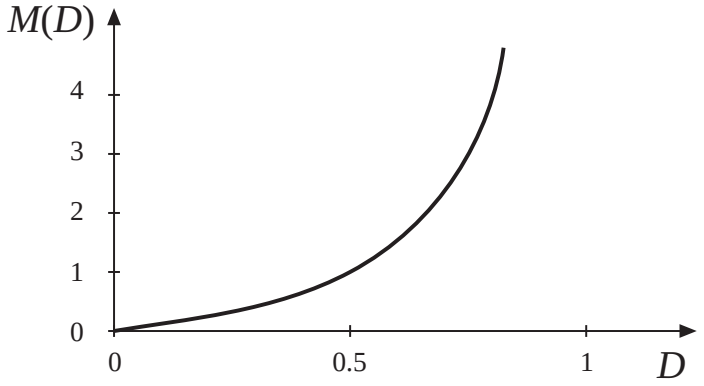
3. *Buck-boost* $M(D) = -\frac{D}{1-D}$





4. *Noninverting buck-boost* $M(D) = \frac{D}{1-D}$

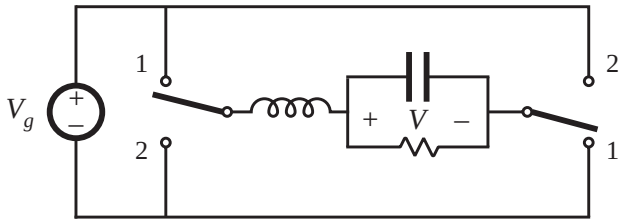


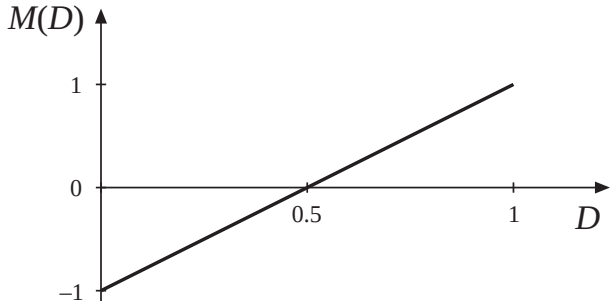


Converters producing a bipolar output voltage suitable as dc-ac inverters

5. *Bridge*

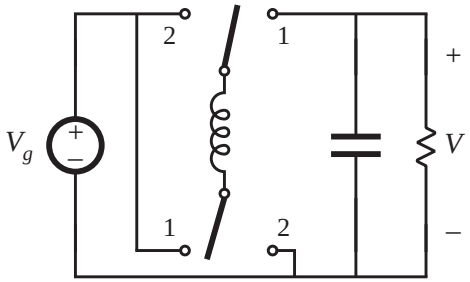
$M(D) = 2D - 1$



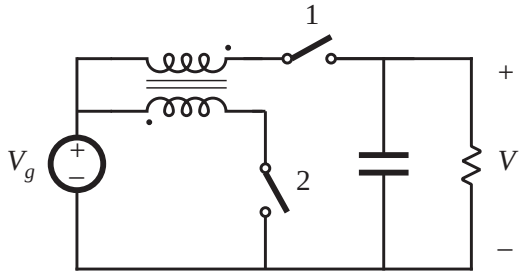


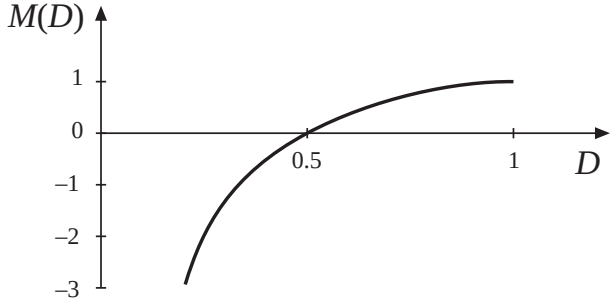
6. *Watkins-Johnson*

$M(D) = \dfrac{2D - 1}{D}$



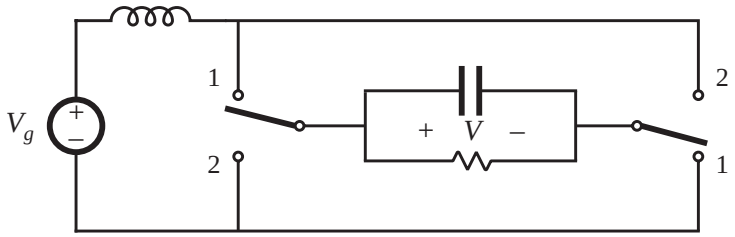
or

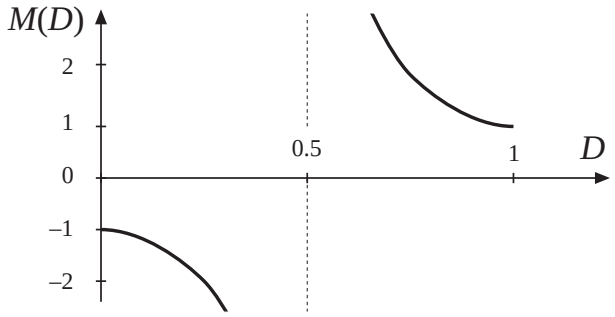




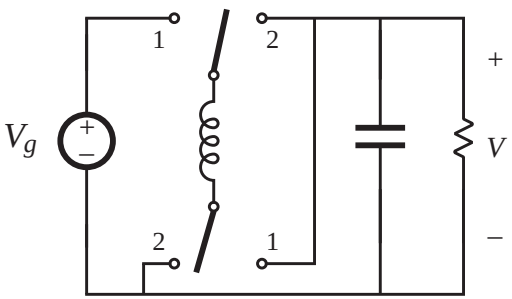
Converters producing a bipolar output voltage suitable as ac-dc rectifiers

7. *Current-fed bridge* $M(D) = \dfrac{1}{2D-1}$

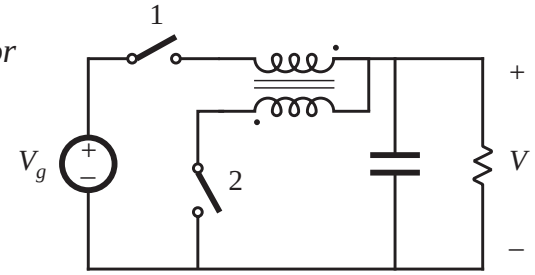


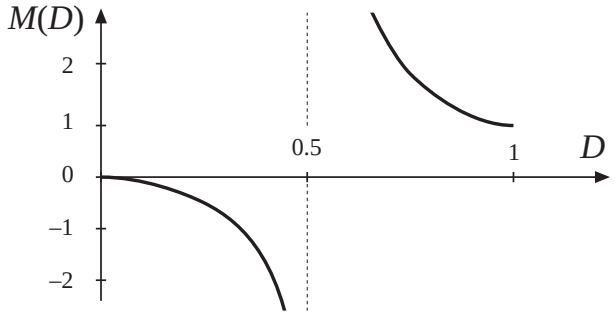


8. *Inverse of Watkins-Johnson* $M(D) = \dfrac{D}{2D-1}$



or

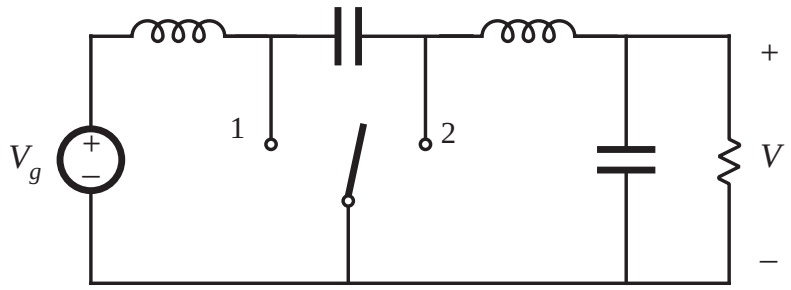


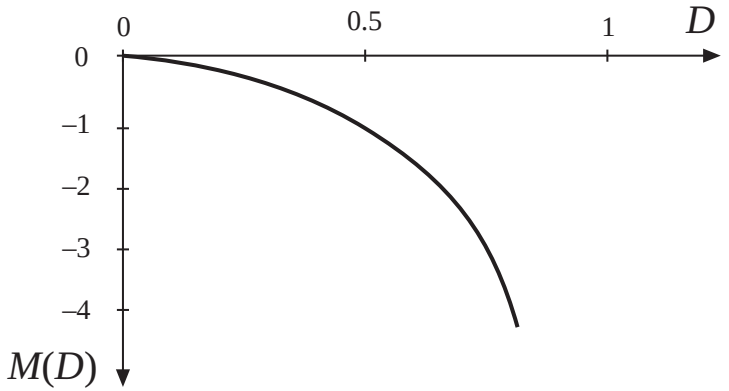


Several members of the class of two-inductor converters

1. *Ćuk*

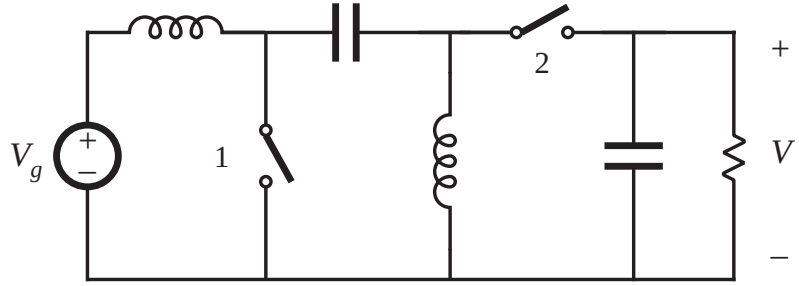
$$M(D) = -\frac{D}{1-D}$$

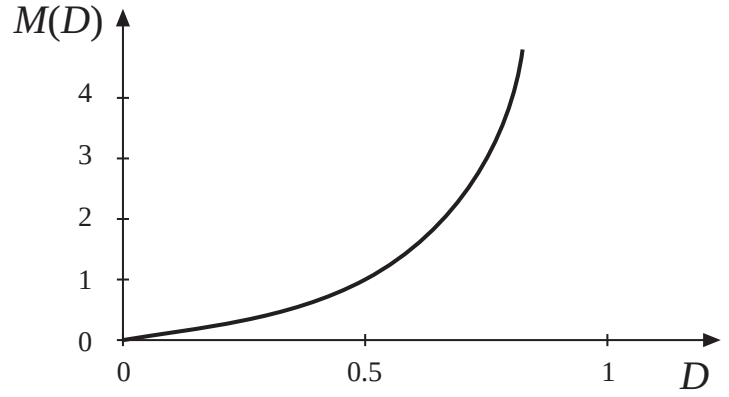




2. *SEPIC*

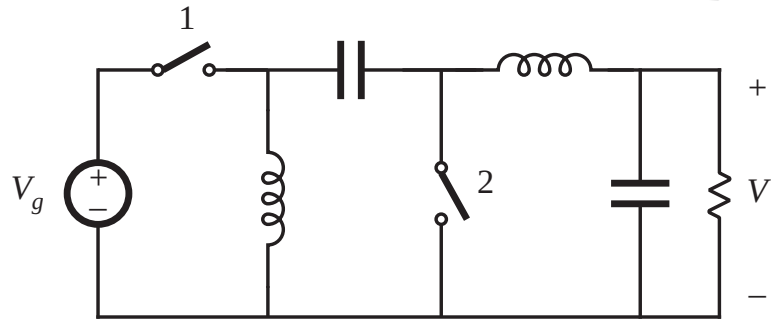
$$M(D) = \frac{D}{1-D}$$

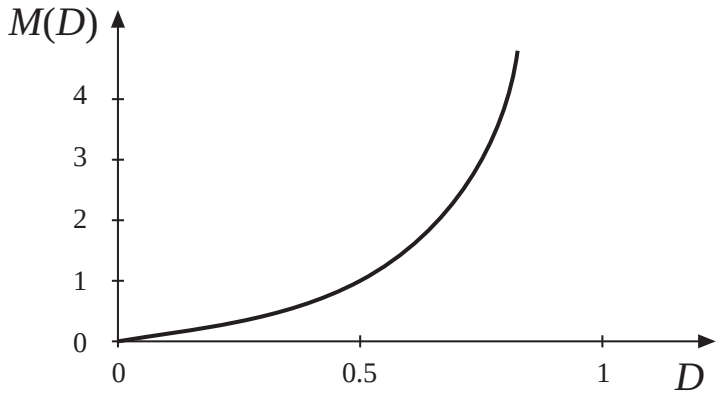




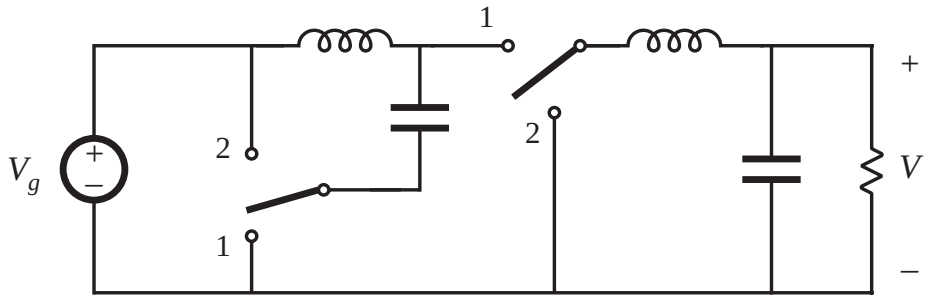
Several members of the class of two-inductor converters

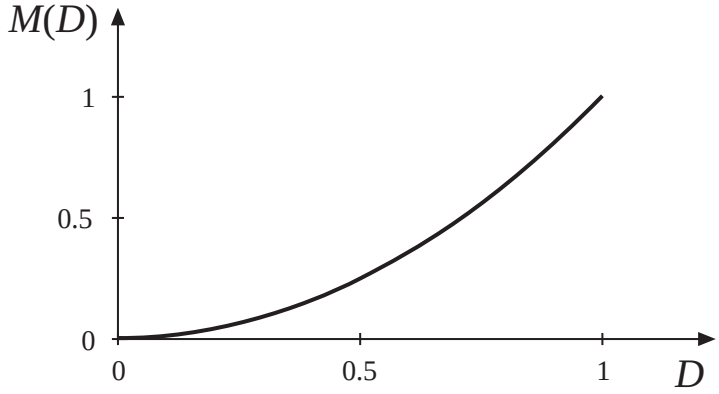
3. *Inverse of SEPIC* $M(D) = \dfrac{D}{1-D}$





4. *Buck* [2] $M(D) = D^2$





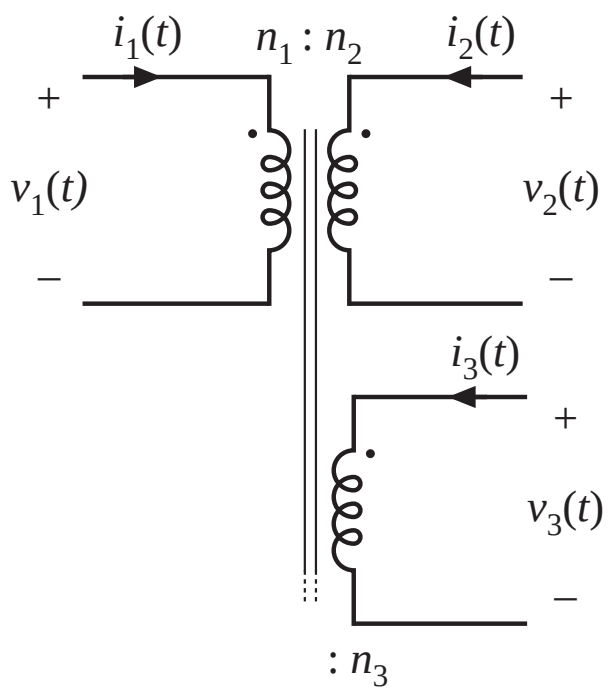
6.3. Transformer isolation

Objectives:

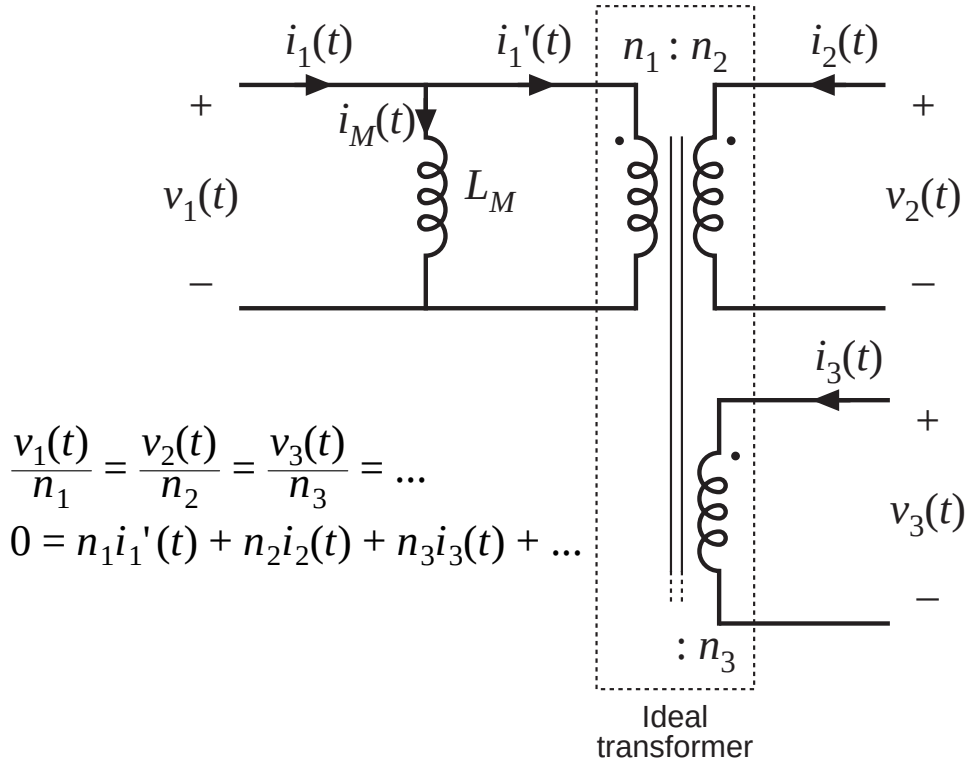
- Isolation of input and output ground connections, to meet safety requirements
- Reduction of transformer size by incorporating high frequency isolation transformer inside converter
- Minimization of current and voltage stresses when a large step-up or step-down conversion ratio is needed —use transformer turns ratio
- Obtain multiple output voltages via multiple transformer secondary windings and multiple converter secondary circuits

A simple transformer model

Multiple winding transformer



Equivalent circuit model

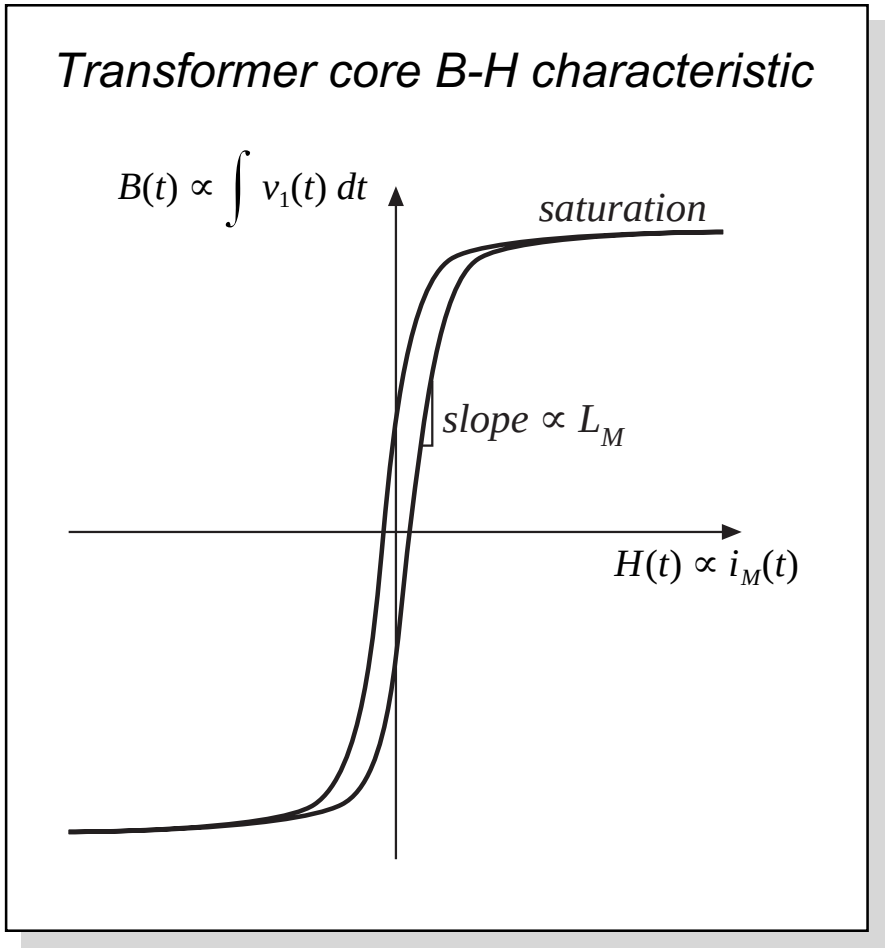


$$\frac{v_1(t)}{n_1} = \frac{v_2(t)}{n_2} = \frac{v_3(t)}{n_3} = \ldots$$

$$0 = n_1 i_1'(t) + n_2 i_2(t) + n_3 i_3(t) + \ldots$$

The magnetizing inductance L_M

- Models magnetization of transformer core material
- Appears effectively in parallel with windings
- If all secondary windings are disconnected, then primary winding behaves as an inductor, equal to the magnetizing inductance
- At dc: magnetizing inductance tends to short-circuit. Transformers cannot pass dc voltages
- Transformer saturates when magnetizing current i_M is too large



Volt-second balance in L_M

The magnetizing inductance is a real inductor, obeying

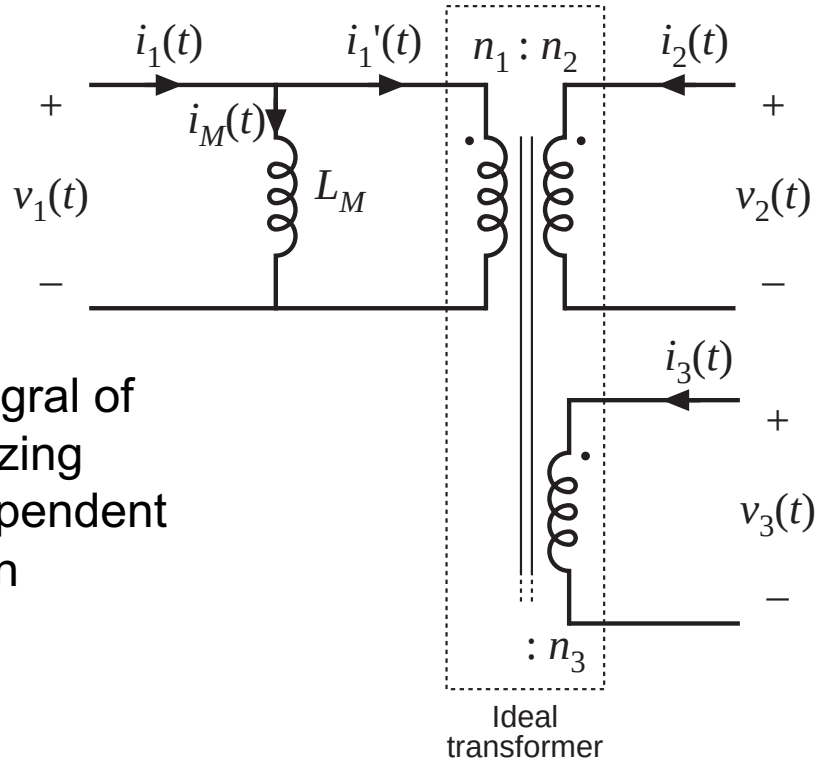
$$v_1(t) = L_M \frac{d i_M(t)}{dt}$$

integrate:

$$i_M(t) - i_M(0) = \frac{1}{L_M} \int_0^t v_1(\tau) d\tau$$

Magnetizing current is determined by integral of the applied winding voltage. The magnetizing current and the winding currents are independent quantities. Volt-second balance applies: in steady-state, $i_M(T_s) = i_M(0)$, and hence

$$0 = \frac{1}{T_s} \int_0^{T_s} v_1(t) dt$$

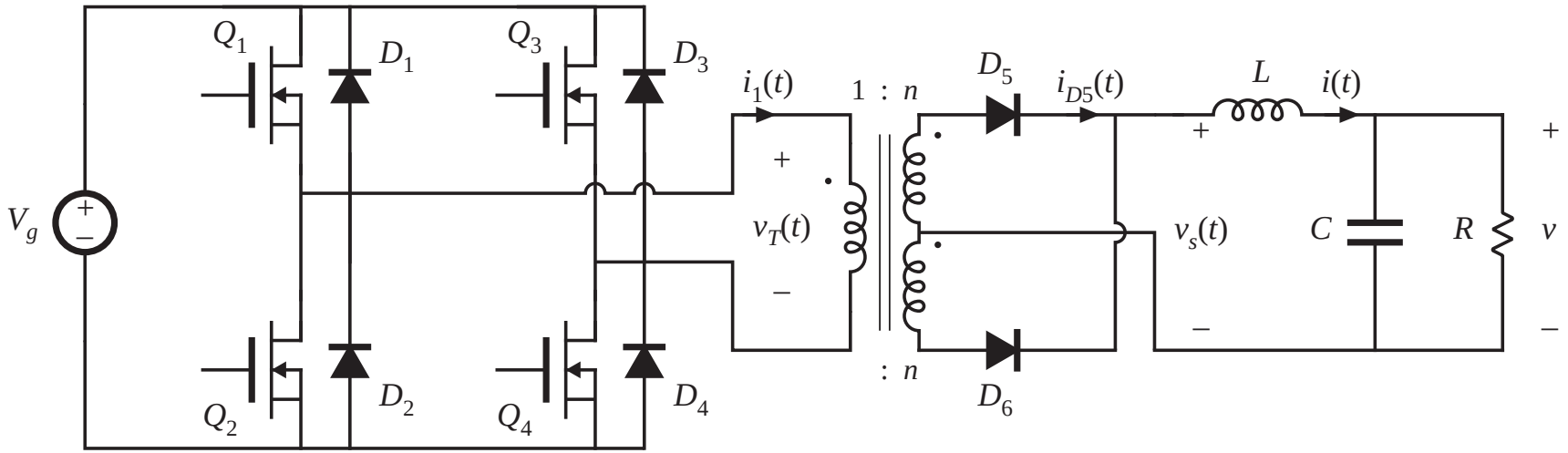


Transformer reset

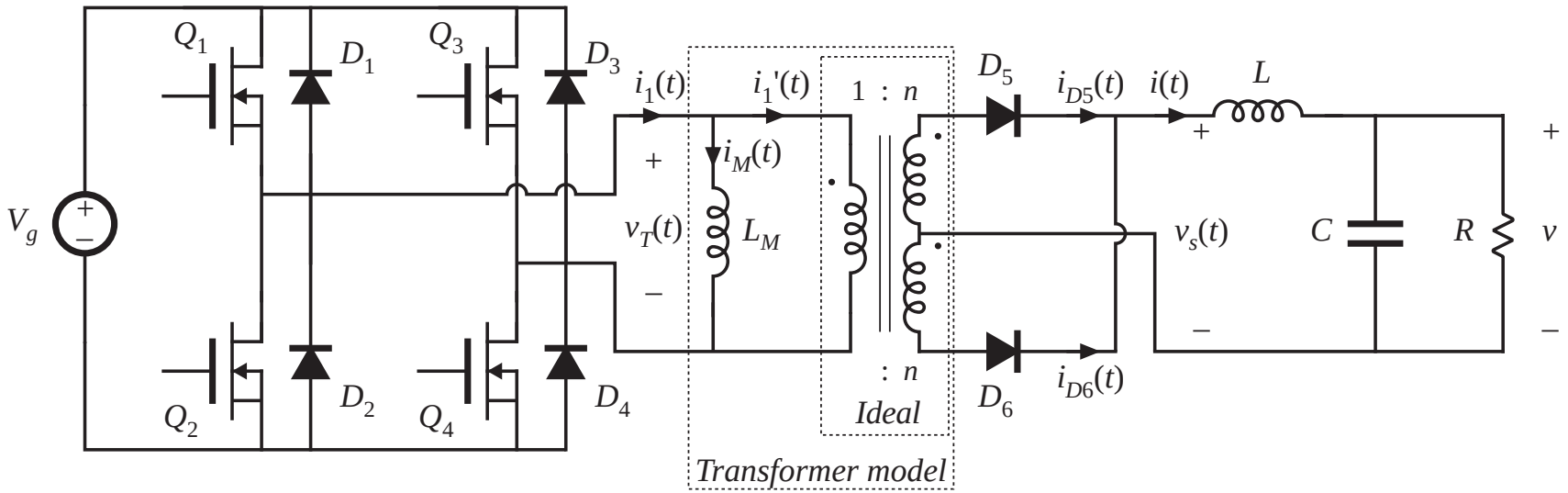
- "Transformer reset" is the mechanism by which magnetizing inductance volt-second balance is obtained
- The need to reset the transformer volt-seconds to zero by the end of each switching period adds considerable complexity to converters
- To understand operation of transformer-isolated converters:
  - replace transformer by equivalent circuit model containing magnetizing inductance
  - analyze converter as usual, treating magnetizing inductance as any other inductor
  - apply volt-second balance to all converter inductors, including magnetizing inductance

6.3.1. Full-bridge and half-bridge isolated buck converters

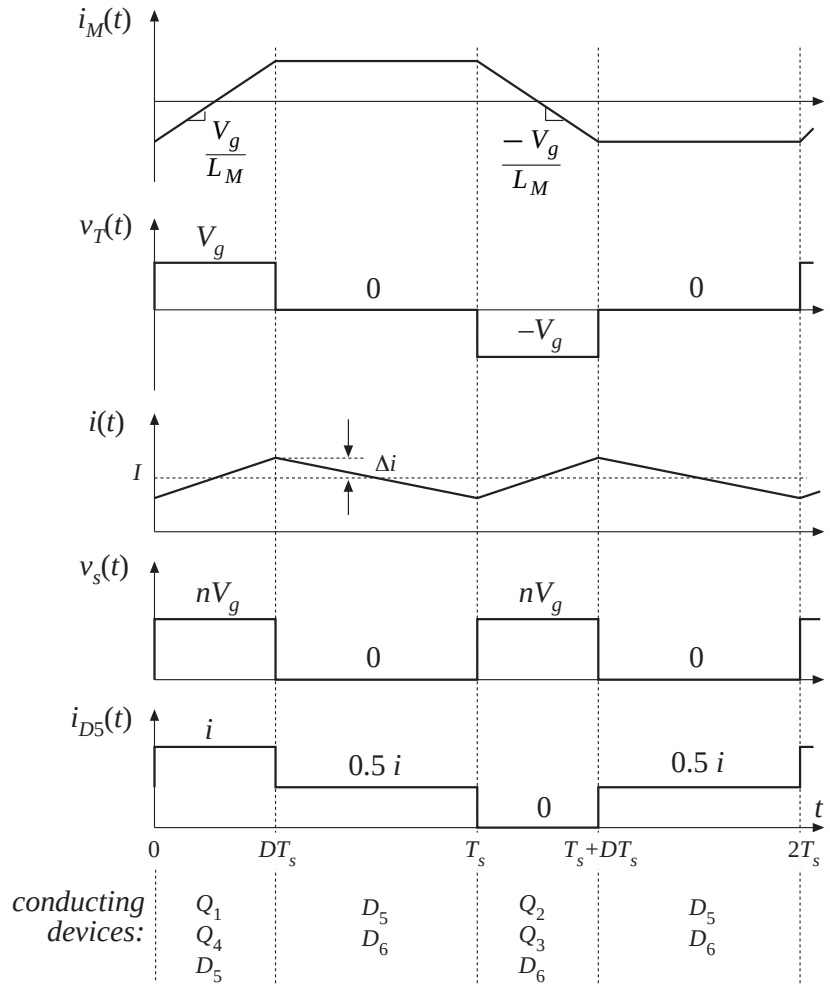
Full-bridge isolated buck converter



Full-bridge, with transformer equivalent circuit



Full-bridge: waveforms



- During first switching period: transistors Q_1 and Q_4 conduct for time DT_s , applying volt-seconds $V_g\,DT_s$ to primary winding
- During next switching period: transistors Q_2 and Q_3 conduct for time DT_s , applying volt-seconds $-V_g\,DT_s$ to primary winding
- Transformer volt-second balance is obtained over two switching periods
- Effect of nonidealities?

Effect of nonidealities on transformer volt-second balance

Volt-seconds applied to primary winding during first switching period:

$$(V_g - (Q_1 \text{ and } Q_4 \text{ forward voltage drops}))(Q_1 \text{ and } Q_4 \text{ conduction time})$$

Volt-seconds applied to primary winding during next switching period:

$$-(V_g - (Q_2 \text{ and } Q_3 \text{ forward voltage drops}))(Q_2 \text{ and } Q_3 \text{ conduction time})$$

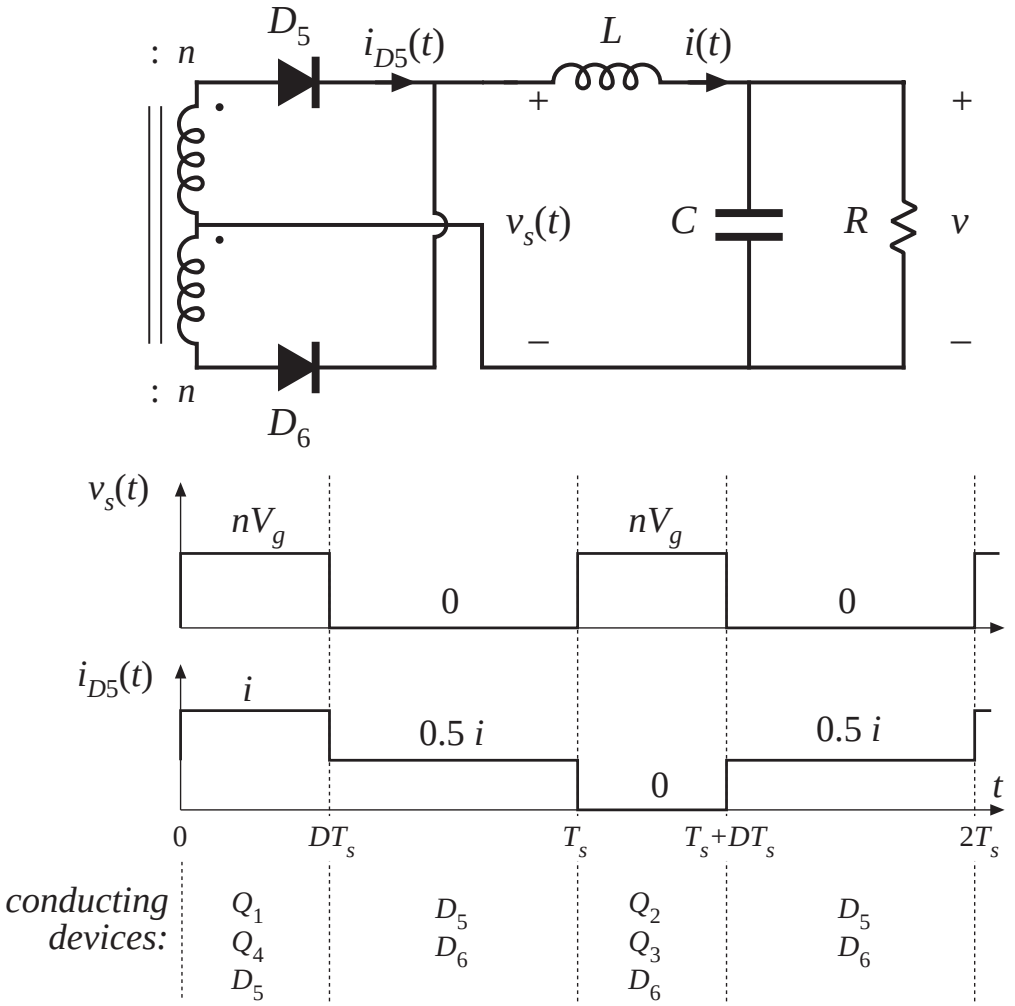
These volt-seconds never add to *exactly* zero.

Net volt-seconds are applied to primary winding

Magnetizing current slowly increases in magnitude

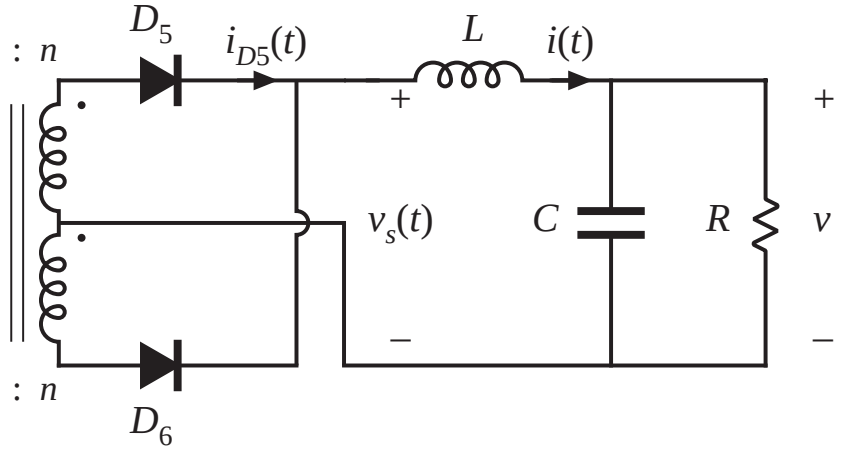
Saturation can be prevented by placing a capacitor in series with primary, or by use of current programmed mode (Chapter 12)

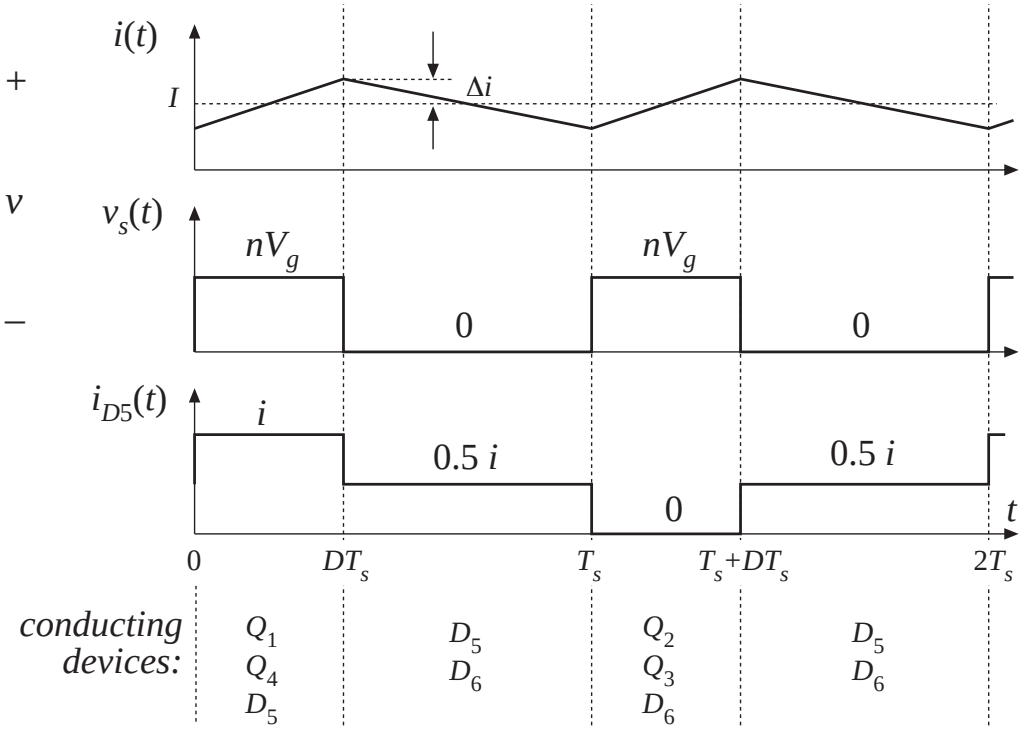
Operation of secondary-side diodes



- During second (D') subinterval, both secondary-side diodes conduct
- Output filter inductor current divides approximately equally between diodes
- Secondary amp-turns add to approximately zero
- Essentially no net magnetization of transformer core by secondary winding currents

Volt-second balance on output filter inductor



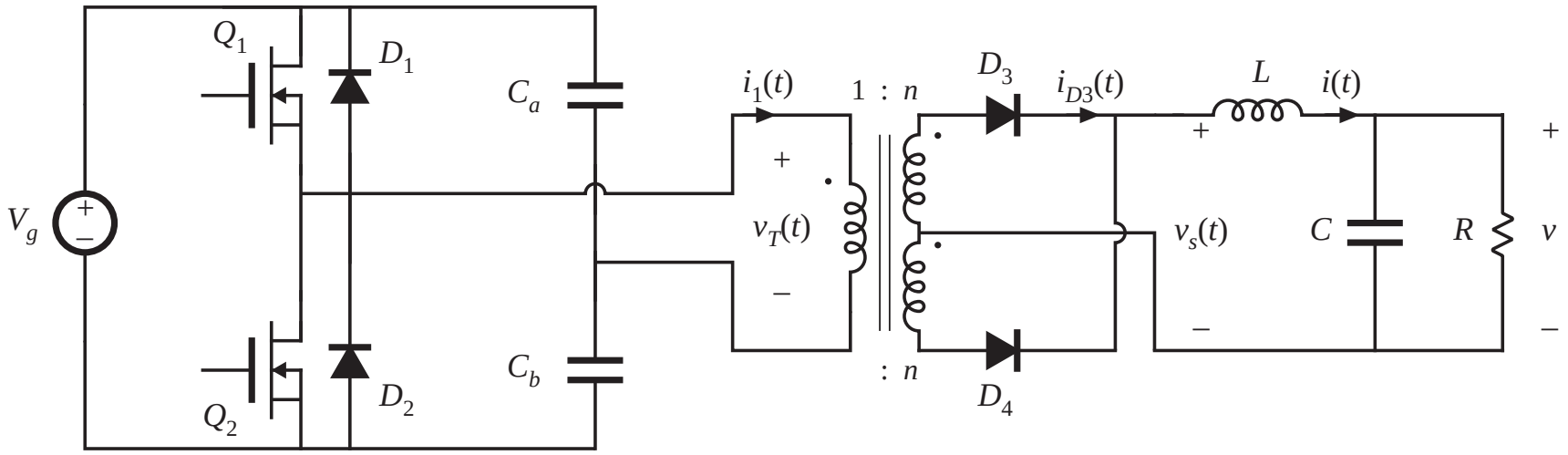


$$V = \langle v_s \rangle$$

$$V = nDV_g$$

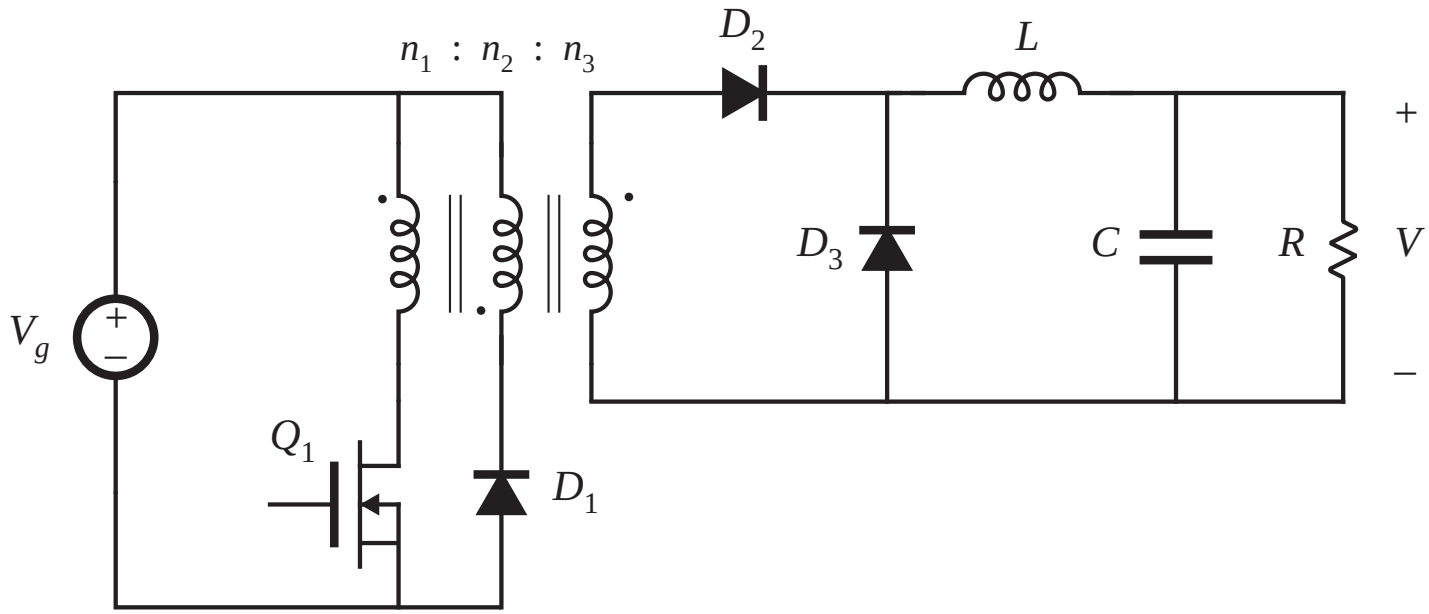
$$M(D) = nD$$ buck converter with turns ratio

Half-bridge isolated buck converter



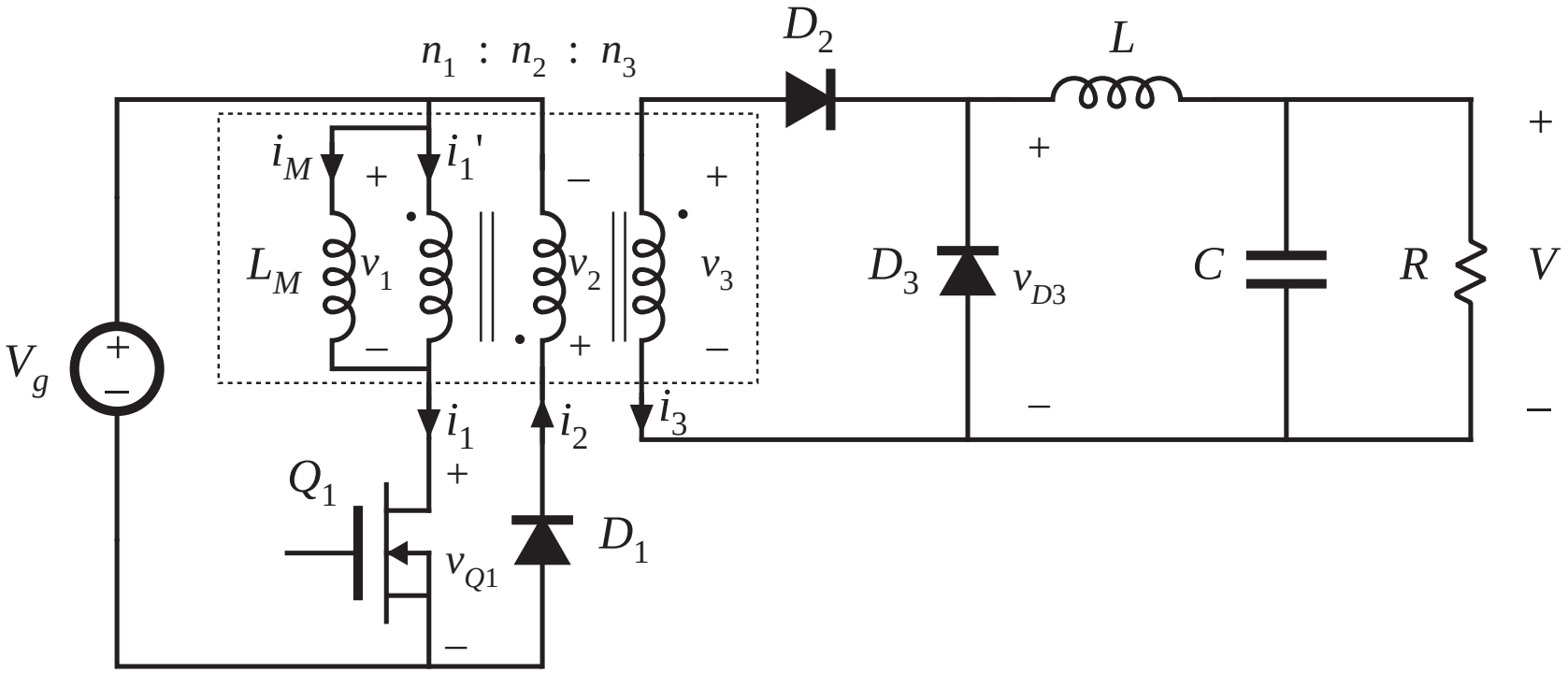
- Replace transistors Q_3 and Q_4 with large capacitors
- Voltage at capacitor centerpoint is $0.5 V_g$
- $v_s(t)$ is reduced by a factor of two
- $M = 0.5\ nD$

6.3.2. Forward converter

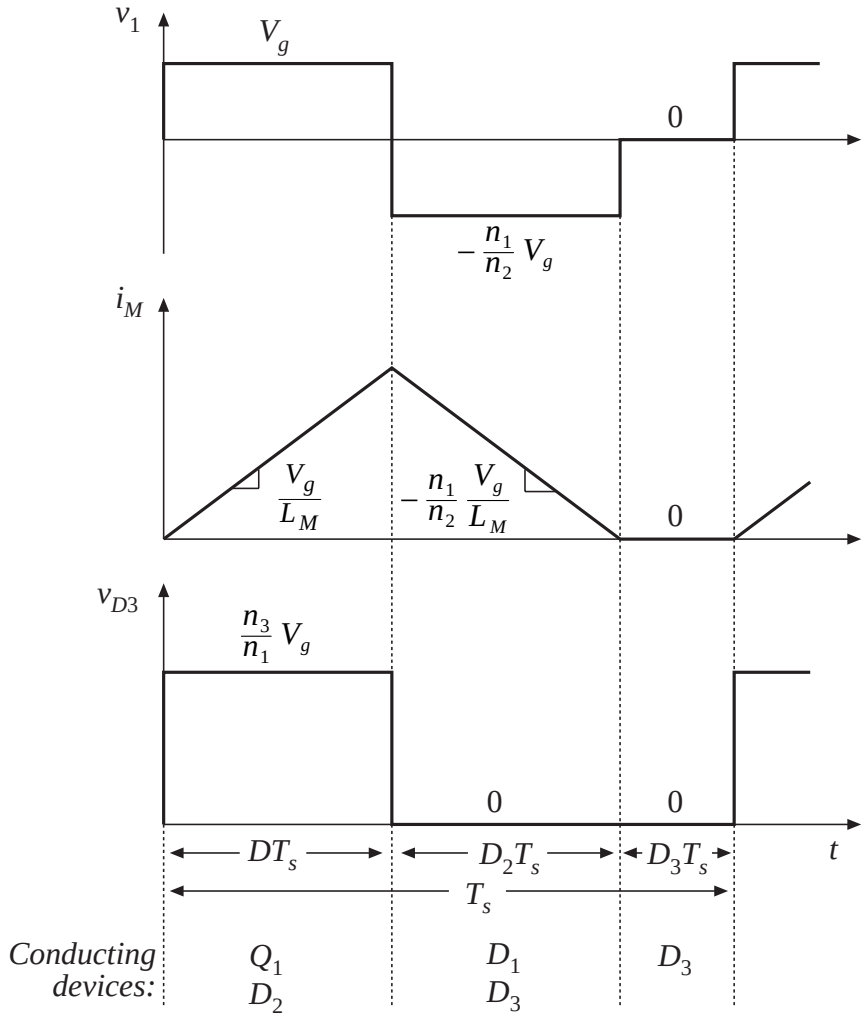


- Buck-derived transformer-isolated converter
- Single-transistor and two-transistor versions
- Maximum duty cycle is limited
- Transformer is reset while transistor is off

Forward converter with transformer equivalent circuit

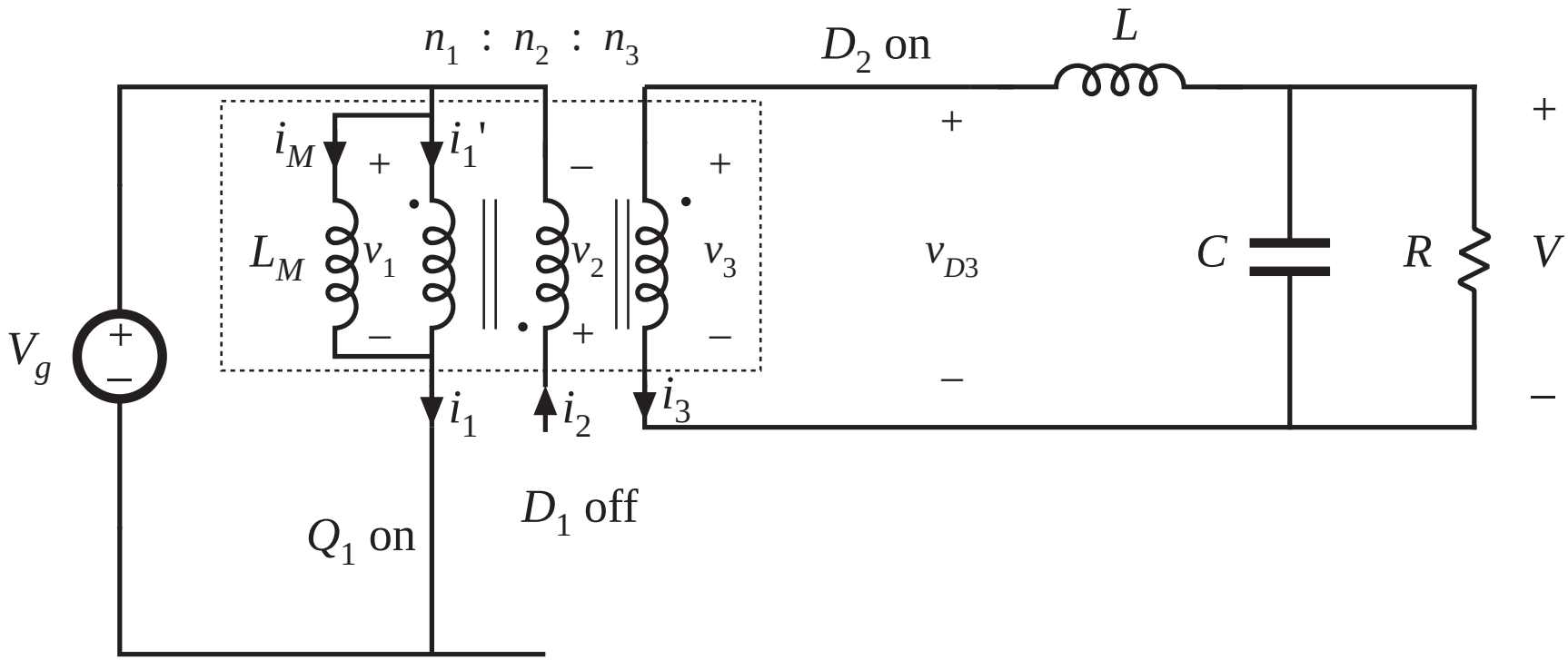


Forward converter: waveforms

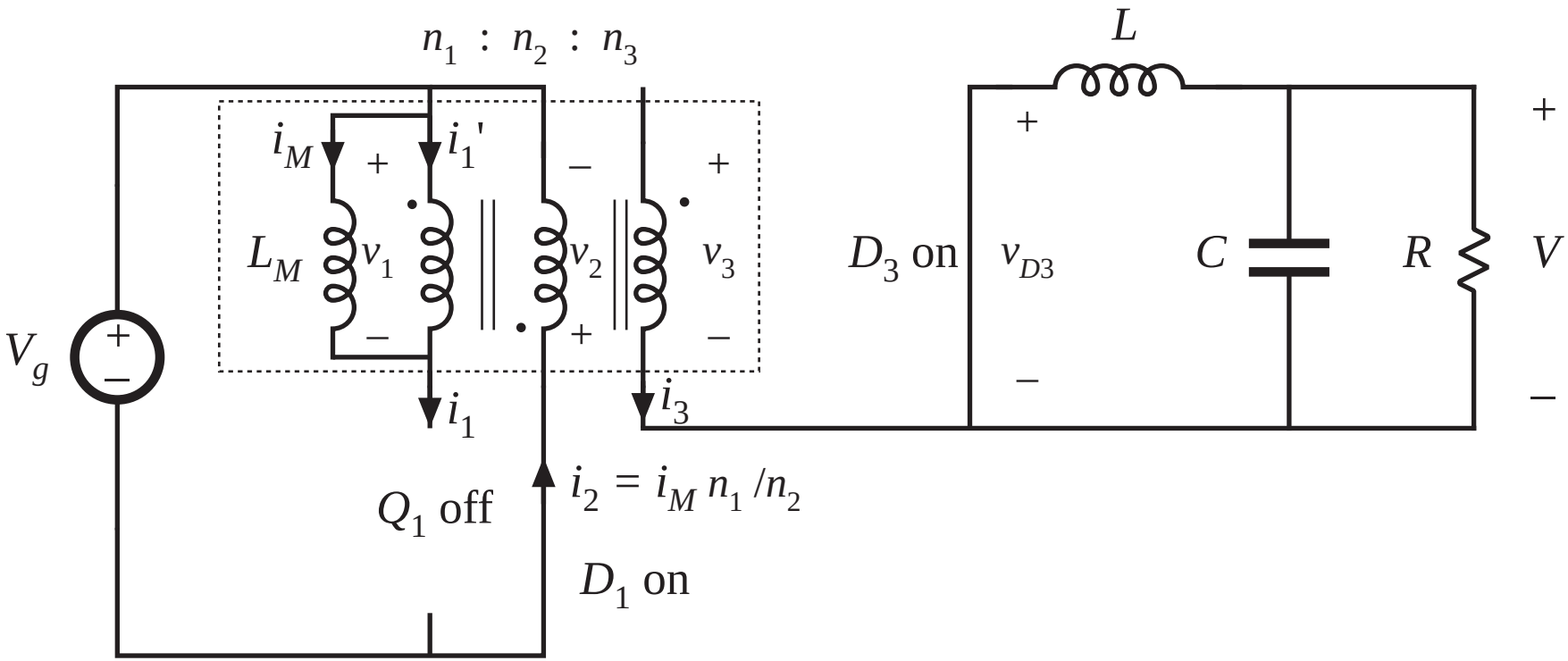


- Magnetizing current, in conjunction with diode D_1, operates in discontinuous conduction mode
- Output filter inductor, in conjunction with diode D_3, may operate in either CCM or DCM

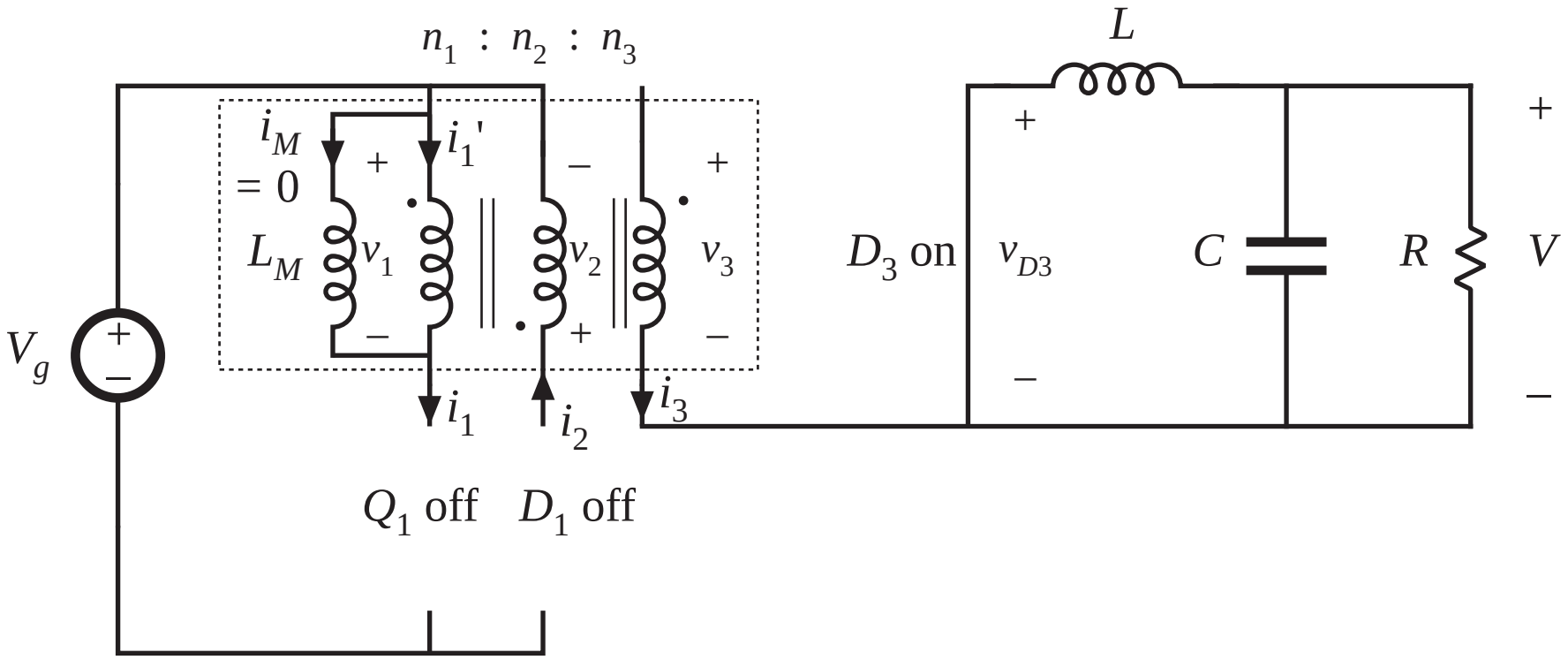
Subinterval 1: transistor conducts



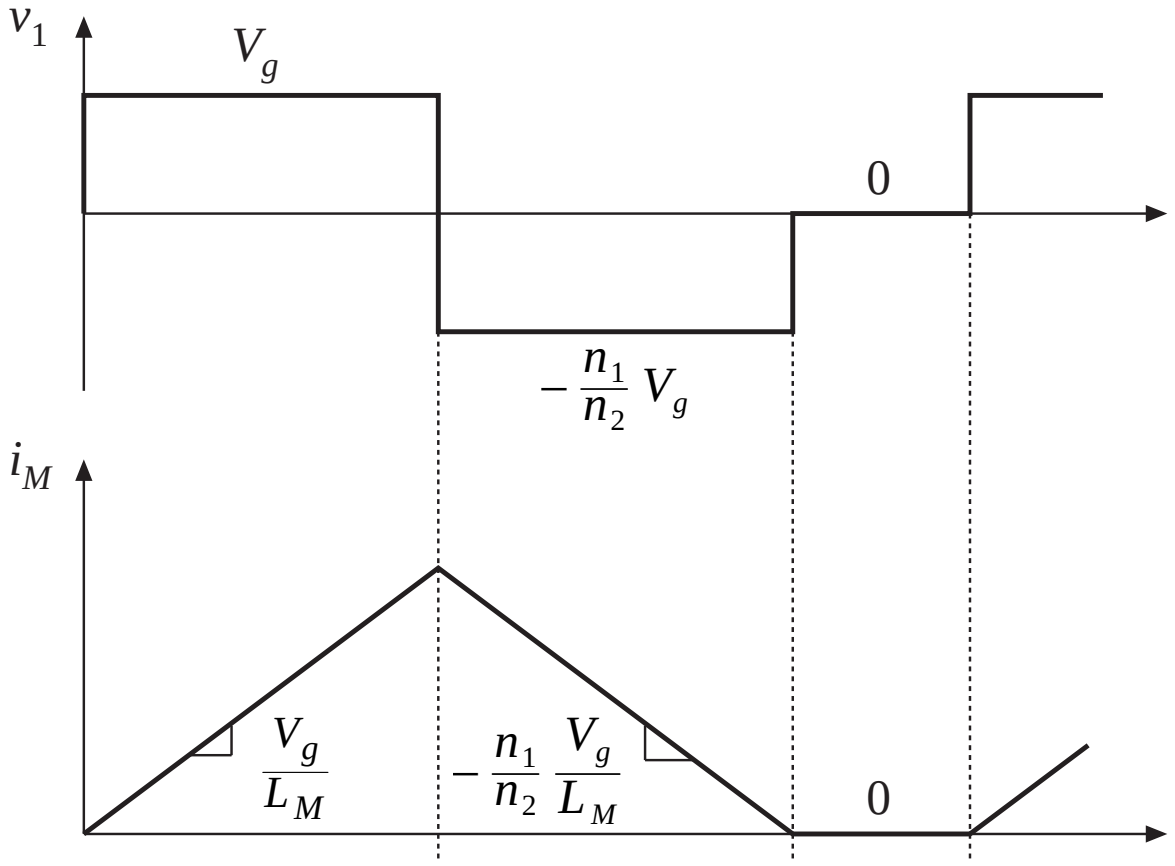
Subinterval 2: transformer reset



Subinterval 3



Magnetizing inductance volt-second balance



$$\langle v_1 \rangle = D\left(V_g\right) + D_2\left(-V_g n_1/n_2\right) + D_3\left(0\right) = 0$$

Transformer reset

From magnetizing current volt-second balance:

$$\langle v_1 \rangle = D\left(V_g\right) + D_2\left(-V_g n_1/n_2\right) + D_3\left(0\right) = 0$$

Solve for D_2:

$$D_2 = \frac{n_2}{n_1} D$$

D_3 cannot be negative. But $D_3 = 1 - D - D_2$. Hence

$$D_3 = 1 - D - D_2 \geq 0$$

$$D_3 = 1 - D\left(1 + \frac{n_2}{n_1}\right) \geq 0$$

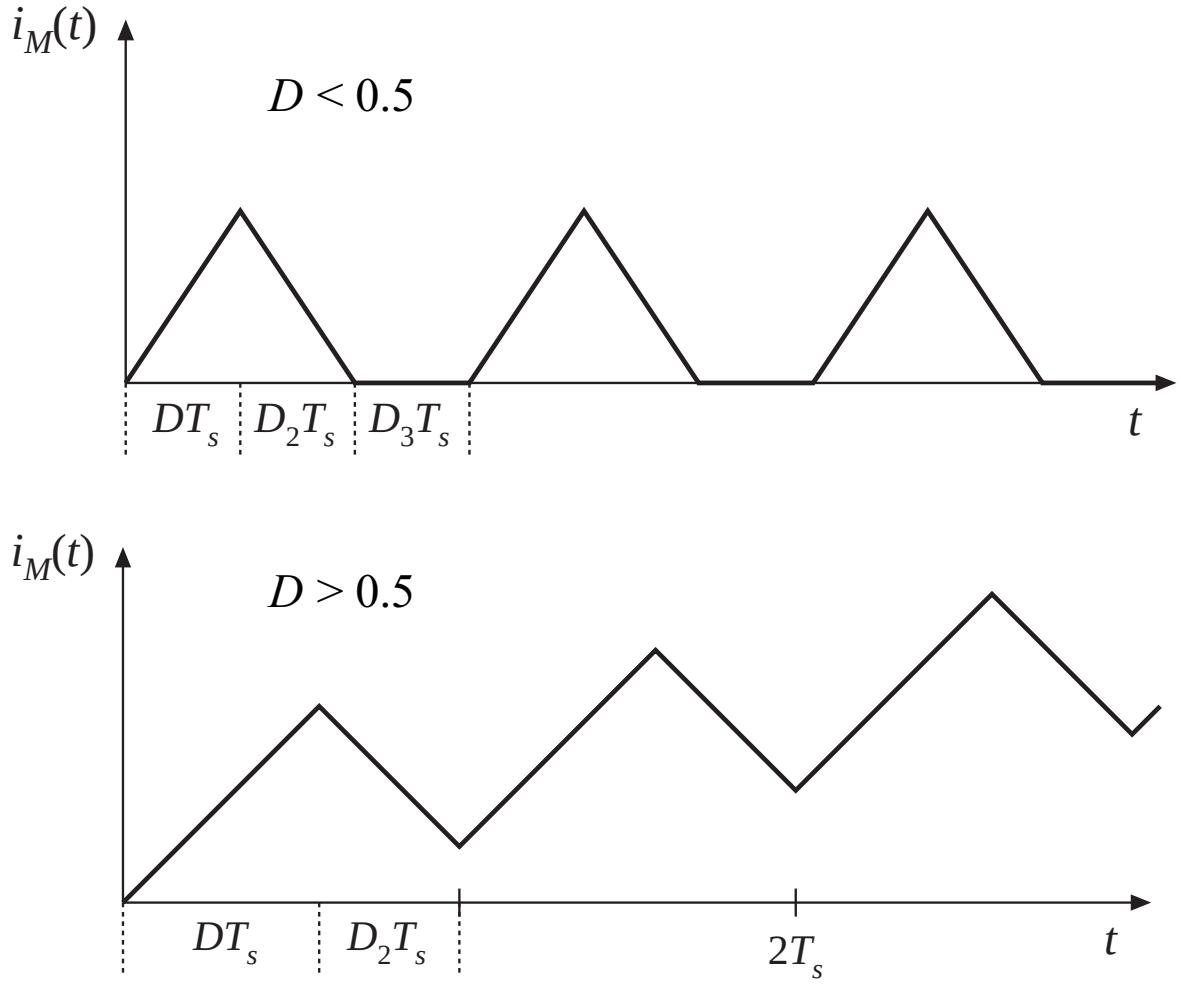
Solve for D

$$D \leq \frac{1}{1 + \frac{n_2}{n_1}}$$

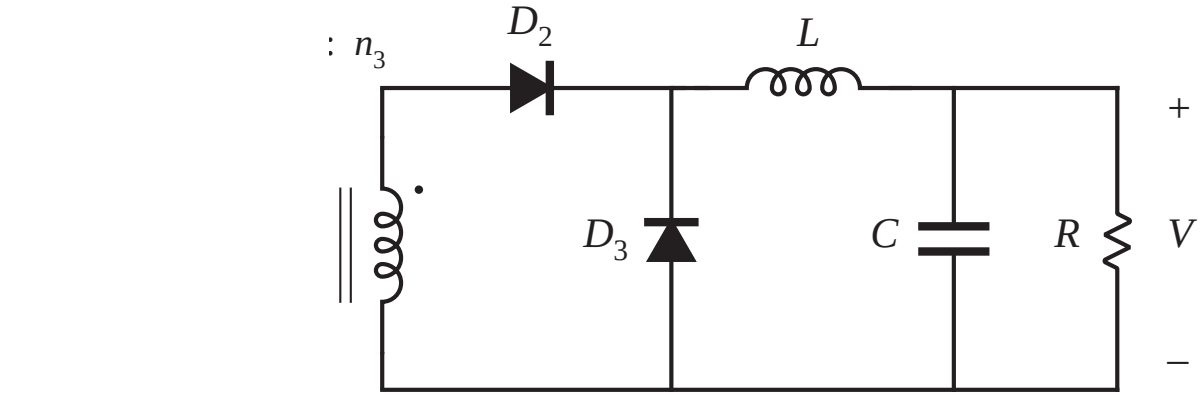
for $n_1 = n_2$: $D \leq \frac{1}{2}$

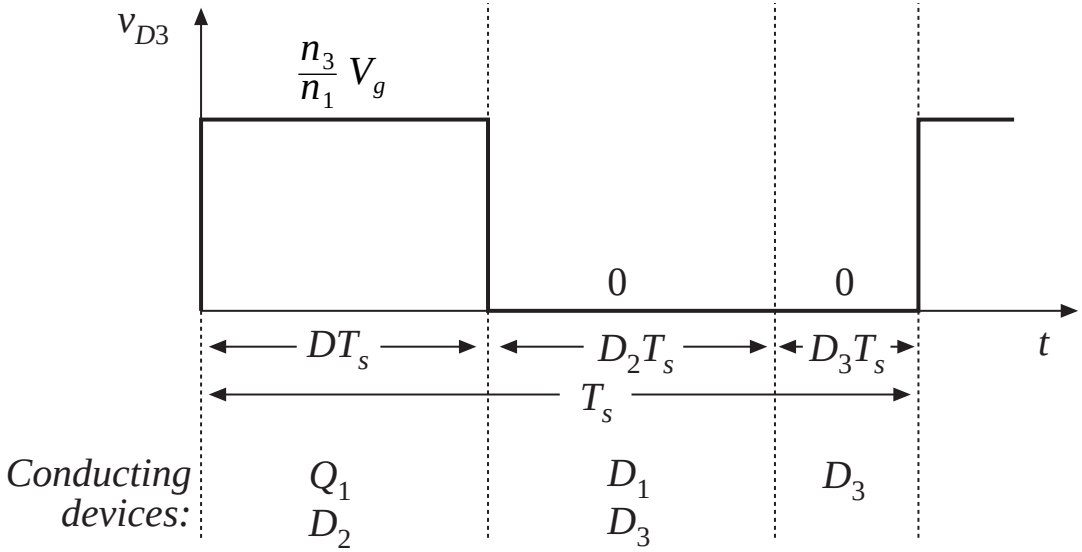
What happens when $D > 0.5$

magnetizing current waveforms, for $n_1 = n_2$



Conversion ratio *M(D)*





$$\left\langle v_{D3} \right\rangle = V = \frac{n_3}{n_1} D V_g$$

Maximum duty cycle vs. transistor voltage stress

Maximum duty cycle limited to

$$D \leq \frac{1}{1 + \frac{n_2}{n_1}}$$

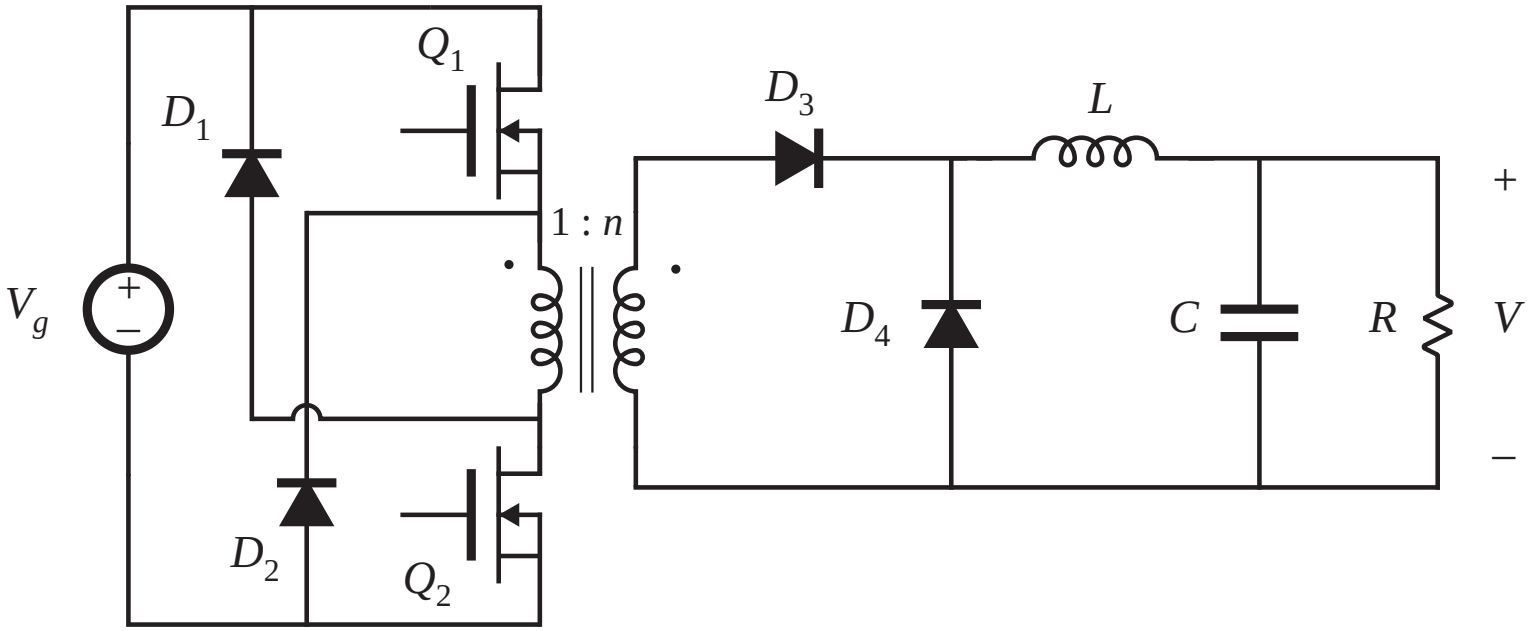
which can be increased by increasing the turns ratio n_2 / n_1. But this increases the peak transistor voltage:

$$\max\left(v_{Q1}\right) = V_g\left(1 + \frac{n_1}{n_2}\right)$$

For $n_1 = n_2$

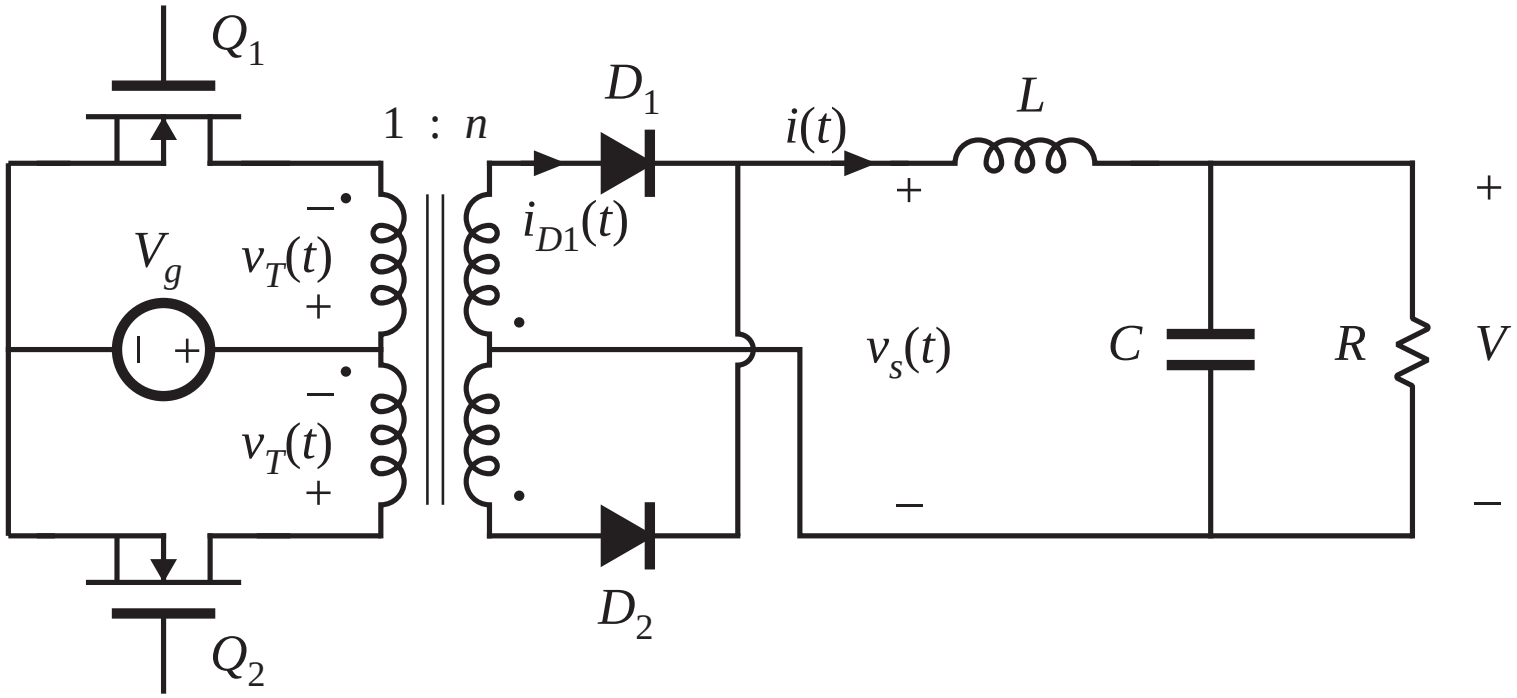
$$D \leq \frac{1}{2} \qquad \text{and} \qquad \max(v_{Q1}) = 2V_g$$

The two-transistor forward converter



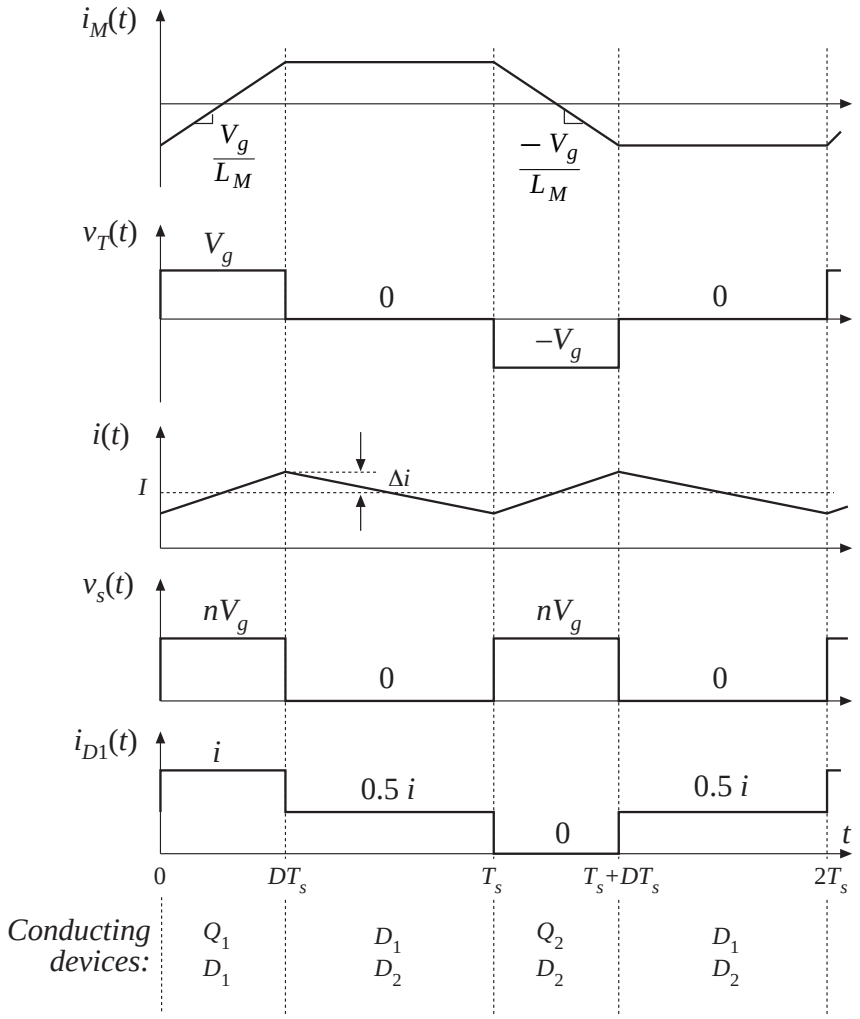
$$V = nDV_g \qquad D \le \frac{1}{2} \qquad \max(v_{Q1}) = \max(v_{Q2}) = V_g$$

6.3.3. Push-pull isolated buck converter



$$V = nDV_g \qquad 0 \le D \le 1$$

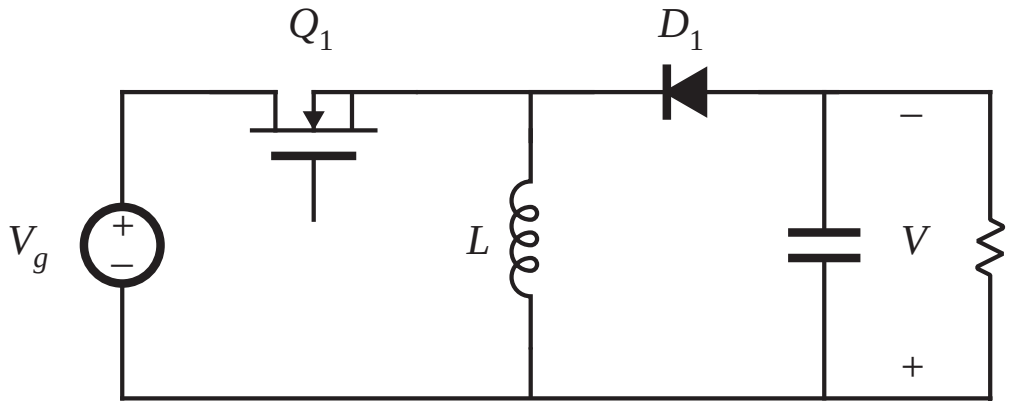
Waveforms: push-pull



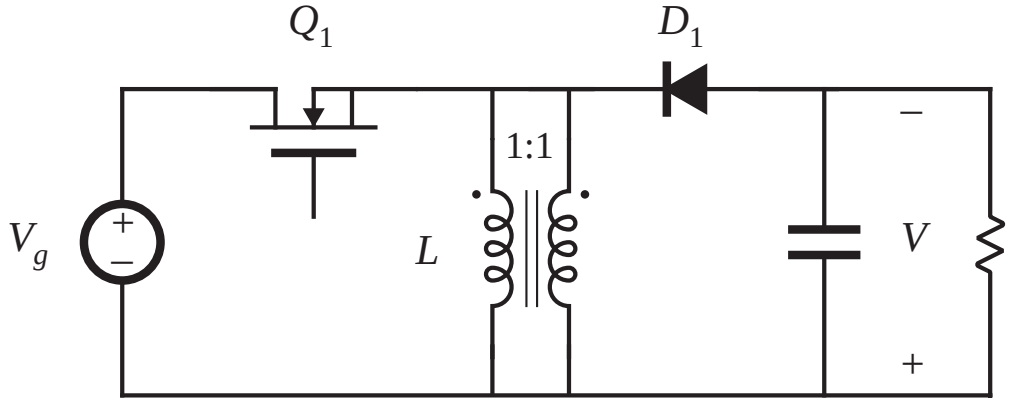
- Used with low-voltage inputs
- Secondary-side circuit identical to full bridge
- As in full bridge, transformer volt-second balance is obtained over two switching periods
- Effect of nonidealities on transformer volt-second balance?
- Current programmed control can be used to mitigate transformer saturation problems. Duty cycle control not recommended.

6.3.4. Flyback converter

buck-boost converter:

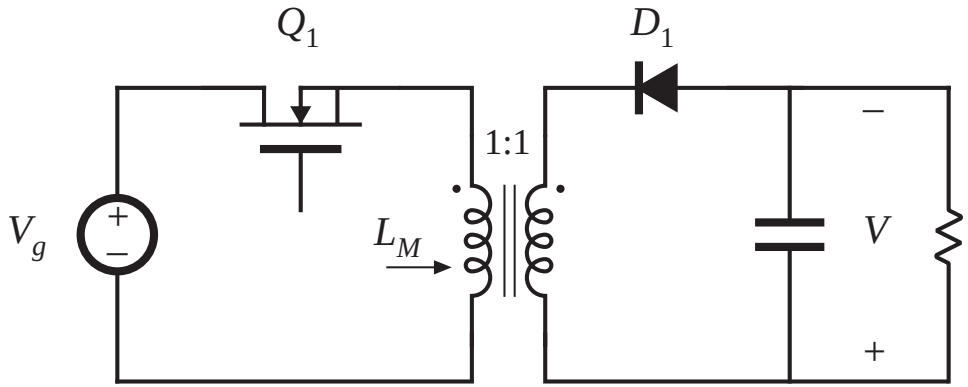


construct inductor winding using two parallel wires:

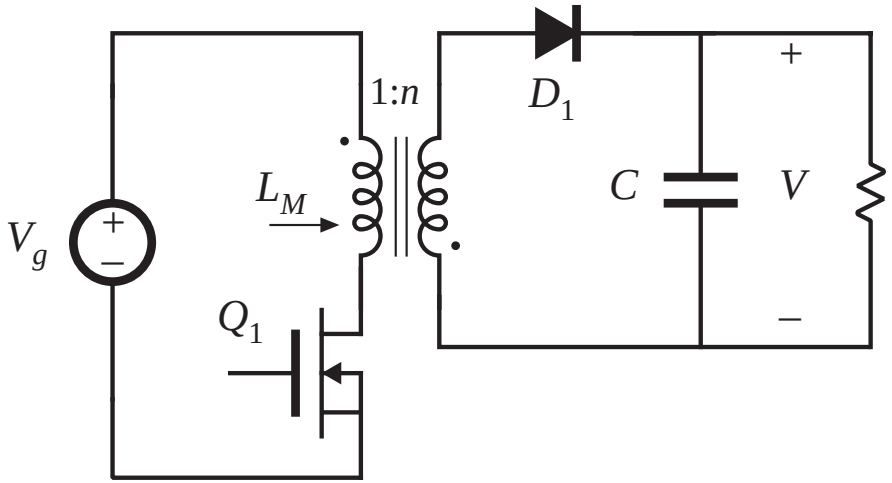


Derivation of flyback converter, cont.

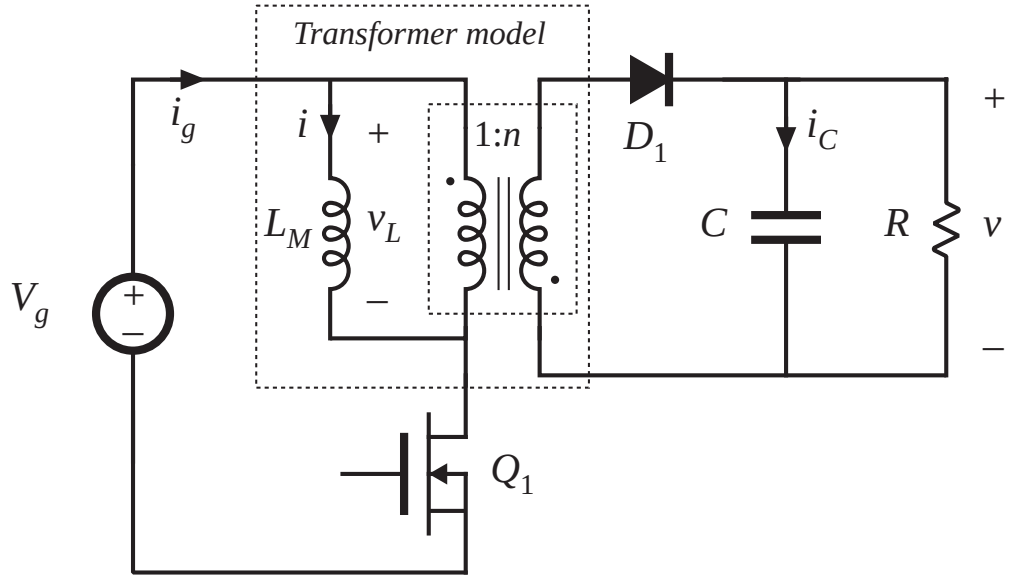
Isolate inductor windings: the flyback converter



Flyback converter having a $1{:}n$ turns ratio and positive output:



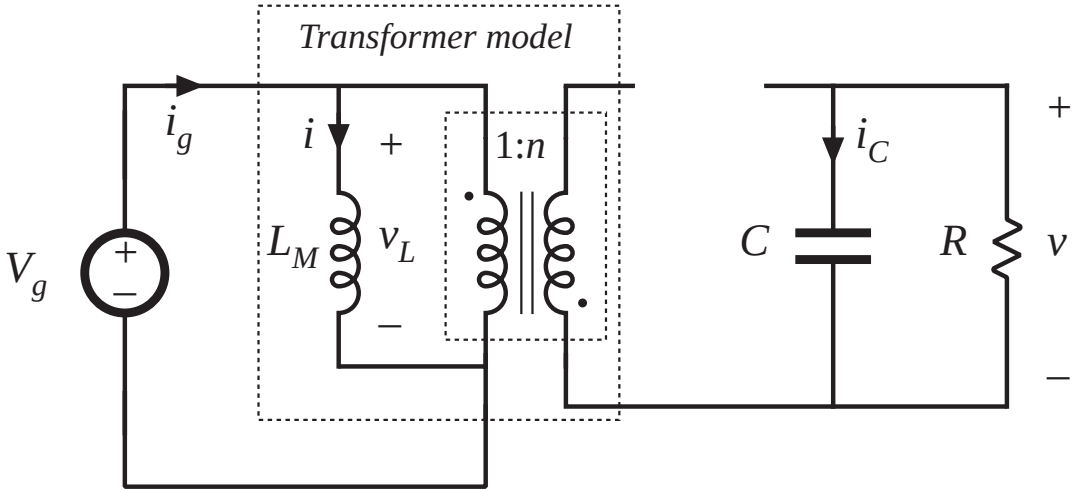
The "flyback transformer"



- A two-winding inductor
- Symbol is same as transformer, but function differs significantly from ideal transformer
- Energy is stored in magnetizing inductance
- Magnetizing inductance is relatively small

- Current does not simultaneously flow in primary and secondary windings
- Instantaneous winding voltages follow turns ratio
- Instantaneous (and rms) winding currents do not follow turns ratio
- Model as (small) magnetizing inductance in parallel with ideal transformer

Subinterval 1



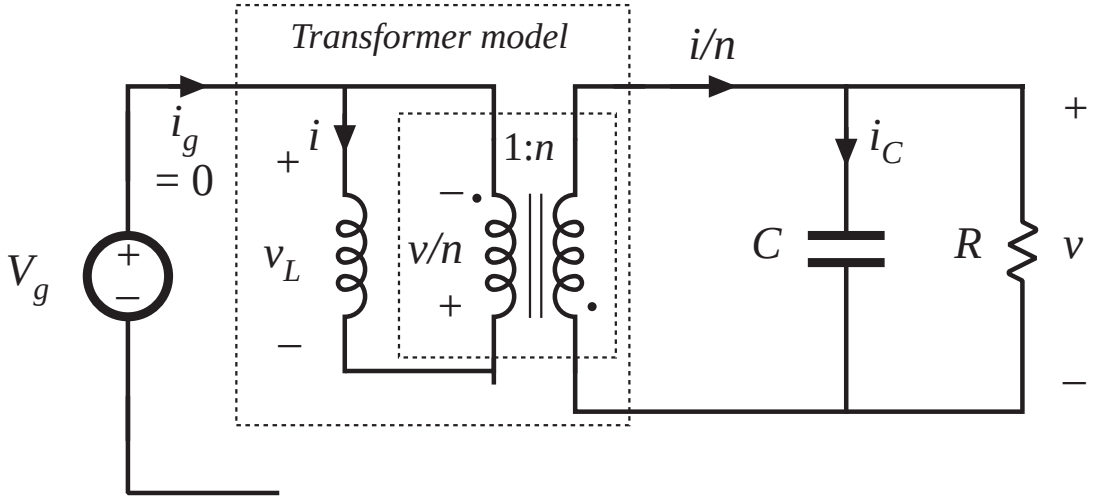
Q_1 on, D_1 off

$$v_L = V_g$$
$$i_C = -\frac{v}{R}$$
$$i_g = i$$

CCM: small ripple approximation leads to

$$v_L = V_g$$
$$i_C = -\frac{V}{R}$$
$$i_g = I$$

Subinterval 2



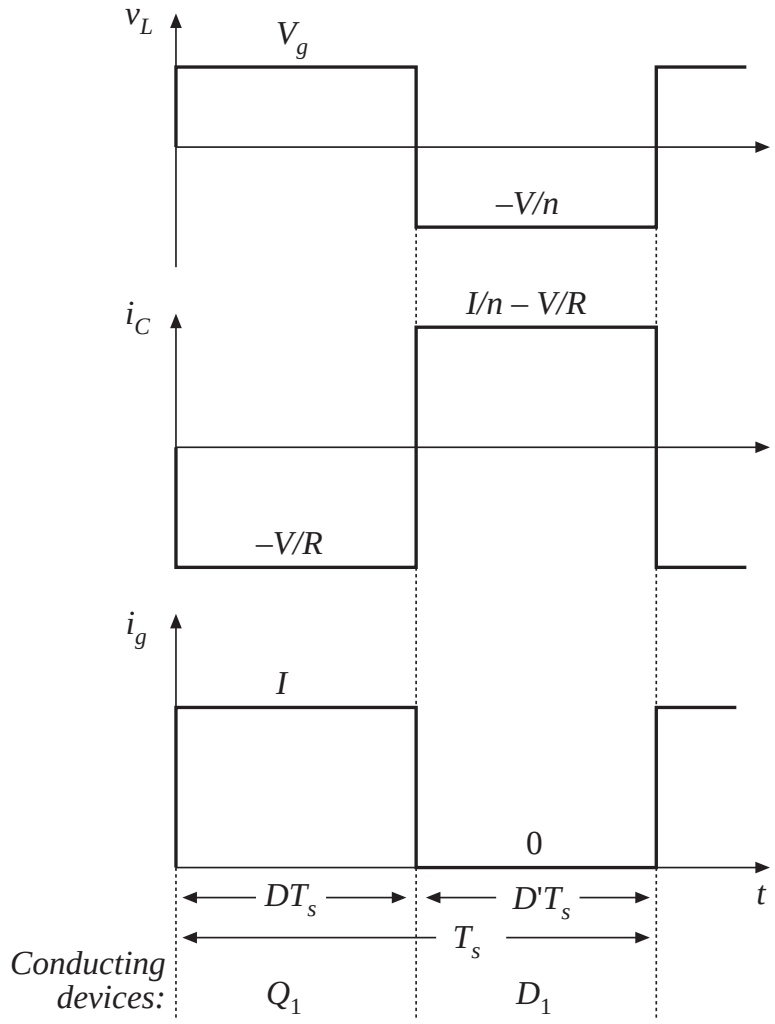
Q_1 off, D_1 on

$$v_L = -\frac{v}{n}$$
$$i_C = \frac{i}{n} - \frac{v}{R}$$
$$i_g = 0$$

CCM: small ripple approximation leads to

$$v_L = -\frac{V}{n}$$
$$i_C = \frac{I}{n} - \frac{V}{R}$$
$$i_g = 0$$

CCM Flyback waveforms and solution



Volt-second balance:

$$\langle v_L \rangle = D\left(V_g\right) + D'\left(-\frac{V}{n}\right) = 0$$

Conversion ratio is

$$M(D) = \frac{V}{V_g} = n\,\frac{D}{D'}$$

Charge balance:

$$\langle i_C \rangle = D\left(-\frac{V}{R}\right) + D'\left(\frac{I}{n} - \frac{V}{R}\right) = 0$$

Dc component of magnetizing current is

$$I = \frac{nV}{D'R}$$

Dc component of source current is

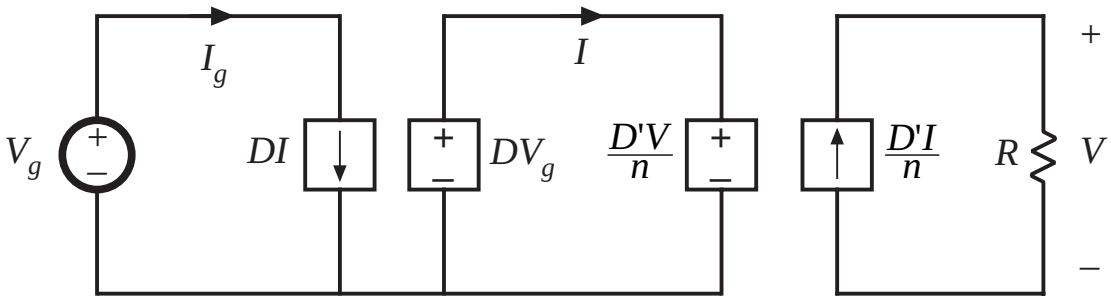
$$I_g = \langle i_g \rangle = D\left(I\right) + D'\left(0\right)$$

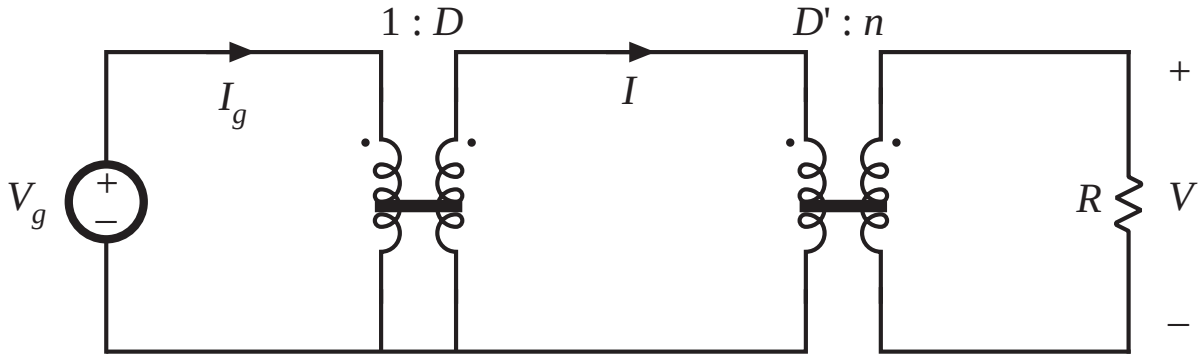
Equivalent circuit model: CCM Flyback

$$\langle v_L \rangle = D\left(V_g\right) + D'\left(-\frac{V}{n}\right) = 0$$

$$\langle i_C \rangle = D\left(-\frac{V}{R}\right) + D'\left(\frac{I}{n} - \frac{V}{R}\right) = 0$$

$$I_g = \langle i_g \rangle = D\left(I\right) + D'\left(0\right)$$





Discussion: Flyback converter

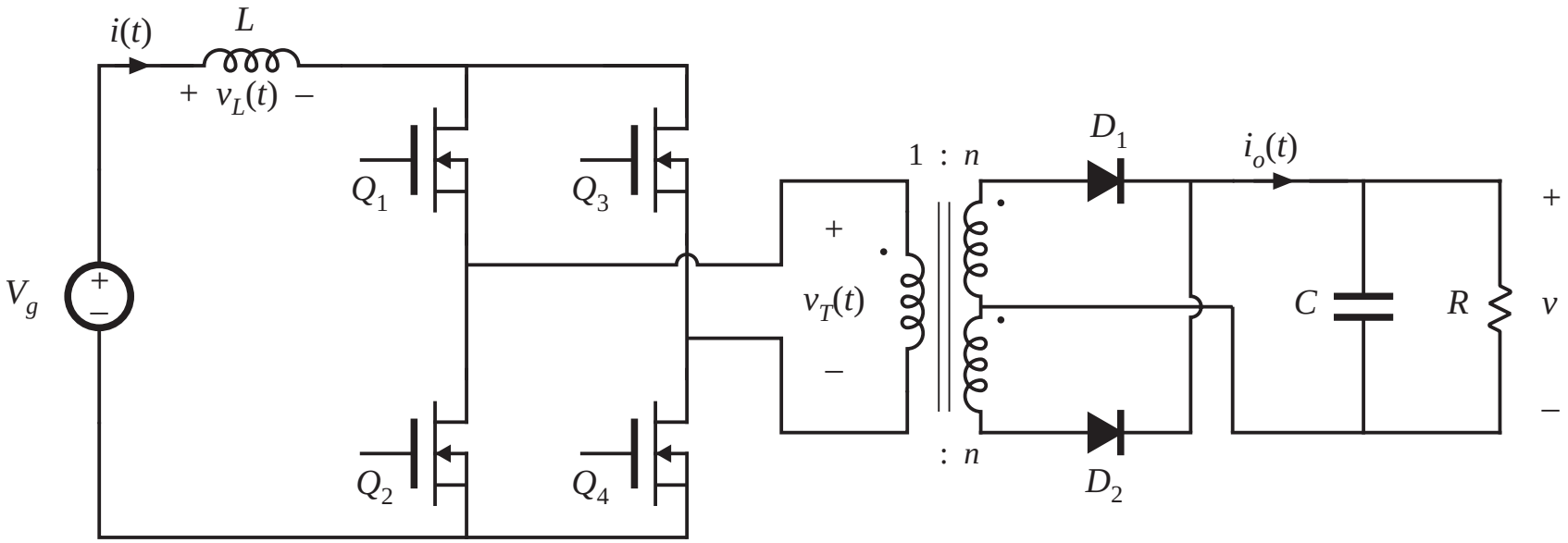
- Widely used in low power and/or high voltage applications
- Low parts count
- Multiple outputs are easily obtained, with minimum additional parts
- Cross regulation is inferior to buck-derived isolated converters
- Often operated in discontinuous conduction mode
- DCM analysis: DCM buck-boost with turns ratio

6.3.5. Boost-derived isolated converters

- A wide variety of boost-derived isolated dc-dc converters can be derived, by inversion of source and load of buck-derived isolated converters:
  - full-bridge and half-bridge isolated boost converters
  - inverse of forward converter: the “reverse” converter
  - push-pull boost-derived converter

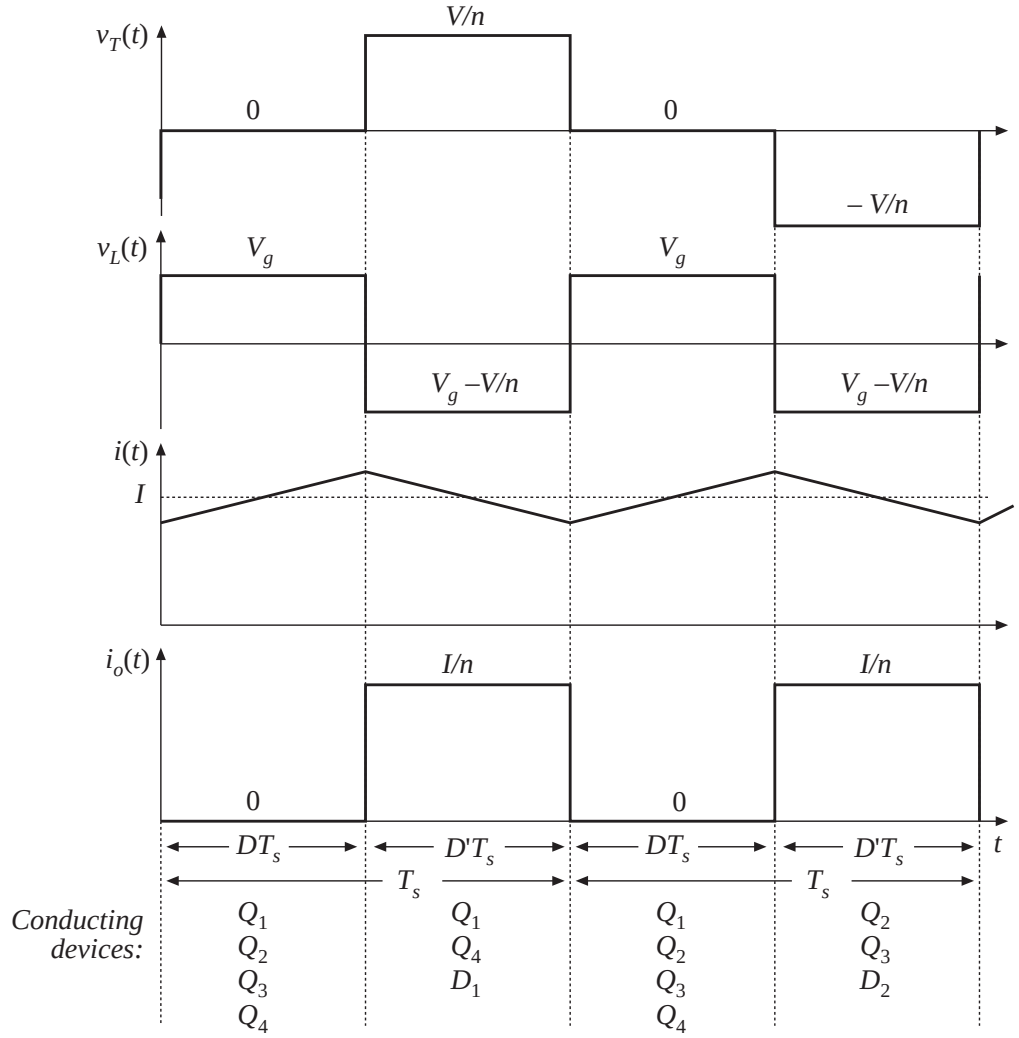
Of these, the full-bridge and push-pull boost-derived isolated converters are the most popular, and are briefly discussed here.

Full-bridge transformer-isolated boost-derived converter



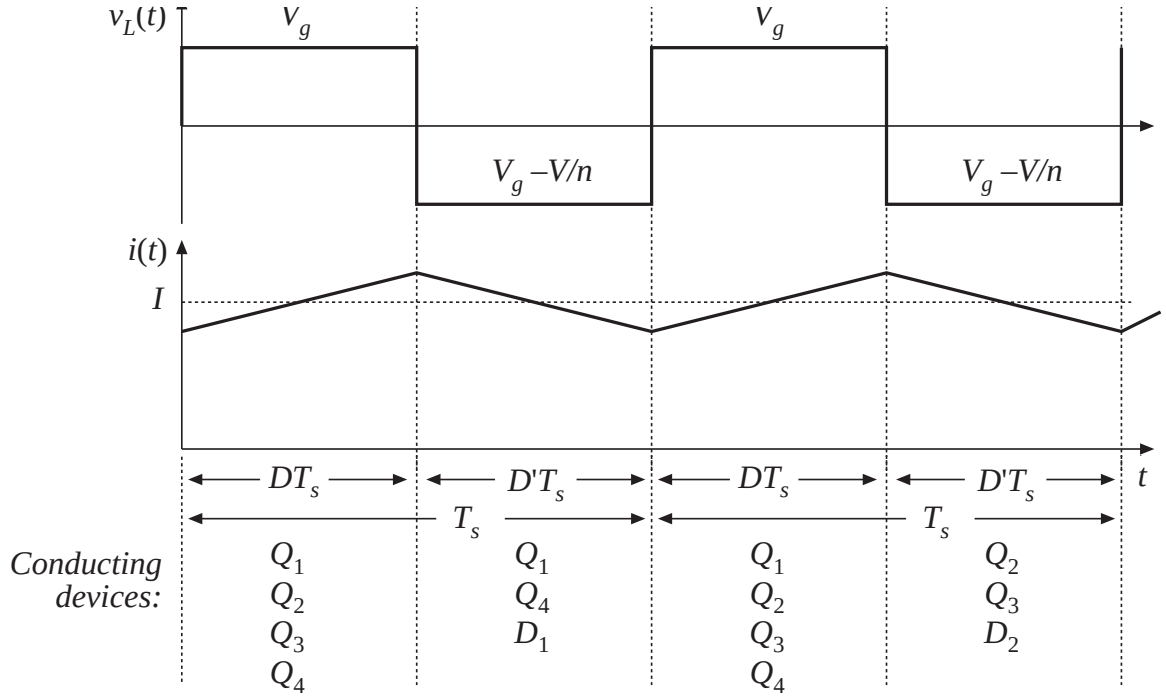
- Circuit topologies are equivalent to those of nonisolated boost converter
- With 1:1 turns ratio, inductor current $i(t)$ and output current $i_o(t)$ waveforms are identical to nonisolated boost converter

Transformer reset mechanism



- As in full-bridge buck topology, transformer volt-second balance is obtained over two switching periods.
- During first switching period: transistors Q_1 and Q_4 conduct for time DT_s , applying volt-seconds VDT_s to secondary winding.
- During next switching period: transistors Q_2 and Q_3 conduct for time DT_s , applying volt-seconds $-VDT_s$ to secondary winding.

Conversion ratio $M(D)$



Application of volt-second balance to inductor voltage waveform:

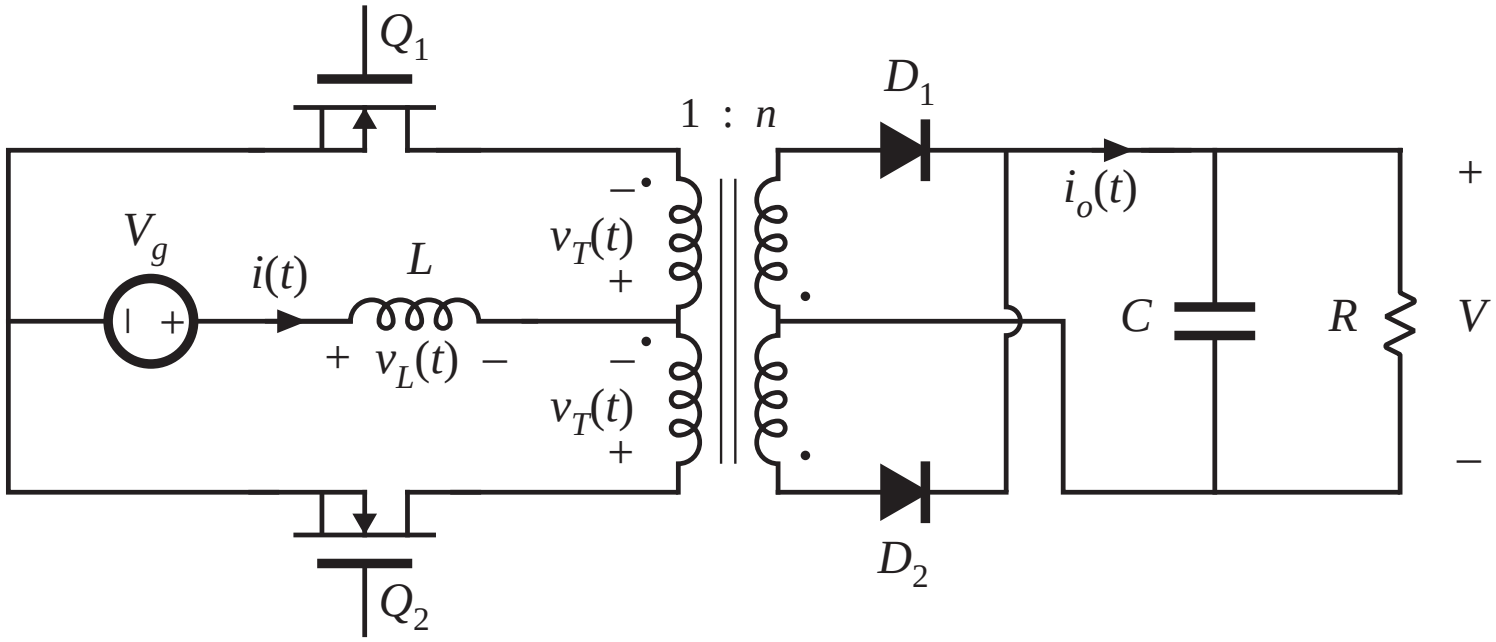
$$\langle v_L \rangle = D\left(V_g\right) + D'\left(V_g - \frac{V}{n}\right) = 0$$

Solve for $M(D)$:

$$M(D) = \frac{V}{V_g} = \frac{n}{D'}$$

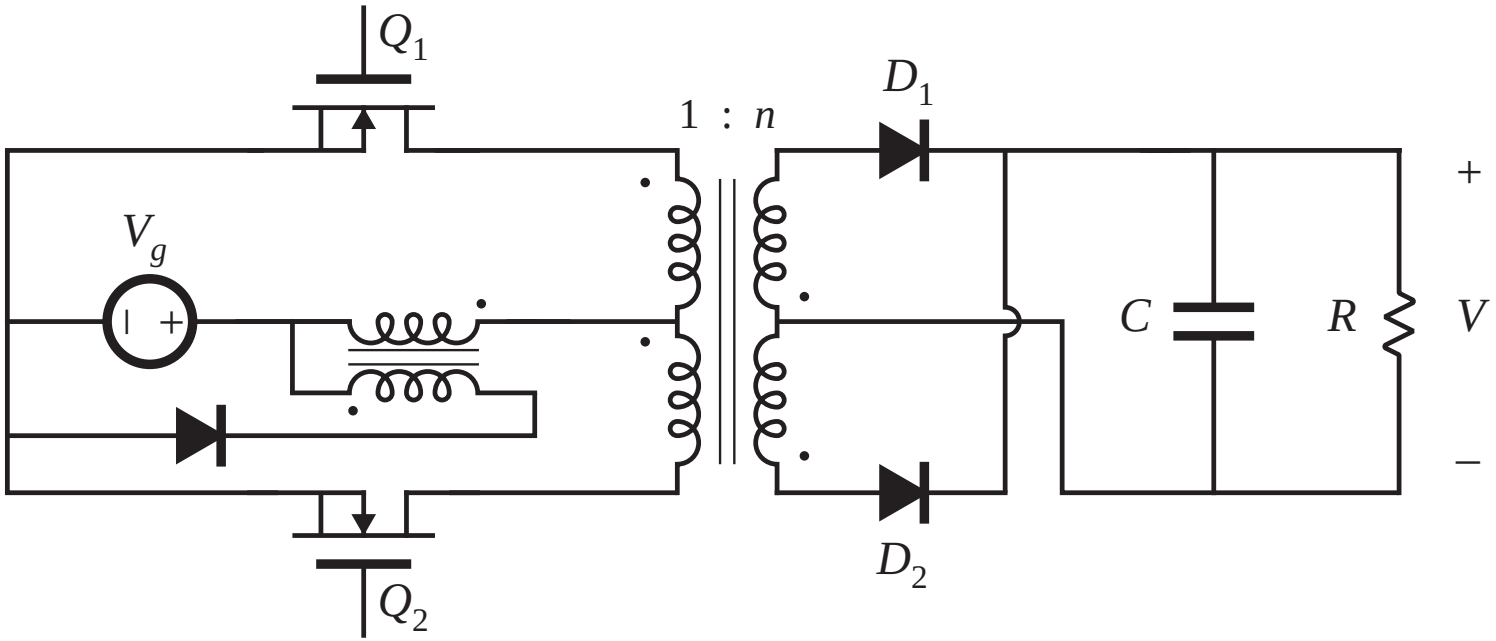
—boost with turns ratio n

Push-pull boost-derived converter



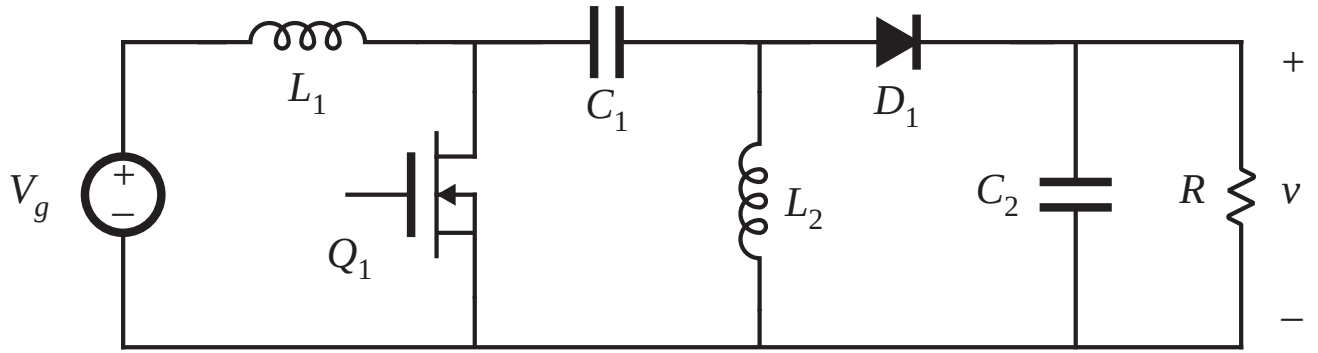
$$M(D) = \frac{V}{V_g} = \frac{n}{D'}$$

Push-pull converter based on Watkins-Johnson converter

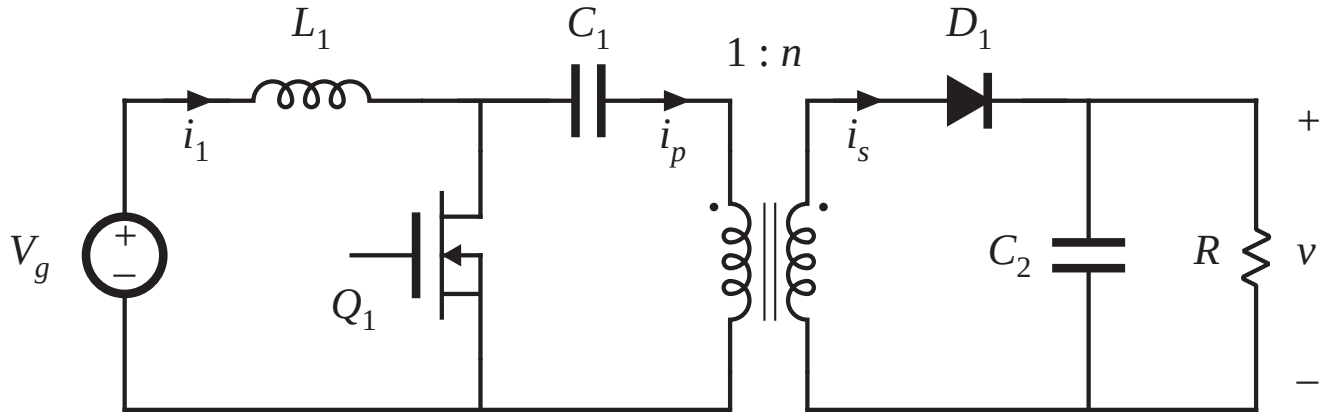


6.3.6. Isolated versions of the SEPIC and Cuk converter

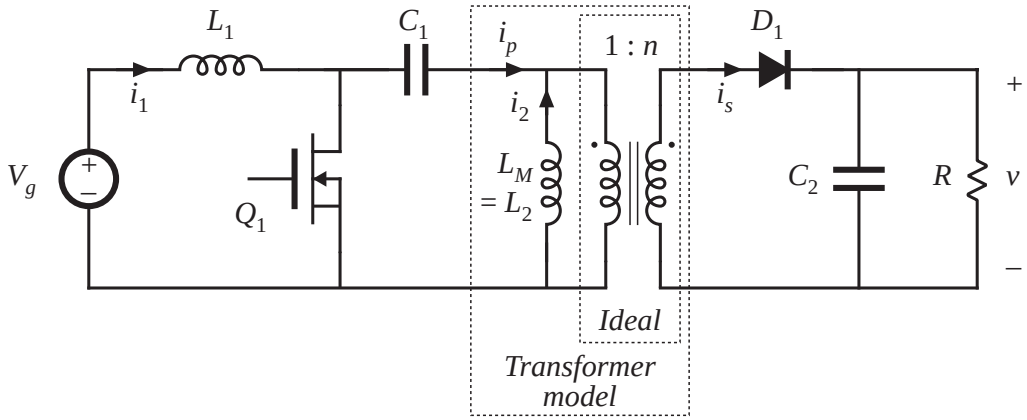
Basic nonisolated SEPIC



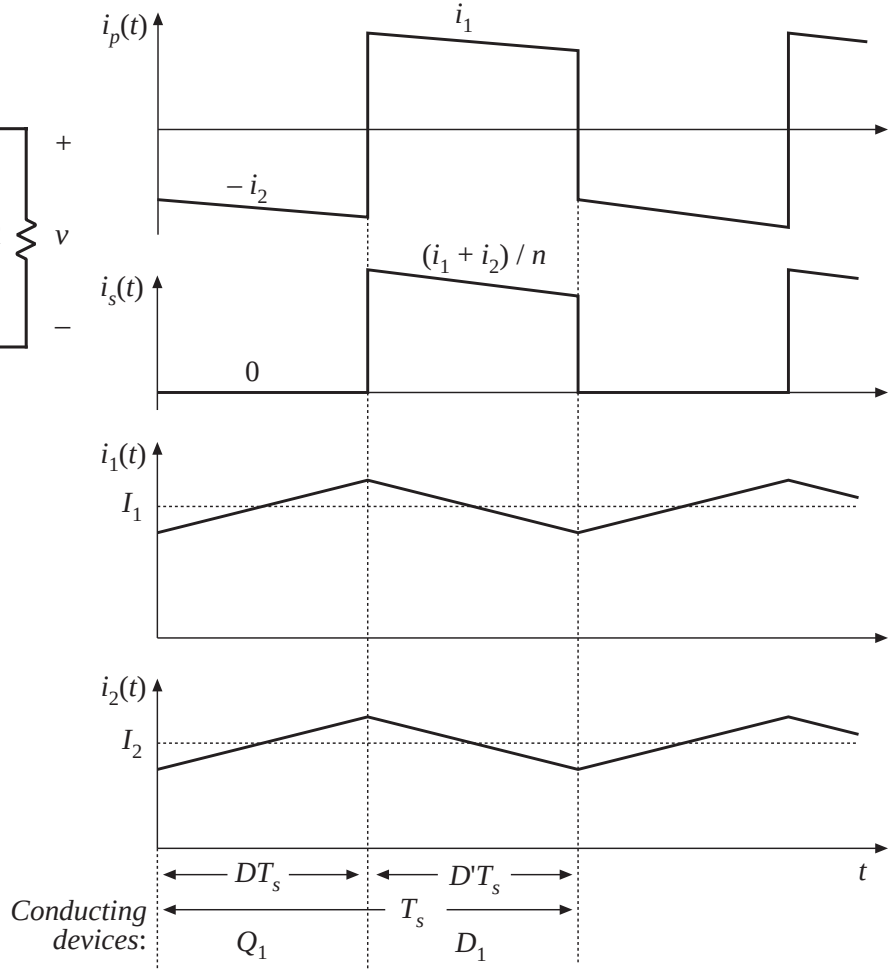
Isolated SEPIC



Isolated SEPIC

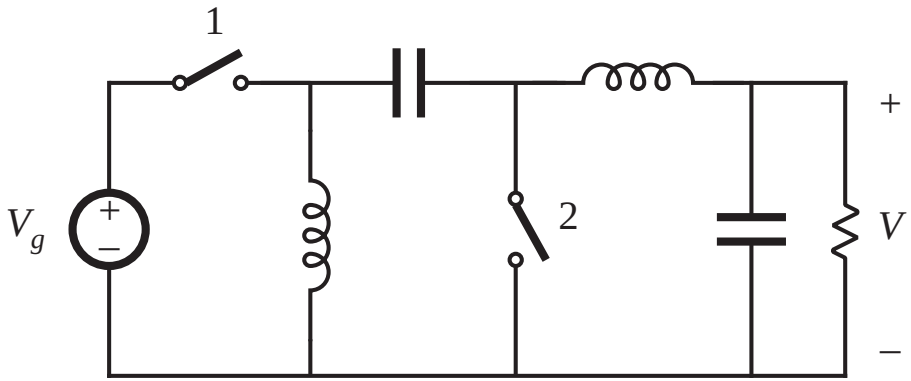


$$M(D) = \frac{V}{V_g} = \frac{nD}{D'}$$

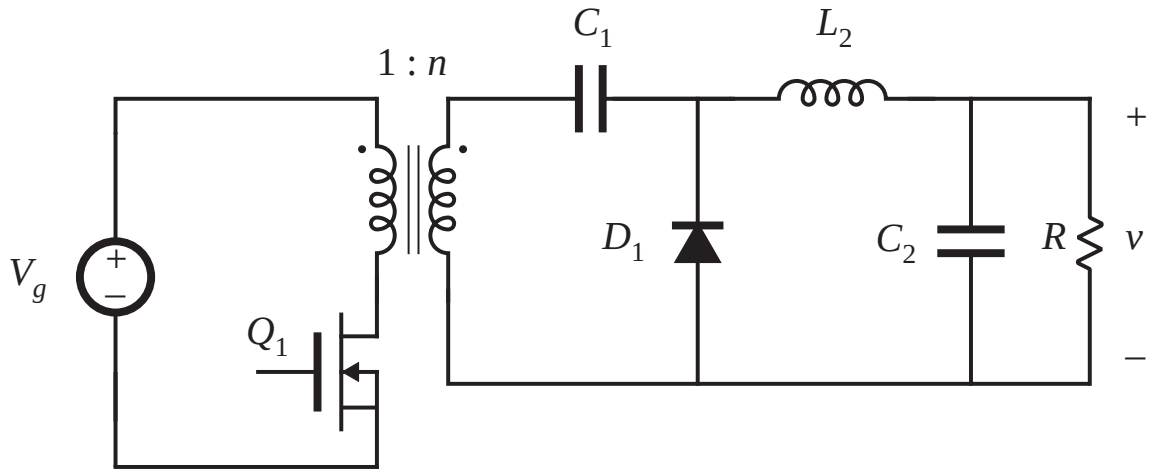


Inverse SEPIC

Nonisolated inverse SEPIC

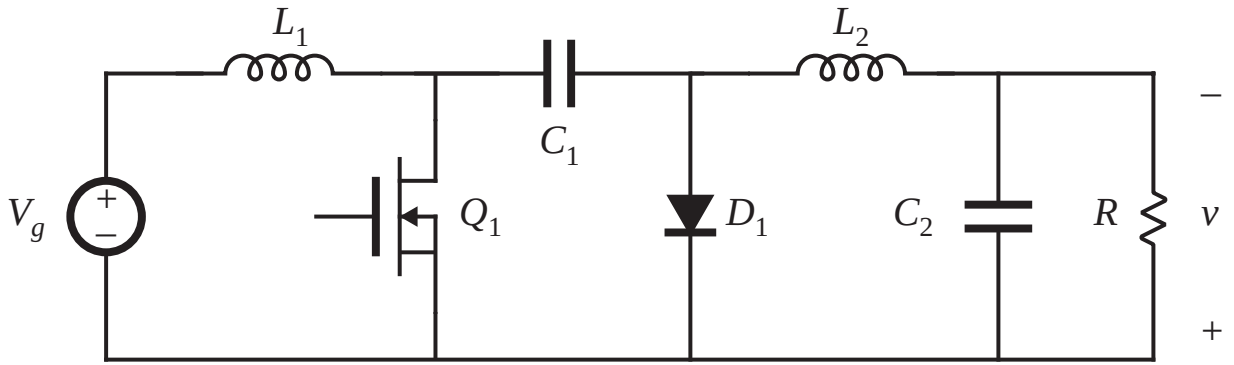


Isolated inverse SEPIC

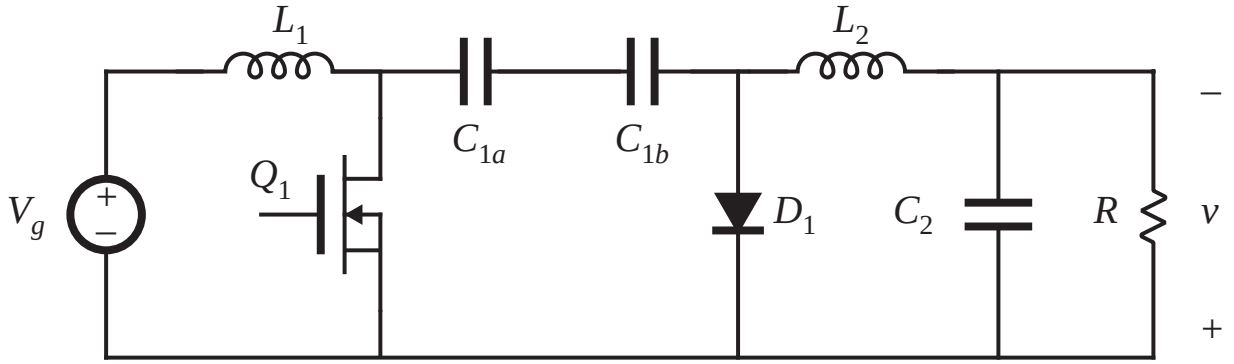


Obtaining isolation in the Cuk converter

Nonisolated Cuk converter



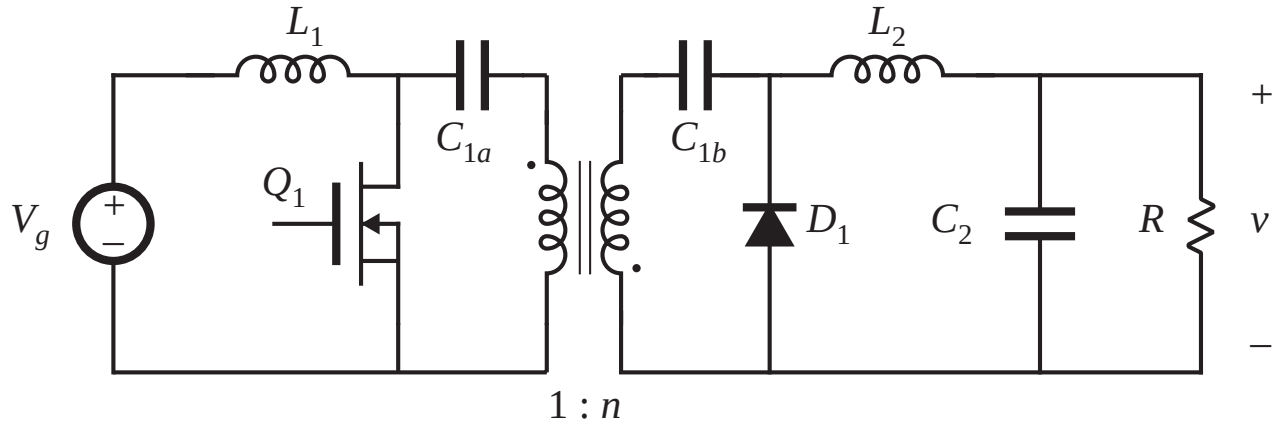
Split capacitor C_1 into series capacitors C_{1a} and C_{1b}



Isolated Cuk converter

Insert transformer between capacitors C_{1a} and C_{1b}

$$M(D) = \frac{V}{V_g} = \frac{nD}{D'}$$



Discussion

- Capacitors C_{1a} *and* C_{1b} ensure that no dc voltage is applied to transformer primary or secondary windings
- Transformer functions in conventional manner, with small magnetizing current and negligible energy storage within the magnetizing inductance

6.4. Converter evaluation and design

For a given application, which converter topology is best?

There is no ultimate converter, perfectly suited for all possible applications

Trade studies

- Rough designs of several converter topologies to meet the given specifications
- An unbiased quantitative comparison of worst-case transistor currents and voltages, transformer size, etc.

Comparison via switch stress, switch utilization, and semiconductor cost

Spreadsheet design

6.4.1. Switch stress and switch utilization

- Largest single cost in a converter is usually the cost of the active semiconductor devices
- Conduction and switching losses associated with the active semiconductor devices often dominate the other sources of loss

This suggests evaluating candidate converter approaches by comparing the voltage and current stresses imposed on the active semiconductor devices.

Minimization of total switch stresses leads to reduced loss, and to minimization of the total silicon area required to realize the power devices of the converter.

Total active switch stress S

In a converter having k active semiconductor devices, the total active switch stress S is defined as

$$S = \sum_{j=1}^{k} V_j I_j$$

where

V_j is the peak voltage applied to switch j,

I_j is the rms current applied to switch j (peak current is also sometimes used).

In a good design, the total active switch stress is minimized.

Active switch utilization U

It is desired to minimize the total active switch stress, while maximizing the output power P_{load}.

The active switch utilization U is defined as

$$U = \frac{P_{load}}{S}$$

The active switch utilization is the converter output power obtained per unit of active switch stress. It is a converter figure-of-merit, which measures how well a converter utilizes its semiconductor devices.

Active switch utilization is less than 1 in transformer-isolated converters, and is a quantity to be maximized.

Converters having low switch utilizations require extra active silicon area, and operate with relatively low efficiency.

Active switch utilization is a function of converter operating point.

CCM flyback example: Determination of S

During subinterval 2, the transistor blocks voltage $V_{Q1,pk}$ equal to V_g plus the reflected load voltage:

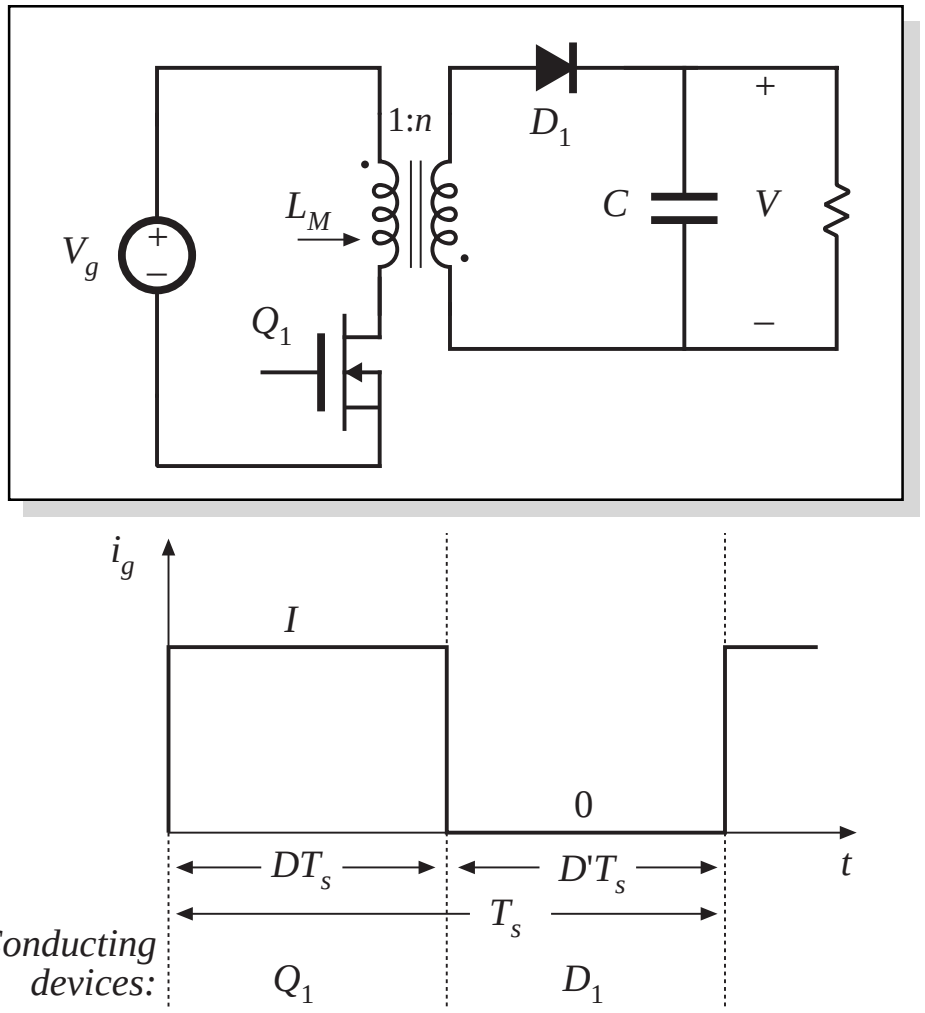
$$V_{Q1,pk} = V_g + \frac{V}{n} = \frac{V_g}{D'}$$

Transistor current coincides with $i_g(t)$. RMS value is

$$I_{Q1,rms} = I\sqrt{D} = \frac{P_{load}}{V_g\sqrt{D}}$$

Switch stress S is

$$S = V_{Q1,pk}\, I_{Q1,rms} = \left(V_g + \frac{V}{n}\right)\left(I\sqrt{D}\right)$$



CCM flyback example: Determination of U

Express load power P_{load} in terms of V and I:

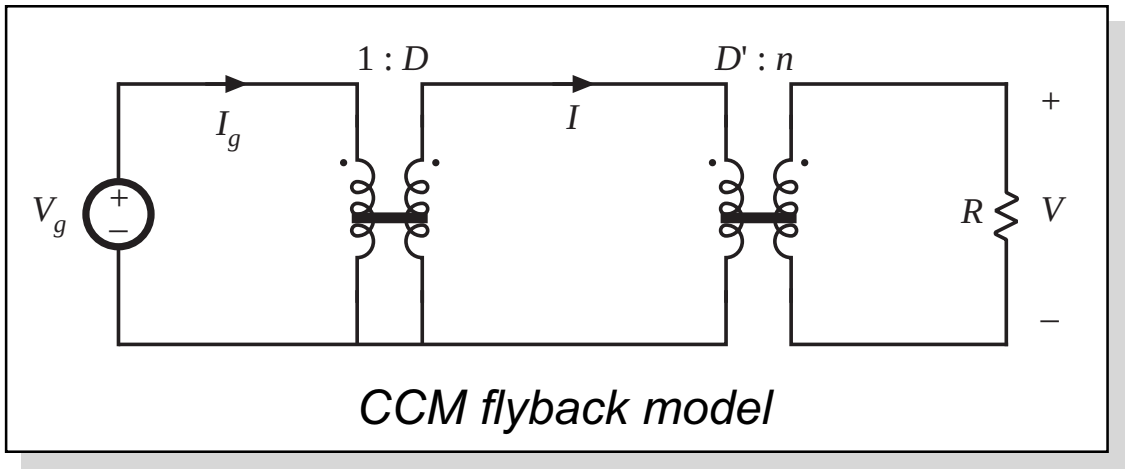
$$P_{load} = D' V \frac{I}{n}$$

Previously-derived expression for S:

$$S = V_{Q1,pk}\, I_{Q1,rms} = \left(V_g + \frac{V}{n} \right) \left(I \sqrt{D} \right)$$

Hence switch utilization U is

$$U = \frac{P_{load}}{S} = D' \sqrt{D}$$



CCM flyback model

Flyback example: switch utilization *U(D)*

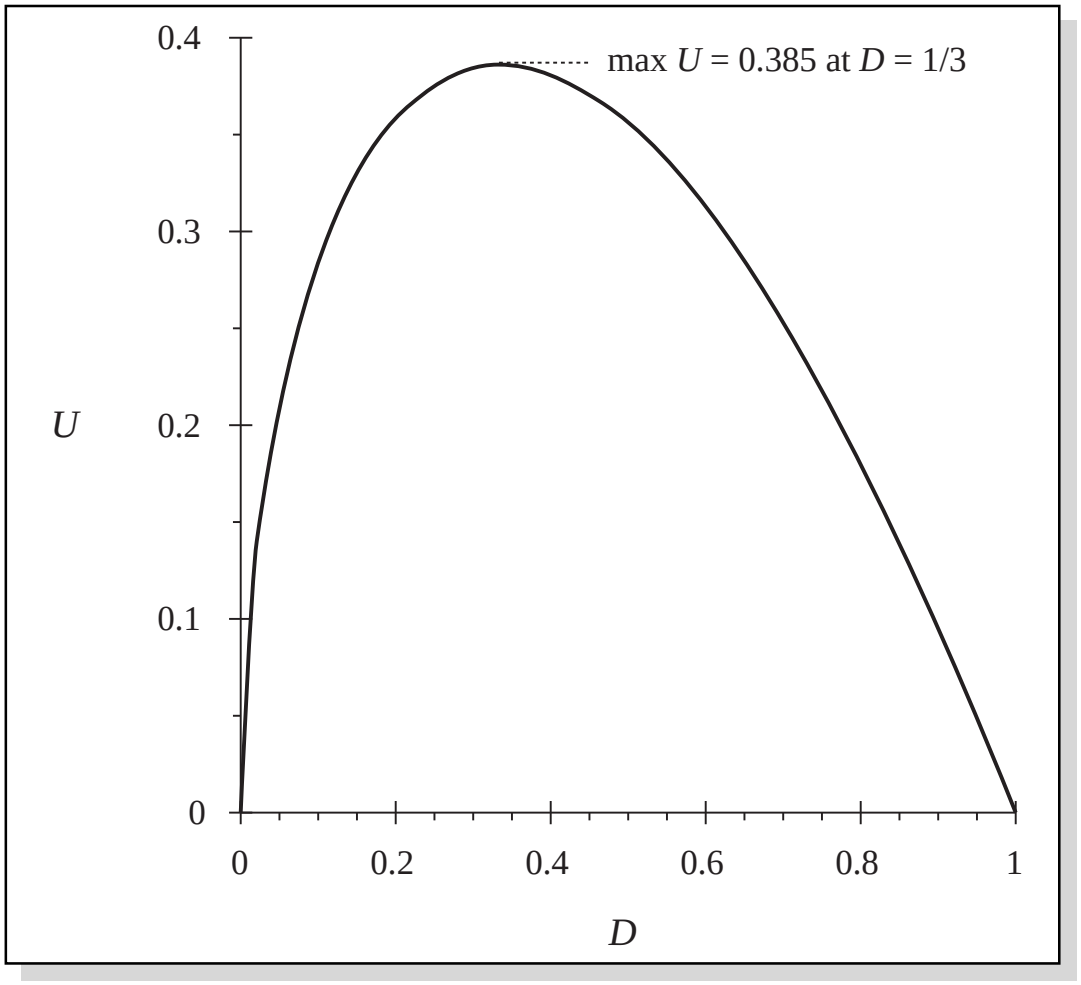
For given V, V_g, P_{load}, the designer can arbitrarily choose D. The turns ratio n must then be chosen according to

$$n = \frac{V}{V_g}\frac{D'}{D}$$

Single operating point design: choose $D = 1/3$.

small D leads to large transistor current

large D leads to large transistor voltage



Comparison of switch utilizations of some common converters

Table 6.1. Active switch utilizations of some common dc-dc converters, single operating point.

Converter	*U(D)*	max *U(D)*	max *U(D)* *occurs at D =*
Buck	$\sqrt{D}$	1	1
Boost	$\frac{D'}{\sqrt{D}}$	∞	0
Buck-boost, flyback, nonisolated SEPIC, isolated SEPIC, nonisolated Cuk, isolated Cuk	$D'\sqrt{D}$	$\frac{2}{3\sqrt{3}} = 0.385$	$\frac{1}{3}$
Forward, $n_1 = n_2$	$\frac{1}{2}\sqrt{D}$	$\frac{1}{2\sqrt{2}} = 0.353$	$\frac{1}{2}$
Other isolated buck-derived converters (full-bridge, half-bridge, push-pull)	$\frac{\sqrt{D}}{2\sqrt{2}}$	$\frac{1}{2\sqrt{2}} = 0.353$	1
Isolated boost-derived converters (full bridge, push-pull)	$\frac{D'}{2\sqrt{1+D}}$	$\frac{1}{2}$	0

Switch utilization : Discussion

- Increasing the range of operating points leads to reduced switch utilization
- Buck converter
  - can operate with high switch utilization (U approaching 1) when D is close to 1
- Boost converter
  - can operate with high switch utilization (U approaching ∞) when D is close to 1
- Transformer isolation leads to reduced switch utilization
- Buck-derived transformer-isolated converters
  - $U \leq 0.353$
  - should be designed to operate with D as large as other considerations allow
  - transformer turns ratio can be chosen to optimize design

Switch utilization: Discussion

- Nonisolated and isolated versions of buck-boost, SEPIC, and Cuk converters
  - $U \leq 0.385$
  - Single-operating-point optimum occurs at $D = 1/3$
  - Nonisolated converters have lower switch utilizations than buck or boost
  - Isolation can be obtained without penalizing switch utilization

Active semiconductor cost vs. switch utilization

$$\left(\begin{array}{c}\text{semiconductor cost}\\ \text{per kW output power}\end{array}\right) = \frac{\left(\begin{array}{c}\text{semiconductor device cost}\\ \text{per rated kVA}\end{array}\right)}{\left(\begin{array}{c}\text{voltage}\\ \text{derating}\\ \text{factor}\end{array}\right)\left(\begin{array}{c}\text{current}\\ \text{derating}\\ \text{factor}\end{array}\right)\left(\begin{array}{c}\text{converter}\\ \text{switch}\\ \text{utilization}\end{array}\right)}$$

(semiconductor device cost per rated kVA) = cost of device, divided by product of rated blocking voltage and rms current, in $/kVA. Typical values are less than $1/kVA

(voltage derating factor) and (current derating factor) are required to obtain reliable operation. Typical derating factors are 0.5 - 0.75

Typical cost of active semiconductor devices in an isolated dc-dc converter: $1 - $10 per kW of output power.

6.4.2. Converter design using computer spreadsheet

Given ranges of V_g and P_{load} , as well as desired value of V and other quantities such as switching frequency, ripple, etc., there are two basic engineering design tasks:

- Compare converter topologies and select the best for the given specifications
- Optimize the design of a given converter

A computer spreadsheet is a very useful tool for this job. The results of the steady-state converter analyses of Chapters 1-6 can be entered, and detailed design investigations can be quickly performed:

- Evaluation of worst-case stresses over a range of operating points
- Evaluation of design tradeoffs

Spreadsheet design example

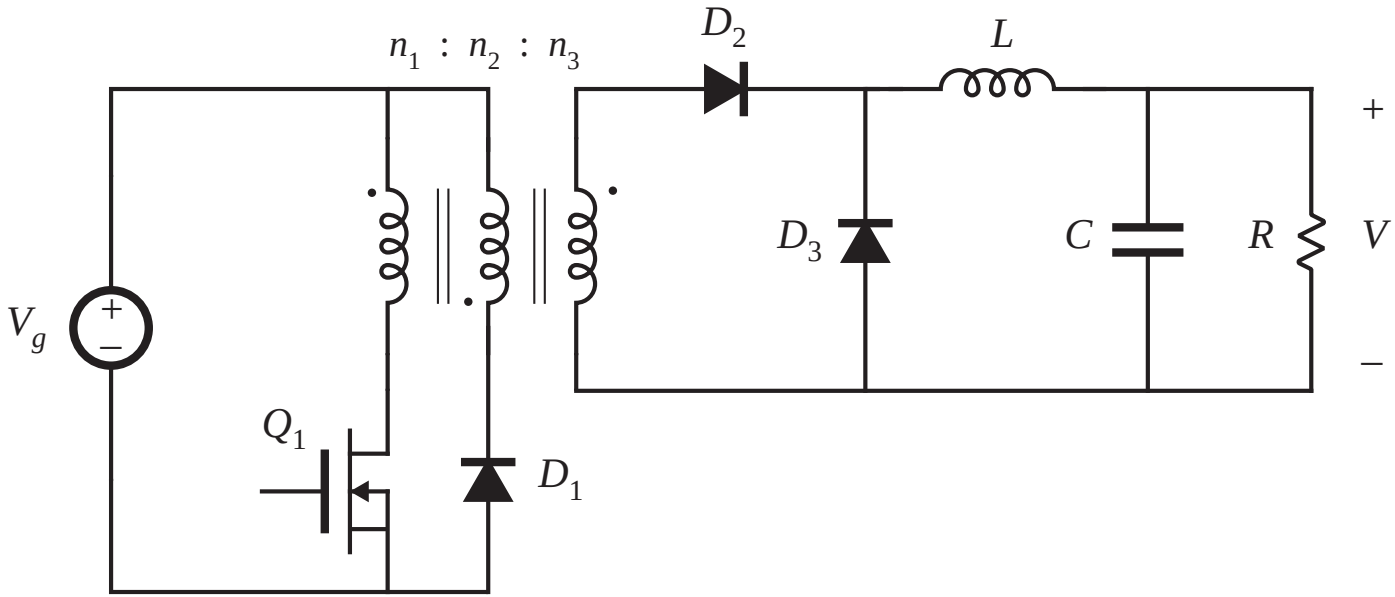
Specifications	
Maximum input voltage V_g	390 V
Minimum input voltage V_g	260 V
Output voltage V	15 V
Maximum load power P_{load}	200 W
Minimum load power P_{load}	20 W
Switching frequency f_s	100 kHz
Maximum output ripple Δv	0.1 V

- Input voltage: rectified 230 Vrms ±20%
- Regulated output of 15 V
- Rated load power 200 W
- Must operate at 10% load
- Select switching frequency of 100 kHz
- Output voltage ripple ≤ 0.1V

Compare single-transistor forward and flyback converters in this application

Specifications are entered at top of spreadsheet

Forward converter design, CCM

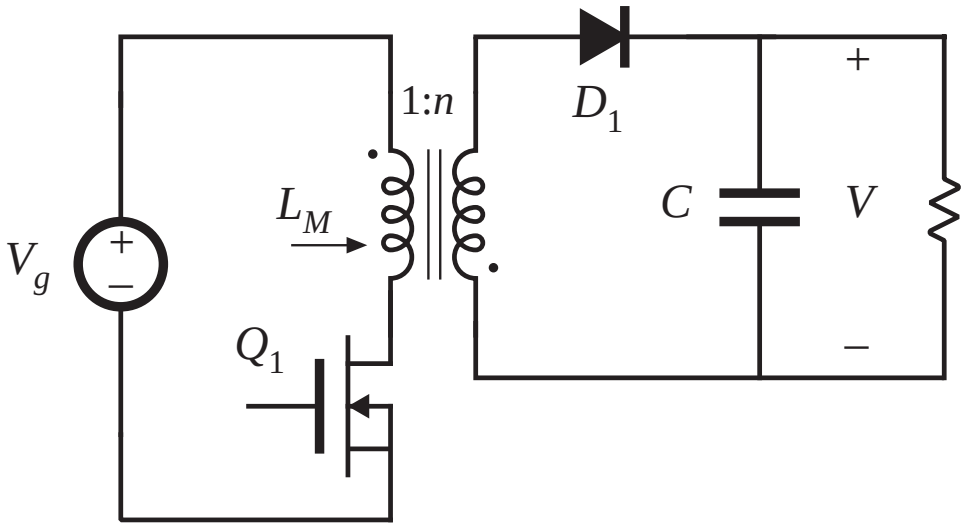


Design variables

Reset winding turns ratio n_2 / n_1	1
Turns ratio n_3 / n_1	0.125
Inductor current ripple Δi	2A ref to sec

- Design for CCM at full load; may operate in DCM at light load

Flyback converter design, CCM



Design variables

Turns ratio n_2 / n_1	0.125
Inductor current ripple Δi	3 A ref to sec

- Design for CCM at full load; may operate in DCM at light load

Enter results of converter analysis into spreadsheet (Forward converter example)

Maximum duty cycle occurs at minimum V_g and maximum P_{load}. Converter then operates in CCM, with

$$D = \frac{n_1}{n_3} \frac{V}{V_g}$$

Inductor current ripple is

$$\Delta i = \frac{D'VT_s}{2L}$$

Solve for L:

$$L = \frac{D'VT_s}{2\Delta i}$$

Δi is a design variable. For a given Δi, the equation above can be used to determine L. To ensure CCM operation at full load, Δi should be less than the full-load output current. C can be found in a similar manner.

Forward converter example, continued

Check for DCM at light load. The solution of the buck converter operating in DCM is

$$V = \frac{n_3}{n_1} V_g \frac{2}{\sqrt{1 + \frac{4K}{D^2}}}$$

with $K = 2 L / R T_s$, and $R = V^2 / P_{load}$

These equations apply equally well to the forward converter, provided that all quantities are referred to the transformer secondary side.

Solve for D:

$$D = \frac{2\sqrt{K}}{\sqrt{\left(\frac{2n_3 V_g}{n_1 V} - 1\right)^2 - 1}} \quad \textit{in DCM}$$

$$D = \frac{n_1}{n_3} \frac{V}{V_g} \quad \textit{in CCM}$$

at a given operating point, the actual duty cycle is the small of the values calculated by the CCM and DCM equations above. Minimum D occurs at minimum P_{load} and maximum V_g.

More regarding forward converter example

Worst-case component stresses can now be evaluated.

Peak transistor voltage is

$$\max\left(v_{Q1}\right) = V_g\left(1 + \frac{n_1}{n_2}\right)$$

RMS transistor current is

$$I_{Q1,rms} = \frac{n_3}{n_1}\sqrt{D}\sqrt{I^2 + \frac{\left(\Delta i\right)^2}{3}} \approx \frac{n_3}{n_1}\sqrt{D}\, I$$

(this neglects transformer magnetizing current)

Other component stresses can be found in a similar manner.
Magnetics design is left for a later chapter.

Results: forward and flyback converter spreadsheets

Forward converter design, CCM		***Flyback converter design, CCM***	
Design variables		*Design variables*	
Reset winding turns ratio n_2/n_1	1	Turns ratio n_2/n_1	0.125
Turns ratio n_3/n_1	0.125	Inductor current ripple Δi	3 A ref to sec
Inductor current ripple Δi	2 A ref to sec		
Results		*Results*	
Maximum duty cycle D	0.462	Maximum duty cycle D	0.316
Minimum D, at full load	0.308	Minimum D, at full load	0.235
Minimum D, at minimum load	0.251	Minimum D, at minimum load	0.179
Worst-case stresses		*Worst-case stresses*	
Peak transistor voltage v_{Q1}	780 V	Peak transistor voltage v_{Q1}	510 V
Rms transistor current i_{Q1}	1.13 A	Rms transistor current i_{Q1}	1.38 A
Transistor utilization U	0.226	Transistor utilization U	0.284
Peak diode voltage v_{D2}	49 V	Peak diode voltage v_{D1}	64 V
Rms diode current i_{D2}	9.1 A	Rms diode current i_{D1}	16.3 A
Peak diode voltage v_{D3}	49 V	Peak diode current i_{D1}	22.2 A
Rms diode current i_{D3}	11.1 A		
Rms output capacitor current i_C	1.15 A	Rms output capacitor current i_C	9.1 A

Discussion: transistor voltage

Flyback converter

Ideal peak transistor voltage: 510V

Actual peak voltage will be higher, due to ringing causes by transformer leakage inductance

An 800V or 1000V MOSFET would have an adequate design margin

Forward converter

Ideal peak transistor voltage: 780V, 53% greater than flyback

Few MOSFETs having voltage rating of over 1000 V are available —when ringing due to transformer leakage inductance is accounted for, this design will have an inadequate design margin

Fix: use two-transistor forward converter, or change reset winding turns ratio

A conclusion: reset mechanism of flyback is superior to forward

Discussion: rms transistor current

Forward

1.13A worst-case

transistor utilization 0.226

Flyback

1.38A worst case, 22% higher than forward

transistor utilization 0.284

CCM flyback exhibits higher peak and rms currents. Currents in DCM flyback are even higher

Discussion: secondary-side diode and capacitor stresses

Forward

peak diode voltage 49V

rms diode current 9.1A / 11.1A

rms capacitor current 1.15A

Flyback

peak diode voltage 64V

rms diode current 16.3A

peak diode current 22.2A

rms capacitor current 9.1A

Secondary-side currents, especially capacitor currents, limit the practical application of the flyback converter to situations where the load current is not too great.

Summary of key points

1. The boost converter can be viewed as an inverse buck converter, while the buck-boost and Cuk converters arise from cascade connections of buck and boost converters. The properties of these converters are consistent with their origins. Ac outputs can be obtained by differential connection of the load. An infinite number of converters are possible, and several are listed in this chapter.

2. For understanding the operation of most converters containing transformers, the transformer can be modeled as a magnetizing inductance in parallel with an ideal transformer. The magnetizing inductance must obey all of the usual rules for inductors, including the principle of volt-second balance.

Summary of key points

3. The steady-state behavior of transformer-isolated converters may be understood by first replacing the transformer with the magnetizing-inductance-plus-ideal-transformer equivalent circuit. The techniques developed in the previous chapters can then be applied, including use of inductor volt-second balance and capacitor charge balance to find dc currents and voltages, use of equivalent circuits to model losses and efficiency, and analysis of the discontinuous conduction mode.

4. In the full-bridge, half-bridge, and push-pull isolated versions of the buck and/or boost converters, the transformer frequency is twice the output ripple frequency. The transformer is reset while it transfers energy: the applied voltage polarity alternates on successive switching periods.

Summary of key points

5. In the conventional forward converter, the transformer is reset while the transistor is off. The transformer magnetizing inductance operates in the discontinuous conduction mode, and the maximum duty cycle is limited.
6. The flyback converter is based on the buck-boost converter. The flyback transformer is actually a two-winding inductor, which stores and transfers energy.
7. The transformer turns ratio is an extra degree-of-freedom which the designer can choose to optimize the converter design. Use of a computer spreadsheet is an effective way to determine how the choice of turns ratio affects the component voltage and current stresses.
8. Total active switch stress, and active switch utilization, are two simplified figures-of-merit which can be used to compare the various converter circuits.

Part II
Converter Dynamics and Control

7. AC equivalent circuit modeling
8. Converter transfer functions
9. Controller design
10. Ac and dc equivalent circuit modeling of the discontinuous conduction mode
11. Current programmed control

Chapter 7. AC Equivalent Circuit Modeling

7.1. Introduction

Objective: maintain $v(t)$ equal to an accurate, constant value V.

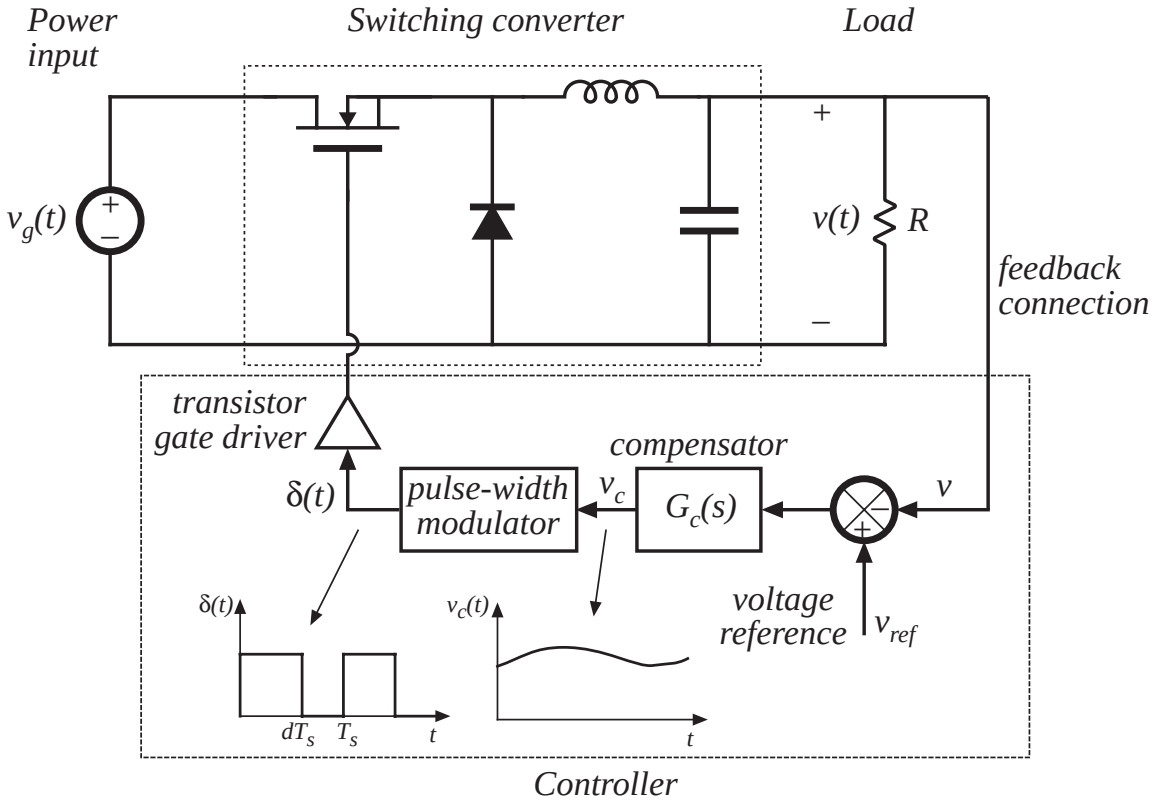
There are disturbances:

- in $v_g(t)$
- in R

There are uncertainties:

- in element values
- in V_g
- in R

A simple dc-dc regulator system, employing a buck converter



Applications of control in power electronics

Dc-dc converters

Regulate dc output voltage.

Control the duty cycle $d(t)$ such that $v(t)$ accurately follows a reference signal v_{ref}.

Dc-ac inverters

Regulate an ac output voltage.

Control the duty cycle $d(t)$ such that $v(t)$ accurately follows a reference signal $v_{ref}(t)$.

Ac-dc rectifiers

Regulate the dc output voltage.

Regulate the ac input current waveform.

Control the duty cycle $d(t)$ such that $i_g(t)$ accurately follows a reference signal $i_{ref}(t)$, and $v(t)$ accurately follows a reference signal v_{ref}.

Objective of Part II

Develop tools for modeling, analysis, and design of converter control systems

Need dynamic models of converters:

How do ac variations in $v_g(t)$, R, or $d(t)$ affect the output voltage $v(t)$?

What are the small-signal transfer functions of the converter?

- Extend the steady-state converter models of Chapters 2 and 3, to include CCM converter dynamics (Chapter 7)
- Construct converter small-signal transfer functions (Chapter 8)
- Design converter control systems (Chapter 9)
- Model converters operating in DCM (Chapter 10)
- Current-programmed control of converters (Chapter 11)

Modeling

- Representation of physical behavior by mathematical means
- Model dominant behavior of system, ignore other insignificant phenomena
- Simplified model yields physical insight, allowing engineer to design system to operate in specified manner
- Approximations neglect small but complicating phenomena
- After basic insight has been gained, model can be refined (if it is judged worthwhile to expend the engineering effort to do so), to account for some of the previously neglected phenomena

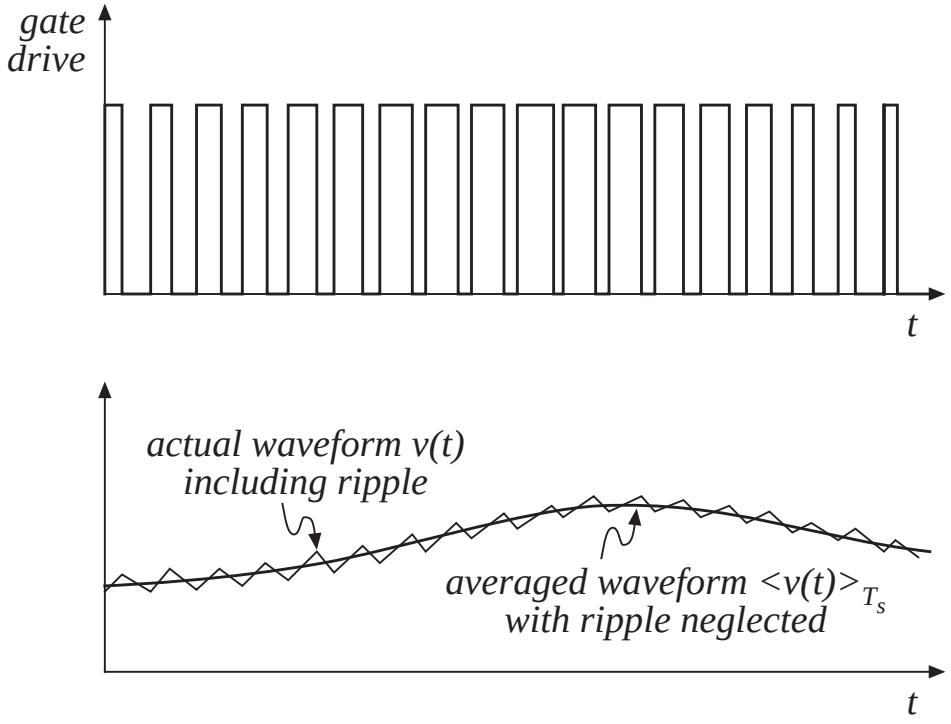
Neglecting the switching ripple

Suppose the duty cycle is modulated sinusoidally:

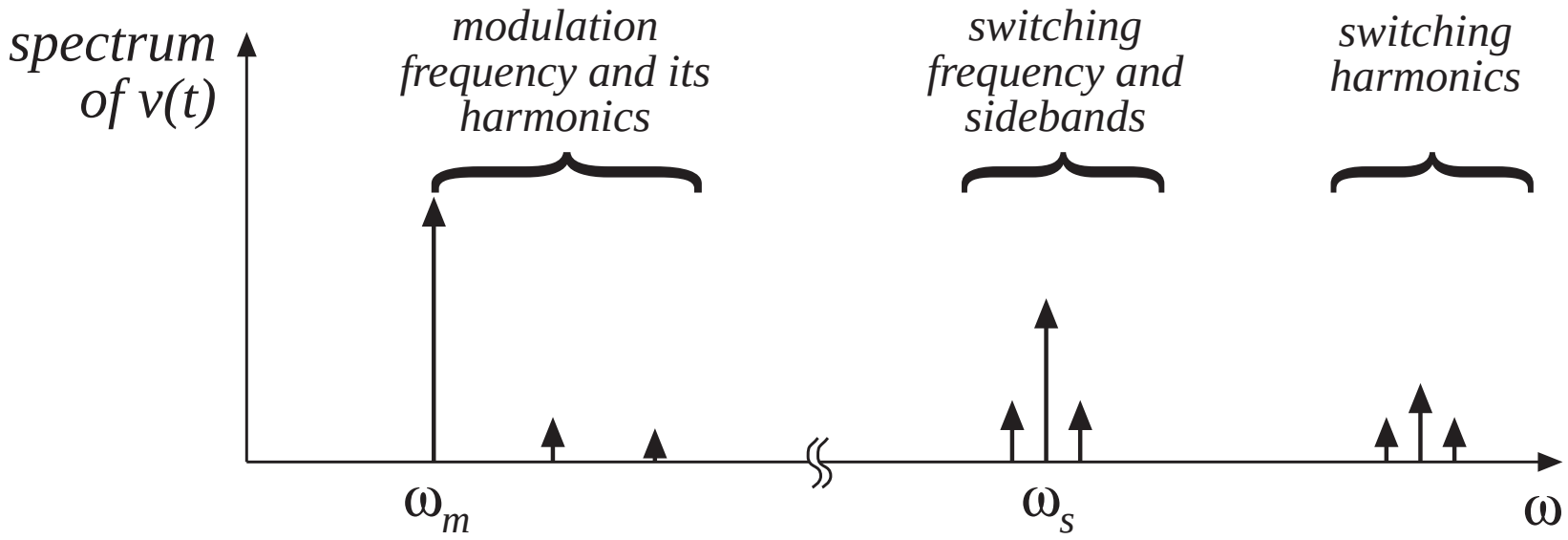
$$d(t) = D + D_m \cos \omega_m t$$

where D and D_m are constants, $| D_m | << D$, and the modulation frequency ω_m is much smaller than the converter switching frequency $\omega_s = 2\pi f_s$.

The resulting variations in transistor gate drive signal and converter output voltage:



Output voltage spectrum
with sinusoidal modulation of duty cycle



Contains frequency components at:

- Modulation frequency and its harmonics
- Switching frequency and its harmonics
- Sidebands of switching frequency

With small switching ripple, high-frequency components (switching harmonics and sidebands) are small.

If ripple is neglected, then only low-frequency components (modulation frequency and harmonics) remain.

Objective of ac converter modeling

- Predict how low-frequency variations in duty cycle induce low-frequency variations in the converter voltages and currents
- Ignore the switching ripple
- Ignore complicated switching harmonics and sidebands

Approach:

- Remove switching harmonics by averaging all waveforms over one switching period

Averaging to remove switching ripple

Average over one switching period to remove switching ripple:

$$L \frac{d\left\langle i_L(t)\right\rangle_{T_s}}{dt} = \left\langle v_L(t)\right\rangle_{T_s}$$

$$C \frac{d\left\langle v_C(t)\right\rangle_{T_s}}{dt} = \left\langle i_C(t)\right\rangle_{T_s}$$

where

$$\left\langle x_L(t)\right\rangle_{T_s} = \frac{1}{T_s}\int_t^{t+T_s} x(\tau)\, d\tau$$

Note that, in steady-state,

$$\left\langle v_L(t)\right\rangle_{T_s} = 0$$

$$\left\langle i_C(t)\right\rangle_{T_s} = 0$$

by inductor volt-second balance and capacitor charge balance.

Nonlinear averaged equations

The averaged voltages and currents are, in general, nonlinear functions of the converter duty cycle, voltages, and currents. Hence, the averaged equations

$$L \frac{d\left\langle i_L(t) \right\rangle_{T_s}}{dt} = \left\langle v_L(t) \right\rangle_{T_s}$$

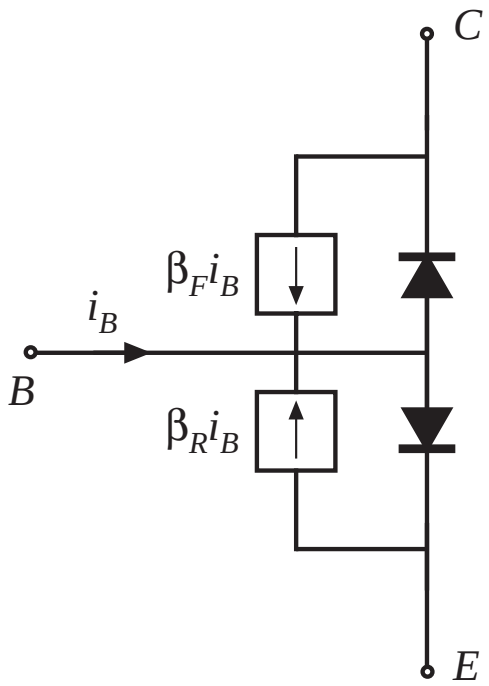
$$C \frac{d\left\langle v_C(t) \right\rangle_{T_s}}{dt} = \left\langle i_C(t) \right\rangle_{T_s}$$

constitute a system of nonlinear differential equations.

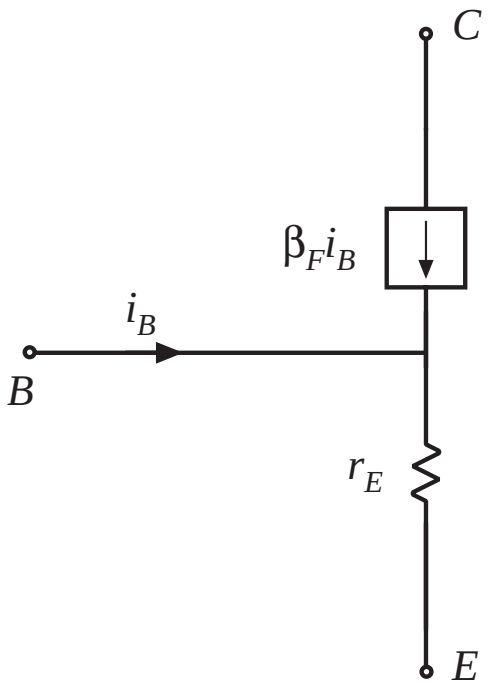
Hence, must linearize by constructing a small-signal converter model.

Small-signal modeling of the BJT

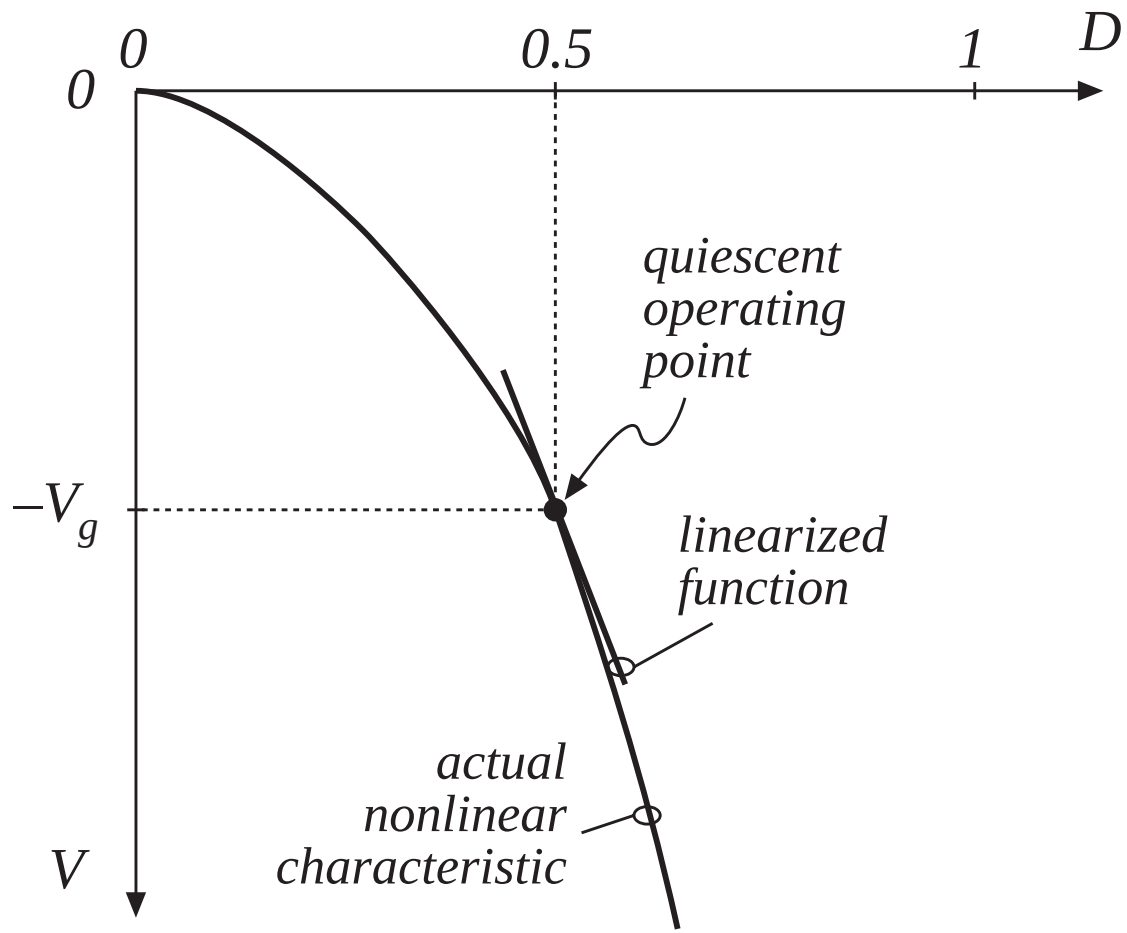
Nonlinear Ebers-Moll model



Linearized small-signal model, active region



Buck-boost converter: nonlinear static control-to-output characteristic

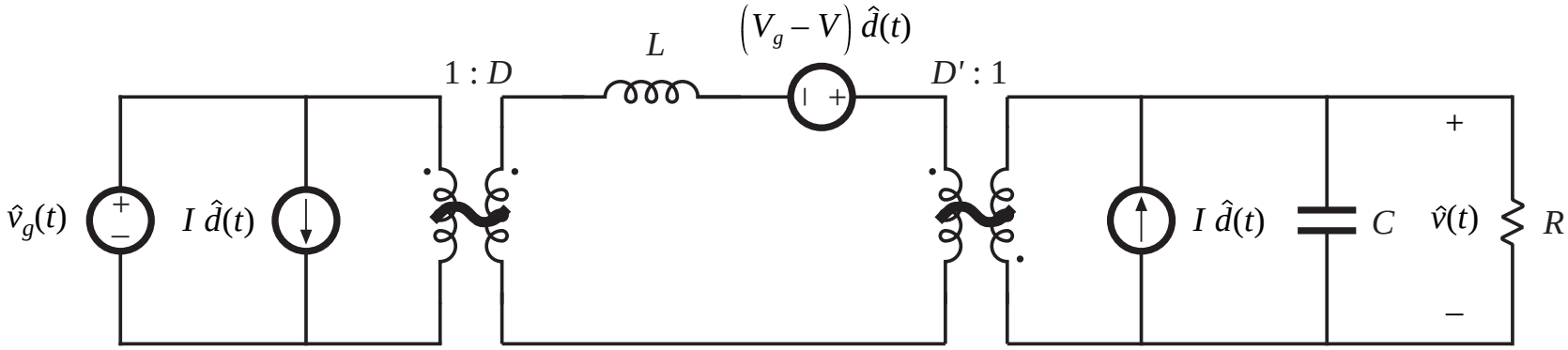


Example: linearization at the quiescent operating point

$D = 0.5$

Result of averaged small-signal ac modeling

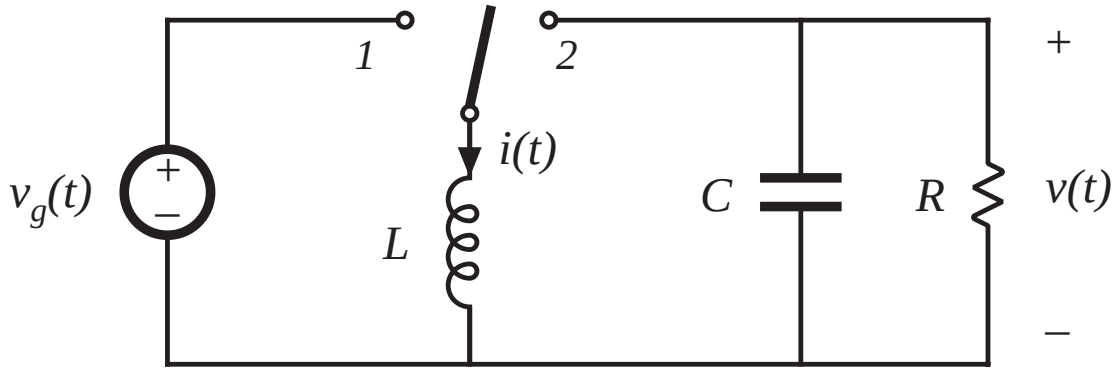
Small-signal ac equivalent circuit model



buck-boost example

7.2. The basic ac modeling approach

Buck-boost converter example

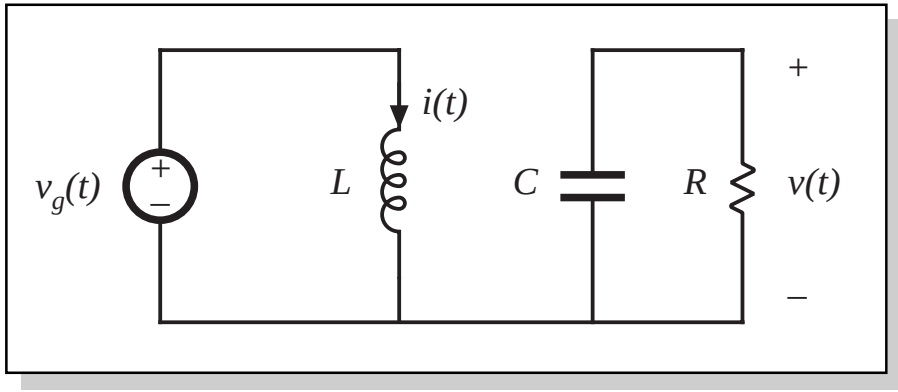


Switch in position 1

Inductor voltage and capacitor current are:

$$v_L(t) = L\,\frac{di(t)}{dt} = v_g(t)$$

$$i_C(t) = C\,\frac{dv(t)}{dt} = -\,\frac{v(t)}{R}$$



Small ripple approximation: replace waveforms with their low-frequency averaged values:

$$v_L(t) = L\,\frac{di(t)}{dt} \approx \left\langle v_g(t) \right\rangle_{T_s}$$

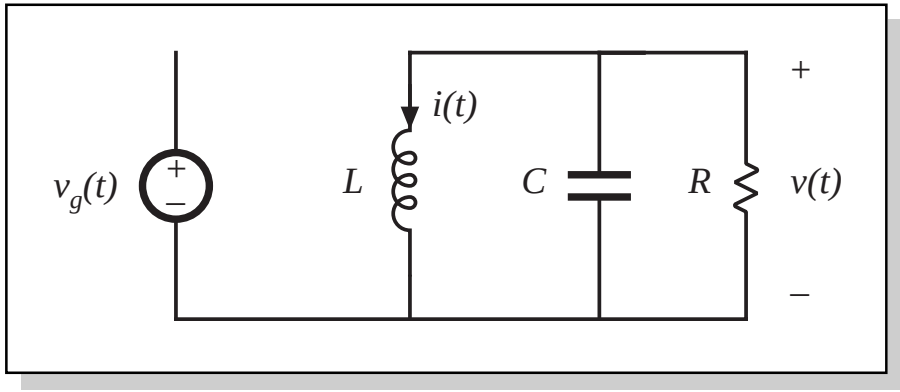
$$i_C(t) = C\,\frac{dv(t)}{dt} \approx -\,\frac{\left\langle v(t) \right\rangle_{T_s}}{R}$$

Switch in position 2

Inductor voltage and capacitor current are:

$$v_L(t) = L\,\frac{d\,i(t)}{d\,t} = v(t)$$

$$i_C(t) = C\,\frac{d\,v(t)}{d\,t} = -\,i(t) - \frac{v(t)}{R}$$



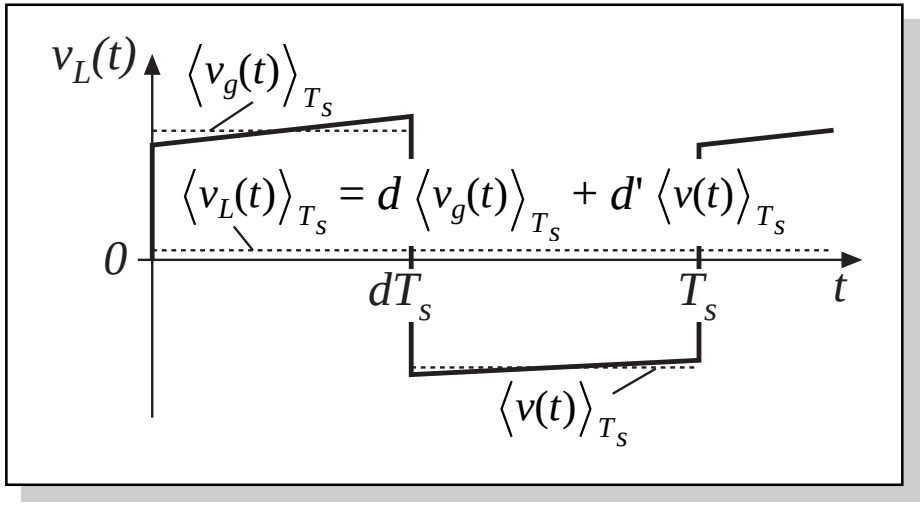
Small ripple approximation: replace waveforms with their low-frequency averaged values:

$$v_L(t) = L\,\frac{d\,i(t)}{d\,t} \approx \left\langle v(t) \right\rangle_{T_s}$$

$$i_C(t) = C\,\frac{d\,v(t)}{d\,t} \approx -\left\langle i(t) \right\rangle_{T_s} - \frac{\left\langle v(t) \right\rangle_{T_s}}{R}$$

7.2.1 Averaging the inductor waveforms

Inductor voltage waveform



Low-frequency average is found by evaluation of

$$\left\langle x_L(t) \right\rangle_{T_s} = \frac{1}{T_s} \int_t^{t+T_s} x(\tau) d\tau$$

Average the inductor voltage in this manner:

$$\left\langle v_L(t) \right\rangle_{T_s} = \frac{1}{T_s} \int_t^{t+T_s} v_L(\tau) d\tau \approx d(t) \left\langle v_g(t) \right\rangle_{T_s} + d'(t) \left\langle v(t) \right\rangle_{T_s}$$

Insert into Eq. (7.2):

$$L \frac{d\left\langle i(t) \right\rangle_{T_s}}{dt} = d(t) \left\langle v_g(t) \right\rangle_{T_s} + d'(t) \left\langle v(t) \right\rangle_{T_s}$$

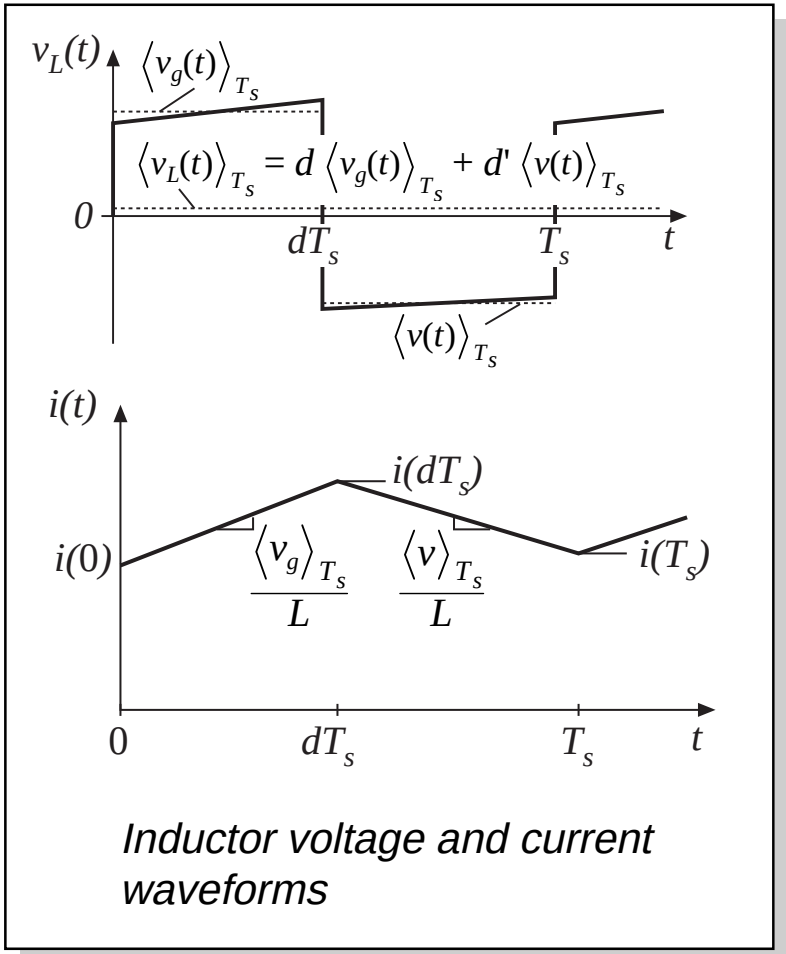
This equation describes how the low-frequency components of the inductor waveforms evolve in time.

7.2.2 Discussion of the averaging approximation

Use of the average inductor voltage allows us to determine the net change in inductor current over one switching period, while neglecting the switching ripple.

In steady-state, the average inductor voltage is zero (volt-second balance), and hence the inductor current waveform is periodic: $i(t + T_s) = i(t)$. There is no net change in inductor current over one switching period.

During transients or ac variations, the average inductor voltage is not zero in general, and this leads to net variations in inductor current.



Inductor voltage and current waveforms

Net change in inductor current is correctly predicted by the average inductor voltage

Inductor equation:

$$L \frac{di(t)}{dt} = v_L(t)$$

Divide by L and integrate over one switching period:

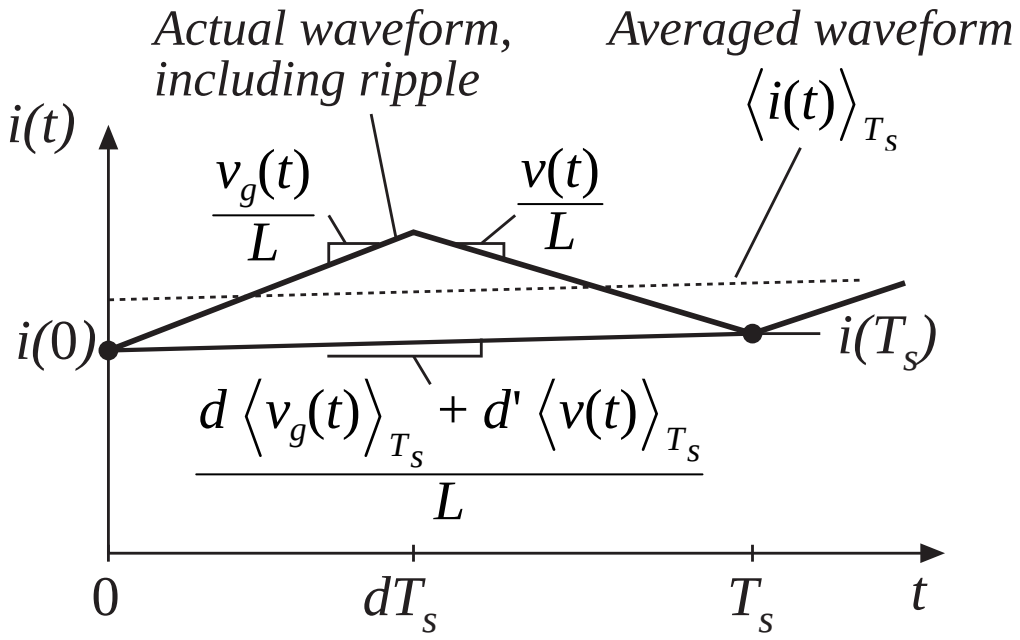
$$\int_t^{t+T_s} di = \frac{1}{L} \int_t^{t+T_s} v_L(\tau) d\tau$$

Left-hand side is the change in inductor current. Right-hand side can be related to average inductor voltage by multiplying and dividing by T_s as follows:

$$i(t + T_s) - i(t) = \frac{1}{L} T_s \left\langle v_L(t) \right\rangle_{T_s}$$

So the net change in inductor current over one switching period is exactly equal to the period T_s multiplied by the average slope $\langle v_L \rangle_{T_s} / L$.

Average inductor voltage correctly predicts average slope of $i_L(t)$



The net change in inductor current over one switching period is exactly equal to the period T_s multiplied by the average slope $\langle v_L \rangle_{T_s} / L$.

$$\frac{d\left\langle i(t)\right\rangle_{T_s}}{dt}$$

We have

$$i(t+T_s) - i(t) = \frac{1}{L}\, T_s \left\langle v_L(t)\right\rangle_{T_s}$$

Rearrange:

$$L\,\frac{i(t+T_s) - i(t)}{T_s} = \left\langle v_L(t)\right\rangle_{T_s}$$

Define the derivative of $\langle\, i \,\rangle_{T_s}$ as (Euler formula):

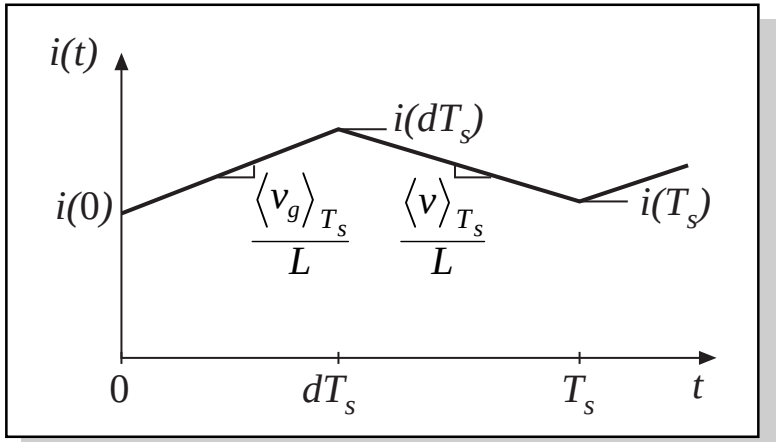
$$\frac{d\left\langle i(t)\right\rangle_{T_s}}{dt} = \frac{i(t+T_s) - i(t)}{T_s}$$

Hence,

$$L\,\frac{d\left\langle i(t)\right\rangle_{T_s}}{dt} = \left\langle v_L(t)\right\rangle_{T_s}$$

Computing how the inductor current changes over one switching period

Let's compute the actual inductor current waveform, using the linear ripple approximation.



With switch in position 1:

$$\underbrace{i(dT_s)}_{\text{final value}} = \underbrace{i(0)}_{\text{initial value}} + \underbrace{\left(dT_s\right)}_{\text{length of interval}} \underbrace{\left(\frac{\left\langle v_g(t)\right\rangle_{T_s}}{L}\right)}_{\text{average slope}}$$

(final value) = (initial value) + (length of interval) (average slope)

With switch in position 2:

$$\underbrace{i(T_s)}_{\text{final value}} = \underbrace{i(dT_s)}_{\text{initial value}} + \underbrace{\left(d'T_s\right)}_{\text{length of interval}} \underbrace{\left(\frac{\left\langle v(t)\right\rangle_{T_s}}{L}\right)}_{\text{average slope}}$$

(final value) = (initial value) + (length of interval) (average slope)

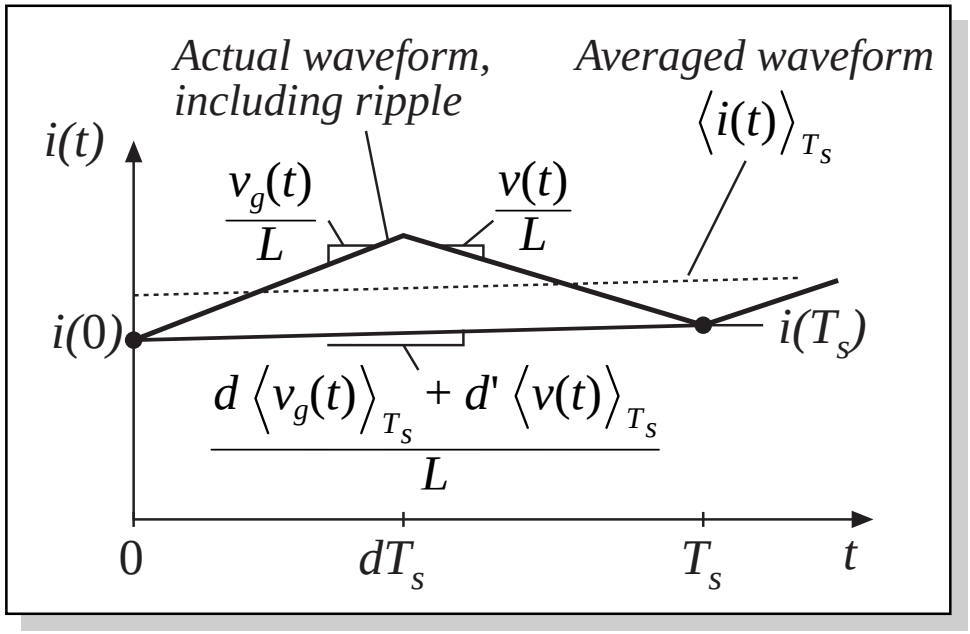
Net change in inductor current over one switching period

Eliminate $i(dT_s)$, to express $i(T_s)$ directly as a function of $i(0)$:

$$i(T_s) = i(0) + \frac{T_s}{L} \underbrace{\left(d(t) \left\langle v_g(t) \right\rangle_{T_s} + d'(t) \left\langle v(t) \right\rangle_{T_s} \right)}_{\left\langle v_L(t) \right\rangle_{T_s}}$$

The intermediate step of computing $i(dT_s)$ is eliminated.

The final value $i(T_s)$ is equal to the initial value $i(0)$, plus the switching period Ts multiplied by the average slope $\langle v_L \rangle_{T_s} / L$.



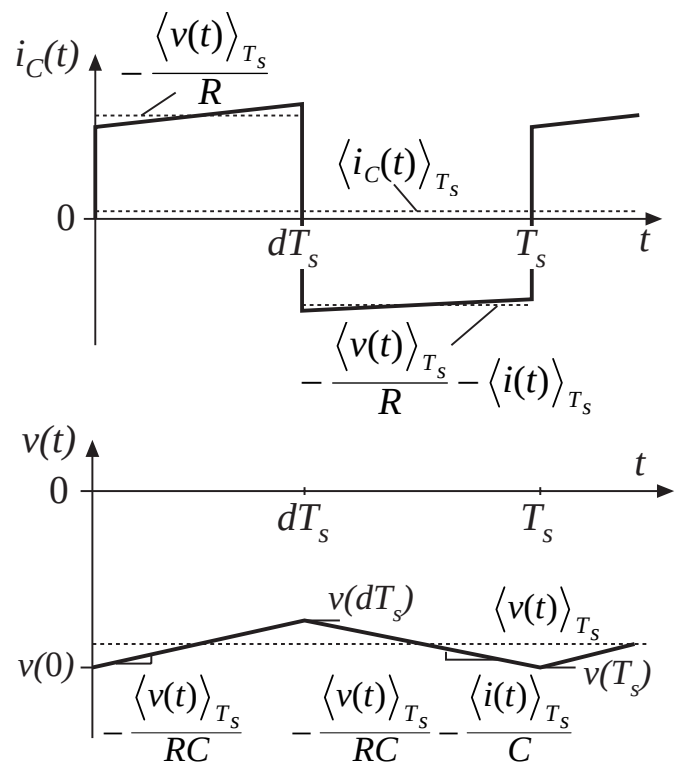
7.2.3 Averaging the capacitor waveforms

Average capacitor current:

$$\left\langle i_C(t) \right\rangle_{T_s} = d(t) \left(- \frac{\left\langle v(t) \right\rangle_{T_s}}{R} \right) + d'(t) \left(- \left\langle i(t) \right\rangle_{T_s} - \frac{\left\langle v(t) \right\rangle_{T_s}}{R} \right)$$

Collect terms, and equate to $C\, d\langle v \rangle_{T_s} / dt$:

$$C \frac{d \left\langle v(t) \right\rangle_{T_s}}{dt} = - d'(t) \left\langle i(t) \right\rangle_{T_s} - \frac{\left\langle v(t) \right\rangle_{T_s}}{R}$$



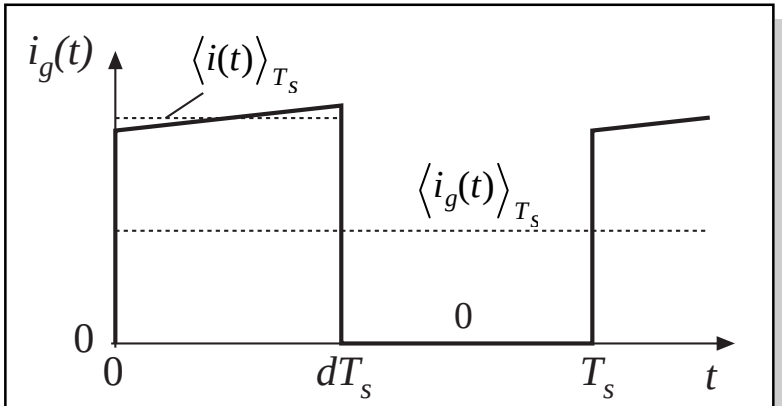
Capacitor voltage and current waveforms

7.2.4 The average input current

We found in Chapter 3 that it was sometimes necessary to write an equation for the average converter input current, to derive a complete dc equivalent circuit model. It is likewise necessary to do this for the ac model.

Buck-boost input current waveform is

$$i_g(t) = \begin{cases} \left\langle i(t) \right\rangle_{T_s} & \text{during subinterval 1} \\ 0 & \text{during subinterval 2} \end{cases}$$



Converter input current waveform

Average value:

$$\left\langle i_g(t) \right\rangle_{T_s} = d(t) \left\langle i(t) \right\rangle_{T_s}$$

7.2.5. Perturbation and linearization

Converter averaged equations:

$$L \frac{d\left\langle i(t)\right\rangle_{T_s}}{dt} = d(t) \left\langle v_g(t)\right\rangle_{T_s} + d'(t) \left\langle v(t)\right\rangle_{T_s}$$

$$C \frac{d\left\langle v(t)\right\rangle_{T_s}}{dt} = - d'(t) \left\langle i(t)\right\rangle_{T_s} - \frac{\left\langle v(t)\right\rangle_{T_s}}{R}$$

$$\left\langle i_g(t)\right\rangle_{T_s} = d(t) \left\langle i(t)\right\rangle_{T_s}$$

—nonlinear because of multiplication of the time-varying quantity *d(t)* with other time-varying quantities such as *i(t)* and *v(t)*.

Construct small-signal model: Linearize about quiescent operating point

If the converter is driven with some steady-state, or quiescent, inputs

$$d(t) = D$$
$$\left\langle v_g(t) \right\rangle_{T_s} = V_g$$

then, from the analysis of Chapter 2, after transients have subsided the inductor current, capacitor voltage, and input current

$$\left\langle i(t) \right\rangle_{T_s}, \left\langle v(t) \right\rangle_{T_s}, \left\langle i_g(t) \right\rangle_{T_s}$$

reach the quiescent values I, V, and I_g, given by the steady-state analysis as

$$V = -\frac{D}{D'} V_g$$
$$I = -\frac{V}{D' R}$$
$$I_g = D I$$

Perturbation

So let us assume that the input voltage and duty cycle are equal to some given (dc) quiescent values, plus superimposed small ac variations:

$$\left\langle v_g(t) \right\rangle_{T_s} = V_g + \hat{v}_g(t)$$
$$d(t) = D + \hat{d}(t)$$

In response, and after any transients have subsided, the converter dependent voltages and currents will be equal to the corresponding quiescent values, plus small ac variations:

$$\left\langle i(t) \right\rangle_{T_s} = I + \hat{i}(t)$$
$$\left\langle v(t) \right\rangle_{T_s} = V + \hat{v}(t)$$
$$\left\langle i_g(t) \right\rangle_{T_s} = I_g + \hat{i}_g(t)$$

The small-signal assumption

If the ac variations are much smaller in magnitude than the respective quiescent values,

$$\left| \hat{v}_g(t) \right| << \left| V_g \right|$$
$$\left| \hat{d}(t) \right| << \left| D \right|$$
$$\left| \hat{i}(t) \right| << \left| I \right|$$
$$\left| \hat{v}(t) \right| << \left| V \right|$$
$$\left| \hat{i}_g(t) \right| << \left| I_g \right|$$

then the nonlinear converter equations can be linearized.

Perturbation of inductor equation

Insert the perturbed expressions into the inductor differential equation:

$$L \frac{d\left(I + \hat{i}(t)\right)}{dt} = \left(D + \hat{d}(t)\right)\left(V_g + \hat{v}_g(t)\right) + \left(D' - \hat{d}(t)\right)\left(V + \hat{v}(t)\right)$$

note that *d'(t)* is given by

$$d'(t) = \left(1 - d(t)\right) = 1 - \left(D + \hat{d}(t)\right) = D' - \hat{d}(t)$$

with $D' = 1 - D$

Multiply out and collect terms:

$$L\left(\cancel{\frac{dI}{dt}}^{0} + \frac{d\,\hat{i}(t)}{dt}\right) = \underbrace{\left(DV_g + D'V\right)}_{\text{Dc terms}} + \underbrace{\left(D\hat{v}_g(t) + D'\hat{v}(t) + \left(V_g - V\right)\hat{d}(t)\right)}_{1^{st}\text{ order ac terms (linear)}} + \underbrace{\hat{d}(t)\left(\hat{v}_g(t) - \hat{v}(t)\right)}_{2^{nd}\text{ order ac terms (nonlinear)}}$$

The perturbed inductor equation

$$L\left(\frac{dI}{dt}^{0} + \frac{d\,\hat{i}(t)}{dt}\right) = \underbrace{\left(DV_g + D'V\right)}_{\text{Dc terms}} + \underbrace{\left(D\hat{v}_g(t) + D'\hat{v}(t) + \left(V_g - V\right)\hat{d}(t)\right)}_{1^{st}\text{ order ac terms (linear)}} + \underbrace{\hat{d}(t)\left(\hat{v}_g(t) - \hat{v}(t)\right)}_{2^{nd}\text{ order ac terms (nonlinear)}}$$

Since I is a constant (dc) term, its derivative is zero

The right-hand side contains three types of terms:

- Dc terms, containing only dc quantities
- First-order ac terms, containing a single ac quantity, usually multiplied by a constant coefficient such as a dc term. These are linear functions of the ac variations
- Second-order ac terms, containing products of ac quantities. These are nonlinear, because they involve multiplication of ac quantities

Neglect of second-order terms

$$L\left(\frac{dI}{dt}^{0} + \frac{d\,\hat{i}(t)}{dt}\right) = \underbrace{\left(DV_g + D'V\right)}_{\text{Dc terms}} + \underbrace{\left(D\hat{v}_g(t) + D'\hat{v}(t) + \left(V_g - V\right)\hat{d}(t)\right)}_{1^{st}\text{ order ac terms (linear)}} + \underbrace{\hat{d}(t)\left(\hat{v}_g(t) - \hat{v}(t)\right)}_{2^{nd}\text{ order ac terms (nonlinear)}}$$

Provided

$$\left|\hat{v}_g(t)\right| << \left|V_g\right|$$
$$\left|\hat{d}(t)\right| << \left|D\right|$$
$$\left|\hat{i}(t)\right| << \left|I\right|$$
$$\left|\hat{v}(t)\right| << \left|V\right|$$
$$\left|\hat{i}_g(t)\right| << \left|I_g\right|$$

then the second-order ac terms are much smaller than the first-order terms. For example,

$\left|\hat{d}(t)\,\hat{v}_g(t)\right| << \left|D\,\hat{v}_g(t)\right|$ when $\left|\hat{d}(t)\right| << D$

So neglect second-order terms.
Also, dc terms on each side of equation are equal.

Linearized inductor equation

Upon discarding second-order terms, and removing dc terms (which add to zero), we are left with

$$L \frac{d\hat{i}(t)}{dt} = D\hat{v}_g(t) + D'\hat{v}(t) + \left(V_g - V\right)\hat{d}(t)$$

This is the desired result: a linearized equation which describes small-signal ac variations.

Note that the quiescent values D, D', V, V_g, are treated as given constants in the equation.

Capacitor equation

Perturbation leads to

$$C \frac{d\left(V + \hat{v}(t)\right)}{dt} = -\left(D' - \hat{d}(t)\right)\left(I + \hat{i}(t)\right) - \frac{\left(V + \hat{v}(t)\right)}{R}$$

Collect terms:

$$C\left(\frac{dV}{dt}^{0} + \frac{d\hat{v}(t)}{dt}\right) = \underbrace{\left(-D'I - \frac{V}{R}\right)}_{\text{Dc terms}} + \underbrace{\left(-D'\hat{i}(t) - \frac{\hat{v}(t)}{R} + I\hat{d}(t)\right)}_{1^{st}\text{ order ac terms (linear)}} + \underbrace{\hat{d}(t)\hat{i}(t)}_{2^{nd}\text{ order ac term (nonlinear)}}$$

Neglect second-order terms. Dc terms on both sides of equation are equal. The following terms remain:

$$C \frac{d\hat{v}(t)}{dt} = -D'\hat{i}(t) - \frac{\hat{v}(t)}{R} + I\hat{d}(t)$$

This is the desired small-signal linearized capacitor equation.

Average input current

Perturbation leads to

$$I_g + \hat{i}_g(t) = \left(D + \hat{d}(t)\right)\left(I + \hat{i}(t)\right)$$

Collect terms:

$$\underbrace{I_g}_{\text{Dc term}} + \underbrace{\hat{i}_g(t)}_{1^{st}\text{ order ac term}} = \underbrace{\left(DI\right)}_{\text{Dc term}} + \underbrace{\left(D\hat{i}(t) + I\hat{d}(t)\right)}_{1^{st}\text{ order ac terms (linear)}} + \underbrace{\hat{d}(t)\hat{i}(t)}_{2^{nd}\text{ order ac term (nonlinear)}}$$

Neglect second-order terms. Dc terms on both sides of equation are equal. The following first-order terms remain:

$$\hat{i}_g(t) = D\hat{i}(t) + I\hat{d}(t)$$

This is the linearized small-signal equation which described the converter input port.

7.2.6. Construction of small-signal equivalent circuit model

The linearized small-signal converter equations:

$$L \frac{d\hat{i}(t)}{dt} = D\hat{v}_g(t) + D'\hat{v}(t) + \left(V_g - V\right)\hat{d}(t)$$

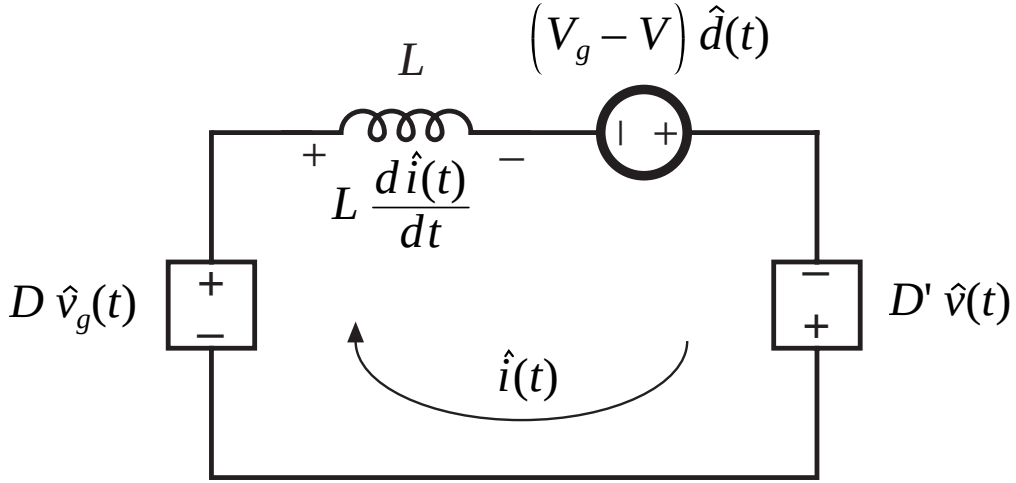
$$C \frac{d\hat{v}(t)}{dt} = -D'\hat{i}(t) - \frac{\hat{v}(t)}{R} + I\hat{d}(t)$$

$$\hat{i}_g(t) = D\hat{i}(t) + I\hat{d}(t)$$

Reconstruct equivalent circuit corresponding to these equations, in manner similar to the process used in Chapter 3.

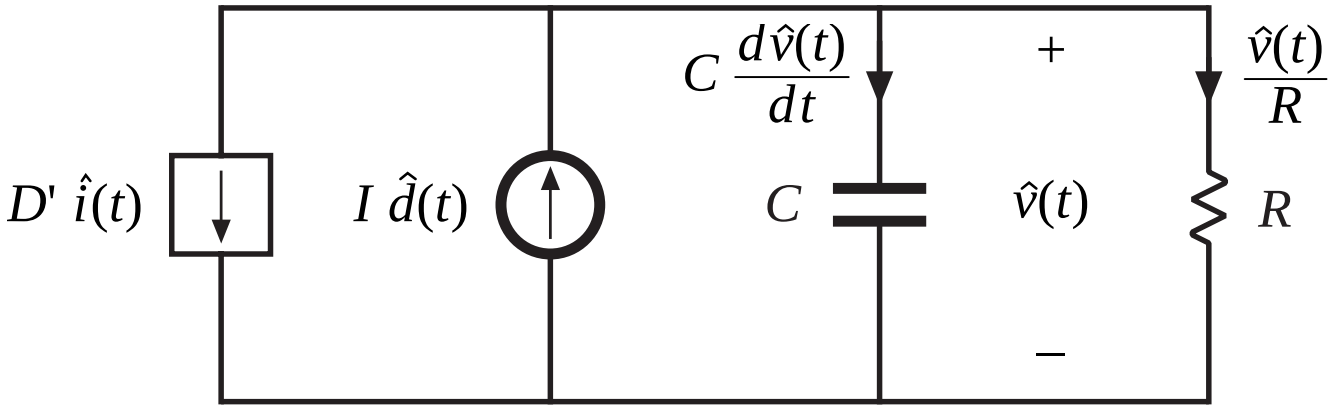
Inductor loop equation

$$L \frac{d\hat{i}(t)}{dt} = D\hat{v}_g(t) + D'\hat{v}(t) + \left(V_g - V\right)\hat{d}(t)$$



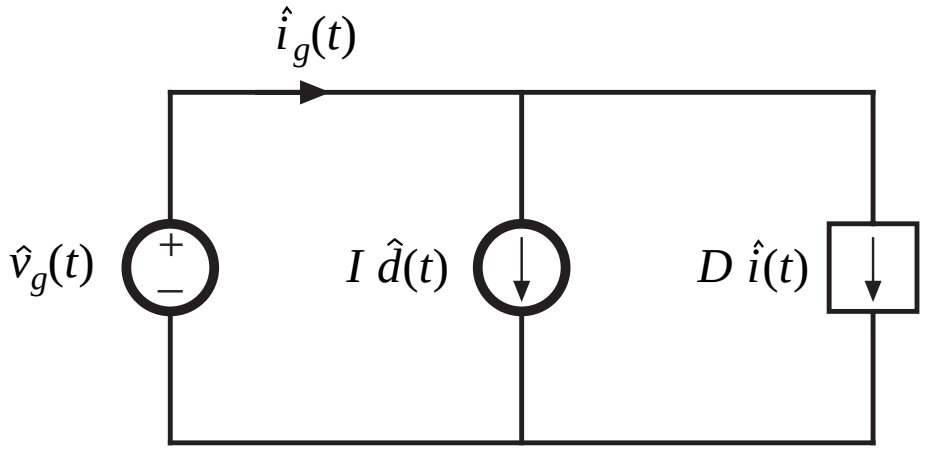
Capacitor node equation

$$C\frac{d\hat{v}(t)}{dt} = -D'\hat{i}(t) - \frac{\hat{v}(t)}{R} + I\hat{d}(t)$$



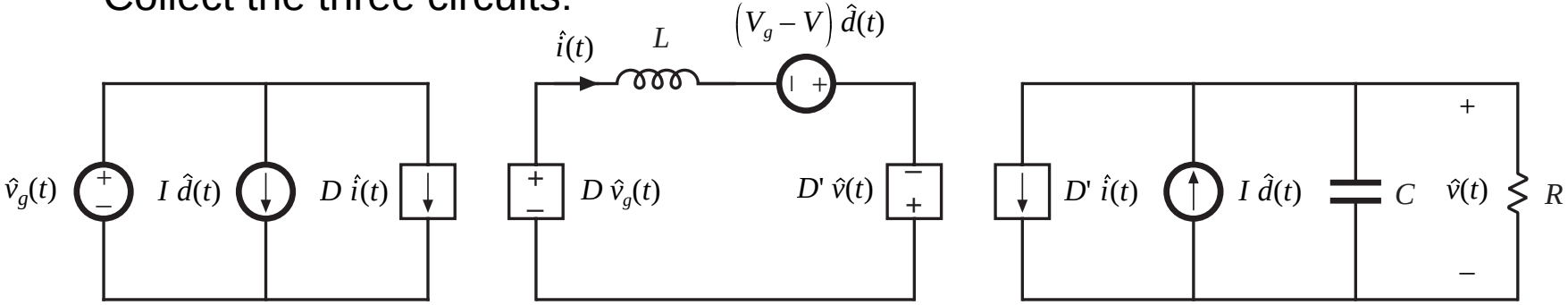
Input port node equation

$$\hat{i}_g(t) = D\hat{i}(t) + I\hat{d}(t)$$

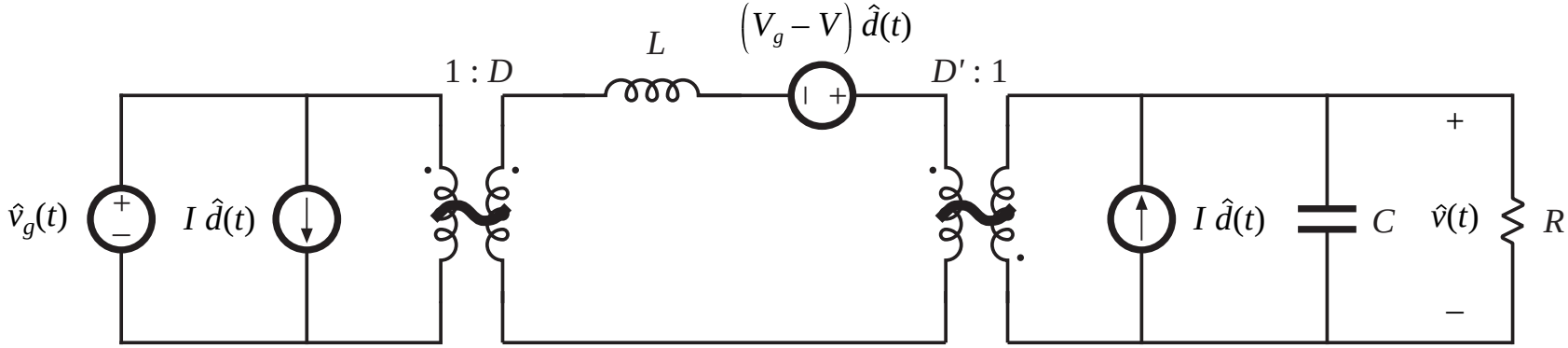


Complete equivalent circuit

Collect the three circuits:



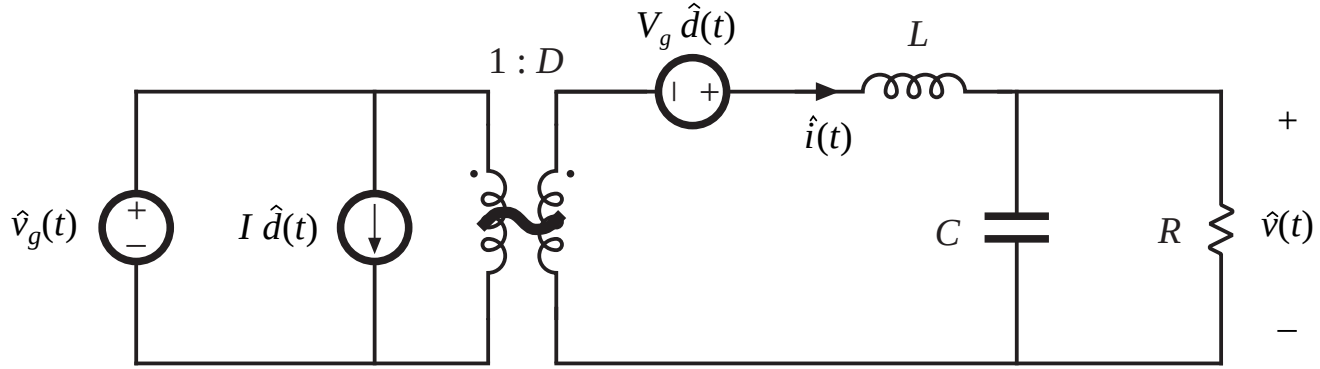
Replace dependent sources with ideal dc transformers:



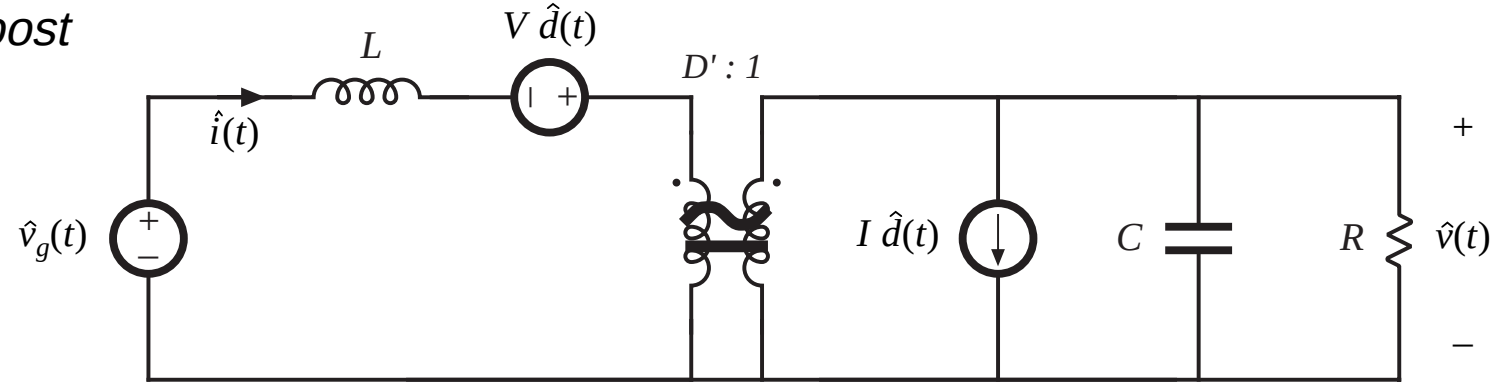
Small-signal ac equivalent circuit model of the buck-boost converter

7.2.7. Results for several basic converters

buck

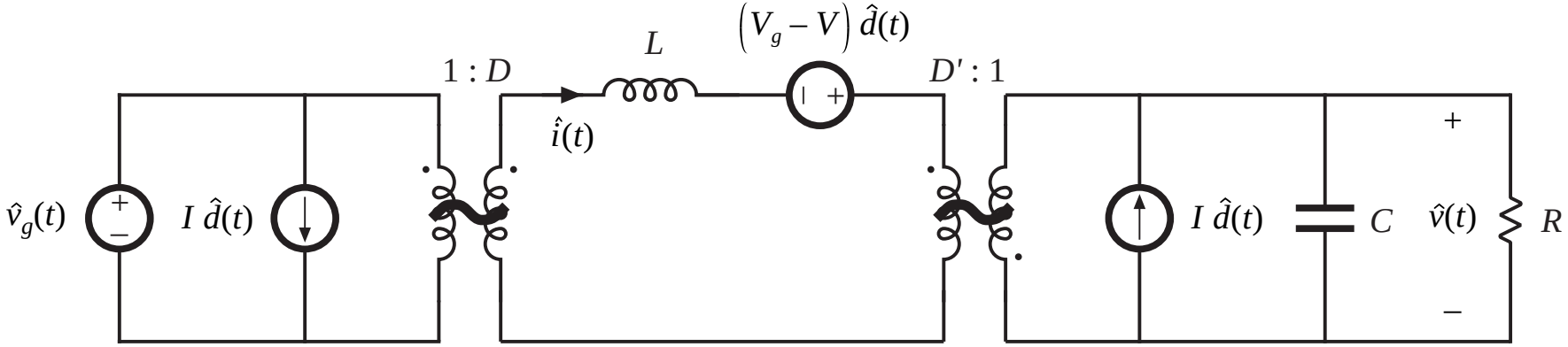


boost



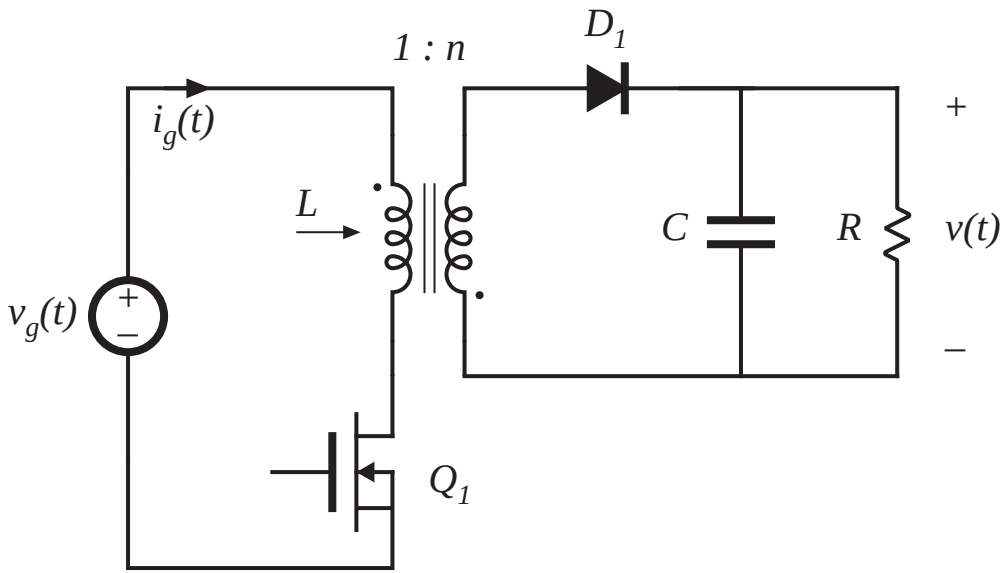
Results for several basic converters

buck-boost



7.3. Example: a nonideal flyback converter

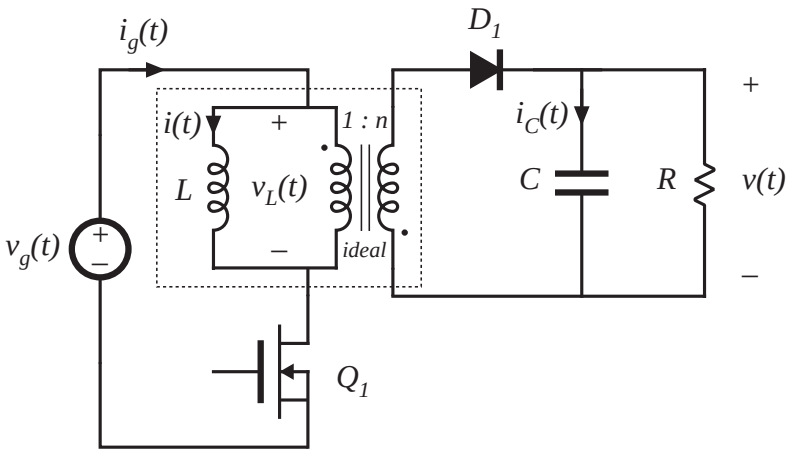
Flyback converter example



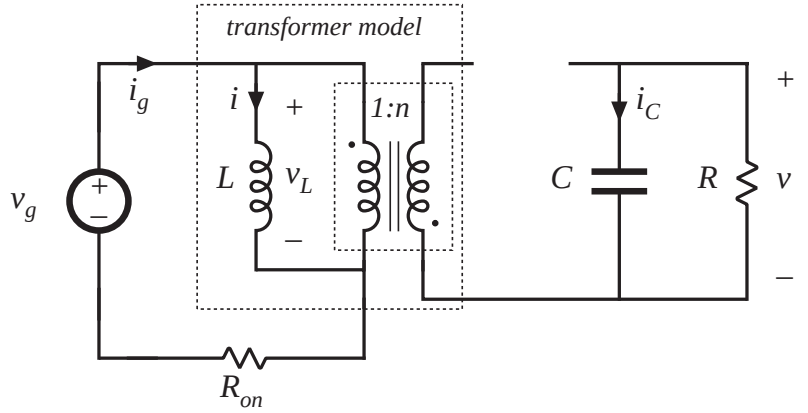
- MOSFET has on-resistance R_{on}
- Flyback transformer has magnetizing inductance L, referred to primary

Circuits during subintervals 1 and 2

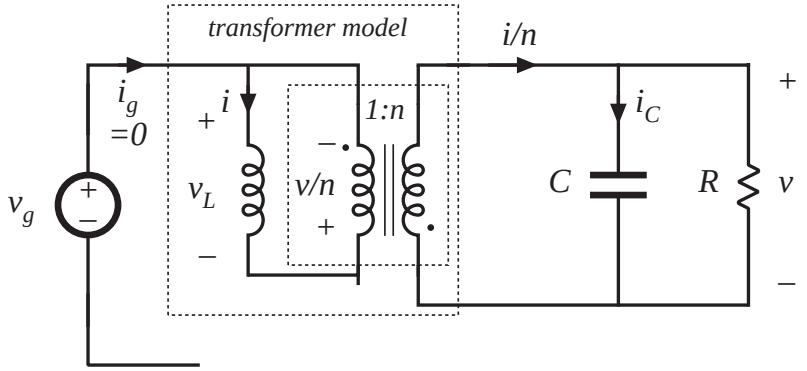
Flyback converter, with transformer equivalent circuit



Subinterval 1



Subinterval 2



Subinterval 1

Circuit equations:

$$v_L(t) = v_g(t) - i(t)\, R_{on}$$

$$i_C(t) = -\frac{v(t)}{R}$$

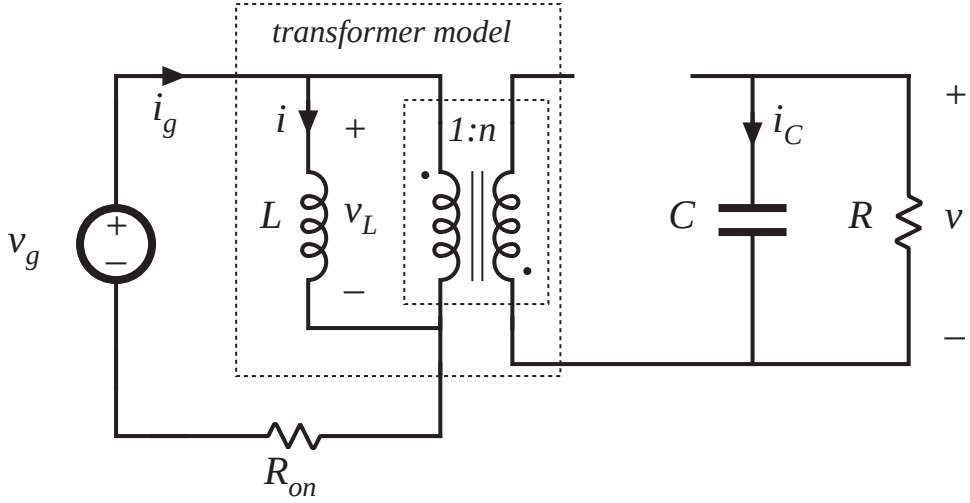
$$i_g(t) = i(t)$$

Small ripple approximation:

$$v_L(t) = \left\langle v_g(t) \right\rangle_{T_s} - \left\langle i(t) \right\rangle_{T_s} R_{on}$$

$$i_C(t) = -\frac{\left\langle v(t) \right\rangle_{T_s}}{R}$$

$$i_g(t) = \left\langle i(t) \right\rangle_{T_s}$$



MOSFET conducts, diode is reverse-biased

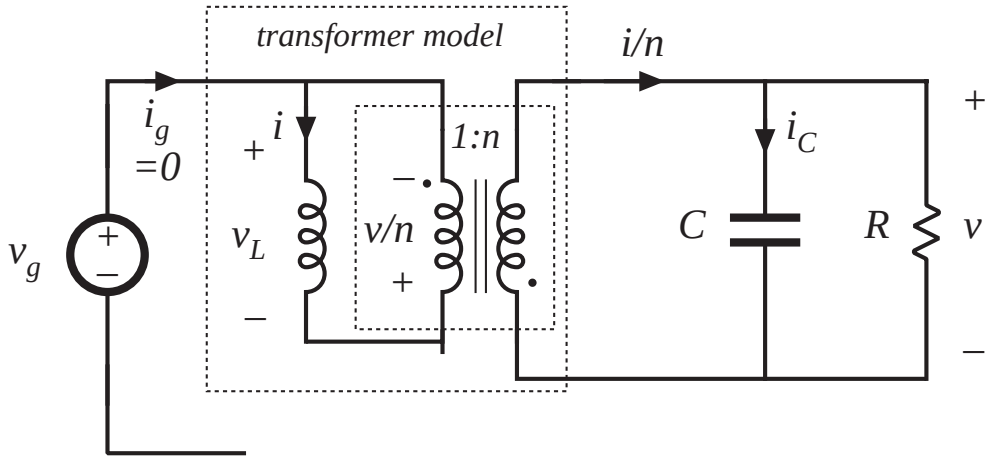
Subinterval 2

Circuit equations:

$$v_L(t) = -\frac{v(t)}{n}$$

$$i_C(t) = -\frac{i(t)}{n} - \frac{v(t)}{R}$$

$$i_g(t) = 0$$



Small ripple approximation:

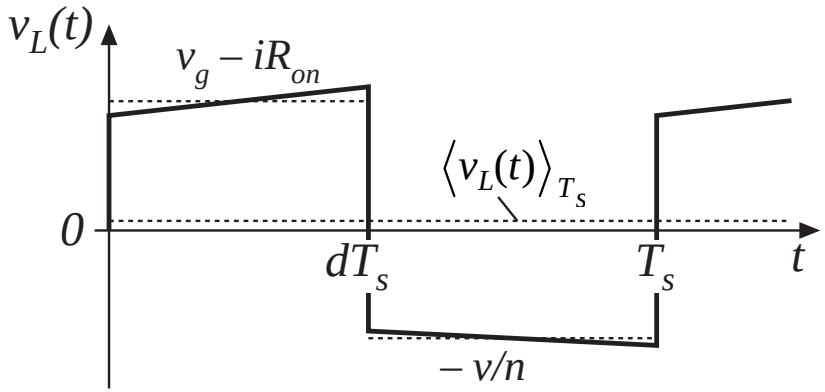
$$v_L(t) = -\frac{\langle v(t) \rangle_{T_s}}{n}$$

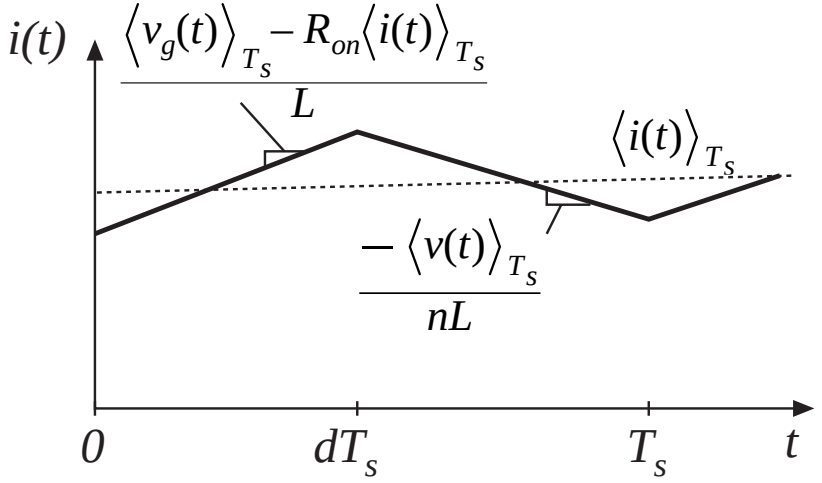
$$i_C(t) = -\frac{\langle i(t) \rangle_{T_s}}{n} - \frac{\langle v(t) \rangle_{T_s}}{R}$$

$$i_g(t) = 0$$

MOSFET is off, diode conducts

Inductor waveforms





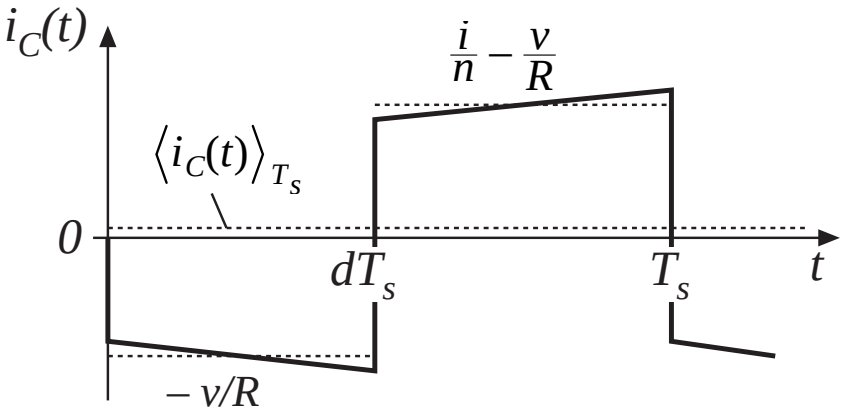
Average inductor voltage:

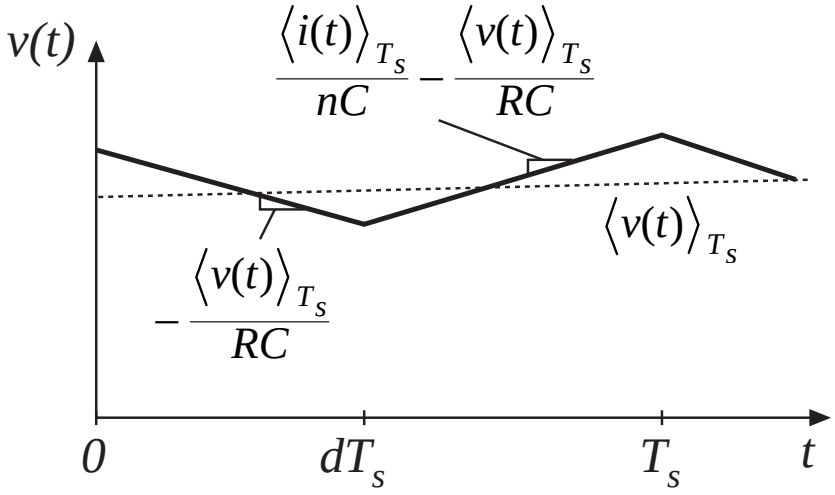
$$\langle v_L(t) \rangle_{T_s} = d(t) \left(\langle v_g(t) \rangle_{T_s} - \langle i(t) \rangle_{T_s} R_{on} \right) + d'(t) \left(\frac{-\langle v(t) \rangle_{T_s}}{n} \right)$$

Hence, we can write:

$$L \frac{d \langle i(t) \rangle_{T_s}}{dt} = d(t) \langle v_g(t) \rangle_{T_s} - d(t) \langle i(t) \rangle_{T_s} R_{on} - d'(t) \frac{\langle v(t) \rangle_{T_s}}{n}$$

Capacitor waveforms





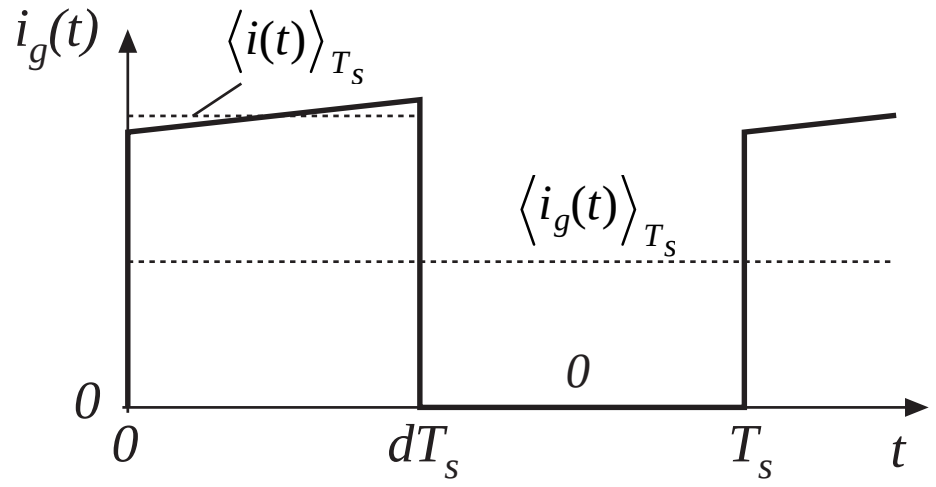
Average capacitor current:

$$\langle i_C(t) \rangle_{T_s} = d(t) \left(\frac{-\langle v(t) \rangle_{T_s}}{R} \right) + d'(t) \left(\frac{\langle i(t) \rangle_{T_s}}{n} - \frac{\langle v(t) \rangle_{T_s}}{R} \right)$$

Hence, we can write:

$$C \frac{d\langle v(t) \rangle_{T_s}}{dt} = d'(t) \frac{\langle i(t) \rangle_{T_s}}{n} - \frac{\langle v(t) \rangle_{T_s}}{R}$$

Input current waveform



Average input current:

$$\langle i_g(t) \rangle_{T_s} = d(t) \langle i(t) \rangle_{T_s}$$

The averaged converter equations

$$L \frac{d\left\langle i(t)\right\rangle_{T_s}}{dt} = d(t) \left\langle v_g(t)\right\rangle_{T_s} - d(t) \left\langle i(t)\right\rangle_{T_s} R_{on} - d'(t) \frac{\left\langle v(t)\right\rangle_{T_s}}{n}$$

$$C \frac{d\left\langle v(t)\right\rangle_{T_s}}{dt} = d'(t) \frac{\left\langle i(t)\right\rangle_{T_s}}{n} - \frac{\left\langle v(t)\right\rangle_{T_s}}{R}$$

$$\left\langle i_g(t)\right\rangle_{T_s} = d(t) \left\langle i(t)\right\rangle_{T_s}$$

— a system of nonlinear differential equations

Next step: perturbation and linearization. Let

$$\left\langle v_g(t)\right\rangle_{T_s} = V_g + \hat{v}_g(t) \qquad \left\langle i(t)\right\rangle_{T_s} = I + \hat{i}(t)$$

$$d(t) = D + \hat{d}(t) \qquad \left\langle v(t)\right\rangle_{T_s} = V + \hat{v}(t)$$

$$\left\langle i_g(t)\right\rangle_{T_s} = I_g + \hat{i}_g(t)$$

Perturbation of the averaged inductor equation

$$L \frac{d\left\langle i(t) \right\rangle_{T_s}}{dt} = d(t) \left\langle v_g(t) \right\rangle_{T_s} - d(t) \left\langle i(t) \right\rangle_{T_s} R_{on} - d'(t) \frac{\left\langle v(t) \right\rangle_{T_s}}{n}$$

$$L \frac{d\left(I + \hat{i}(t)\right)}{dt} = \left(D + \hat{d}(t)\right)\left(V_g + \hat{v}_g(t)\right) - \left(D' - \hat{d}(t)\right)\frac{\left(V + \hat{v}(t)\right)}{n} - \left(D + \hat{d}(t)\right)\left(I + \hat{i}(t)\right) R_{on}$$

$$L\left(\frac{dI}{dt}^{0} + \frac{d\,\hat{i}(t)}{dt}\right) = \underbrace{\left(DV_g - D'\frac{V}{n} - DR_{on}I\right)}_{\text{Dc terms}} + \underbrace{\left(D\hat{v}_g(t) - D'\frac{\hat{v}(t)}{n} + \left(V_g + \frac{V}{n} - IR_{on}\right)\hat{d}(t) - DR_{on}\hat{i}(t)\right)}_{1^{st}\ \text{order ac terms (linear)}}$$

$$+ \underbrace{\left(\hat{d}(t)\hat{v}_g(t) + \hat{d}(t)\frac{\hat{v}(t)}{n} - \hat{d}(t)\hat{i}(t)R_{on}\right)}_{2^{nd}\ \text{order ac terms (nonlinear)}}$$

Linearization of averaged inductor equation

Dc terms:

$$0 = DV_g - D'\frac{V}{n} - DR_{on}I$$

Second-order terms are small when the small-signal assumption is satisfied. The remaining first-order terms are:

$$L\frac{d\hat{i}(t)}{dt} = D\hat{v}_g(t) - D'\frac{\hat{v}(t)}{n} + \left(V_g + \frac{V}{n} - IR_{on}\right)\hat{d}(t) - DR_{on}\hat{i}(t)$$

This is the desired linearized inductor equation.

Perturbation of averaged capacitor equation

Original averaged equation:

$$C \frac{d\left\langle v(t) \right\rangle_{T_s}}{dt} = d'(t) \frac{\left\langle i(t) \right\rangle_{T_s}}{n} - \frac{\left\langle v(t) \right\rangle_{T_s}}{R}$$

Perturb about quiescent operating point:

$$C \frac{d\left(V + \hat{v}(t)\right)}{dt} = \left(D' - \hat{d}(t)\right) \frac{\left(I + \hat{i}(t)\right)}{n} - \frac{\left(V + \hat{v}(t)\right)}{R}$$

Collect terms:

$$C \left(\frac{dV}{dt}^{0} + \frac{d\hat{v}(t)}{dt} \right) = \underbrace{\left(\frac{D'I}{n} - \frac{V}{R} \right)}_{\text{Dc terms}} + \underbrace{\left(\frac{D'\hat{i}(t)}{n} - \frac{\hat{v}(t)}{R} - \frac{I\hat{d}(t)}{n} \right)}_{1^{st} \text{ order ac terms (linear)}} - \underbrace{\frac{\hat{d}(t)\hat{i}(t)}{n}}_{2^{nd} \text{ order ac term (nonlinear)}}$$

Linearization of averaged capacitor equation

Dc terms:

$$0 = \left(\frac{D'I}{n} - \frac{V}{R} \right)$$

Second-order terms are small when the small-signal assumption is satisfied. The remaining first-order terms are:

$$C \frac{d\hat{v}(t)}{dt} = \frac{D'\hat{i}(t)}{n} - \frac{\hat{v}(t)}{R} - \frac{I\hat{d}(t)}{n}$$

This is the desired linearized capacitor equation.

Perturbation of averaged input current equation

Original averaged equation:

$$\left\langle i_g(t) \right\rangle_{T_s} = d(t) \left\langle i(t) \right\rangle_{T_s}$$

Perturb about quiescent operating point:

$$I_g + \hat{i}_g(t) = \left(D + \hat{d}(t) \right) \left(I + \hat{i}(t) \right)$$

Collect terms:

$$\underbrace{I_g}_{\text{Dc term}} + \underbrace{\hat{i}_g(t)}_{1^{st}\text{ order ac term}} = \underbrace{\left(DI \right)}_{\text{Dc term}} + \underbrace{\left(D\hat{i}(t) + I\hat{d}(t) \right)}_{1^{st}\text{ order ac terms (linear)}} + \underbrace{\hat{d}(t)\hat{i}(t)}_{2^{nd}\text{ order ac term (nonlinear)}}$$

Linearization of averaged input current equation

Dc terms:

$$I_g = DI$$

Second-order terms are small when the small-signal assumption is satisfied. The remaining first-order terms are:

$$\hat{i}_g(t) = D\hat{i}(t) + I\hat{d}(t)$$

This is the desired linearized input current equation.

Summary: dc and small-signal ac converter equations

Dc equations:

$$0 = DV_g - D'\frac{V}{n} - DR_{on}I$$

$$0 = \left(\frac{D'I}{n} - \frac{V}{R}\right)$$

$$I_g = DI$$

Small-signal ac equations:

$$L\,\frac{d\,\hat{i}(t)}{dt} = D\hat{v}_g(t) - D'\frac{\hat{v}(t)}{n} + \left(V_g + \frac{V}{n} - IR_{on}\right)\hat{d}(t) - DR_{on}\hat{i}(t)$$

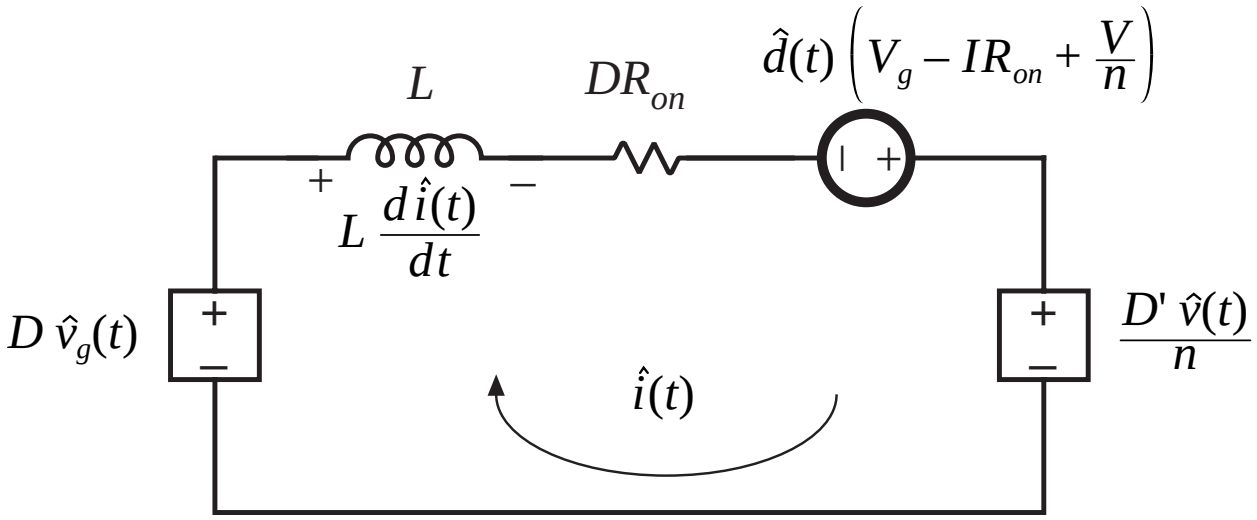
$$C\,\frac{d\hat{v}(t)}{dt} = \frac{D'\hat{i}(t)}{n} - \frac{\hat{v}(t)}{R} - \frac{I\hat{d}(t)}{n}$$

$$\hat{i}_g(t) = D\hat{i}(t) + I\hat{d}(t)$$

Next step: construct equivalent circuit models.

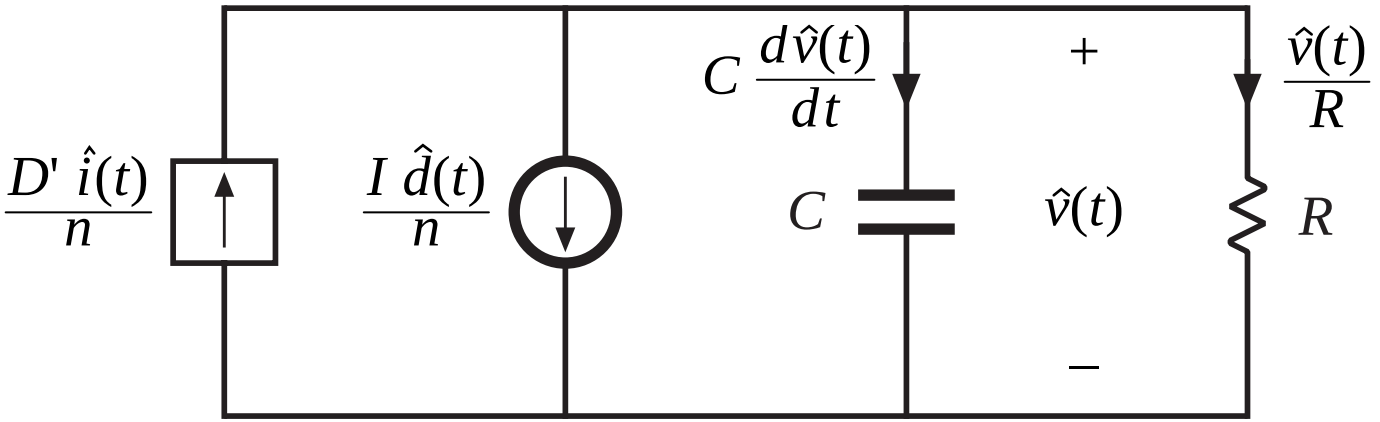
Small-signal ac equivalent circuit: inductor loop

$$L\frac{d\hat{i}(t)}{dt} = D\hat{v}_g(t) - D'\frac{\hat{v}(t)}{n} + \left(V_g + \frac{V}{n} - IR_{on}\right)\hat{d}(t) - DR_{on}\hat{i}(t)$$



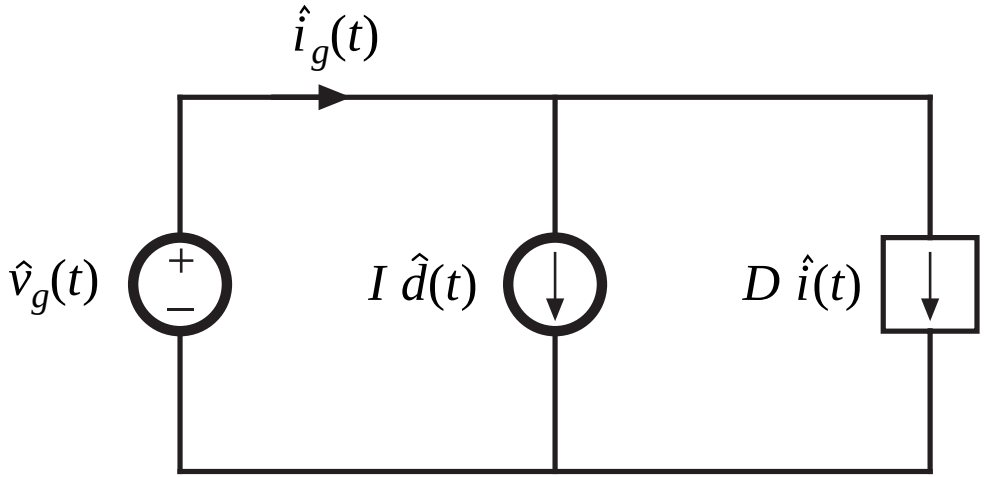
Small-signal ac equivalent circuit: capacitor node

$$C \frac{d\hat{v}(t)}{dt} = \frac{D'\hat{i}(t)}{n} - \frac{\hat{v}(t)}{R} - \frac{I\hat{d}(t)}{n}$$



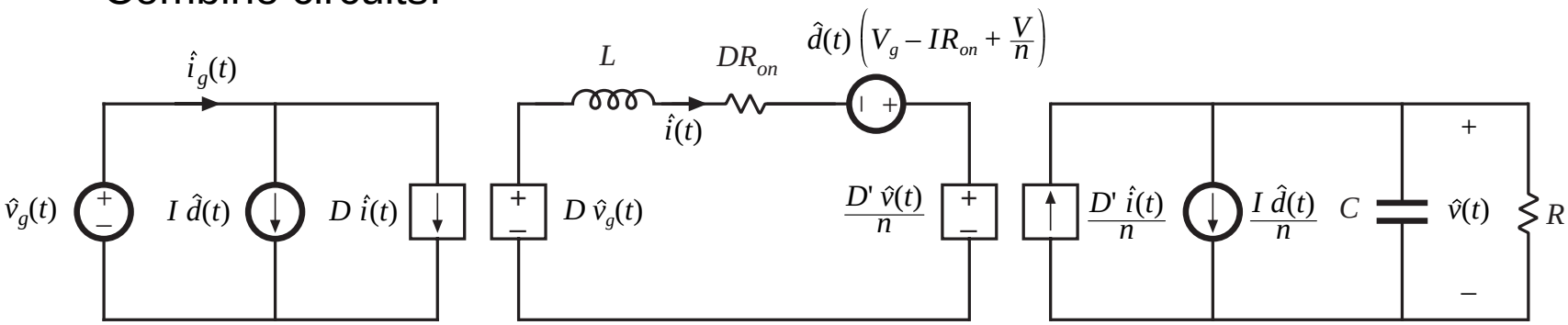
Small-signal ac equivalent circuit: converter input node

$$\hat{i}_g(t) = D\hat{i}(t) + I\hat{d}(t)$$

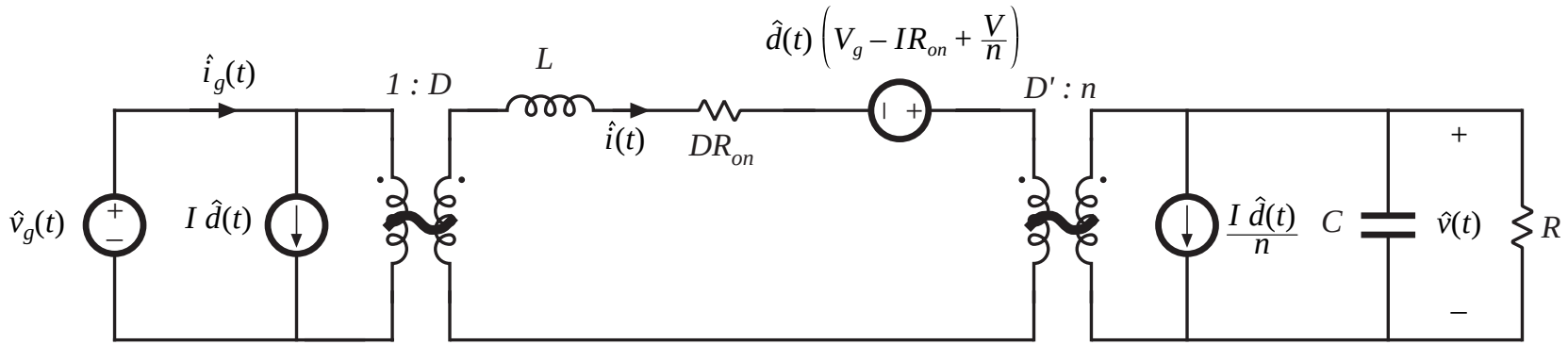


Small-signal ac model, nonideal flyback converter example

Combine circuits:



Replace dependent sources with ideal transformers:



7.4. State Space Averaging

- A formal method for deriving the small-signal ac equations of a switching converter
- Equivalent to the modeling method of the previous sections
- Uses the state-space matrix description of linear circuits
- Often cited in the literature
- A general approach: if the state equations of the converter can be written for each subinterval, then the small-signal averaged model can always be derived
- Computer programs exist which utilize the state-space averaging method

7.4.1. The state equations of a network

- A canonical form for writing the differential equations of a system
- If the system is linear, then the derivatives of the *state variables* are expressed as linear combinations of the system independent inputs and state variables themselves
- The physical state variables of a system are usually associated with the storage of energy
- For a typical converter circuit, the physical state variables are the inductor currents and capacitor voltages
- Other typical physical state variables: position and velocity of a motor shaft
- At a given point in time, the values of the state variables depend on the previous history of the system, rather than the present values of the system inputs
- To solve the differential equations of a system, the initial values of the state variables must be specified

State equations of a linear system, in matrix form

A canonical matrix form:

$$\mathbf{K}\,\frac{d\mathbf{x}(t)}{dt} = \mathbf{A}\,\mathbf{x}(t) + \mathbf{B}\,\mathbf{u}(t)$$

$$\mathbf{y}(t) = \mathbf{C}\,\mathbf{x}(t) + \mathbf{E}\,\mathbf{u}(t)$$

State vector $\mathbf{x}(t)$ contains inductor currents, capacitor voltages, etc.:

$$\mathbf{x}(t) = \begin{bmatrix} x_1(t) \\ x_2(t) \\ \vdots \end{bmatrix}, \qquad \frac{d\mathbf{x}(t)}{dt} = \begin{bmatrix} \frac{dx_1(t)}{dt} \\ \frac{dx_2(t)}{dt} \\ \vdots \end{bmatrix}$$

Input vector $\mathbf{u}(t)$ contains independent sources such as $v_g(t)$

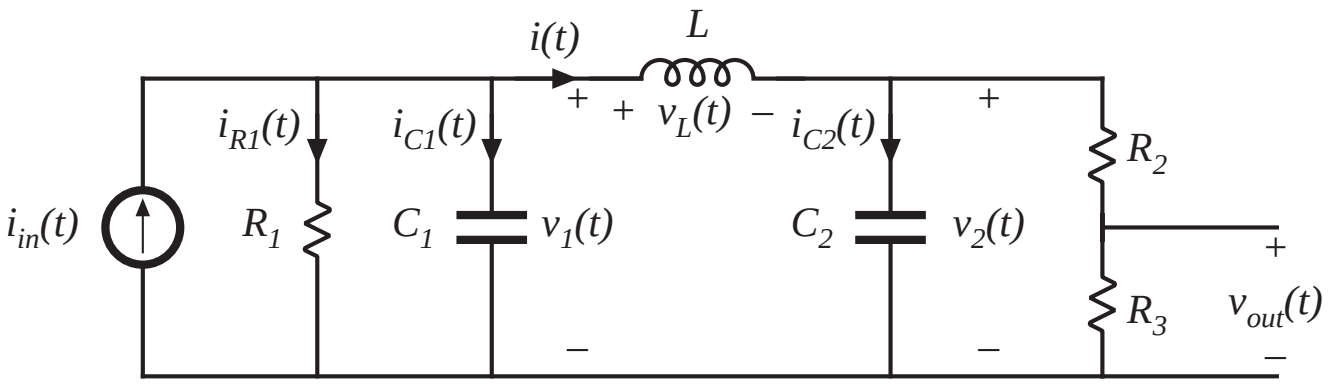
Output vector $\mathbf{y}(t)$ contains other dependent quantities to be computed, such as $i_g(t)$

Matrix $\mathbf{K}$ contains values of capacitance, inductance, and mutual inductance, so that $\mathbf{K}\,d\mathbf{x}/dt$ is a vector containing capacitor currents and inductor winding voltages. These quantities are expressed as linear combinations of the independent inputs and state variables. The matrices $\mathbf{A}$, $\mathbf{B}$, $\mathbf{C}$, and $\mathbf{E}$ contain the constants of proportionality.

Example

State vector

$$\mathbf{x}(t) = \begin{bmatrix} v_1(t) \\ v_2(t) \\ i(t) \end{bmatrix}$$



Matrix $\mathbf{K}$

$$\mathbf{K} = \begin{bmatrix} C_1 & 0 & 0 \\ 0 & C_2 & 0 \\ 0 & 0 & L \end{bmatrix}$$

Input vector

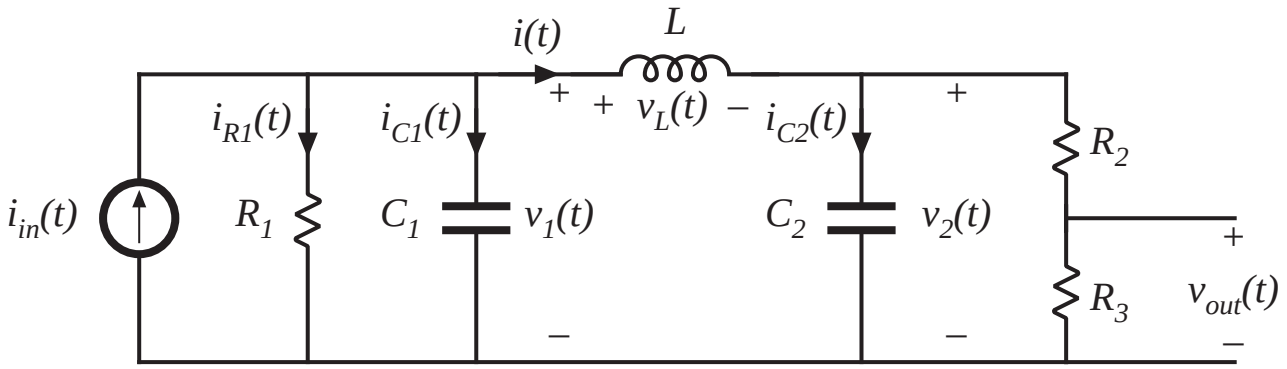
$$\mathbf{u}(t) = \begin{bmatrix} i_{in}(t) \end{bmatrix}$$

Choose output vector as

$$\mathbf{y}(t) = \begin{bmatrix} v_{out}(t) \\ i_{R1}(t) \end{bmatrix}$$

To write the state equations of this circuit, we must express the inductor voltages and capacitor currents as linear combinations of the elements of the $\mathbf{x}(t)$ and $\mathbf{u}(t)$ vectors.

Circuit equations



Find i_{C1} via node equation:

$$i_{C1}(t) = C_1 \frac{dv_1(t)}{dt} = i_{in}(t) - \frac{v_1(t)}{R} - i(t)$$

Find i_{C2} via node equation:

$$i_{C2}(t) = C_2 \frac{dv_2(t)}{dt} = i(t) - \frac{v_2(t)}{R_2 + R_3}$$

Find v_L via loop equation:

$$v_L(t) = L \frac{di(t)}{dt} = v_1(t) - v_2(t)$$

Equations in matrix form

The same equations:

$$i_{C1}(t) = C_1 \frac{dv_1(t)}{dt} = i_{in}(t) - \frac{v_1(t)}{R} - i(t)$$

$$i_{C2}(t) = C_2 \frac{dv_2(t)}{dt} = i(t) - \frac{v_2(t)}{R_2 + R_3}$$

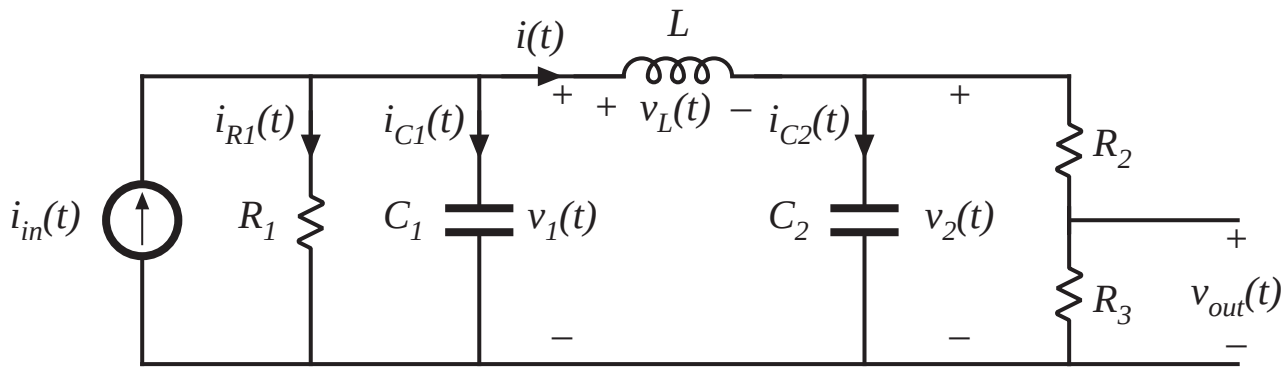
$$v_L(t) = L \frac{di(t)}{dt} = v_1(t) - v_2(t)$$

Express in matrix form:

$$\underbrace{\begin{bmatrix} C_1 & 0 & 0 \\ 0 & C_2 & 0 \\ 0 & 0 & L \end{bmatrix}}_{\mathbf{K}} \underbrace{\begin{bmatrix} \frac{dv_1(t)}{dt} \\ \frac{dv_2(t)}{dt} \\ \frac{di(t)}{dt} \end{bmatrix}}_{\frac{d\mathbf{x}(t)}{dt}} = \underbrace{\begin{bmatrix} -\frac{1}{R_1} & 0 & -1 \\ 0 & -\frac{1}{R_2 + R_3} & 1 \\ 1 & -1 & 0 \end{bmatrix}}_{\mathbf{A}} \underbrace{\begin{bmatrix} v_1(t) \\ v_2(t) \\ i(t) \end{bmatrix}}_{\mathbf{x}(t)} + \underbrace{\begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix}}_{\mathbf{B}} \underbrace{\begin{bmatrix} i_{in}(t) \end{bmatrix}}_{\mathbf{u}(t)}$$

Output (dependent signal) equations

$$\mathbf{y}(t) = \begin{vmatrix} v_{out}(t) \\ i_{R1}(t) \end{vmatrix}$$



Express elements of the vector **y** as linear combinations of elements of **x** and **u**:

$$v_{out}(t) = v_2(t)\,\frac{R_3}{R_2 + R_3}$$

$$i_{R1}(t) = \frac{v_1(t)}{R_1}$$

Express in matrix form

The same equations:

$$v_{out}(t) = v_2(t)\,\frac{R_3}{R_2 + R_3}$$

$$i_{R1}(t) = \frac{v_1(t)}{R_1}$$

Express in matrix form:

$$\underbrace{\begin{bmatrix} v_{out}(t) \\ i_{R1}(t) \end{bmatrix}}_{\mathbf{y}(t)} = \underbrace{\begin{bmatrix} 0 & \frac{R_3}{R_2 + R_3} & 0 \\ \frac{1}{R_1} & 0 & 0 \end{bmatrix}}_{\mathbf{C}} \underbrace{\begin{bmatrix} v_1(t) \\ v_2(t) \\ i(t) \end{bmatrix}}_{\mathbf{x}(t)} + \underbrace{\begin{bmatrix} 0 \\ 0 \end{bmatrix}}_{\mathbf{E}} \underbrace{\begin{bmatrix} i_{in}(t) \end{bmatrix}}_{\mathbf{u}(t)}$$

7.4.2. The basic state-space averaged model

Given: a PWM converter, operating in continuous conduction mode, with two subintervals during each switching period.

During subinterval 1, when the switches are in position 1, the converter reduces to a linear circuit that can be described by the following state equations:

$$\mathbf{K}\,\frac{d\mathbf{x}(t)}{dt} = \mathbf{A}_1\,\mathbf{x}(t) + \mathbf{B}_1\,\mathbf{u}(t)$$
$$\mathbf{y}(t) = \mathbf{C}_1\,\mathbf{x}(t) + \mathbf{E}_1\,\mathbf{u}(t)$$

During subinterval 2, when the switches are in position 2, the converter reduces to another linear circuit, that can be described by the following state equations:

$$\mathbf{K}\,\frac{d\mathbf{x}(t)}{dt} = \mathbf{A}_2\,\mathbf{x}(t) + \mathbf{B}_2\,\mathbf{u}(t)$$
$$\mathbf{y}(t) = \mathbf{C}_2\,\mathbf{x}(t) + \mathbf{E}_2\,\mathbf{u}(t)$$

Equilibrium (dc) state-space averaged model

Provided that the natural frequencies of the converter, as well as the frequencies of variations of the converter inputs, are much slower than the switching frequency, then the state-space averaged model that describes the converter in equilibrium is

$$\mathbf{0} = \mathbf{A}\,\mathbf{X} + \mathbf{B}\,\mathbf{U}$$

$$\mathbf{Y} = \mathbf{C}\,\mathbf{X} + \mathbf{E}\,\mathbf{U}$$

where the averaged matrices are

$$\mathbf{A} = D\,\mathbf{A}_1 + D'\,\mathbf{A}_2$$

$$\mathbf{B} = D\,\mathbf{B}_1 + D'\,\mathbf{B}_2$$

$$\mathbf{C} = D\,\mathbf{C}_1 + D'\,\mathbf{C}_2$$

$$\mathbf{E} = D\,\mathbf{E}_1 + D'\,\mathbf{E}_2$$

and the equilibrium dc components are

$\mathbf{X}$ = *equilibrium* (*dc*) *state vector*

$\mathbf{U}$ = *equilibrium* (*dc*) *input vector*

$\mathbf{Y}$ = *equilibrium* (*dc*) *output vector*

D = *equilibrium* (*dc*) *duty cycle*

Solution of equilibrium averaged model

Equilibrium state-space averaged model:

$$\mathbf{0} = \mathbf{A}\,\mathbf{X} + \mathbf{B}\,\mathbf{U}$$
$$\mathbf{Y} = \mathbf{C}\,\mathbf{X} + \mathbf{E}\,\mathbf{U}$$

Solution for **X** and **Y**:

$$\mathbf{X} = -\,\mathbf{A}^{-1}\,\mathbf{B}\,\mathbf{U}$$
$$\mathbf{Y} = \left(-\,\mathbf{C}\,\mathbf{A}^{-1}\,\mathbf{B} + \mathbf{E}\right)\mathbf{U}$$

Small-signal ac state-space averaged model

$$\mathbf{K}\,\frac{d\hat{\mathbf{x}}(t)}{dt} = \mathbf{A}\,\hat{\mathbf{x}}(t) + \mathbf{B}\,\hat{\mathbf{u}}(t) + \left\{\left(\mathbf{A}_1 - \mathbf{A}_2\right)\mathbf{X} + \left(\mathbf{B}_1 - \mathbf{B}_2\right)\mathbf{U}\right\}\hat{d}(t)$$

$$\hat{\mathbf{y}}(t) = \mathbf{C}\,\hat{\mathbf{x}}(t) + \mathbf{E}\,\hat{\mathbf{u}}(t) + \left\{\left(\mathbf{C}_1 - \mathbf{C}_2\right)\mathbf{X} + \left(\mathbf{E}_1 - \mathbf{E}_2\right)\mathbf{U}\right\}\hat{d}(t)$$

where

$\hat{\mathbf{x}}(t)$ = *small – signal (ac) perturbation in state vector*

$\hat{\mathbf{u}}(t)$ = *small – signal (ac) perturbation in input vector*

$\hat{\mathbf{y}}(t)$ = *small – signal (ac) perturbation in output vector*

$\hat{d}(t)$ = *small – signal (ac) perturbation in duty cycle*

So if we can write the converter state equations during subintervals 1 and 2, then we can always find the averaged dc and small-signal ac models

7.4.3. Discussion of the state-space averaging result

As in Sections 7.1 and 7.2, the low-frequency components of the inductor currents and capacitor voltages are modeled by averaging over an interval of length T_s. Hence, we define the average of the state vector as:

$$\left\langle \mathbf{x}(t) \right\rangle_{T_s} = \frac{1}{T_s} \int_t^{t+T_s} \mathbf{x}(\tau)\, d\tau$$

The low-frequency components of the input and output vectors are modeled in a similar manner.

By averaging the inductor voltages and capacitor currents, one obtains:

$$\mathbf{K} \frac{d\left\langle \mathbf{x}(t) \right\rangle_{T_s}}{dt} = \left(d(t)\, \mathbf{A_1} + d'(t)\, \mathbf{A_2} \right) \left\langle \mathbf{x}(t) \right\rangle_{T_s} + \left(d(t)\, \mathbf{B_1} + d'(t)\, \mathbf{B_2} \right) \left\langle \mathbf{u}(t) \right\rangle_{T_s}$$

Change in state vector during first subinterval

During subinterval 1, we have

$$\mathbf{K}\,\frac{d\mathbf{x}(t)}{dt} = \mathbf{A}_1\,\mathbf{x}(t) + \mathbf{B}_1\,\mathbf{u}(t)$$
$$\mathbf{y}(t) = \mathbf{C}_1\,\mathbf{x}(t) + \mathbf{E}_1\,\mathbf{u}(t)$$

So the elements of $\mathbf{x}(t)$ change with the slope

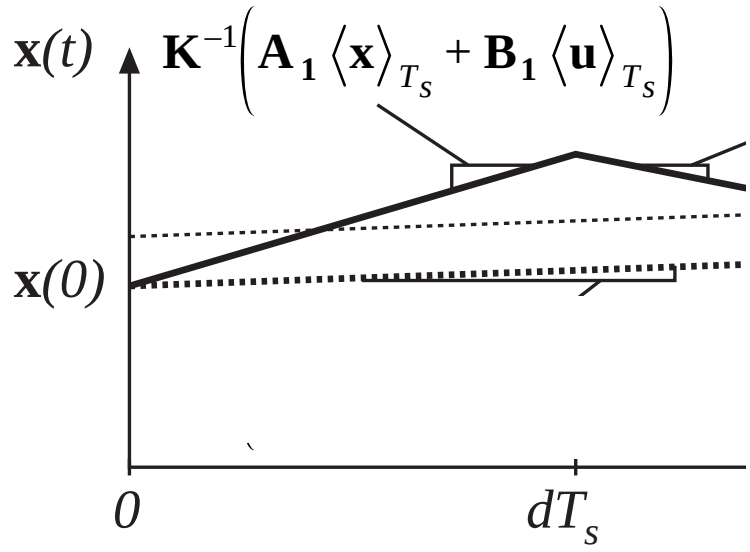
$$\frac{d\mathbf{x}(t)}{dt} = \mathbf{K}^{-1}\left(\mathbf{A}_1\,\mathbf{x}(t) + \mathbf{B}_1\,\mathbf{u}(t)\right)$$

Small ripple assumption: the elements of $\mathbf{x}(t)$ and $\mathbf{u}(t)$ do not change significantly during the subinterval. Hence the slopes are essentially constant and are equal to

$$\frac{d\mathbf{x}(t)}{dt} = \mathbf{K}^{-1}\left(\mathbf{A}_1\left\langle\mathbf{x}(t)\right\rangle_{T_s} + \mathbf{B}_1\left\langle\mathbf{u}(t)\right\rangle_{T_s}\right)$$

Change in state vector during first subinterval

$$\frac{d\mathbf{x}(t)}{dt} = \mathbf{K}^{-1}\left(\mathbf{A_1}\left\langle \mathbf{x}(t)\right\rangle_{T_s} + \mathbf{B_1}\left\langle \mathbf{u}(t)\right\rangle_{T_s}\right)$$



Net change in state vector over first subinterval:

$$\underbrace{\mathbf{x}(dT_s)}_{\substack{\textit{final}\\ \textit{value}}} = \underbrace{\mathbf{x}(0)}_{\substack{\textit{initial}\\ \textit{value}}} + \underbrace{\left(dT_s\right)}_{\substack{\textit{interval}\\ \textit{length}}} \underbrace{\mathbf{K}^{-1}\left(\mathbf{A_1}\left\langle \mathbf{x}(t)\right\rangle_{T_s} + \mathbf{B_1}\left\langle \mathbf{u}(t)\right\rangle_{T_s}\right)}_{\textit{slope}}$$

Change in state vector during second subinterval

Use similar arguments.

State vector now changes with the essentially constant slope

$$\frac{d\mathbf{x}(t)}{dt} = \mathbf{K}^{-1}\left(\mathbf{A}_2 \left\langle \mathbf{x}(t) \right\rangle_{T_s} + \mathbf{B}_2 \left\langle \mathbf{u}(t) \right\rangle_{T_s}\right)$$

The value of the state vector at the end of the second subinterval is therefore

$$\underbrace{\mathbf{x}(T_s)}_{\substack{\textit{final}\\ \textit{value}}} = \underbrace{\mathbf{x}(dT_s)}_{\substack{\textit{initial}\\ \textit{value}}} + \underbrace{\left(d'T_s\right)}_{\substack{\textit{interval}\\ \textit{length}}} \underbrace{\mathbf{K}^{-1}\left(\mathbf{A}_2 \left\langle \mathbf{x}(t) \right\rangle_{T_s} + \mathbf{B}_2 \left\langle \mathbf{u}(t) \right\rangle_{T_s}\right)}_{\textit{slope}}$$

Net change in state vector over one switching period

We have:

$$\mathbf{x}(dT_s) = \mathbf{x}(0) + \left(dT_s\right)\mathbf{K}^{-1}\left(\mathbf{A_1}\left\langle\mathbf{x}(t)\right\rangle_{T_s} + \mathbf{B_1}\left\langle\mathbf{u}(t)\right\rangle_{T_s}\right)$$

$$\mathbf{x}(T_s) = \mathbf{x}(dT_s) + \left(d'T_s\right)\mathbf{K}^{-1}\left(\mathbf{A_2}\left\langle\mathbf{x}(t)\right\rangle_{T_s} + \mathbf{B_2}\left\langle\mathbf{u}(t)\right\rangle_{T_s}\right)$$

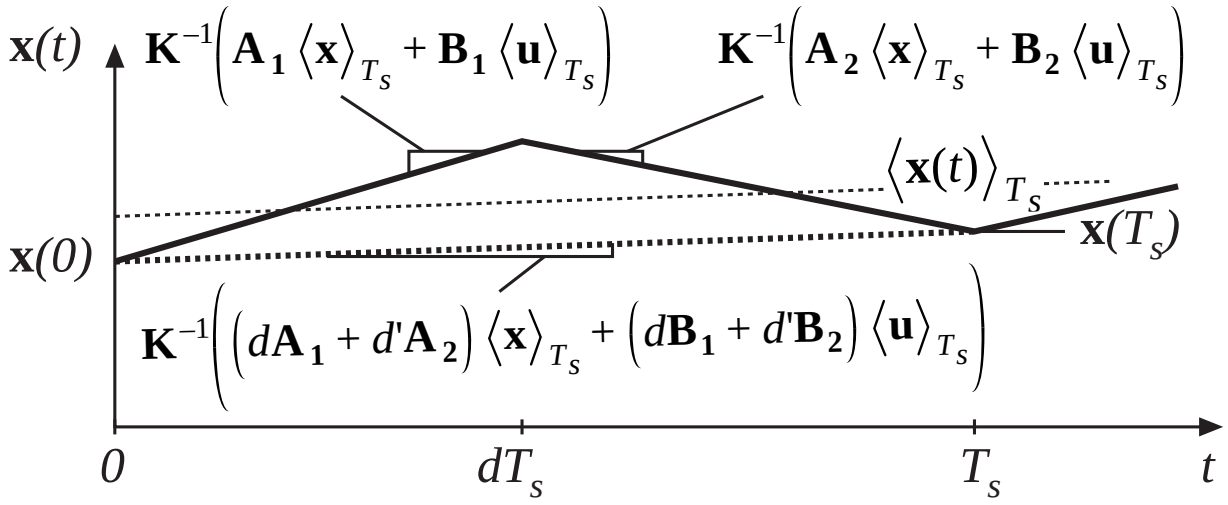
Eliminate $\mathbf{x}(dT_s)$, to express $\mathbf{x}(T_s)$ directly in terms of $\mathbf{x}(0)$:

$$\mathbf{x}(T_s) = \mathbf{x}(0) + dT_s\mathbf{K}^{-1}\left(\mathbf{A_1}\left\langle\mathbf{x}(t)\right\rangle_{T_s} + \mathbf{B_1}\left\langle\mathbf{u}(t)\right\rangle_{T_s}\right) + d'T_s\mathbf{K}^{-1}\left(\mathbf{A_2}\left\langle\mathbf{x}(t)\right\rangle_{T_s} + \mathbf{B_2}\left\langle\mathbf{u}(t)\right\rangle_{T_s}\right)$$

Collect terms:

$$\mathbf{x}(T_s) = \mathbf{x}(0) + T_s\mathbf{K}^{-1}\left(d(t)\mathbf{A_1} + d'(t)\mathbf{A_2}\right)\left\langle\mathbf{x}(t)\right\rangle_{T_s} + T_s\mathbf{K}^{-1}\left(d(t)\mathbf{B_1} + d'(t)\mathbf{B_2}\right)\left\langle\mathbf{u}(t)\right\rangle_{T_s}$$

Approximate derivative of state vector



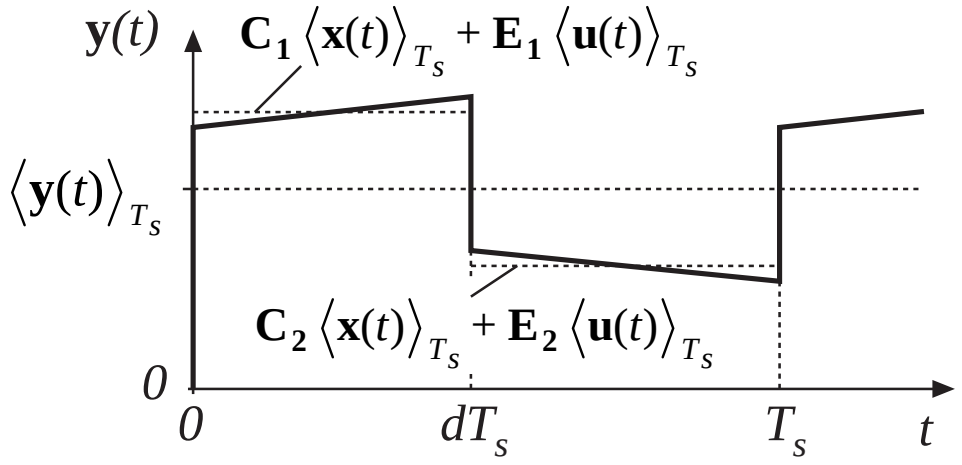
Use Euler approximation:

$$\frac{d\left\langle \mathbf{x}(t)\right\rangle_{T_s}}{dt} \approx \frac{\mathbf{x}(T_s) - \mathbf{x}(0)}{T_s}$$

We obtain:

$$\mathbf{K}\,\frac{d\left\langle \mathbf{x}(t)\right\rangle_{T_s}}{dt} = \left(d(t)\,\mathbf{A_1} + d'(t)\,\mathbf{A_2}\right)\left\langle \mathbf{x}(t)\right\rangle_{T_s} + \left(d(t)\,\mathbf{B_1} + d'(t)\,\mathbf{B_2}\right)\left\langle \mathbf{u}(t)\right\rangle_{T_s}$$

Low-frequency components of output vector



Remove switching harmonics by averaging over one switching period:

$$\left\langle \mathbf{y}(t) \right\rangle_{T_s} = d(t) \left(\mathbf{C_1} \left\langle \mathbf{x}(t) \right\rangle_{T_s} + \mathbf{E_1} \left\langle \mathbf{u}(t) \right\rangle_{T_s} \right) + d'(t) \left(\mathbf{C_2} \left\langle \mathbf{x}(t) \right\rangle_{T_s} + \mathbf{E_2} \left\langle \mathbf{u}(t) \right\rangle_{T_s} \right)$$

Collect terms:

$$\left\langle \mathbf{y}(t) \right\rangle_{T_s} = \left(d(t)\, \mathbf{C_1} + d'(t)\, \mathbf{C_2} \right) \left\langle \mathbf{x}(t) \right\rangle_{T_s} + \left(d(t)\, \mathbf{E_1} + d'(t)\, \mathbf{E_2} \right) \left\langle \mathbf{u}(t) \right\rangle_{T_s}$$

Averaged state equations: quiescent operating point

The averaged (nonlinear) state equations:

$$\mathbf{K}\,\frac{d\left\langle \mathbf{x}(t)\right\rangle_{T_s}}{dt} = \left(d(t)\,\mathbf{A_1} + d'(t)\,\mathbf{A_2}\right)\left\langle \mathbf{x}(t)\right\rangle_{T_s} + \left(d(t)\,\mathbf{B_1} + d'(t)\,\mathbf{B_2}\right)\left\langle \mathbf{u}(t)\right\rangle_{T_s}$$

$$\left\langle \mathbf{y}(t)\right\rangle_{T_s} = \left(d(t)\,\mathbf{C_1} + d'(t)\,\mathbf{C_2}\right)\left\langle \mathbf{x}(t)\right\rangle_{T_s} + \left(d(t)\,\mathbf{E_1} + d'(t)\,\mathbf{E_2}\right)\left\langle \mathbf{u}(t)\right\rangle_{T_s}$$

The converter operates in equilibrium when the derivatives of all elements of $\langle \mathbf{x}(t) \rangle_{T_s}$ are zero. Hence, the converter quiescent operating point is the solution of

$$\mathbf{0} = \mathbf{A}\,\mathbf{X} + \mathbf{B}\,\mathbf{U}$$

$$\mathbf{Y} = \mathbf{C}\,\mathbf{X} + \mathbf{E}\,\mathbf{U}$$

where

$$\mathbf{A} = D\,\mathbf{A_1} + D'\,\mathbf{A_2}$$

$$\mathbf{B} = D\,\mathbf{B_1} + D'\,\mathbf{B_2}$$

$$\mathbf{C} = D\,\mathbf{C_1} + D'\,\mathbf{C_2}$$

$$\mathbf{E} = D\,\mathbf{E_1} + D'\,\mathbf{E_2}$$

and

$\mathbf{X}$ = *equilibrium* (*dc*) *state vector*

$\mathbf{U}$ = *equilibrium* (*dc*) *input vector*

$\mathbf{Y}$ = *equilibrium* (*dc*) *output vector*

D = *equilibrium* (*dc*) *duty cycle*

Averaged state equations: perturbation and linearization

Let $\left\langle \mathbf{x}(t) \right\rangle_{T_s} = \mathbf{X} + \hat{\mathbf{x}}(t)$ with $\| \mathbf{U} \| >> \| \hat{\mathbf{u}}(t) \|$

$\left\langle \mathbf{u}(t) \right\rangle_{T_s} = \mathbf{U} + \hat{\mathbf{u}}(t)$ $D >> \left| \hat{d}(t) \right|$

$\left\langle \mathbf{y}(t) \right\rangle_{T_s} = \mathbf{Y} + \hat{\mathbf{y}}(t)$ $\| \mathbf{X} \| >> \| \hat{\mathbf{x}}(t) \|$

$d(t) = D + \hat{d}(t) \quad \Rightarrow \quad d'(t) = D' - \hat{d}(t)$ $\| \mathbf{Y} \| >> \| \hat{\mathbf{y}}(t) \|$

Substitute into averaged state equations:

$$\mathbf{K} \frac{d\left(\mathbf{X}+\hat{\mathbf{x}}(t)\right)}{dt} = \left(\left(D+\hat{d}(t)\right) \mathbf{A}_1 + \left(D'-\hat{d}(t)\right) \mathbf{A}_2 \right) \left(\mathbf{X}+\hat{\mathbf{x}}(t)\right) + \left(\left(D+\hat{d}(t)\right) \mathbf{B}_1 + \left(D'-\hat{d}(t)\right) \mathbf{B}_2 \right) \left(\mathbf{U}+\hat{\mathbf{u}}(t)\right)$$

$$\left(\mathbf{Y}+\hat{\mathbf{y}}(t)\right) = \left(\left(D+\hat{d}(t)\right) \mathbf{C}_1 + \left(D'-\hat{d}(t)\right) \mathbf{C}_2 \right) \left(\mathbf{X}+\hat{\mathbf{x}}(t)\right) + \left(\left(D+\hat{d}(t)\right) \mathbf{E}_1 + \left(D'-\hat{d}(t)\right) \mathbf{E}_2 \right) \left(\mathbf{U}+\hat{\mathbf{u}}(t)\right)$$

Averaged state equations: perturbation and linearization

$$\underbrace{\mathbf{K}\frac{d\hat{\mathbf{x}}(t)}{dt}}_{\text{first–order ac}} = \underbrace{\left(\mathbf{AX}+\mathbf{BU}\right)}_{\text{dc terms}} + \underbrace{\mathbf{A}\hat{\mathbf{x}}(t)+\mathbf{B}\hat{\mathbf{u}}(t)+\left\{\left(\mathbf{A}_1-\mathbf{A}_2\right)\mathbf{X}+\left(\mathbf{B}_1-\mathbf{B}_2\right)\mathbf{U}\right\}\hat{d}(t)}_{\text{first–order ac terms}}$$

$$+ \underbrace{\left(\mathbf{A}_1-\mathbf{A}_2\right)\hat{\mathbf{x}}(t)\hat{d}(t)+\left(\mathbf{B}_1-\mathbf{B}_2\right)\hat{\mathbf{u}}(t)\hat{d}(t)}_{\text{second–order nonlinear terms}}$$

$$\underbrace{\left(\mathbf{Y}+\hat{\mathbf{y}}(t)\right)}_{dc+1st\ order\ ac} = \underbrace{\left(\mathbf{CX}+\mathbf{EU}\right)}_{\text{dc terms}} + \underbrace{\mathbf{C}\hat{\mathbf{x}}(t)+\mathbf{E}\hat{\mathbf{u}}(t)+\left\{\left(\mathbf{C}_1-\mathbf{C}_2\right)\mathbf{X}+\left(\mathbf{E}_1-\mathbf{E}_2\right)\mathbf{U}\right\}\hat{d}(t)}_{\text{first–order ac terms}}$$

$$+ \underbrace{\left(\mathbf{C}_1-\mathbf{C}_2\right)\hat{\mathbf{x}}(t)\hat{d}(t)+\left(\mathbf{E}_1-\mathbf{E}_2\right)\hat{\mathbf{u}}(t)\hat{d}(t)}_{\text{second–order nonlinear terms}}$$

Linearized small-signal state equations

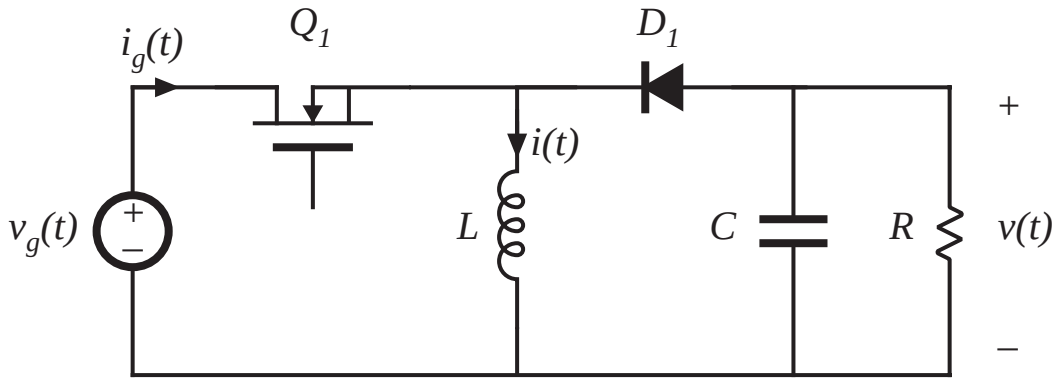
Dc terms drop out of equations. Second-order (nonlinear) terms are small when the small-signal assumption is satisfied. We are left with:

$$\mathbf{K}\,\frac{d\hat{\mathbf{x}}(t)}{dt} = \mathbf{A}\,\hat{\mathbf{x}}(t) + \mathbf{B}\,\hat{\mathbf{u}}(t) + \left\{\left(\mathbf{A}_1 - \mathbf{A}_2\right)\mathbf{X} + \left(\mathbf{B}_1 - \mathbf{B}_2\right)\mathbf{U}\right\}\hat{d}(t)$$

$$\hat{\mathbf{y}}(t) = \mathbf{C}\,\hat{\mathbf{x}}(t) + \mathbf{E}\,\hat{\mathbf{u}}(t) + \left\{\left(\mathbf{C}_1 - \mathbf{C}_2\right)\mathbf{X} + \left(\mathbf{E}_1 - \mathbf{E}_2\right)\mathbf{U}\right\}\hat{d}(t)$$

This is the desired result.

7.4.4. Example: State-space averaging of a nonideal buck-boost converter



Model nonidealities:

- MOSFET on-resistance R_{on}
- Diode forward voltage drop V_D

state vector

$$\mathbf{x}(t) = \begin{bmatrix} i(t) \\ v(t) \end{bmatrix}$$

input vector

$$\mathbf{u}(t) = \begin{bmatrix} v_g(t) \\ V_D \end{bmatrix}$$

output vector

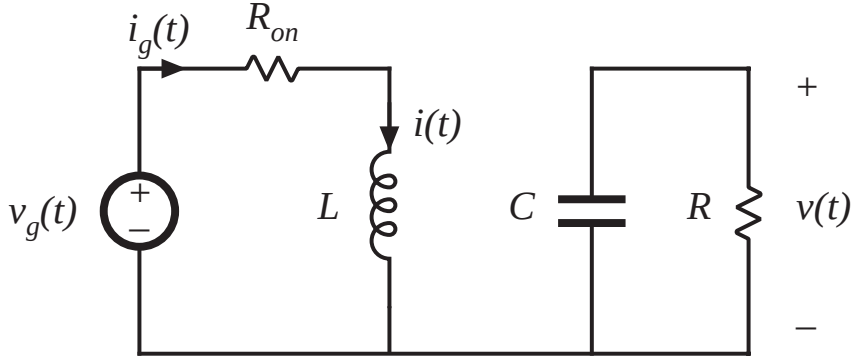
$$\mathbf{y}(t) = \begin{bmatrix} i_g(t) \end{bmatrix}$$

Subinterval 1

$$L \frac{di(t)}{dt} = v_g(t) - i(t)\, R_{on}$$

$$C \frac{dv(t)}{dt} = -\frac{v(t)}{R}$$

$$i_g(t) = i(t)$$



$$\underbrace{\begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix}}_{\mathbf{K}} \underbrace{\frac{d}{dt}\begin{bmatrix} i(t) \\ v(t) \end{bmatrix}}_{\frac{d\mathbf{x}(t)}{dt}} = \underbrace{\begin{bmatrix} -R_{on} & 0 \\ 0 & -\frac{1}{R} \end{bmatrix}}_{\mathbf{A_1}} \underbrace{\begin{bmatrix} i(t) \\ v(t) \end{bmatrix}}_{\mathbf{x}(t)} + \underbrace{\begin{bmatrix} 1 & 0 \\ 0 & 0 \end{bmatrix}}_{\mathbf{B_1}} \underbrace{\begin{bmatrix} v_g(t) \\ V_D \end{bmatrix}}_{\mathbf{u}(t)}$$

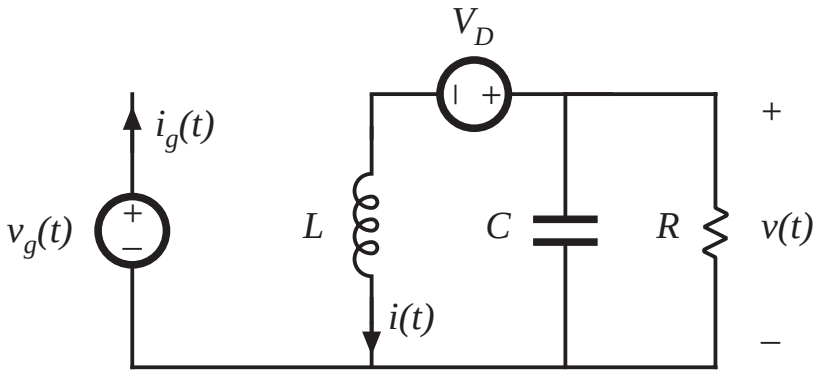
$$\underbrace{\begin{bmatrix} i_g(t) \end{bmatrix}}_{\mathbf{y}(t)} = \underbrace{\begin{bmatrix} 1 & 0 \end{bmatrix}}_{\mathbf{C_1}} \underbrace{\begin{bmatrix} i(t) \\ v(t) \end{bmatrix}}_{\mathbf{x}(t)} + \underbrace{\begin{bmatrix} 0 & 0 \end{bmatrix}}_{\mathbf{E_1}} \underbrace{\begin{bmatrix} v_g(t) \\ V_D \end{bmatrix}}_{\mathbf{u}(t)}$$

Subinterval 2

$$L \frac{di(t)}{dt} = v(t) - V_D$$

$$C \frac{dv(t)}{dt} = -\frac{v(t)}{R} - i(t)$$

$$i_g(t) = 0$$



$$\underbrace{\begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix}}_{\mathbf{K}} \underbrace{\frac{d}{dt}\begin{bmatrix} i(t) \\ v(t) \end{bmatrix}}_{\frac{d\mathbf{x}(t)}{dt}} = \underbrace{\begin{bmatrix} 0 & 1 \\ -1 & -\frac{1}{R} \end{bmatrix}}_{\mathbf{A}_2} \underbrace{\begin{bmatrix} i(t) \\ v(t) \end{bmatrix}}_{\mathbf{x}(t)} + \underbrace{\begin{bmatrix} 0 & -1 \\ 0 & 0 \end{bmatrix}}_{\mathbf{B}_2} \underbrace{\begin{bmatrix} v_g(t) \\ V_D \end{bmatrix}}_{\mathbf{u}(t)}$$

$$\underbrace{\begin{bmatrix} i_g(t) \end{bmatrix}}_{\mathbf{y}(t)} = \underbrace{\begin{bmatrix} 0 & 0 \end{bmatrix}}_{\mathbf{C}_2} \underbrace{\begin{bmatrix} i(t) \\ v(t) \end{bmatrix}}_{\mathbf{x}(t)} + \underbrace{\begin{bmatrix} 0 & 0 \end{bmatrix}}_{\mathbf{E}_2} \underbrace{\begin{bmatrix} v_g(t) \\ V_D \end{bmatrix}}_{\mathbf{u}(t)}$$

Evaluate averaged matrices

$$\mathbf{A} = D\mathbf{A}_1 + D'\mathbf{A}_2 = D\begin{bmatrix} -R_{on} & 0 \\ 0 & -\frac{1}{R} \end{bmatrix} + D'\begin{bmatrix} 0 & 1 \\ -1 & -\frac{1}{R} \end{bmatrix} = \begin{bmatrix} -DR_{on} & D' \\ -D' & -\frac{1}{R} \end{bmatrix}$$

In a similar manner,

$$\mathbf{B} = D\mathbf{B}_1 + D'\mathbf{B}_2 = \begin{bmatrix} D & -D' \\ 0 & 0 \end{bmatrix}$$

$$\mathbf{C} = D\mathbf{C}_1 + D'\mathbf{C}_2 = \begin{bmatrix} D & 0 \end{bmatrix}$$

$$\mathbf{E} = D\mathbf{E}_1 + D'\mathbf{E}_2 = \begin{bmatrix} 0 & 0 \end{bmatrix}$$

DC state equations

$$\mathbf{0} = \mathbf{A}\,\mathbf{X} + \mathbf{B}\,\mathbf{U}$$
$$\mathbf{Y} = \mathbf{C}\,\mathbf{X} + \mathbf{E}\,\mathbf{U}$$

or,

$$\begin{bmatrix} 0 \\ 0 \end{bmatrix} = \begin{bmatrix} -DR_{on} & D' \\ -D' & -\frac{1}{R} \end{bmatrix} \begin{bmatrix} I \\ V \end{bmatrix} + \begin{bmatrix} D & -D' \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_g \\ V_D \end{bmatrix}$$

$$\begin{bmatrix} I_g \end{bmatrix} = \begin{bmatrix} D & 0 \end{bmatrix} \begin{bmatrix} I \\ V \end{bmatrix} + \begin{bmatrix} 0 & 0 \end{bmatrix} \begin{bmatrix} V_g \\ V_D \end{bmatrix}$$

DC solution:

$$\begin{bmatrix} I \\ V \end{bmatrix} = \left(\frac{1}{1 + \frac{D}{D'^2} \frac{R_{on}}{R}} \right) \begin{bmatrix} \frac{D}{D'^2 R} & \frac{1}{D' R} \\ -\frac{D}{D'} & 1 \end{bmatrix} \begin{bmatrix} V_g \\ V_D \end{bmatrix}$$

$$\begin{bmatrix} I_g \end{bmatrix} = \left(\frac{1}{1 + \frac{D}{D'^2} \frac{R_{on}}{R}} \right) \begin{bmatrix} \frac{D^2}{D'^2 R} & \frac{D}{D' R} \end{bmatrix} \begin{bmatrix} V_g \\ V_D \end{bmatrix}$$

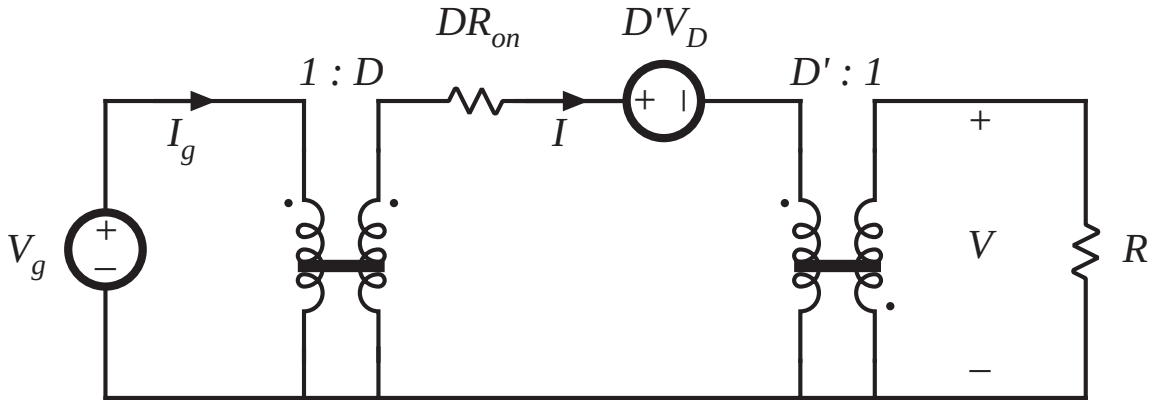
Steady-state equivalent circuit

DC state equations:

$$\begin{bmatrix} 0 \\ 0 \end{bmatrix} = \begin{bmatrix} -DR_{on} & D' \\ -D' & -\frac{1}{R} \end{bmatrix} \begin{bmatrix} I \\ V \end{bmatrix} + \begin{bmatrix} D & -D' \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_g \\ V_D \end{bmatrix}$$

$$\begin{bmatrix} I_g \end{bmatrix} = \begin{bmatrix} D & 0 \end{bmatrix} \begin{bmatrix} I \\ V \end{bmatrix} + \begin{bmatrix} 0 & 0 \end{bmatrix} \begin{bmatrix} V_g \\ V_D \end{bmatrix}$$

Corresponding equivalent circuit:



Small-signal ac model

Evaluate matrices in small-signal model:

$$\left(\mathbf{A}_1 - \mathbf{A}_2\right)\mathbf{X} + \left(\mathbf{B}_1 - \mathbf{B}_2\right)\mathbf{U} = \begin{bmatrix} -V \\ I \end{bmatrix} + \begin{bmatrix} V_g - IR_{on} + V_D \\ 0 \end{bmatrix} = \begin{bmatrix} V_g - V - IR_{on} + V_D \\ I \end{bmatrix}$$

$$\left(\mathbf{C}_1 - \mathbf{C}_2\right)\mathbf{X} + \left(\mathbf{E}_1 - \mathbf{E}_2\right)\mathbf{U} = \begin{bmatrix} I \end{bmatrix}$$

Small-signal ac state equations:

$$\begin{bmatrix} L & 0 \\ 0 & C \end{bmatrix} \frac{d}{dt} \begin{bmatrix} \hat{i}(t) \\ \hat{v}(t) \end{bmatrix} = \begin{bmatrix} -DR_{on} & D' \\ -D' & -\frac{1}{R} \end{bmatrix} \begin{bmatrix} \hat{i}(t) \\ \hat{v}(t) \end{bmatrix} + \begin{bmatrix} D & -D' \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_g(t) \\ \hat{v}_D(t) \end{bmatrix} + \begin{bmatrix} V_g - V - IR_{on} + V_D \\ I \end{bmatrix} \hat{d}(t)$$

$$\begin{bmatrix} \hat{i}_g(t) \end{bmatrix} = \begin{bmatrix} D & 0 \end{bmatrix} \begin{bmatrix} \hat{i}(t) \\ \hat{v}(t) \end{bmatrix} + \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_g(t) \\ \hat{v}_D(t) \end{bmatrix} + \begin{bmatrix} 0 \\ I \end{bmatrix} \hat{d}(t)$$

Construction of ac equivalent circuit

Small-signal ac equations, in scalar form:

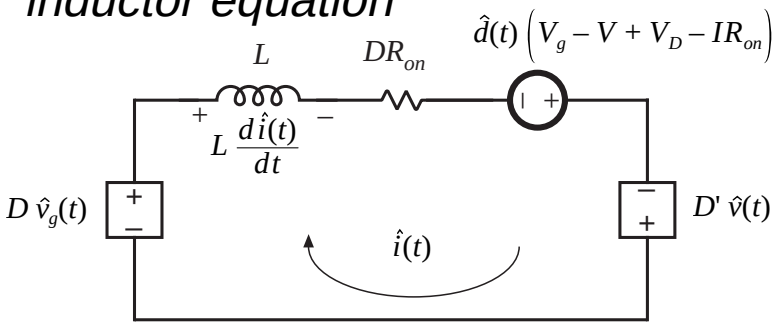
$$L \frac{d\hat{i}(t)}{dt} = D' \hat{v}(t) - DR_{on} \hat{i}(t) + D \hat{v}_g(t) + \left(V_g - V - IR_{on} + V_D \right) \hat{d}(t)$$

$$C \frac{d\hat{v}(t)}{dt} = -D' \hat{i}(t) - \frac{\hat{v}(t)}{R} + I \hat{d}(t)$$

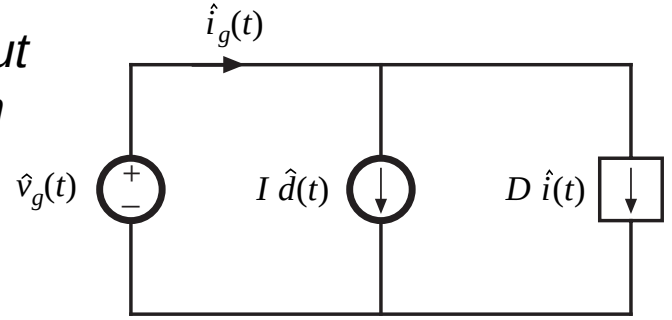
$$\hat{i}_g(t) = D \hat{i}(t) + I \hat{d}(t)$$

Corresponding equivalent circuits:

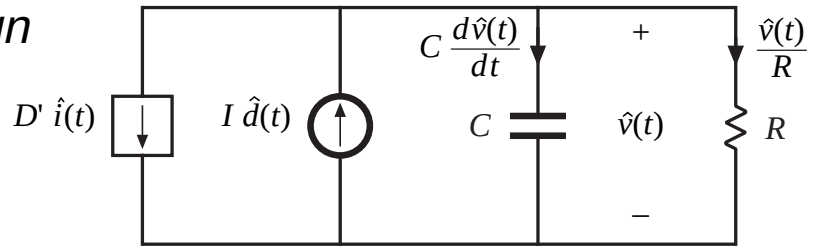
inductor equation



input eqn

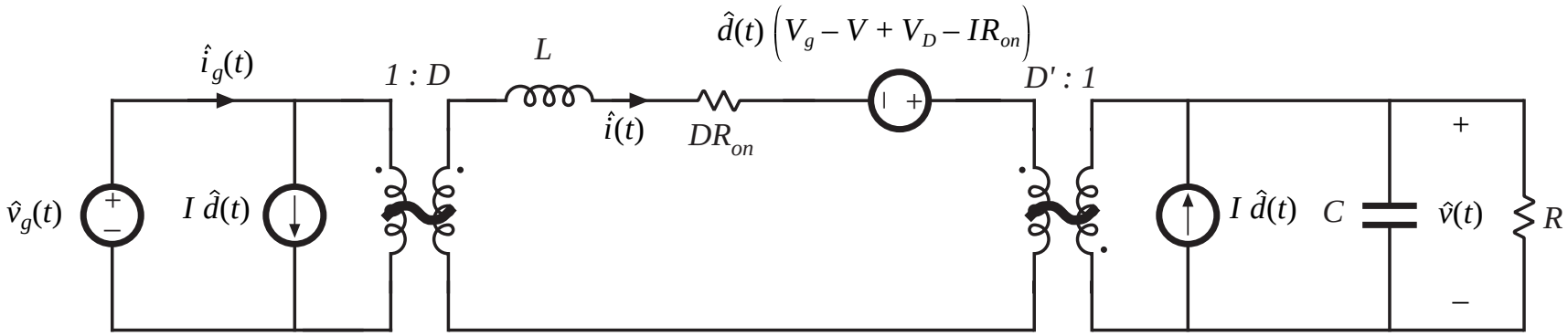


capacitor eqn



Complete small-signal ac equivalent circuit

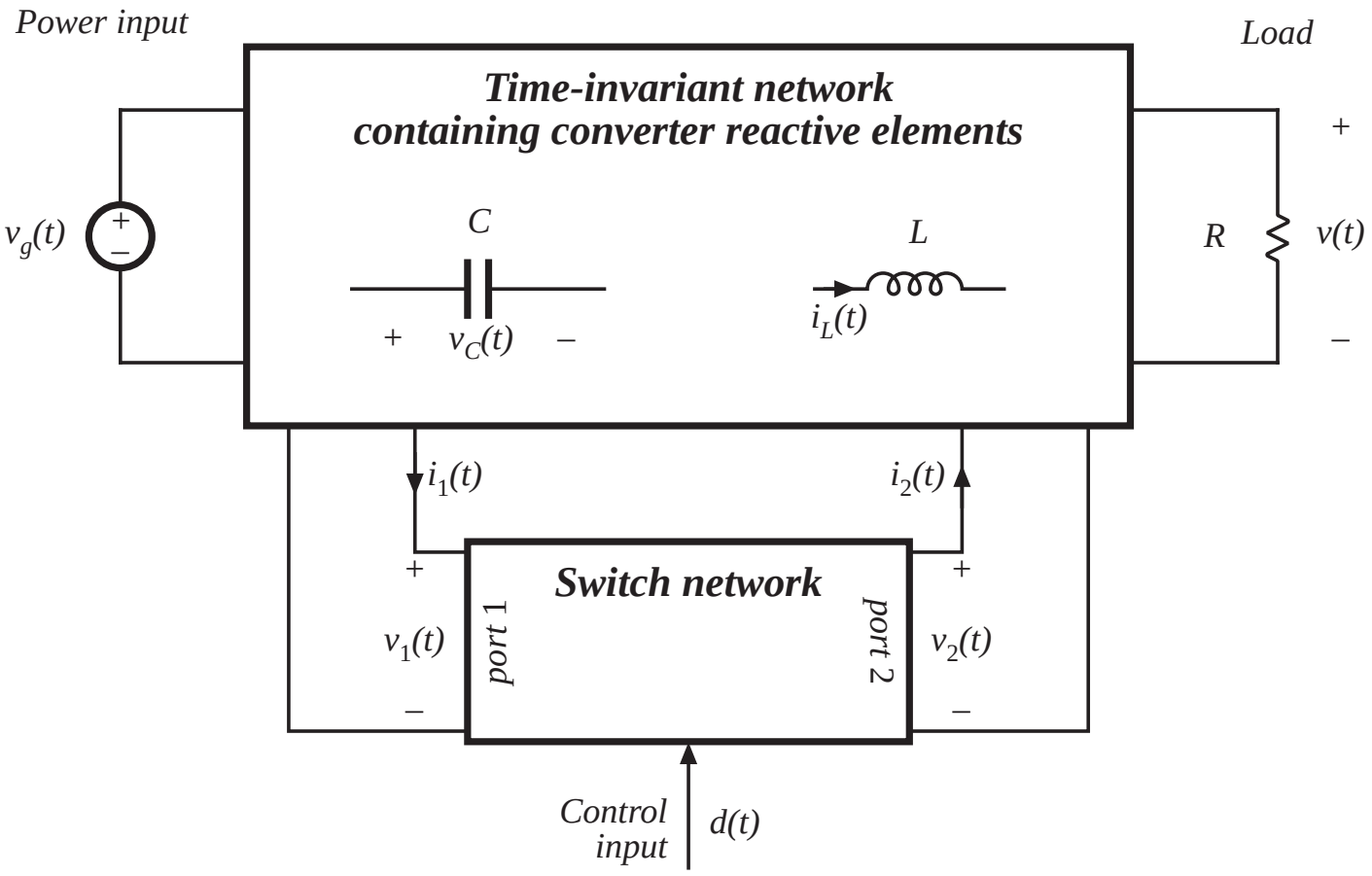
Combine individual circuits to obtain



7.5. Circuit Averaging and Averaged Switch Modeling

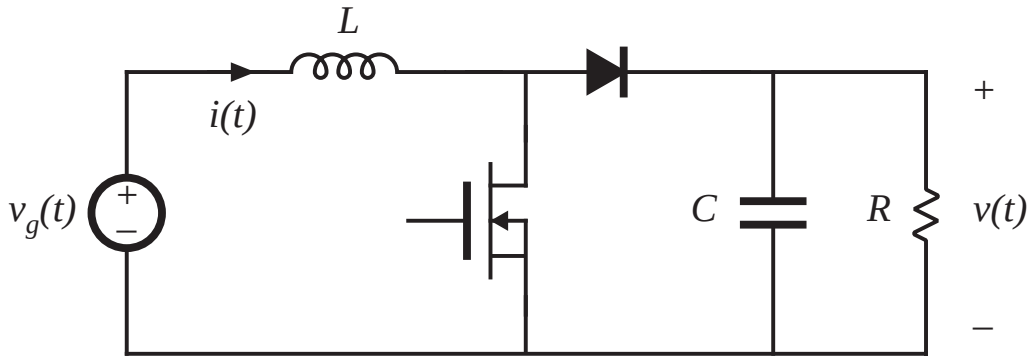
- Historically, circuit averaging was the first method known for modeling the small-signal ac behavior of CCM PWM converters
- It was originally thought to be difficult to apply in some cases
- There has been renewed interest in circuit averaging and its corrolary, averaged switch modeling, in the last decade
- Can be applied to a wide variety of converters
  - We will use it to model DCM, CPM, and resonant converters
  - Also useful for incorporating switching loss into ac model of CCM converters
  - Applicable to 3ø PWM inverters and rectifiers
  - Can be applied to phase-controlled rectifiers
- Rather than averaging and linearizing the converter state equations, the averaging and linearization operations are performed directly on the converter circuit

Separate switch network from remainder of converter



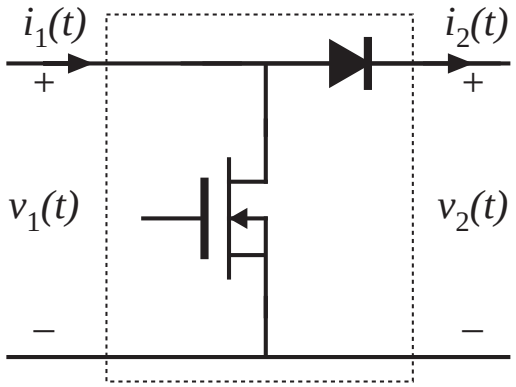
Boost converter example

Ideal boost converter example

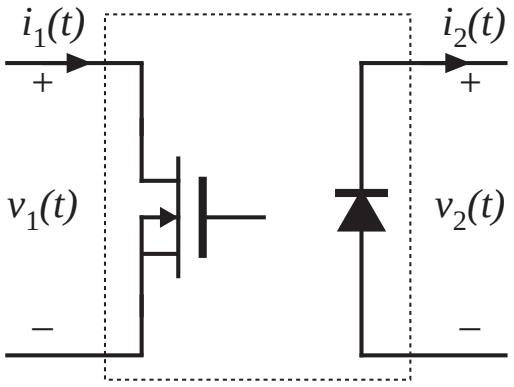


Two ways to define the switch network

(a)



(b)



Discussion

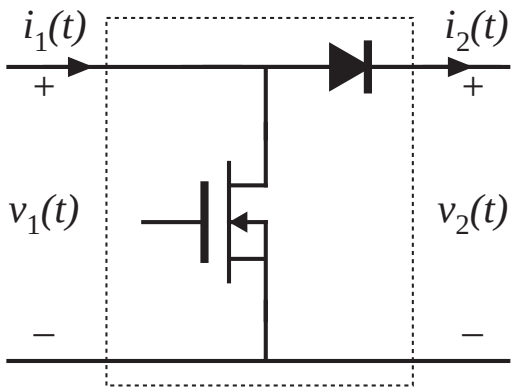
- The number of ports in the switch network is less than or equal to the number of SPST switches
- Simple dc-dc case, in which converter contains two SPST switches: switch network contains two ports

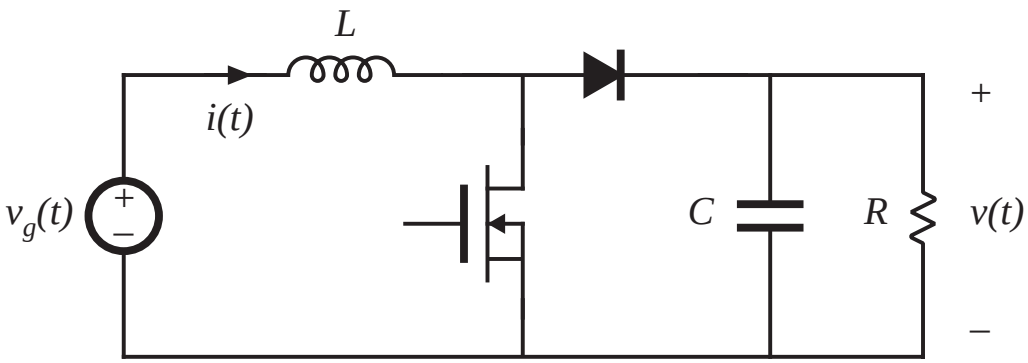
  The switch network terminal waveforms are then the port voltages and currents: $v_1(t)$, $i_1(t)$, $v_2(t)$, and $i_2(t)$.

  Two of these waveforms can be taken as independent inputs to the switch network; the remaining two waveforms are then viewed as dependent outputs of the switch network.
- Definition of the switch network terminal quantities is not unique. Different definitions lead equivalent results having different forms

Boost converter example

Let's use definition *(a):*

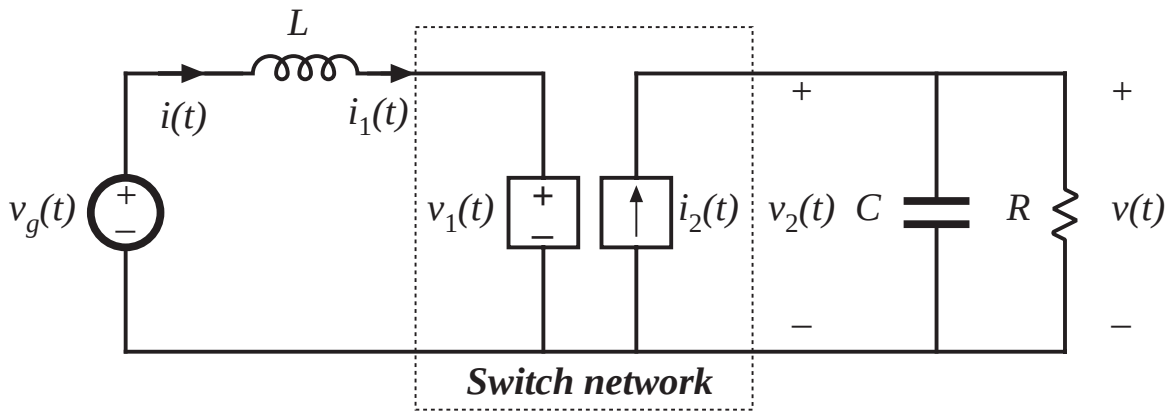




Since $i_1(t)$ and $v_2(t)$ coincide with the converter inductor current and output voltage, it is convenient to define these waveforms as the independent inputs to the switch network. The switch network dependent outputs are then $v_1(t)$ and $i_2(t)$.

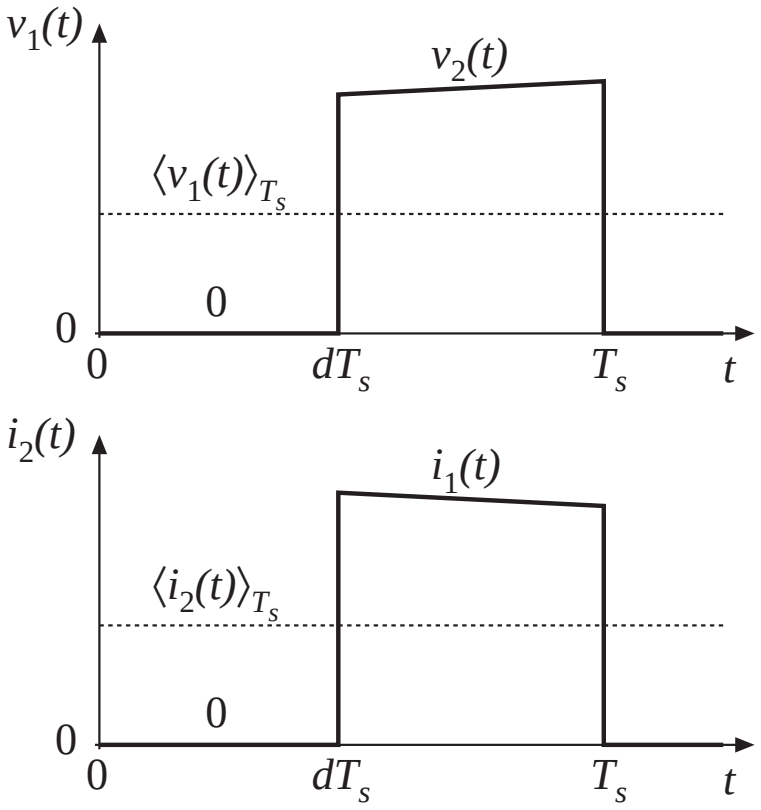
Obtaining a time-invariant network: Modeling the terminal behavior of the switch network

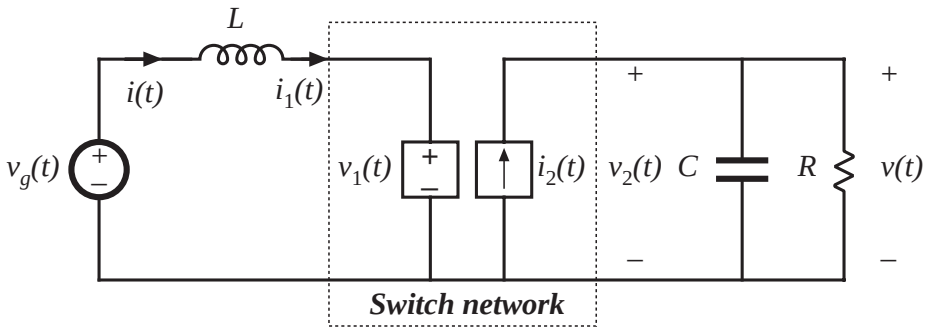
Replace the switch network with dependent sources, which correctly represent the dependent output waveforms of the switch network



Boost converter example

Definition of dependent generator waveforms





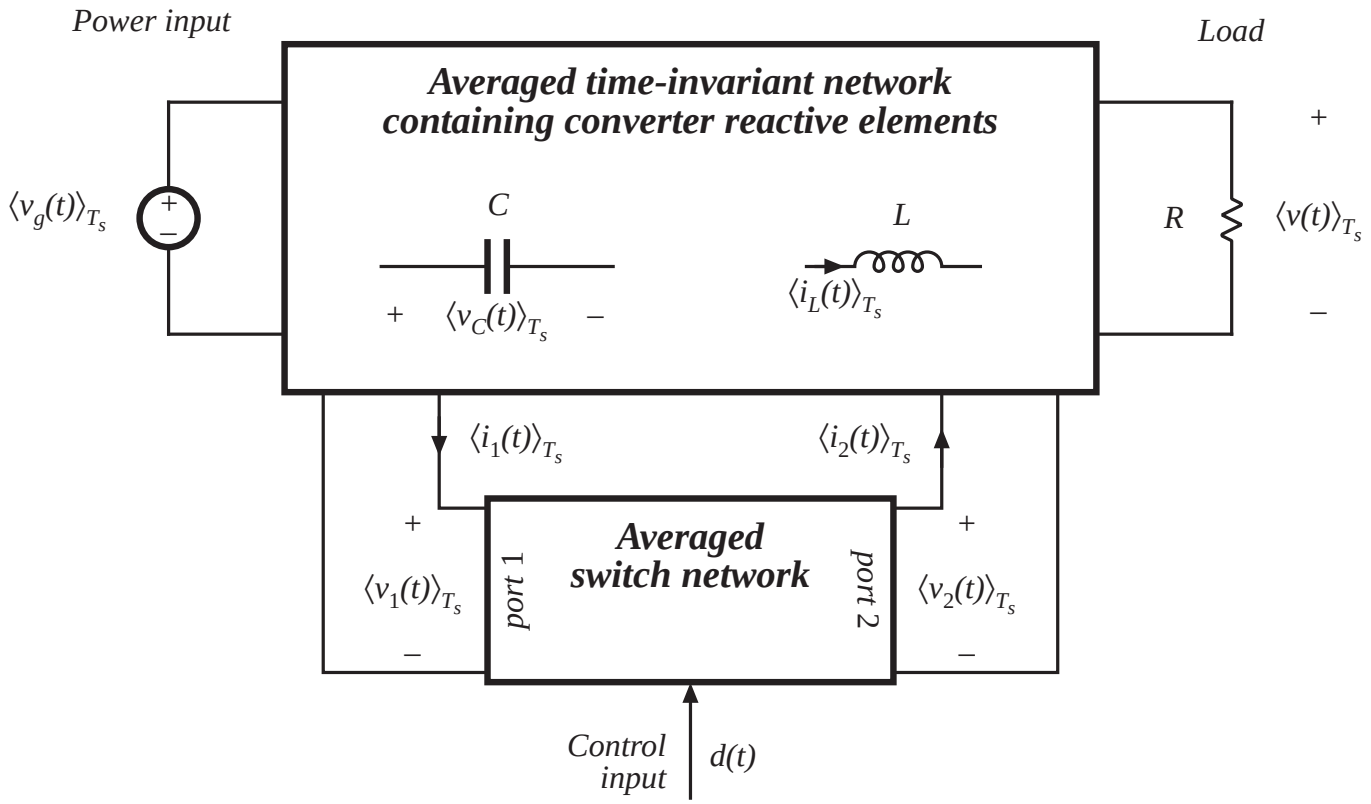
The waveforms of the dependent generators are defined to be identical to the actual terminal waveforms of the switch network.

The circuit is therefore electrical identical to the original converter.

So far, no approximations have been made.

The circuit averaging step

Now average all waveforms over one switching period:

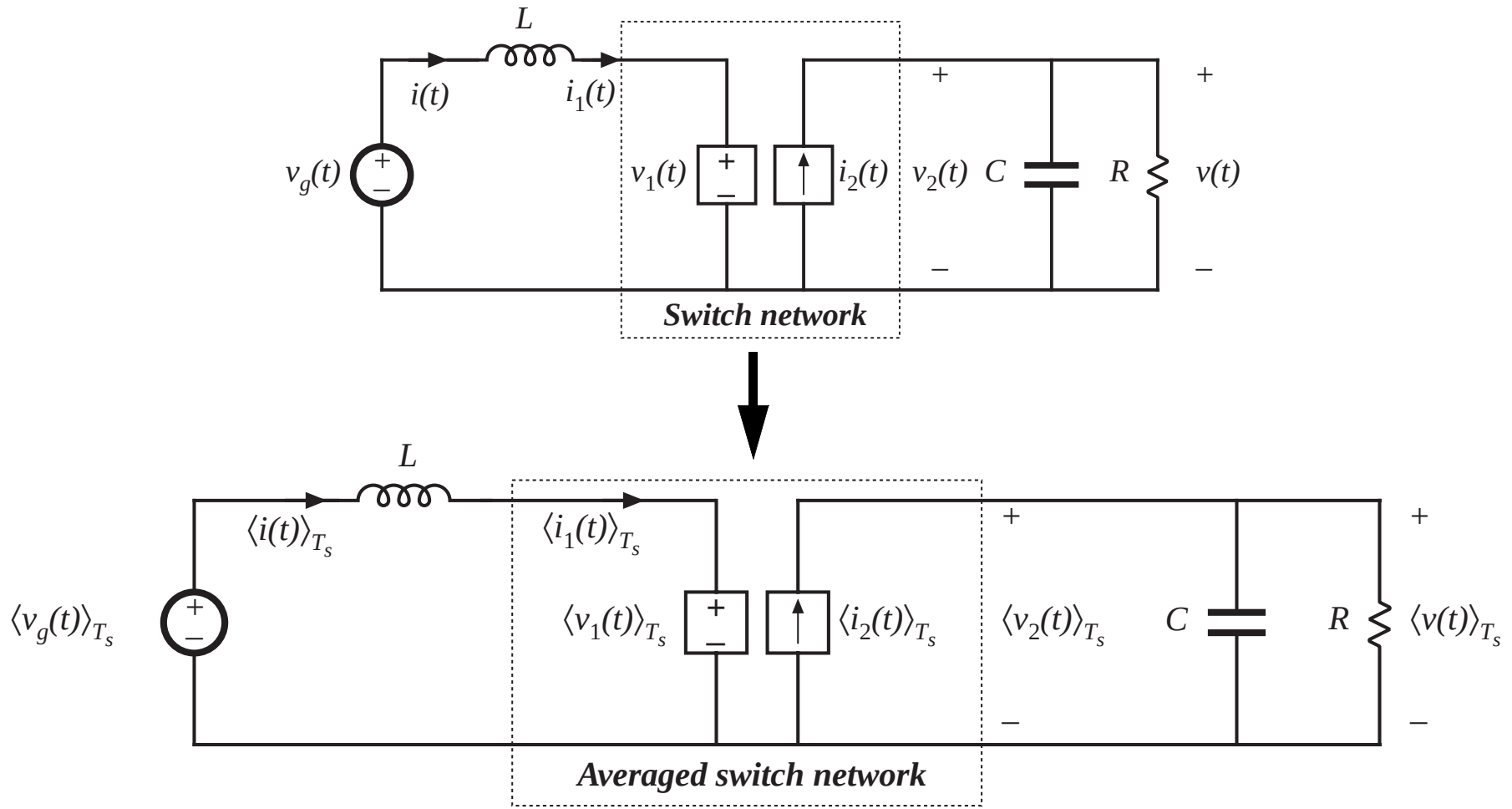


The averaging step

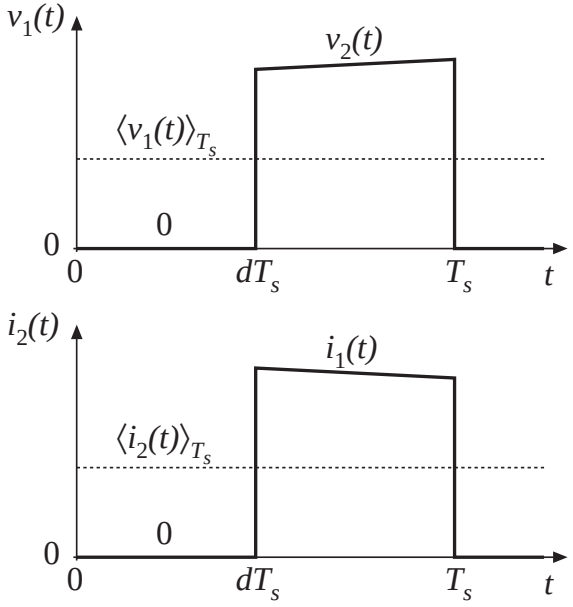
The basic assumption is made that the natural time constants of the converter are much longer than the switching period, so that the converter contains low-pass filtering of the switching harmonics. One may average the waveforms over an interval that is short compared to the system natural time constants, without significantly altering the system response. In particular, averaging over the switching period T_s removes the switching harmonics, while preserving the low-frequency components of the waveforms.

In practice, the only work needed for this step is to average the switch dependent waveforms.

Averaging step: boost converter example



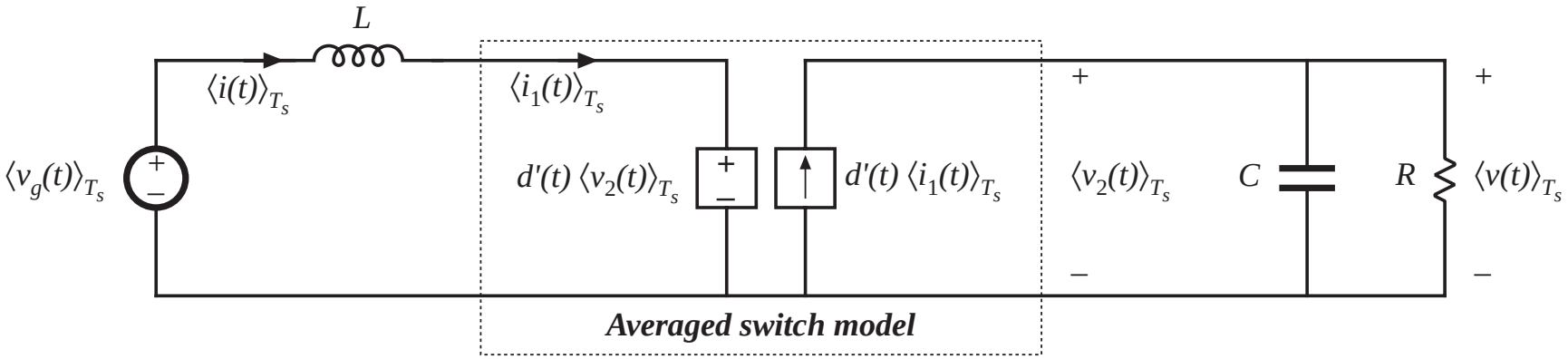
Compute average values of dependent sources



Average the waveforms of the dependent sources:

$$\left\langle v_1(t) \right\rangle_{T_s} = d'(t) \left\langle v_2(t) \right\rangle_{T_s}$$

$$\left\langle i_2(t) \right\rangle_{T_s} = d'(t) \left\langle i_1(t) \right\rangle_{T_s}$$



Perturb and linearize

As usual, let:

$$\left\langle v_g(t) \right\rangle_{T_s} = V_g + \hat{v}_g(t)$$

$$d(t) = D + \hat{d}(t) \quad \Rightarrow d'(t) = D' - \hat{d}(t)$$

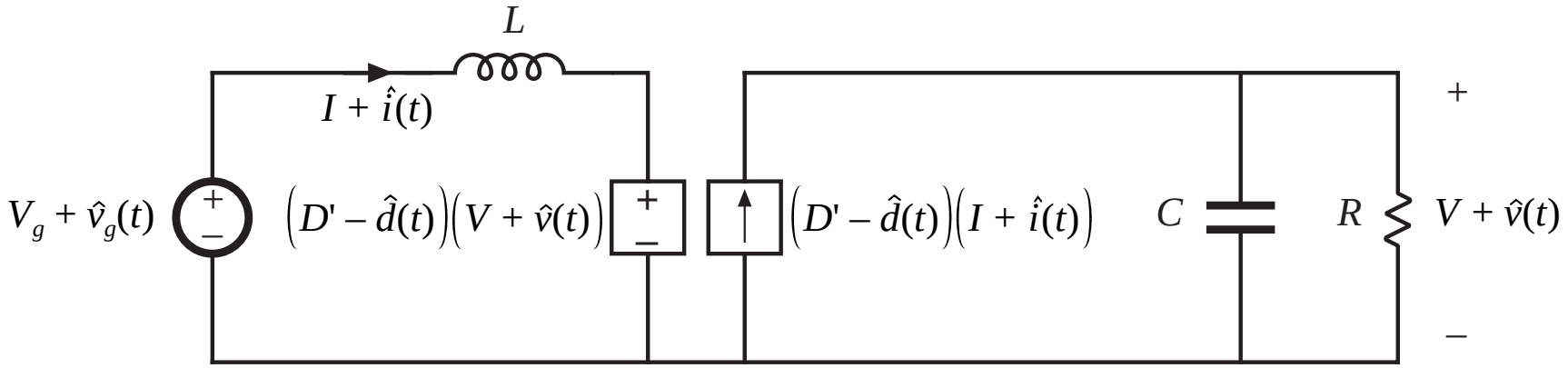
$$\left\langle i(t) \right\rangle_{T_s} = \left\langle i_1(t) \right\rangle_{T_s} = I + \hat{i}(t)$$

$$\left\langle v(t) \right\rangle_{T_s} = \left\langle v_2(t) \right\rangle_{T_s} = V + \hat{v}(t)$$

$$\left\langle v_1(t) \right\rangle_{T_s} = V_1 + \hat{v}_1(t)$$

$$\left\langle i_2(t) \right\rangle_{T_s} = I_2 + \hat{i}_2(t)$$

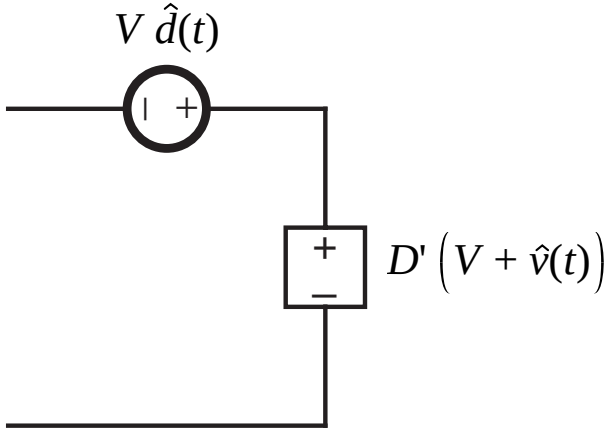
The circuit becomes:



Dependent voltage source

$$\left(D' - \hat{d}(t)\right)\left(V + \hat{v}(t)\right) = D'\left(V + \hat{v}(t)\right) - V\hat{d}(t) - \hat{v}(t)\hat{d}(t)$$

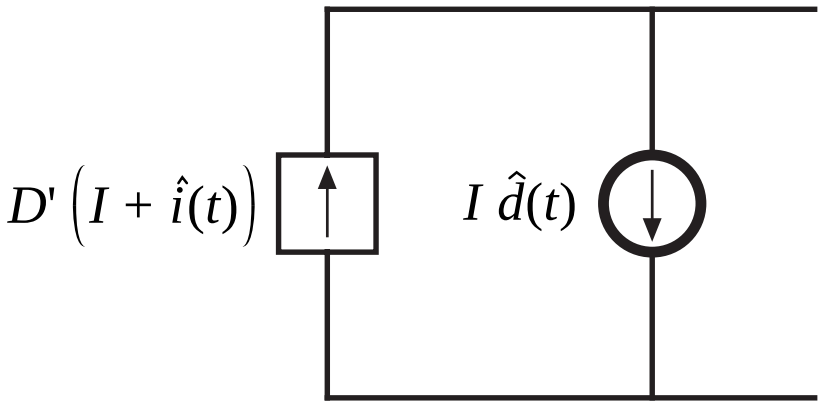
nonlinear, 2nd order



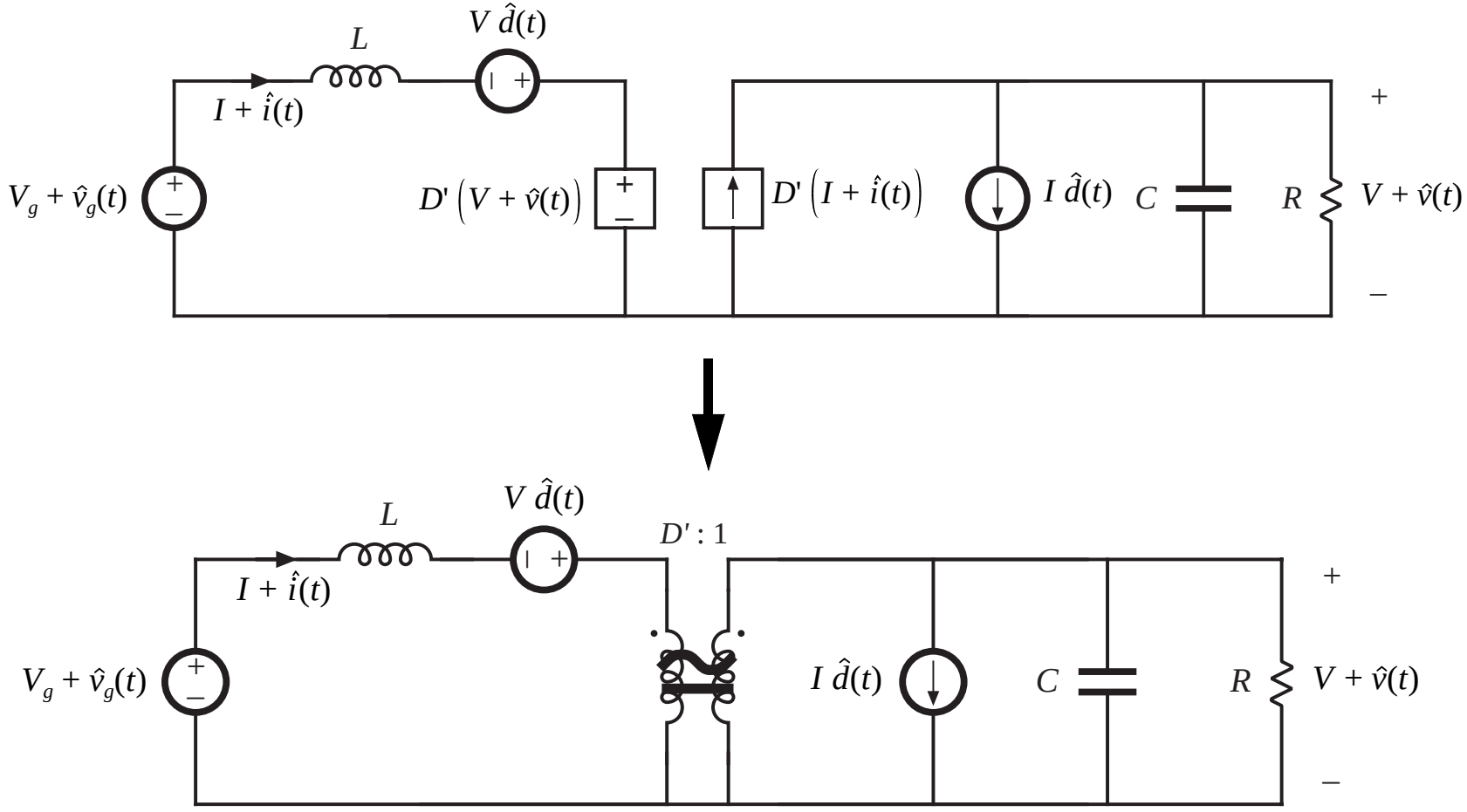
Dependent current source

$$\left(D' - \hat{d}(t)\right)\left(I + \hat{i}(t)\right) = D'\left(I + \hat{i}(t)\right) - I\,\hat{d}(t) - \hat{i}(t)\,\hat{d}(t)$$

nonlinear, 2nd order



Linearized circuit-averaged model



Summary: Circuit averaging method

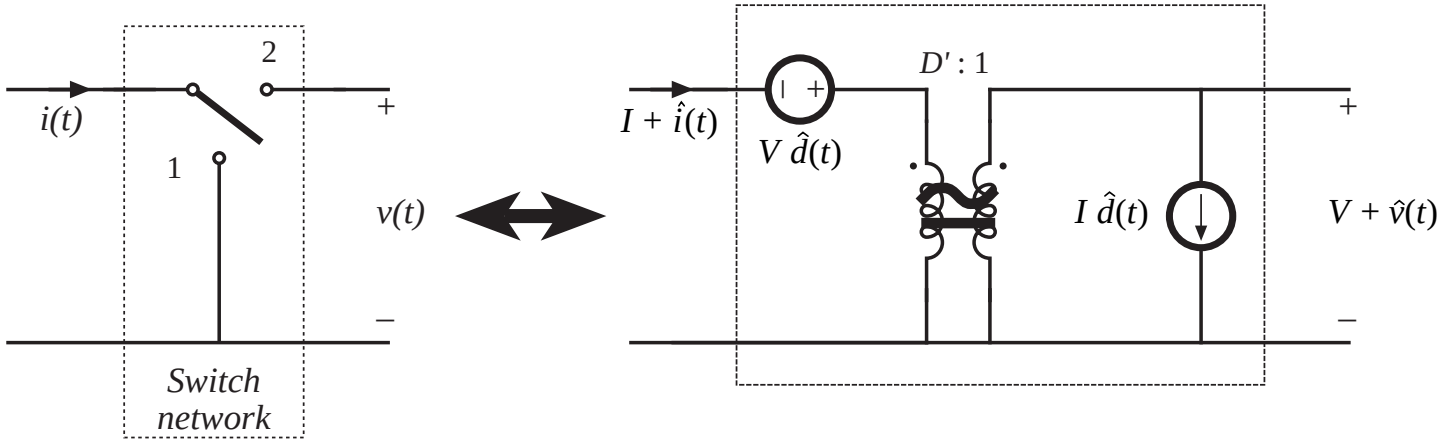
Model the switch network with equivalent voltage and current sources, such that an equivalent time-invariant network is obtained

Average converter waveforms over one switching period, to remove the switching harmonics

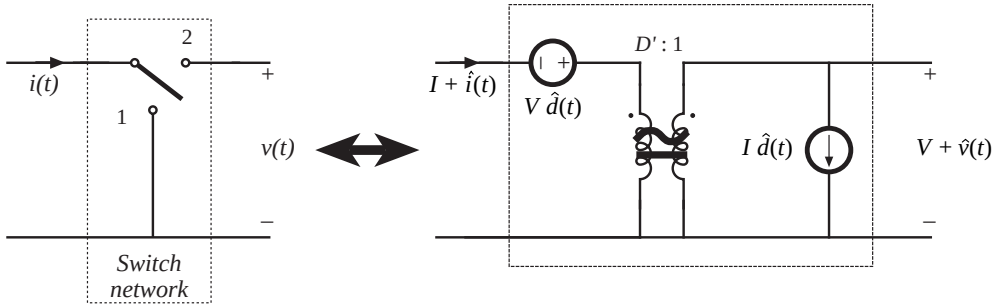
Perturb and linearize the resulting low-frequency model, to obtain a small-signal equivalent circuit

Averaged switch modeling: CCM

Circuit averaging of the boost converter: in essence, the switch network was replaced with an effective ideal transformer and generators:



Basic functions performed by switch network



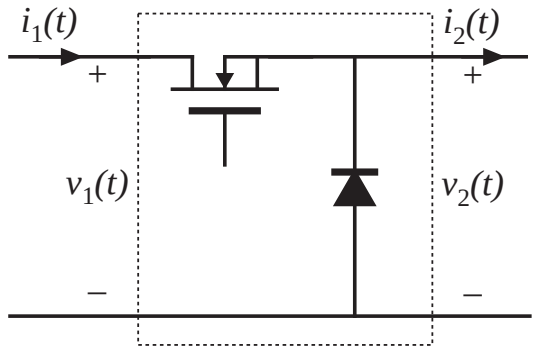
For the boost example, we can conclude that the switch network performs two basic functions:

- Transformation of dc and small-signal ac voltage and current levels, according to the D':1 conversion ratio
- Introduction of ac voltage and current variations, drive by the control input duty cycle variations

Circuit averaging modifies only the switch network. Hence, to obtain a small-signal converter model, we need only replace the switch network with its averaged model. Such a procedure is called *averaged switch modeling.*

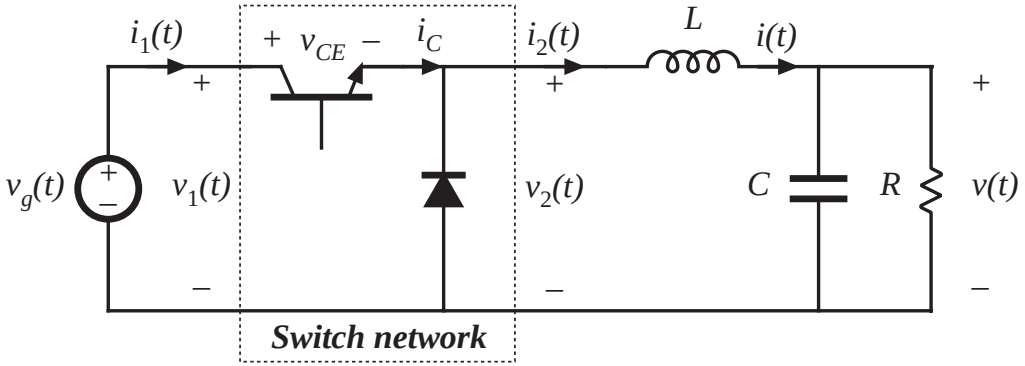
Averaged switch modeling: Procedure

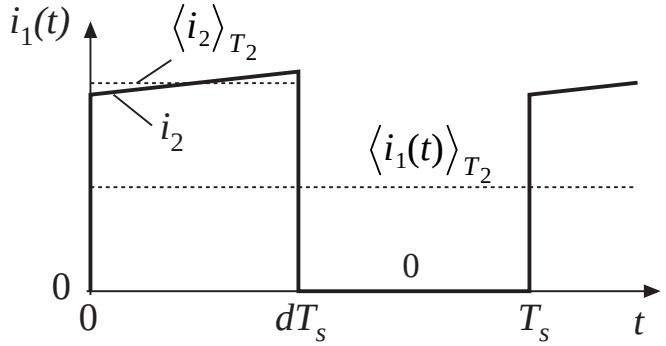
1. Define a switch network and its terminal waveforms. For a simple transistor-diode switch network as in the buck, boost, etc., there are two ports and four terminal quantities: v_1, i_1, v_2, i_2.The switch network also contains a control input d. Buck example:

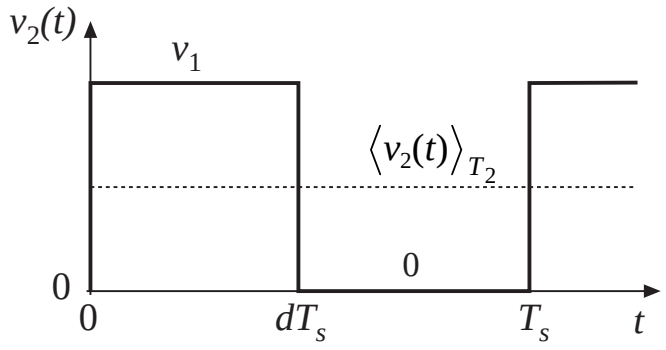


2. To derive an averaged switch model, express the average values of two of the terminal quantities, for example $\langle v_2 \rangle_{T_s}$ and $\langle i_1 \rangle_{T_s}$, as functions of the other average terminal quantities $\langle v_1 \rangle_{T_s}$ and $\langle i_1 \rangle_{T_s}$. $\langle v_2 \rangle_{T_s}$ and $\langle i_1 \rangle_{T_s}$ may also be functions of the control input d, but they should not be expressed in terms of other converter signals.

The basic buck-type CCM switch cell





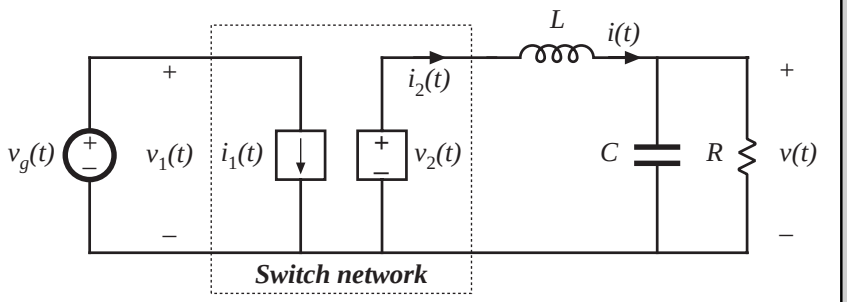


$$\left\langle i_1(t) \right\rangle_{T_s} = d(t) \left\langle i_2(t) \right\rangle_{T_s}$$

$$\left\langle v_2(t) \right\rangle_{T_s} = d(t) \left\langle v_1(t) \right\rangle_{T_s}$$

Replacement of switch network by dependent sources, CCM buck example

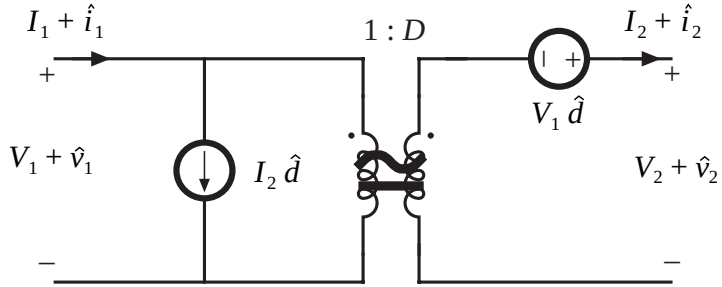
Circuit-averaged model



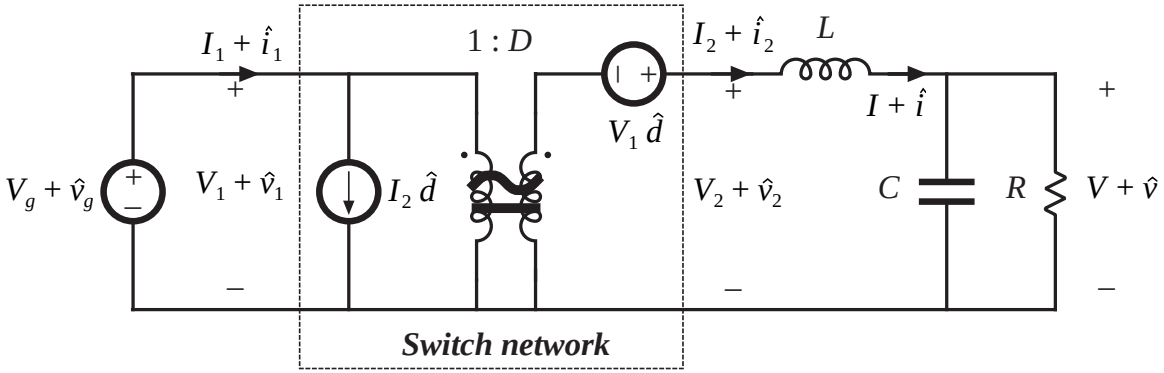
Perturbation and linearization of switch network:

$$I_1 + \hat{i}_1(t) = D\left(I_2 + \hat{i}_2(t)\right) + I_2\,\hat{d}(t)$$

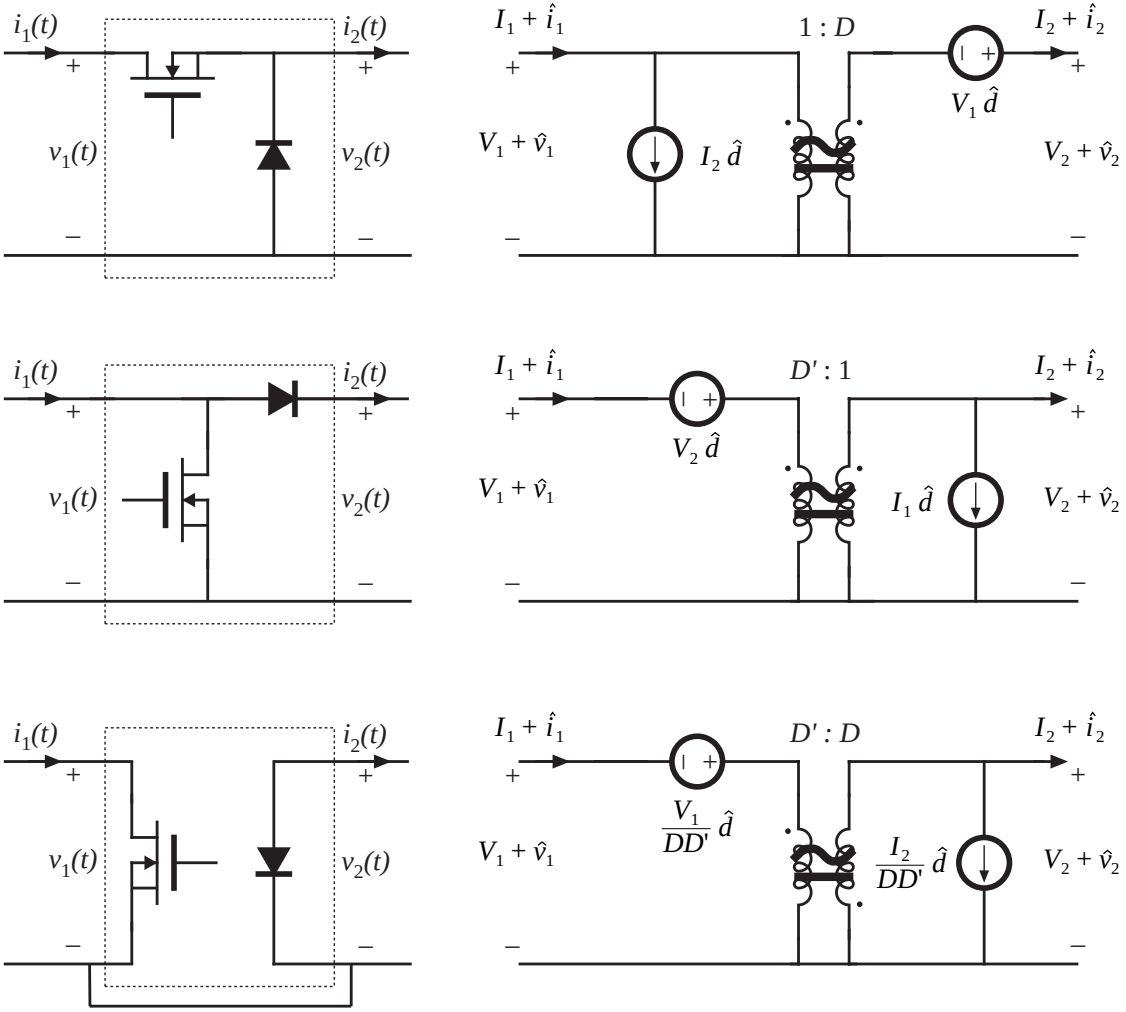
$$V_2 + \hat{v}_2(t) = D\left(V_1 + \hat{v}_1(t)\right) + V_1\,\hat{d}(t)$$



Resulting averaged switch model: CCM buck converter



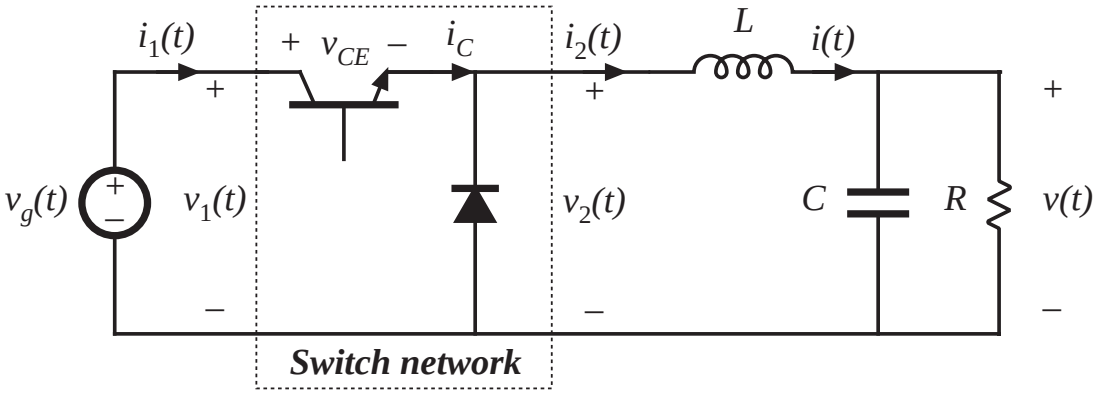
Three basic switch networks, and their CCM dc and small-signal ac averaged switch models

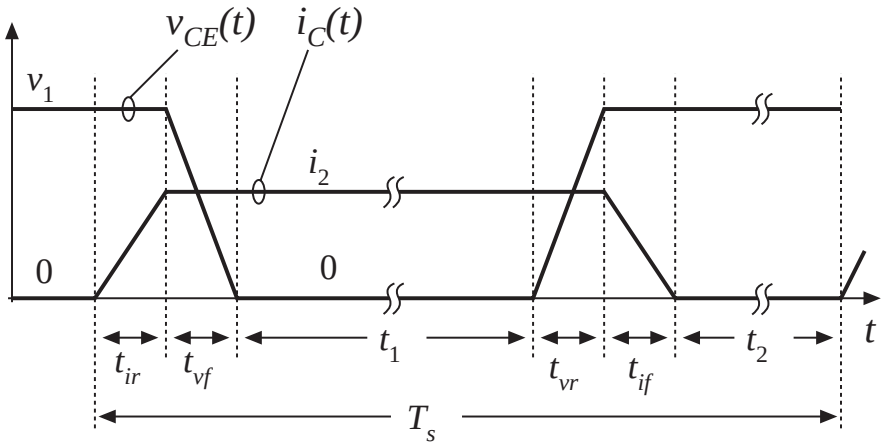


see also

Appendix 3
Averaged switch modeling of a CCM SEPIC

Example: Averaged switch modeling of CCM buck converter, including switching loss

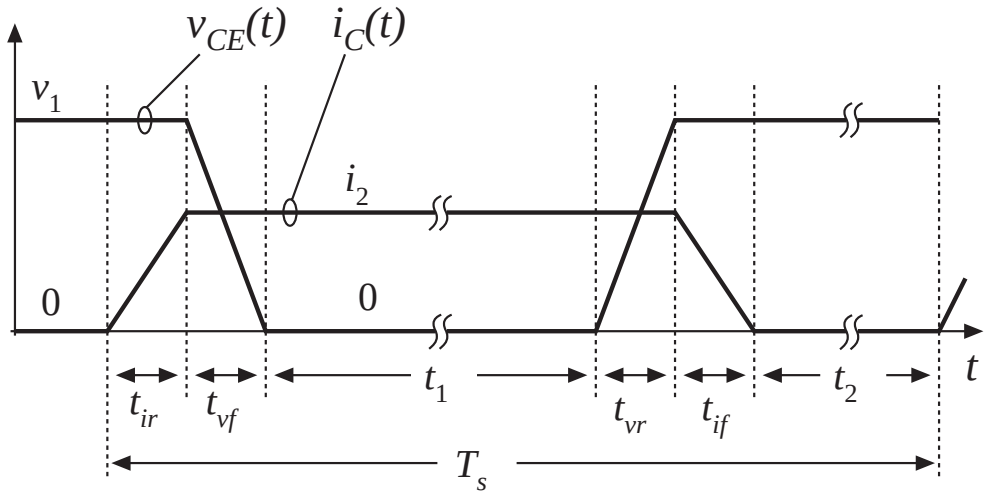




$$i_1(t) = i_C(t)$$
$$v_2(t) = v_1(t) - v_{CE}(t)$$

Switch network terminal waveforms: v_1, i_1, v_2, i_2. To derive averaged switch model, express $\langle v_2 \rangle_{Ts}$ and $\langle i_1 \rangle_{Ts}$ as functions of $\langle v_1 \rangle_{Ts}$ and $\langle i_1 \rangle_{Ts}$. $\langle v_2 \rangle_{Ts}$ and $\langle i_1 \rangle_{Ts}$ may also be functions of the control input d, but they should not be expressed in terms of other converter signals.

Averaging $i_1(t)$



$$\left\langle i_1(t) \right\rangle_{T_s} = \frac{1}{T_s} \int_0^{T_s} i_1(t)\, dt$$

$$= \left\langle i_2(t) \right\rangle_{T_s} \left(\frac{t_1 + t_{vf} + t_{vr} + \frac{1}{2} t_{ir} + \frac{1}{2} t_{if}}{T_s} \right)$$

Expression for $\langle i_1(t) \rangle$

Given

$$\left\langle i_1(t) \right\rangle_{T_s} = \frac{1}{T_s} \int_0^{T_s} i_1(t)\, dt$$

$$= \left\langle i_2(t) \right\rangle_{T_s} \left(\frac{t_1 + t_{vf} + t_{vr} + \frac{1}{2} t_{ir} + \frac{1}{2} t_{if}}{T_s} \right)$$

Let

$$d = \left(\frac{t_1 + \frac{1}{2} t_{vf} + \frac{1}{2} t_{vr} + \frac{1}{2} t_{ir} + \frac{1}{2} t_{if}}{T_s} \right)$$

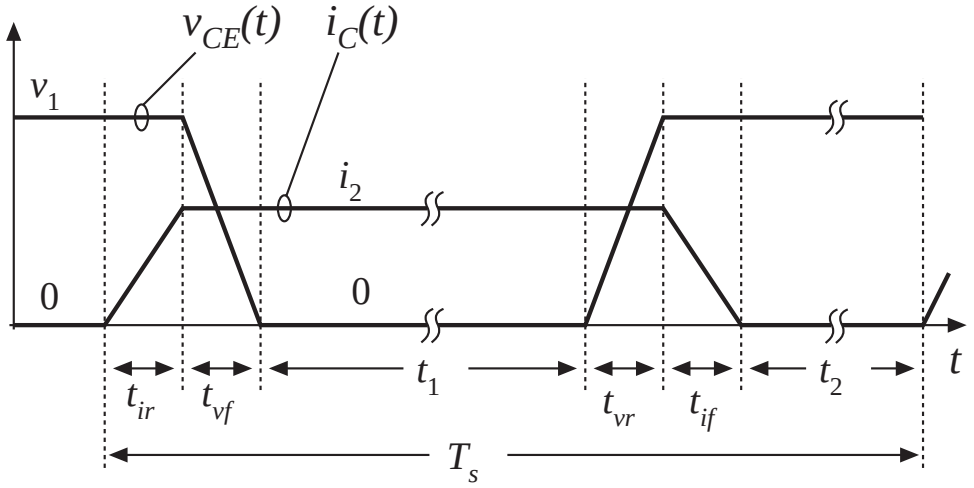
$$d_v = \left(\frac{t_{vf} + t_{vr}}{T_s} \right)$$

$$d_i = \left(\frac{t_{ir} + t_{if}}{T_s} \right)$$

Then we can write

$$\left\langle i_1(t) \right\rangle_{T_s} = \left\langle i_2(t) \right\rangle_{T_s} \left(d + \frac{1}{2} d_v \right)$$

Averaging the switch network output voltage $v_2(t)$



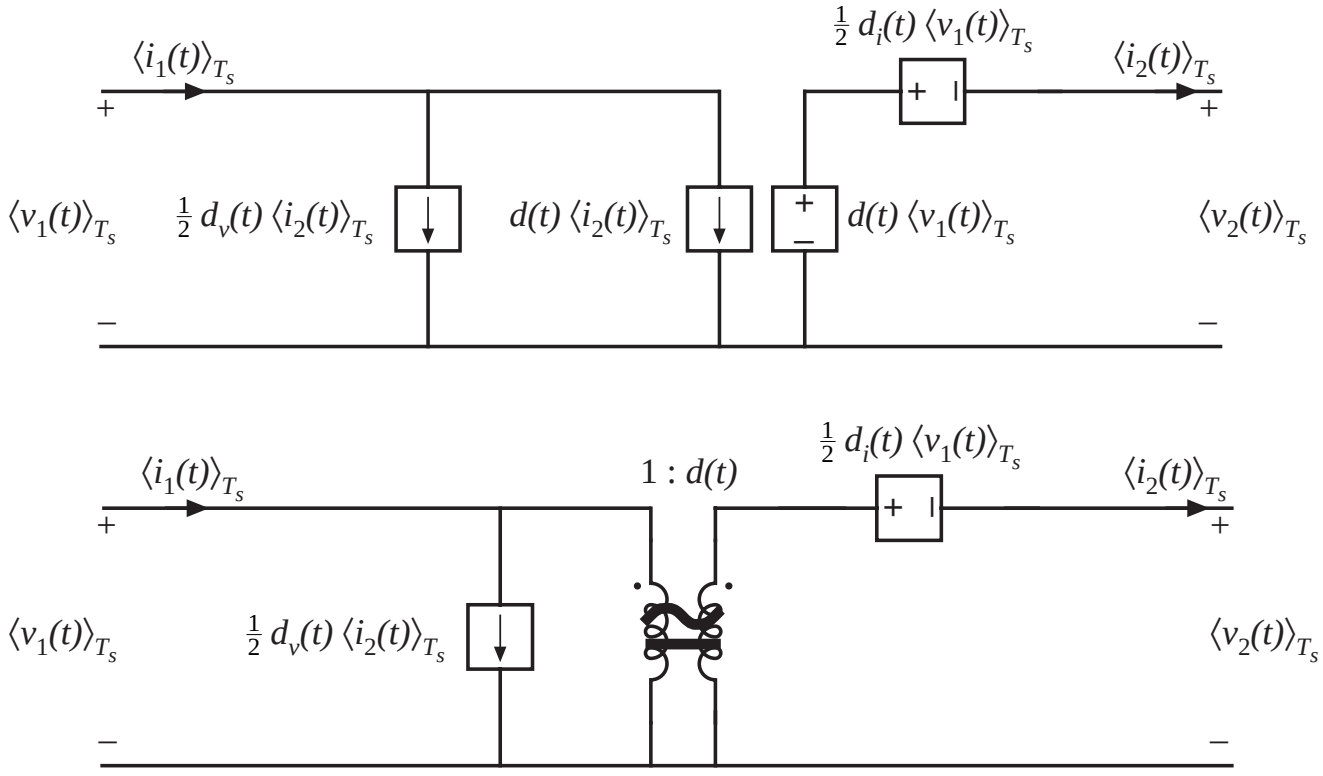
$$\left\langle v_2(t)\right\rangle_{T_s} = \left\langle v_1(t) - v_{CE}(t)\right\rangle_{T_s} = \frac{1}{T_s}\int_0^{T_s}\left(-v_{CE}(t)\right)dt + \left\langle v_1(t)\right\rangle_{T_s}$$

$$\left\langle v_2(t)\right\rangle_{T_s} = \left\langle v_1(t)\right\rangle_{T_s}\left(\frac{t_1 + \frac{1}{2}\,t_{vf} + \frac{1}{2}\,t_{vr}}{T_s}\right)$$

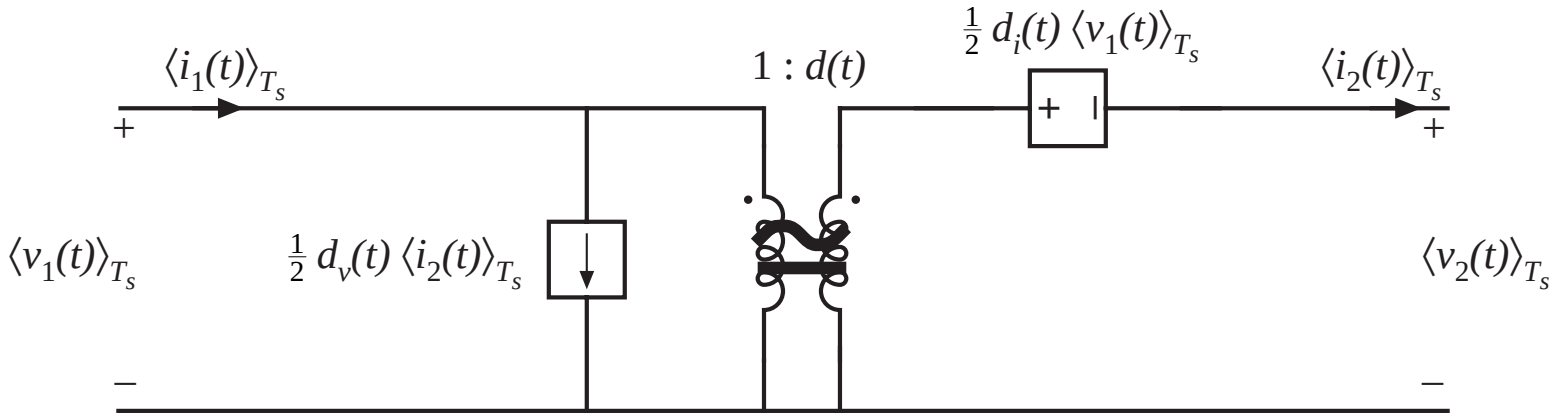
$$\left\langle v_2(t)\right\rangle_{T_s} = \left\langle v_1(t)\right\rangle_{T_s}\left(d - \frac{1}{2}\,d_i\right)$$

Construction of large-signal averaged-switch model

$$\left\langle i_1(t)\right\rangle_{T_s} = \left\langle i_2(t)\right\rangle_{T_s}\left(d + \frac{1}{2}\,d_v\right) \qquad \left\langle v_2(t)\right\rangle_{T_s} = \left\langle v_1(t)\right\rangle_{T_s}\left(d - \frac{1}{2}\,d_i\right)$$

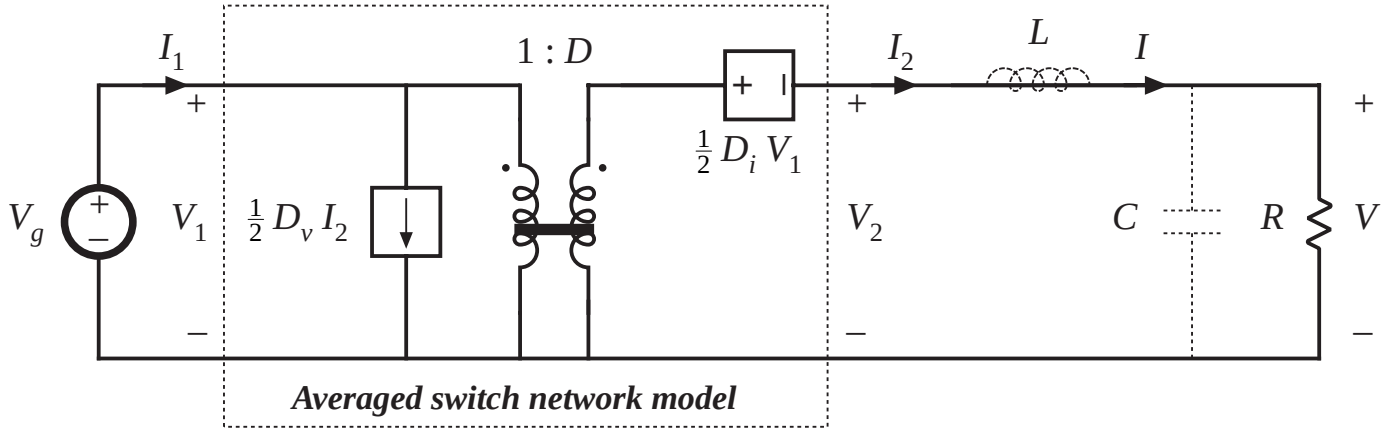


Switching loss predicted by averaged switch model



$$P_{sw} = \frac{1}{2}\left(d_v + d_i\right)\left\langle i_2(t)\right\rangle_{T_s}\left\langle v_1(t)\right\rangle_{T_s}$$

Solution of averaged converter model in steady state



Output voltage:

$$V = \left(D - \tfrac{1}{2} D_i\right) V_g = D V_g \left(1 - \frac{D_i}{2D}\right)$$

Efficiency calcuation:

$$P_{in} = V_g I_1 = V_1 I_2 \left(D + \tfrac{1}{2} D_v\right)$$

$$P_{out} = V I_2 = V_1 I_2 \left(D - \tfrac{1}{2} D_i\right)$$

$$\eta = \frac{P_{out}}{P_{in}} = \frac{\left(D - \tfrac{1}{2} D_i\right)}{\left(D + \tfrac{1}{2} D_v\right)} = \frac{\left(1 - \frac{D_i}{2D}\right)}{\left(1 + \frac{D_v}{2D}\right)}$$

7.6. The canonical circuit model

All PWM CCM dc-dc converters perform the same basic functions:

- Transformation of voltage and current levels, ideally with 100% efficiency
- Low-pass filtering of waveforms
- Control of waveforms by variation of duty cycle

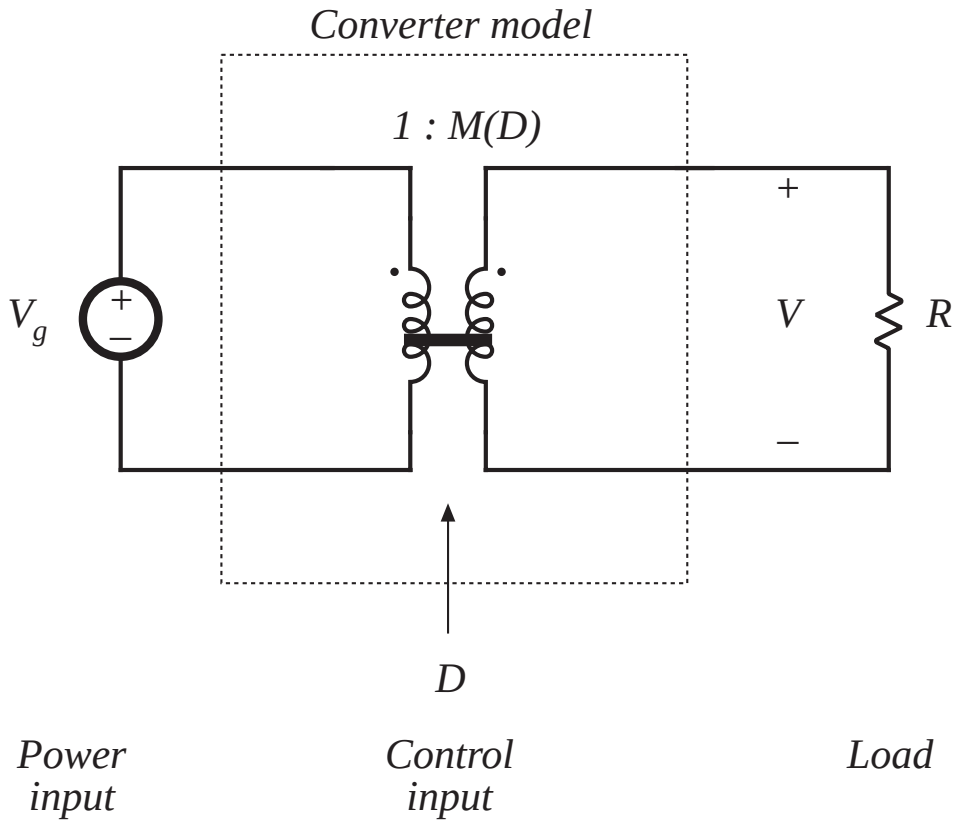
Hence, we expect their equivalent circuit models to be qualitatively similar.

Canonical model:

- A standard form of equivalent circuit model, which represents the above physical properties
- Plug in parameter values for a given specific converter

7.6.1. Development of the canonical circuit model

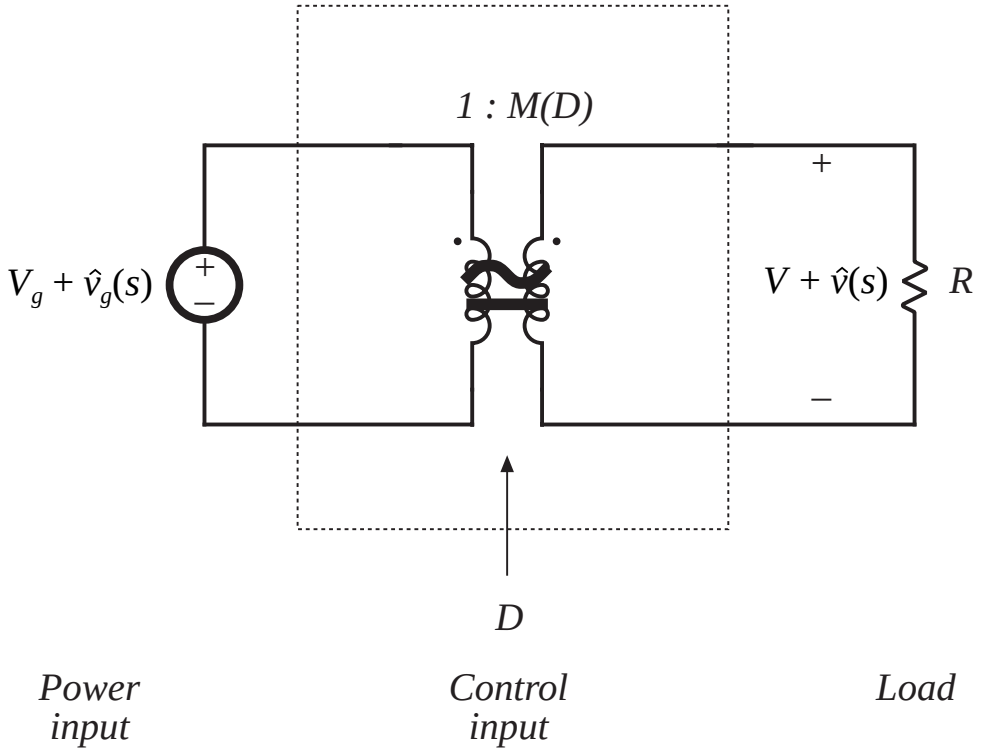
1. *Transformation of dc voltage and current levels*
   - *modeled as in Chapter 3 with ideal dc transformer*
   - *effective turns ratio M(D)*
   - *can refine dc model by addition of effective loss elements, as in Chapter 3*



Steps in the development of the canonical circuit model

2. *Ac variations in $v_g(t)$ induce ac variations in $v(t)$*

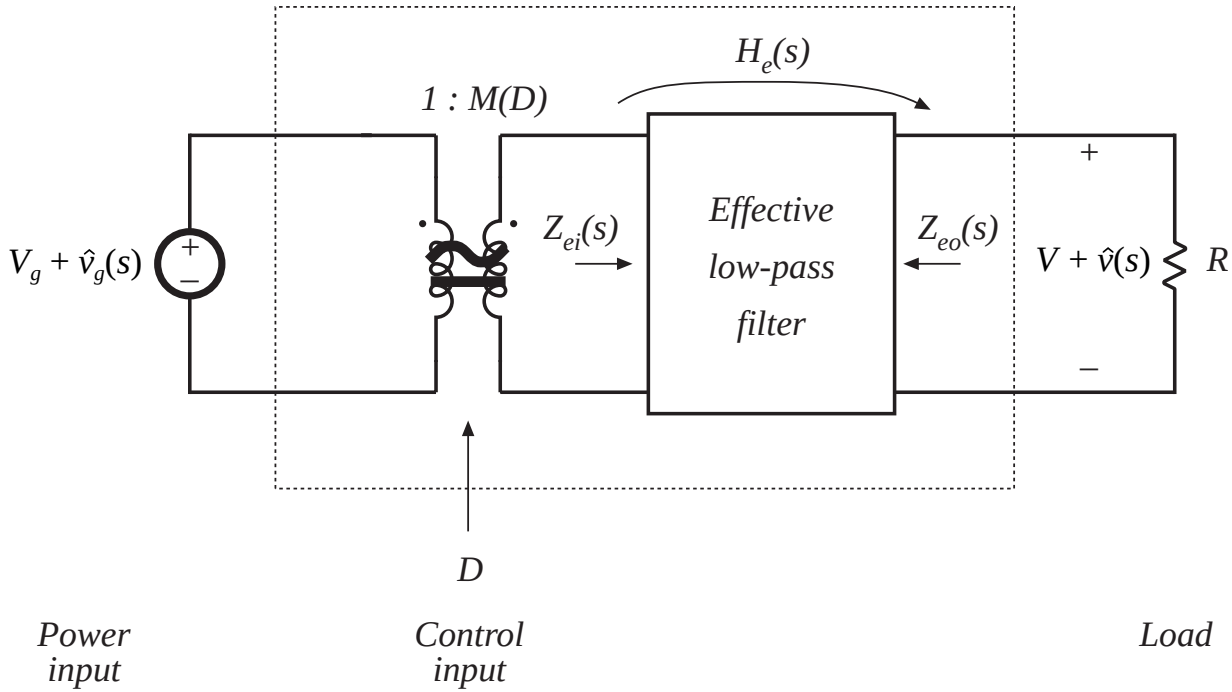
- *these variations are also transformed by the conversion ratio $M(D)$*



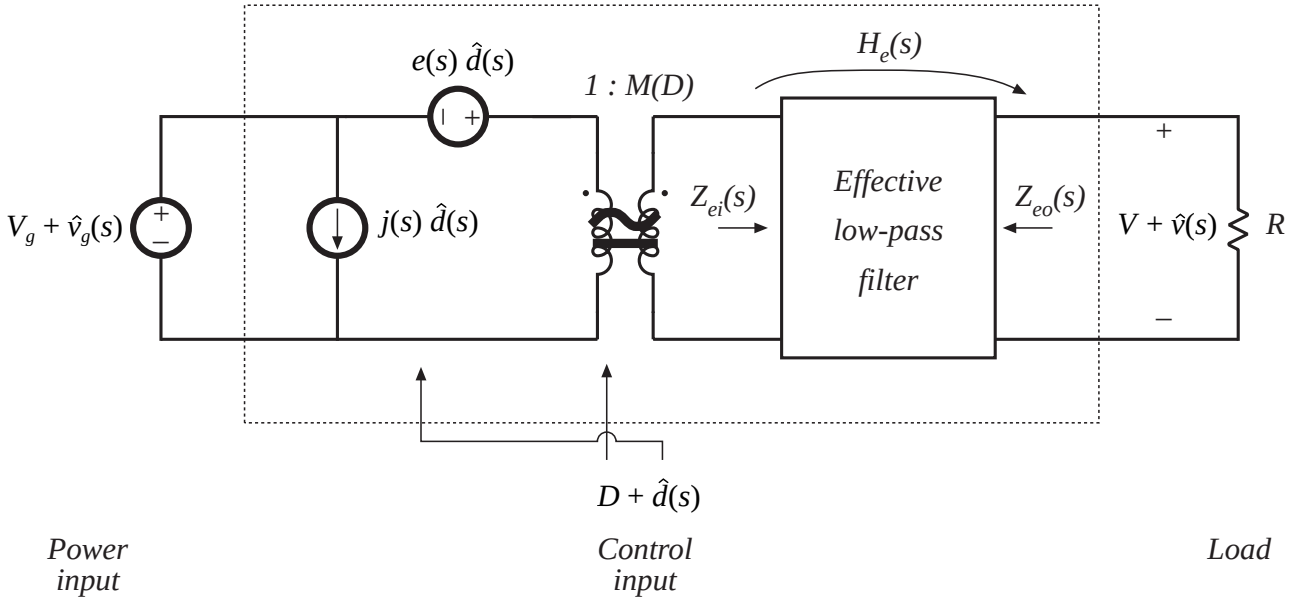
Steps in the development of the canonical circuit model

3. *Converter must contain an effective low-pass filter characteristic*

- *necessary to filter switching ripple*
- *also filters ac variations*
- *effective filter elements may not coincide with actual element values, but can also depend on operating point*



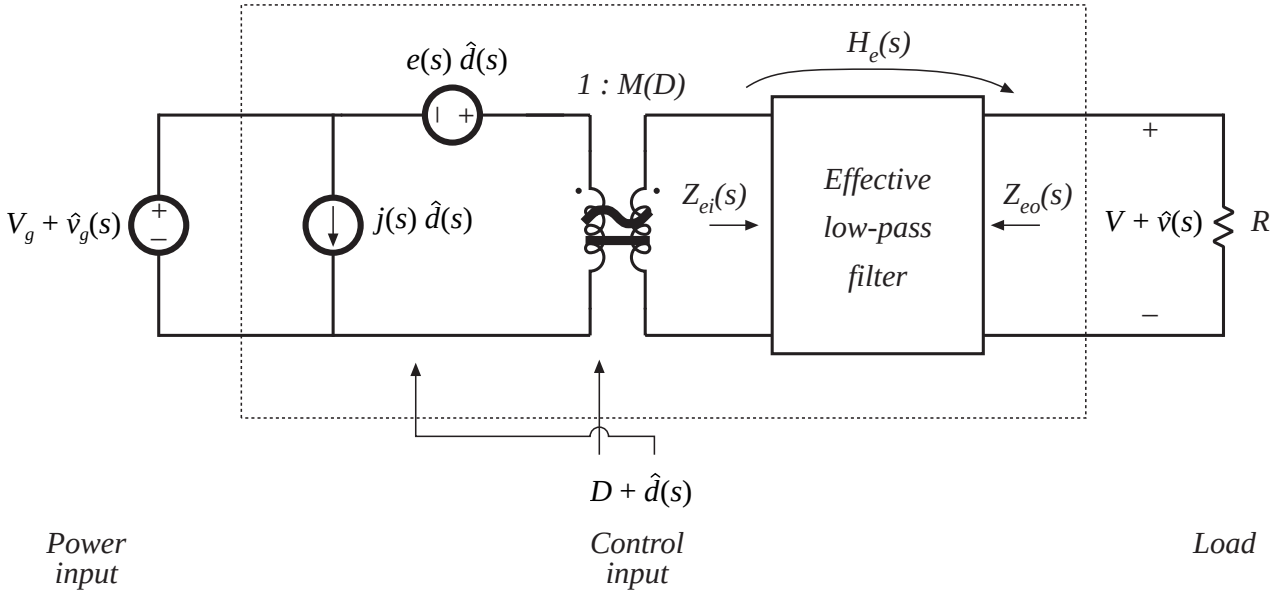
Steps in the development of the canonical circuit model



4. *Control input variations also induce ac variations in converter waveforms*

- *Independent sources represent effects of variations in duty cycle*
- *Can push all sources to input side as shown. Sources may then become frequency-dependent*

Transfer functions predicted by canonical model



Line-to-output transfer function:

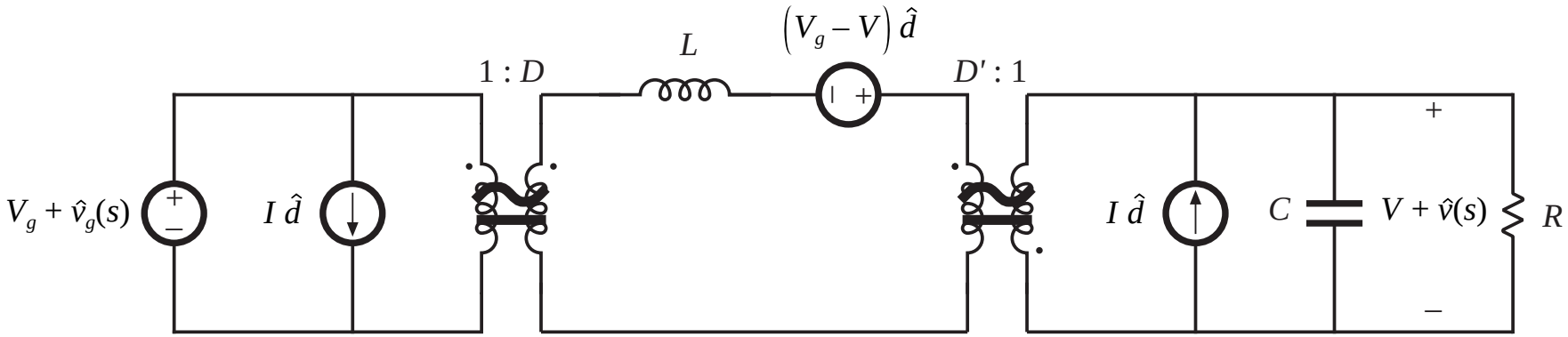
$$G_{vg}(s) = \frac{\hat{v}(s)}{\hat{v}_g(s)} = M(D)\, H_e(s)$$

Control-to-output transfer function:

$$G_{vd}(s) = \frac{\hat{v}(s)}{\hat{d}(s)} = e(s)\, M(D)\, H_e(s)$$

7.6.2. Example: manipulation of the buck-boost converter model into canonical form

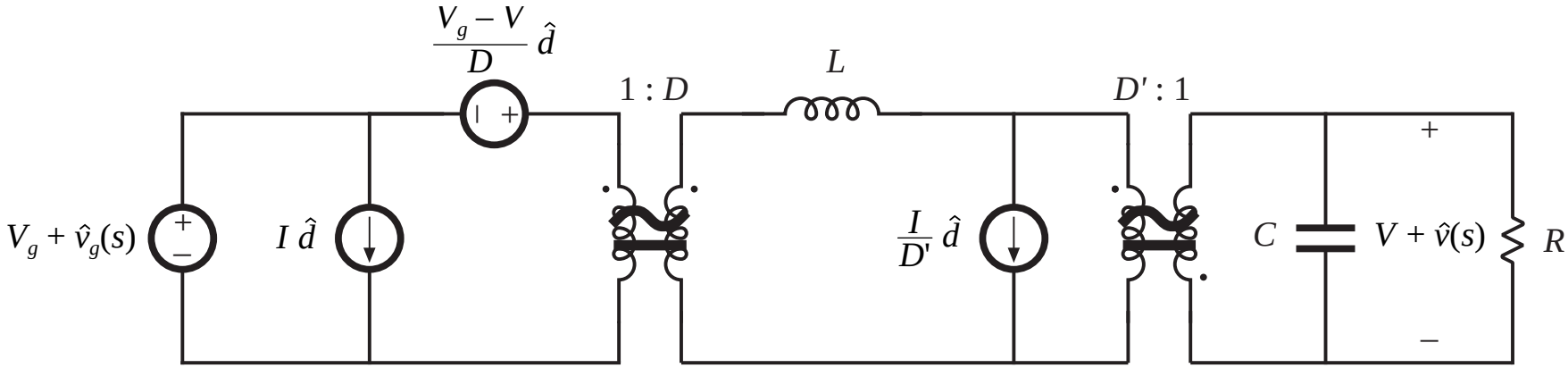
Small-signal ac model of the buck-boost converter



- Push independent sources to input side of transformers
- Push inductor to output side of transformers
- Combine transformers

Step 1

Push voltage source through 1:D transformer
Move current source through D':1 transformer

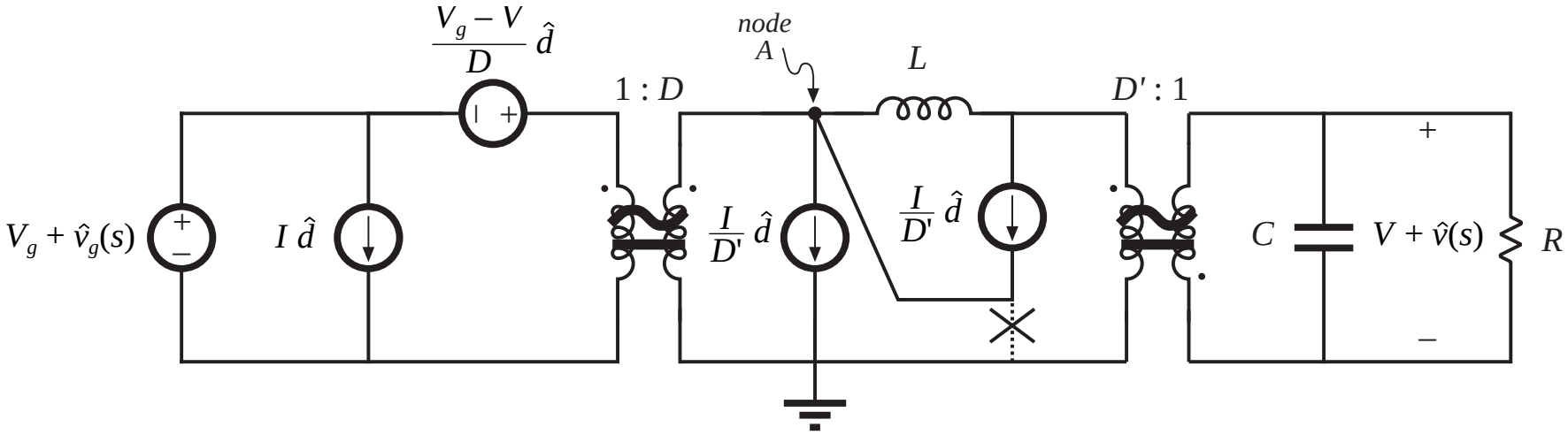


Step 2

How to move the current source past the inductor:

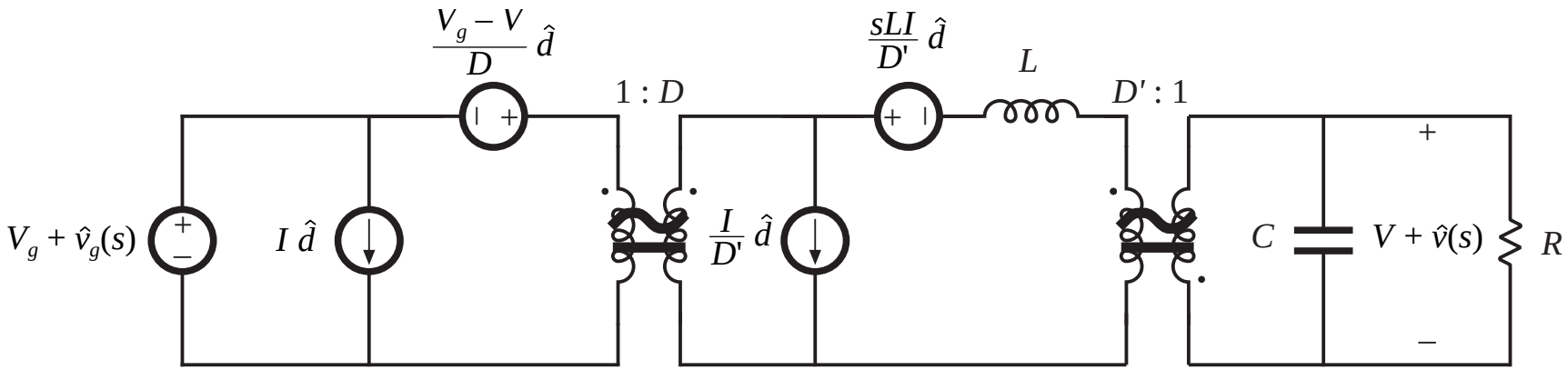
Break ground connection of current source, and connect to node A instead.

Connect an identical current source from node A to ground, so that the node equations are unchanged.



Step 3

The parallel-connected current source and inductor can now be replaced by a Thevenin-equivalent network:

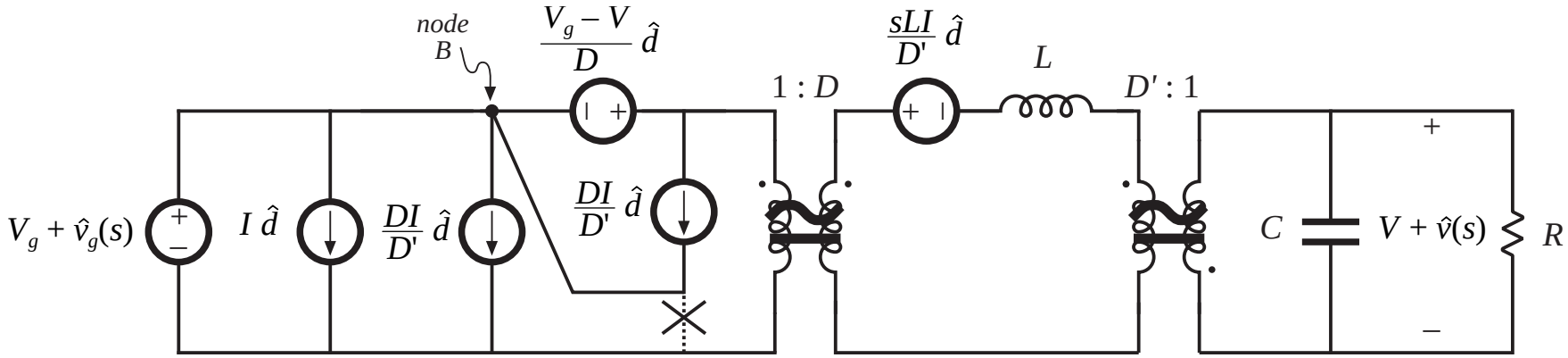


Step 4

Now push current source through 1:D transformer.

Push current source past voltage source, again by:

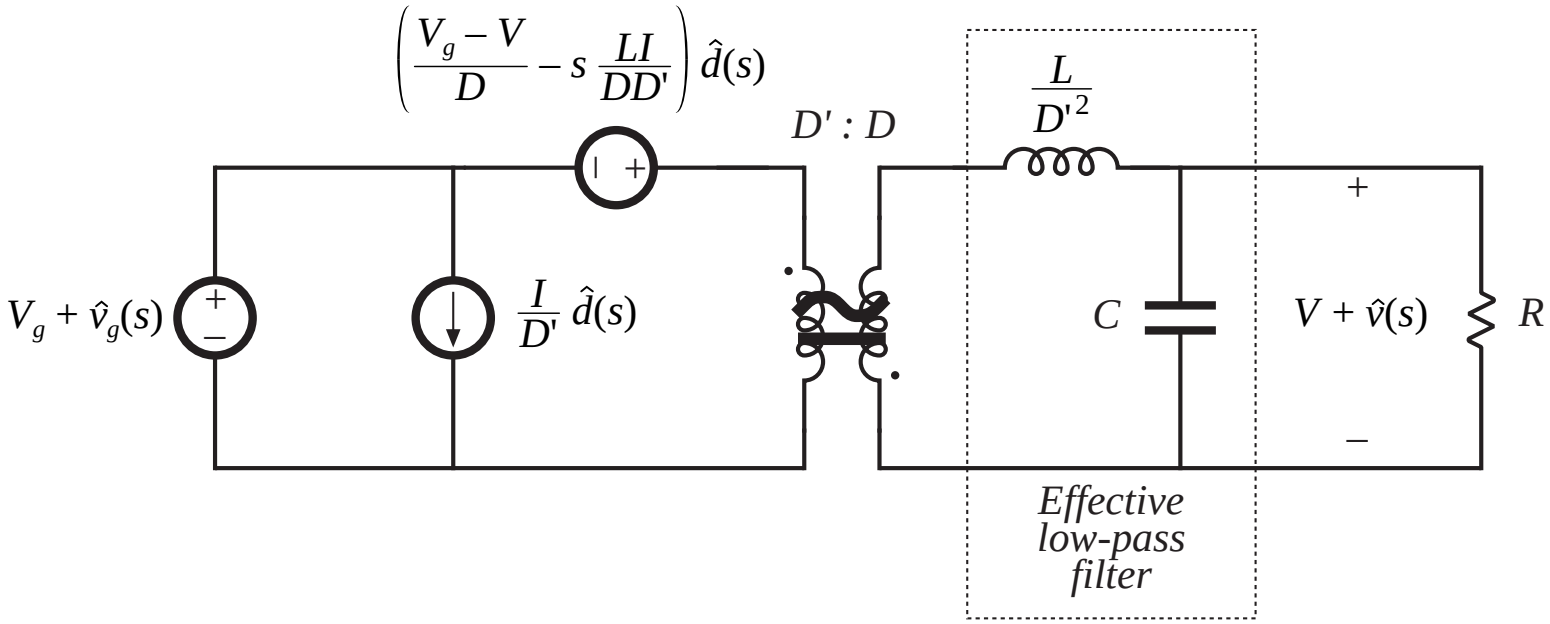
- *Breaking ground connection of current source, and connecting to node B instead.*
- *Connecting an identical current source from node B to ground, so that the node equations are unchanged.*
- *Note that the resulting parallel-connected voltage and current sources are equivalent to a single voltage source.*



Step 5: final result

Push voltage source through 1:D transformer, and combine with existing input-side transformer.

Combine series-connected transformers.



Coefficient of control-input voltage generator

Voltage source coefficient is:

$$e(s) = \frac{V_g + V}{D} - \frac{s\,LI}{D\,D'}$$

Simplification, using dc relations, leads to

$$e(s) = -\frac{V}{D^2}\left(1 - \frac{s\,DL}{D'^2\,R}\right)$$

Pushing the sources past the inductor causes the generator to become frequency-dependent.

7.6.3. Canonical circuit parameters for some common converters

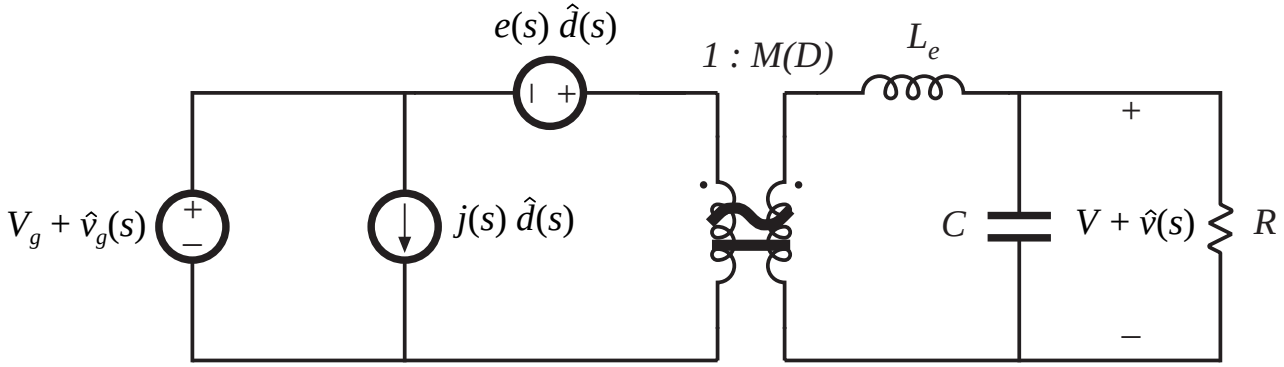


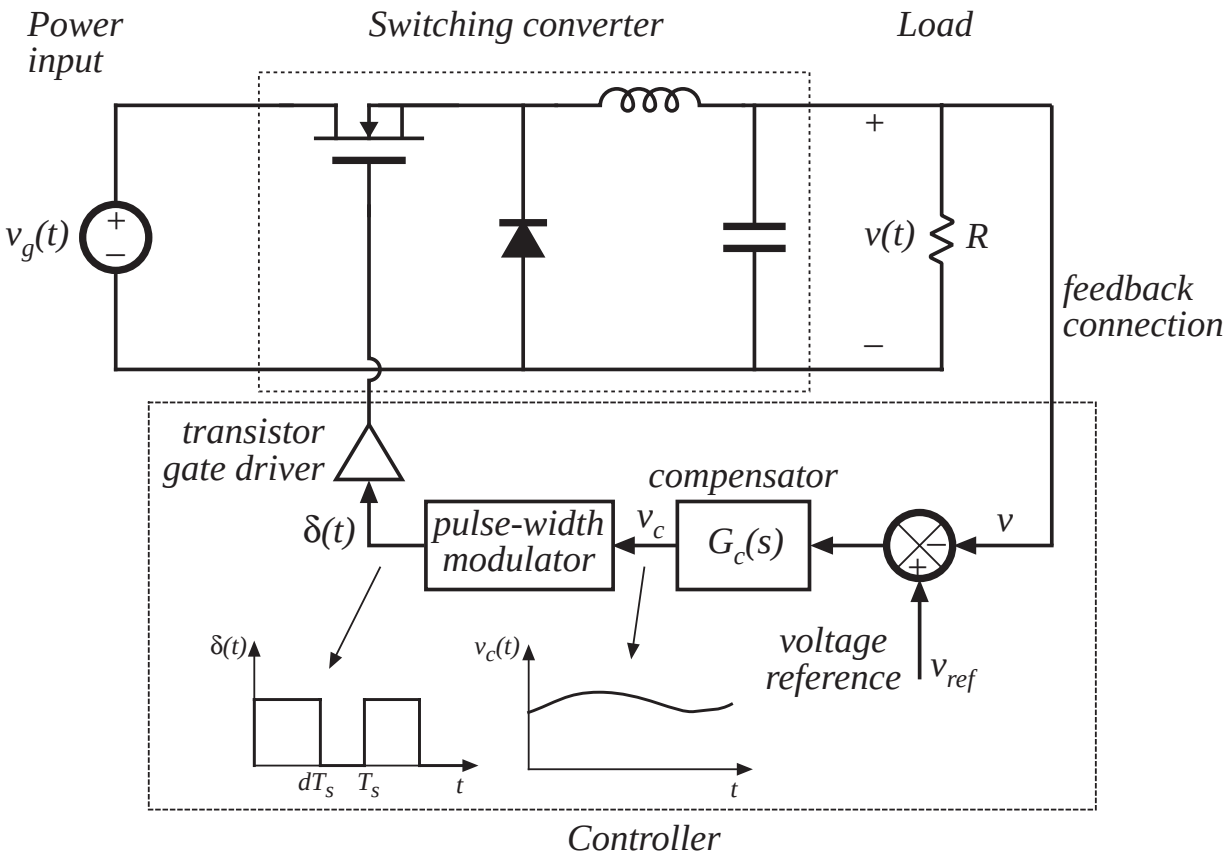
Table 7.1. Canonical model parameters for the ideal buck, boost, and buck-boost converters

Converter	*M(D)*	L_e	*e(s)*	*j(s)*
Buck	D	L	$\frac{V}{D^2}$	$\frac{V}{R}$
Boost	$\frac{1}{D'}$	$\frac{L}{D'^2}$	$V\left(1-\frac{s\,L}{D'^2\,R}\right)$	$\frac{V}{D'^2\,R}$
Buck-boost	$-\frac{D}{D'}$	$\frac{L}{D'^2}$	$-\frac{V}{D^2}\left(1-\frac{s\,DL}{D'^2\,R}\right)$	$-\frac{V}{D'^2\,R}$

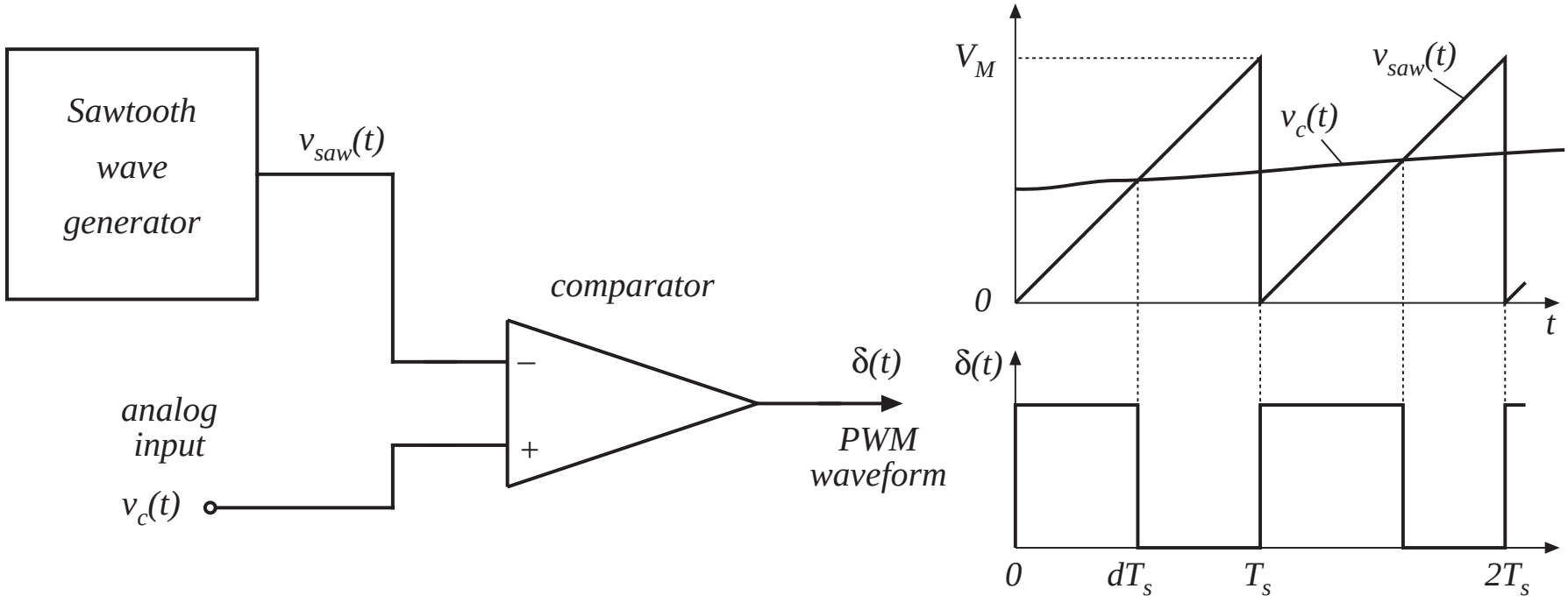
7.7. Modeling the pulse-width modulator

Pulse-width modulator converts voltage signal $v_c(t)$ into duty cycle signal $d(t)$.

What is the relation between $v_c(t)$ and $d(t)$?



A simple pulse-width modulator

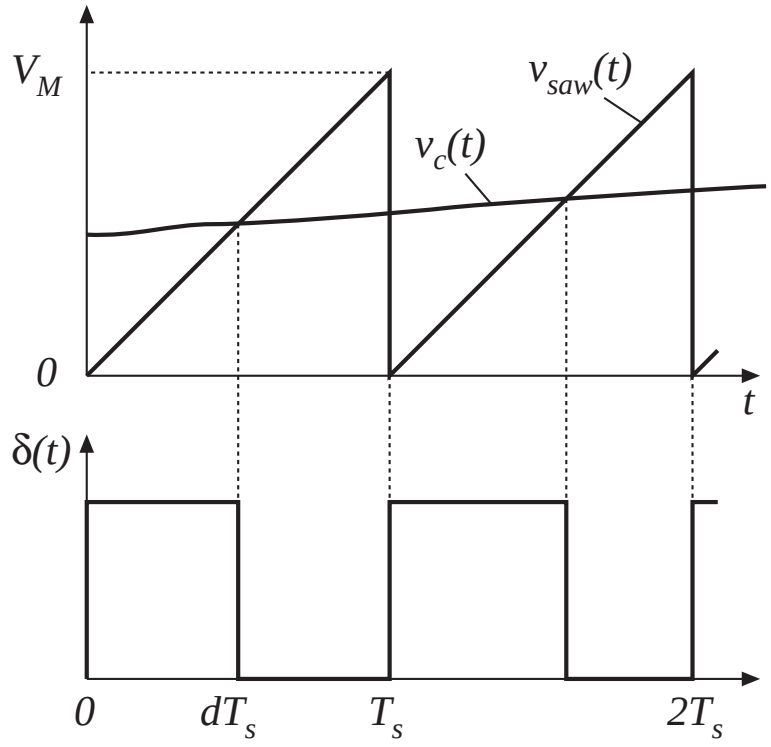


Equation of pulse-width modulator

For a linear sawtooth waveform:

$$d(t) = \frac{v_c(t)}{V_M} \qquad for\ 0 \le v_c(t) \le V_M$$

So $d(t)$ is a linear function of $v_c(t)$.



Perturbed equation of pulse-width modulator

PWM equation:

$$d(t) = \frac{v_c(t)}{V_M} \qquad for\ 0 \le v_c(t) \le V_M$$

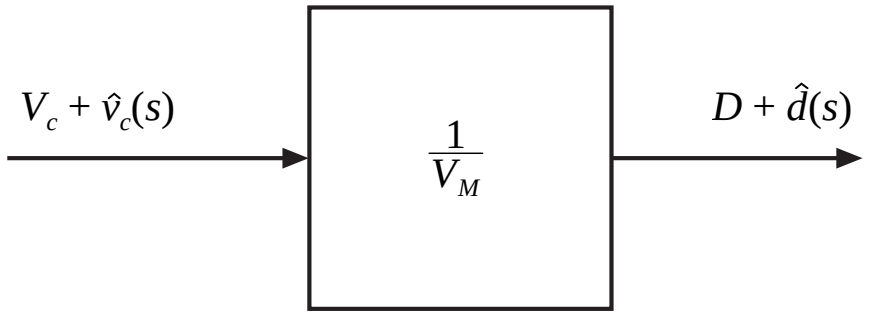
Perturb:

$$v_c(t) = V_c + \hat{v}_c(t)$$
$$d(t) = D + \hat{d}(t)$$

Result:

$$D + \hat{d}(t) = \frac{V_c + \hat{v}_c(t)}{V_M}$$

Block diagram:



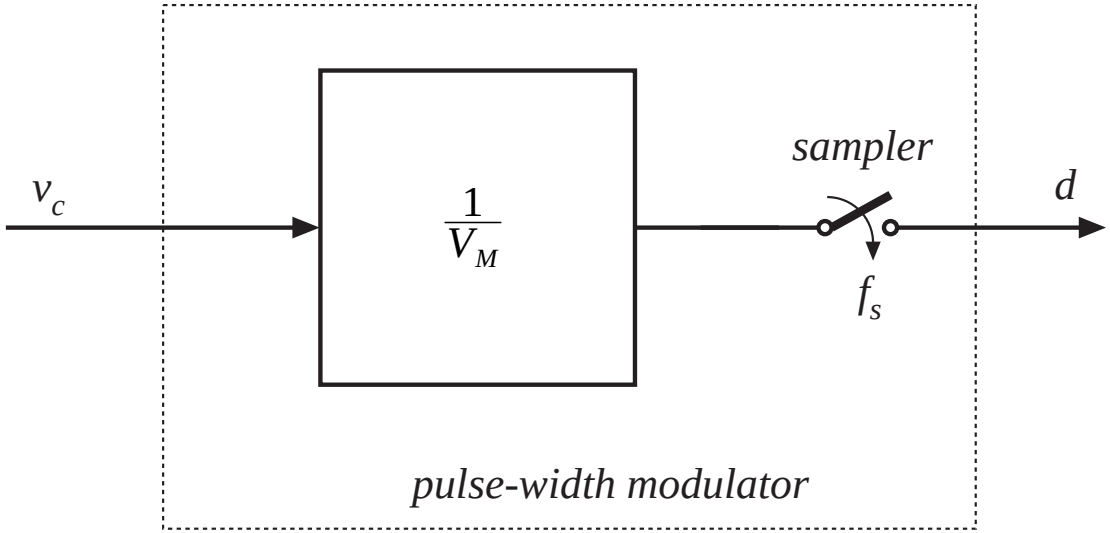
pulse-width modulator

Dc and ac relations:

$$D = \frac{V_c}{V_M}$$
$$\hat{d}(t) = \frac{\hat{v}_c(t)}{V_M}$$

Sampling in the pulse-width modulator

The input voltage is a continuous function of time, but there can be only one discrete value of the duty cycle for each switching period.



Therefore, the pulse-width modulator samples the control waveform, with sampling rate equal to the switching frequency.

In practice, this limits the useful frequencies of ac variations to values much less than the switching frequency. Control system bandwidth must be sufficiently less than the Nyquist rate $f_s/2$. Models that do not account for sampling are accurate only at frequencies much less than $f_s/2$.

7.8. Summary of key points

1. The CCM converter analytical techniques of Chapters 2 and 3 can be extended to predict converter ac behavior. The key step is to average the converter waveforms over one switching period. This removes the switching harmonics, thereby exposing directly the desired dc and low-frequency ac components of the waveforms. In particular, expressions for the averaged inductor voltages, capacitor currents, and converter input current are usually found.
2. Since switching converters are nonlinear systems, it is desirable to construct small-signal linearized models. This is accomplished by perturbing and linearizing the averaged model about a quiescent operating point.
3. Ac equivalent circuits can be constructed, in the same manner used in Chapter 3 to construct dc equivalent circuits. If desired, the ac equivalent circuits may be refined to account for the effects of converter losses and other nonidealities.

Summary of key points

4. The state-space averaging method of section 7.4 is essentially the same as the basic approach of section 7.2, except that the formality of the state-space network description is used. The general results are listed in section 7.4.2.

5. The circuit averaging technique also yields equivalent results, but the derivation involves manipulation of circuits rather than equations. Switching elements are replaced by dependent voltage and current sources, whose waveforms are defined to be identical to the switch waveforms of the actual circuit. This leads to a circuit having a time-invariant topology. The waveforms are then averaged to remove the switching ripple, and perturbed and linearized about a quiescent operating point to obtain a small-signal model.

Summary of key points

6. When the switches are the only time-varying elements in the converter, then circuit averaging affects only the switch network. The converter model can then be derived by simply replacing the switch network with its averaged model. Dc and small-signal ac models of several common CCM switch networks are listed in section 7.5.4. Switching losses can also be modeled using this approach.

7. The canonical circuit describes the basic properties shared by all dc-dc PWM converters operating in the continuous conduction mode. At the heart of the model is the ideal $1{:}M(D)$ transformer, introduced in Chapter 3 to represent the basic dc-dc conversion function, and generalized here to include ac variations. The converter reactive elements introduce an effective low-pass filter into the network. The model also includes independent sources which represent the effect of duty cycle variations. The parameter values in the canonical models of several basic converters are tabulated for easy reference.

Summary of key points

8. The conventional pulse-width modulator circuit has linear gain, dependent on the slope of the sawtooth waveform, or equivalently on its peak-to-peak magnitude.

Chapter 8. Converter Transfer Functions

Converter Transfer Functions

The Engineering Design Process

1. *Specifications and other design goals* are defined.
2. *A circuit is proposed*. This is a creative process that draws on the physical insight and experience of the engineer.
3. *The circuit is modeled*. The converter power stage is modeled as described in Chapter 7. Components and other portions of the system are modeled as appropriate, often with vendor-supplied data.
4. *Design-oriented analysis* of the circuit is performed. This involves development of equations that allow element values to be chosen such that specifications and design goals are met. In addition, it may be necessary for the engineer to gain additional understanding and physical insight into the circuit behavior, so that the design can be improved by adding elements to the circuit or by changing circuit connections.
5. *Model verification*. Predictions of the model are compared to a laboratory prototype, under nominal operating conditions. The model is refined as necessary, so that the model predictions agree with laboratory measurements.

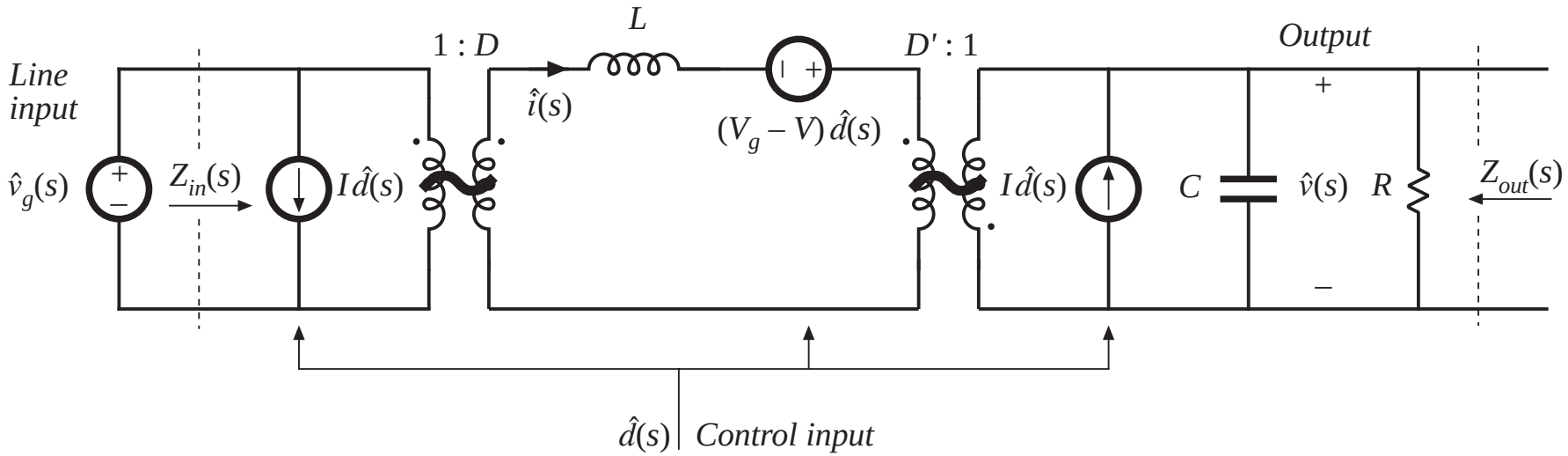
Design Process

6. *Worst-case analysis* (or other reliability and production yield analysis) of the circuit is performed. This involves quantitative evaluation of the model performance, to judge whether specifications are met under all conditions. Computer simulation is well-suited to this task.
7. *Iteration*. The above steps are repeated to improve the design until the worst-case behavior meets specifications, or until the reliability and production yield are acceptably high.

This Chapter: steps 4, 5, and 6

Buck-boost converter model

From Chapter 7

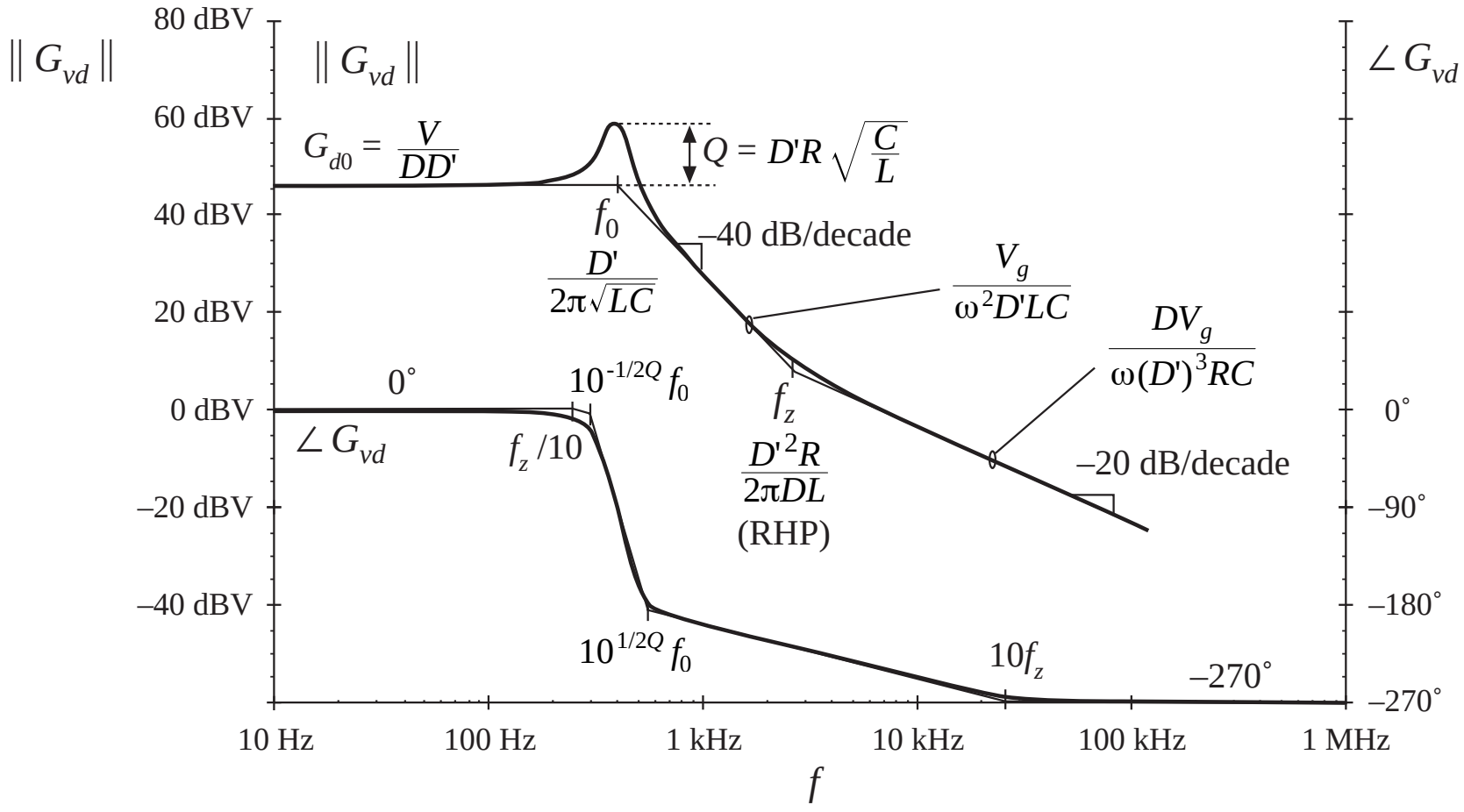


$$G_{vg}(s) = \left.\frac{\hat{v}(s)}{\hat{v}_g(s)}\right|_{\hat{d}(s)\,=\,0}$$

$$G_{vd}(s) = \left.\frac{\hat{v}(s)}{\hat{d}(s)}\right|_{\hat{v}_g(s)\,=\,0}$$

Bode plot of control-to-output transfer function

with analytical expressions for important features



Design-oriented analysis

How to approach a real (and hence, complicated) system

Problems:

- Complicated derivations
- Long equations
- Algebra mistakes

Design objectives:

- Obtain physical insight which leads engineer to synthesis of a good design
- Obtain simple equations that can be inverted, so that element values can be chosen to obtain desired behavior. Equations that cannot be inverted are useless for design!

Design-oriented analysis is a structured approach to analysis, which attempts to avoid the above problems

Some elements of design-oriented analysis, discussed in this chapter

- Writing transfer functions in normalized form, to directly expose salient features
- Obtaining simple analytical expressions for asymptotes, corner frequencies, and other salient features, allows element values to be selected such that a given desired behavior is obtained
- Use of inverted poles and zeroes, to refer transfer function gains to the most important asymptote
- Analytical approximation of roots of high-order polynomials
- Graphical construction of Bode plots of transfer functions and polynomials, to
  - avoid algebra mistakes
  - approximate transfer functions
  - obtain insight into origins of salient features

8.1. Review of Bode plots

Decibels

$$\| G \|_{\text{dB}} = 20 \log_{10}\left(\| G \| \right)$$

Decibels of quantities having units (impedance example): normalize before taking log

$$\| Z \|_{\text{dB}} = 20 \log_{10}\left(\frac{\| Z \|}{R_{base}} \right)$$

Table 8.1. Expressing magnitudes in decibels

Actual magnitude	*Magnitude in dB*
1/2	– 6dB
1	0 dB
2	6 dB
5 = 10/2	20 dB – 6 dB = 14 dB
10	20dB
$1000 = 10^3$	$3 \cdot$ 20dB = 60 dB

5Ω is equivalent to 14dB with respect to a base impedance of R_{base} = 1Ω, also known as 14dBΩ.

60dBμA is a current 60dB greater than a base current of 1μA, or 1mA.

Bode plot of f^n

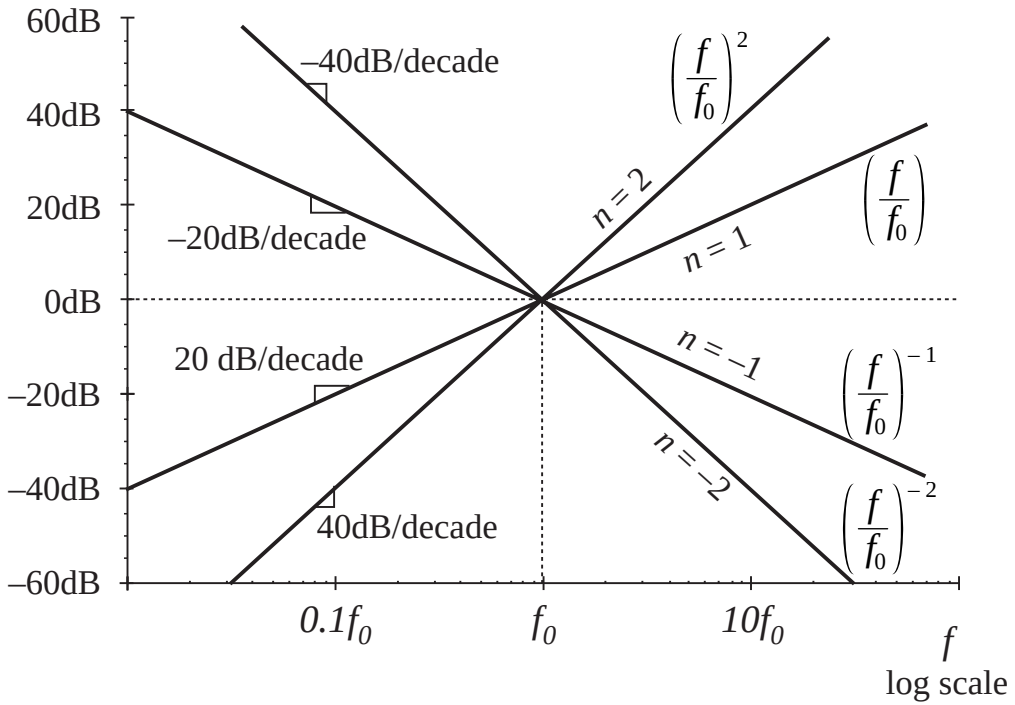
Bode plots are effectively log-log plots, which cause functions which vary as f^n to become linear plots. Given:

$$\| G \| = \left(\frac{f}{f_0} \right)^n$$

Magnitude in dB is

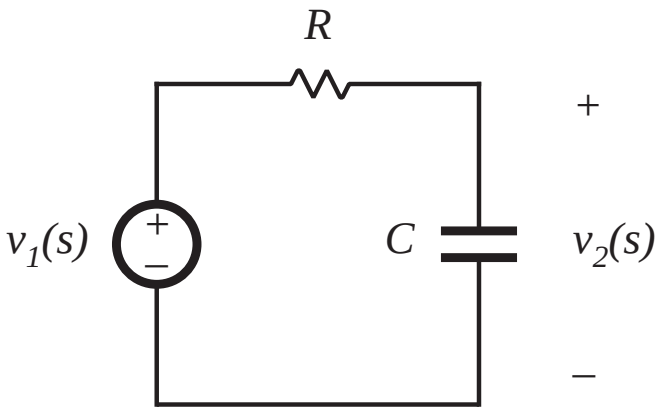
$$\| G \|_{\text{dB}} = 20 \log_{10} \left(\frac{f}{f_0} \right)^n = 20n \log_{10} \left(\frac{f}{f_0} \right)$$

- Slope is $20n$ dB/decade
- Magnitude is 1, or 0dB, at frequency $f = f_0$



8.1.1. Single pole response

Simple R-C example



Transfer function is

$$G(s) = \frac{v_2(s)}{v_1(s)} = \frac{\frac{1}{sC}}{\frac{1}{sC} + R}$$

Express as rational fraction:

$$G(s) = \frac{1}{1 + sRC}$$

This coincides with the normalized form

$$G(s) = \frac{1}{\left(1 + \frac{s}{\omega_0}\right)}$$

with $\omega_0 = \frac{1}{RC}$

$G(j\omega)$ and $\| G(j\omega) \|$

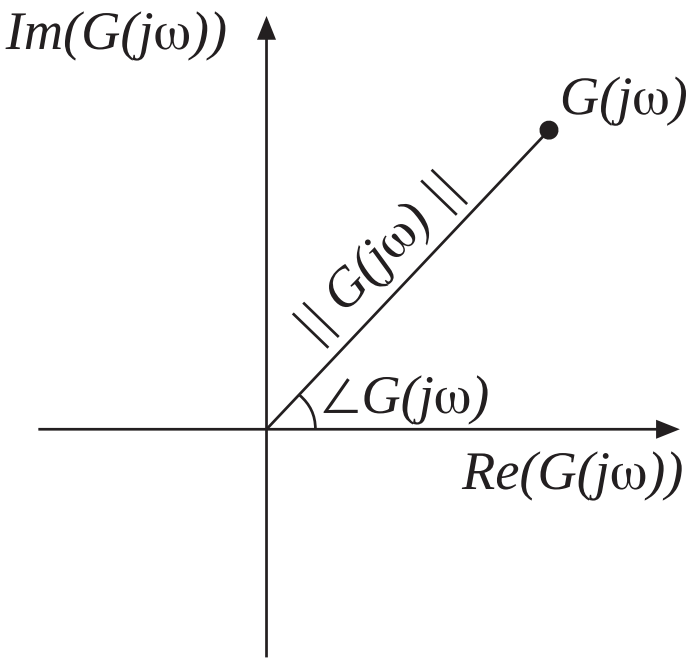
Let $s = j\omega$:

$$G(j\omega) = \frac{1}{\left(1 + j\,\frac{\omega}{\omega_0}\right)} = \frac{1 - j\,\frac{\omega}{\omega_0}}{1 + \left(\frac{\omega}{\omega_0}\right)^2}$$

Magnitude is

$$\| G(j\omega) \| = \sqrt{\left[\text{Re}\,(G(j\omega))\right]^2 + \left[\text{Im}\,(G(j\omega))\right]^2}$$

$$= \frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega_0}\right)^2}}$$



Magnitude in dB:

$$\| G(j\omega) \|_{\text{dB}} = -20 \log_{10} \left(\sqrt{1 + \left(\frac{\omega}{\omega_0}\right)^2} \right) \text{ dB}$$

Asymptotic behavior: low frequency

For small frequency, $\omega << \omega_0$ and $f << f_0$:

$$\left(\frac{\omega}{\omega_0}\right) << 1$$

Then $\| G(j\omega) \|$ becomes

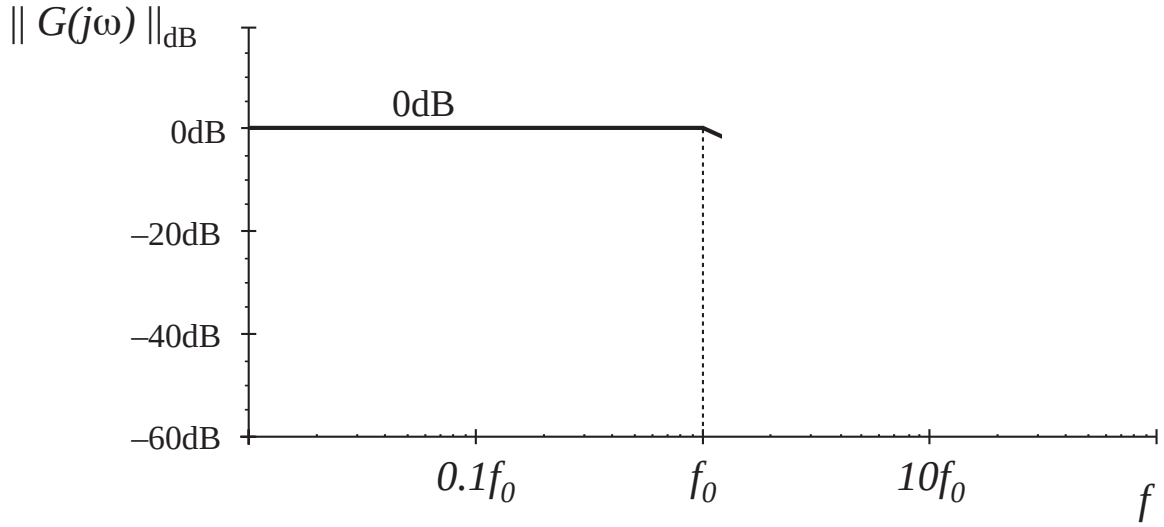
$$\left\| G(j\omega) \right\| \approx \frac{1}{\sqrt{1}} = 1$$

Or, in dB,

$$\left\| G(j\omega) \right\|_{\text{dB}} \approx 0\text{dB}$$

This is the low-frequency asymptote of $\| G(j\omega) \|$

$$\left\| G(j\omega) \right\| = \frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega_0}\right)^2}}$$



Asymptotic behavior: high frequency

For high frequency, $\omega >> \omega_0$ and $f >> f_0$:

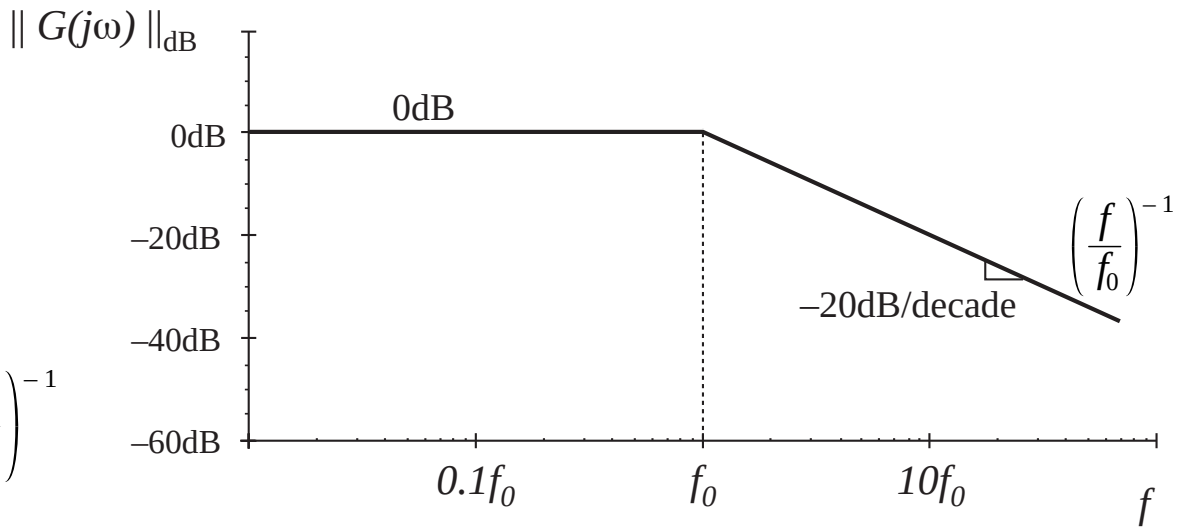
$$\left(\frac{\omega}{\omega_0} \right) >> 1$$

$$1 + \left(\frac{\omega}{\omega_0} \right)^2 \approx \left(\frac{\omega}{\omega_0} \right)^2$$

Then $\| G(j\omega) \|$ becomes

$$\left\| G(j\omega) \right\| \approx \frac{1}{\sqrt{\left(\frac{\omega}{\omega_0} \right)^2}} = \left(\frac{f}{f_0} \right)^{-1}$$

$$\left\| G(j\omega) \right\| = \frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega_0} \right)^2}}$$



The high-frequency asymptote of $\| G(j\omega) \|$ varies as f^{-1}. Hence, $n = -1$, and a straight-line asymptote having a slope of -20dB/decade is obtained. The asymptote has a value of 1 at $f = f_0$.

Deviation of exact curve near $f = f_0$

Evaluate exact magnitude:

at $f = f_0$*:*

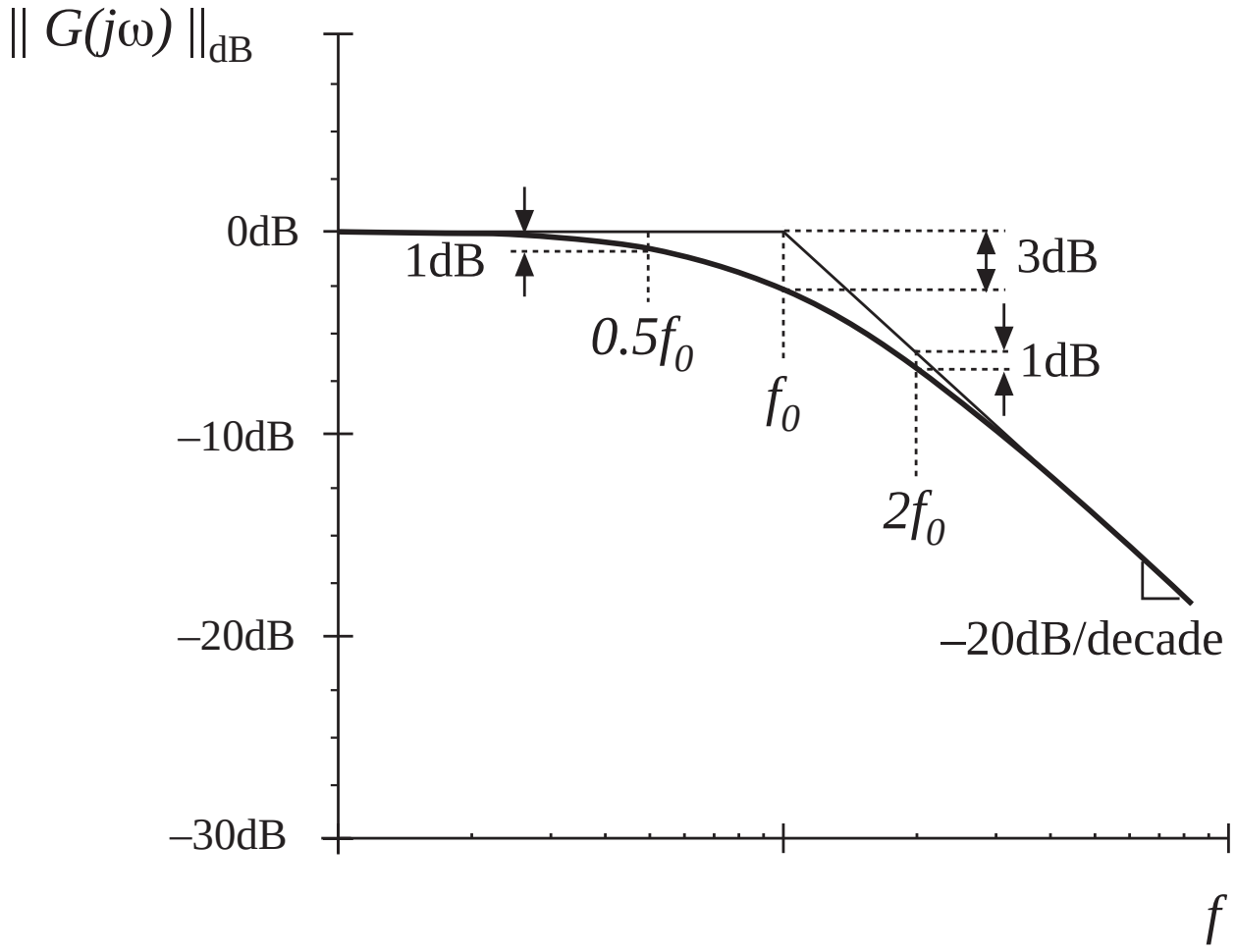
$$\left\| G(j\omega_0) \right\| = \frac{1}{\sqrt{1 + \left(\frac{\omega_0}{\omega_0} \right)^2}} = \frac{1}{\sqrt{2}}$$

$$\left\| G(j\omega_0) \right\|_{\text{dB}} = -20 \log_{10} \left(\sqrt{1 + \left(\frac{\omega_0}{\omega_0} \right)^2} \right) \approx -3 \text{ dB}$$

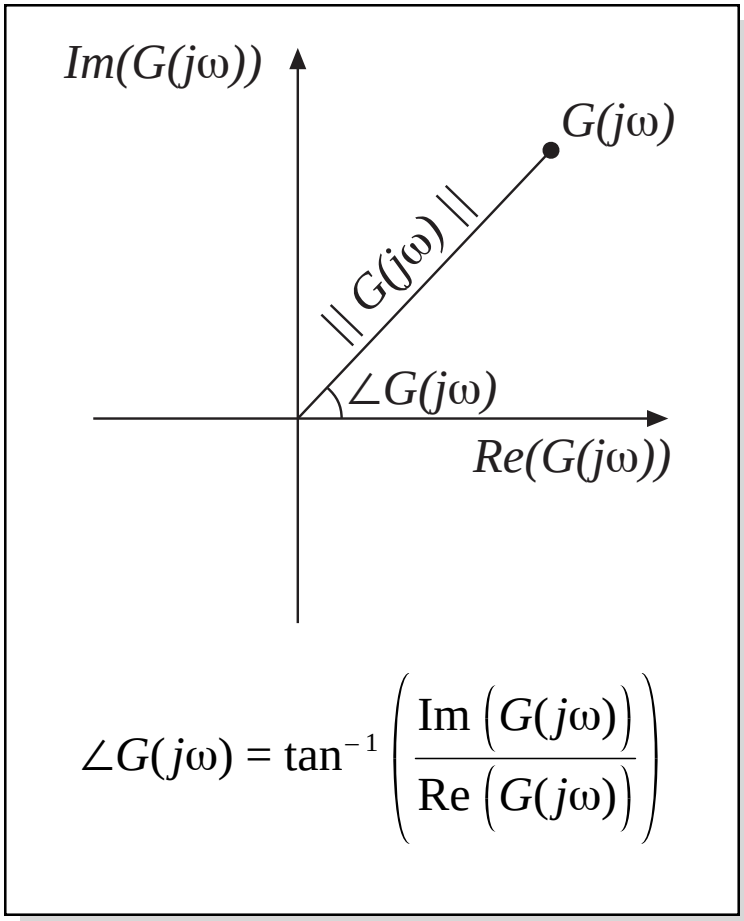
at $f = 0.5f_0$ *and* $2f_0$ *:*

Similar arguments show that the exact curve lies 1dB below the asymptotes.

Summary: magnitude



Phase of $G(j\omega)$

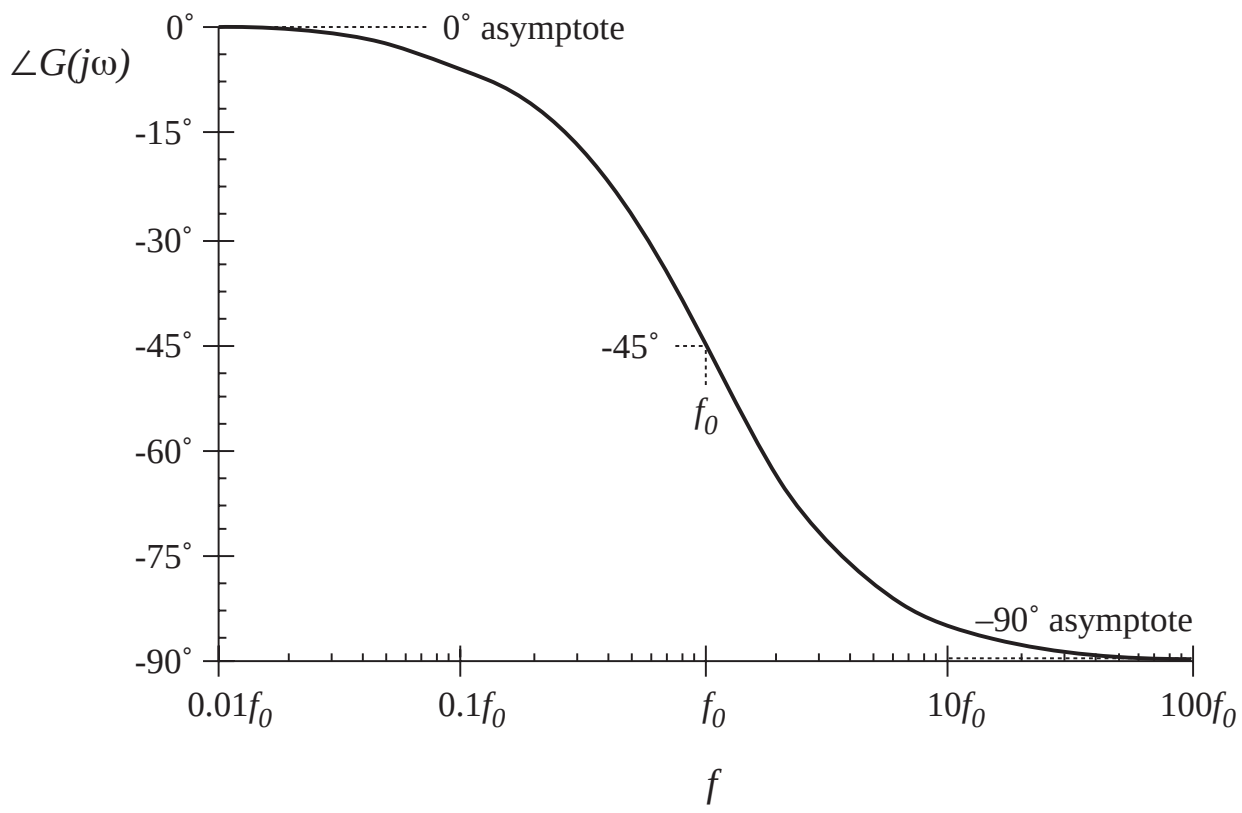


$$\angle G(j\omega) = \tan^{-1}\left(\frac{\text{Im}\left(G(j\omega)\right)}{\text{Re}\left(G(j\omega)\right)}\right)$$

$$G(j\omega) = \frac{1}{\left(1 + j\,\frac{\omega}{\omega_0}\right)} = \frac{1 - j\,\frac{\omega}{\omega_0}}{1 + \left(\frac{\omega}{\omega_0}\right)^2}$$

$$\angle G(j\omega) = -\tan^{-1}\left(\frac{\omega}{\omega_0}\right)$$

Phase of $G(j\omega)$



$$\angle G(j\omega) = -\tan^{-1}\left(\frac{\omega}{\omega_0}\right)$$

ω	$\angle G(j\omega)$
0	0°
ω_0	–45°
∞	–90°

Phase asymptotes

Low frequency: 0°

High frequency: –90°

Low- and high-frequency asymptotes do not intersect

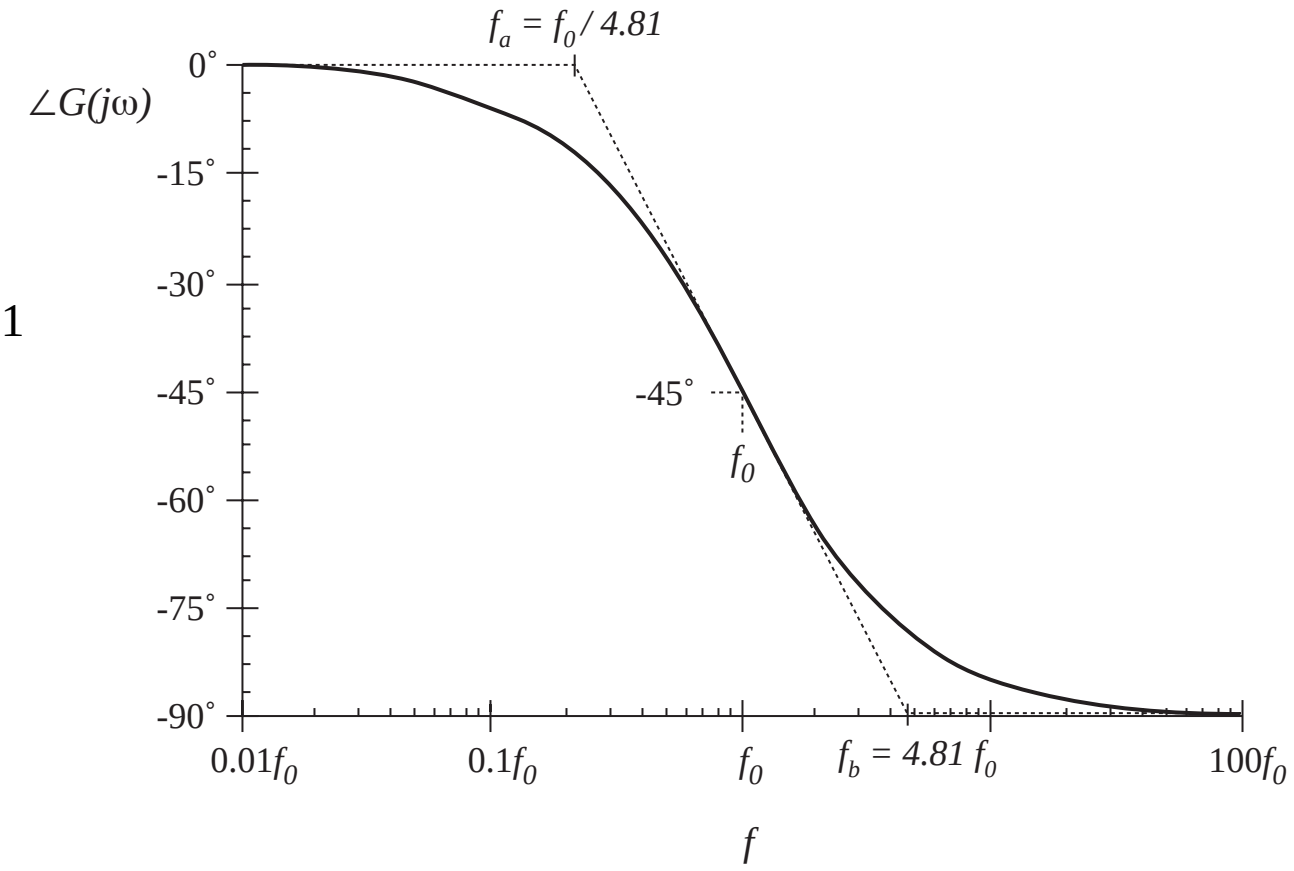
Hence, need a midfrequency asymptote

Try a midfrequency asymptote having slope identical to actual slope at the corner frequency f_0. One can show that the asymptotes then intersect at the break frequencies

$$f_a = f_0 \, e^{-\pi/2} \approx f_0 / 4.81$$
$$f_b = f_0 \, e^{\pi/2} \approx 4.81 \; f_0$$

Phase asymptotes

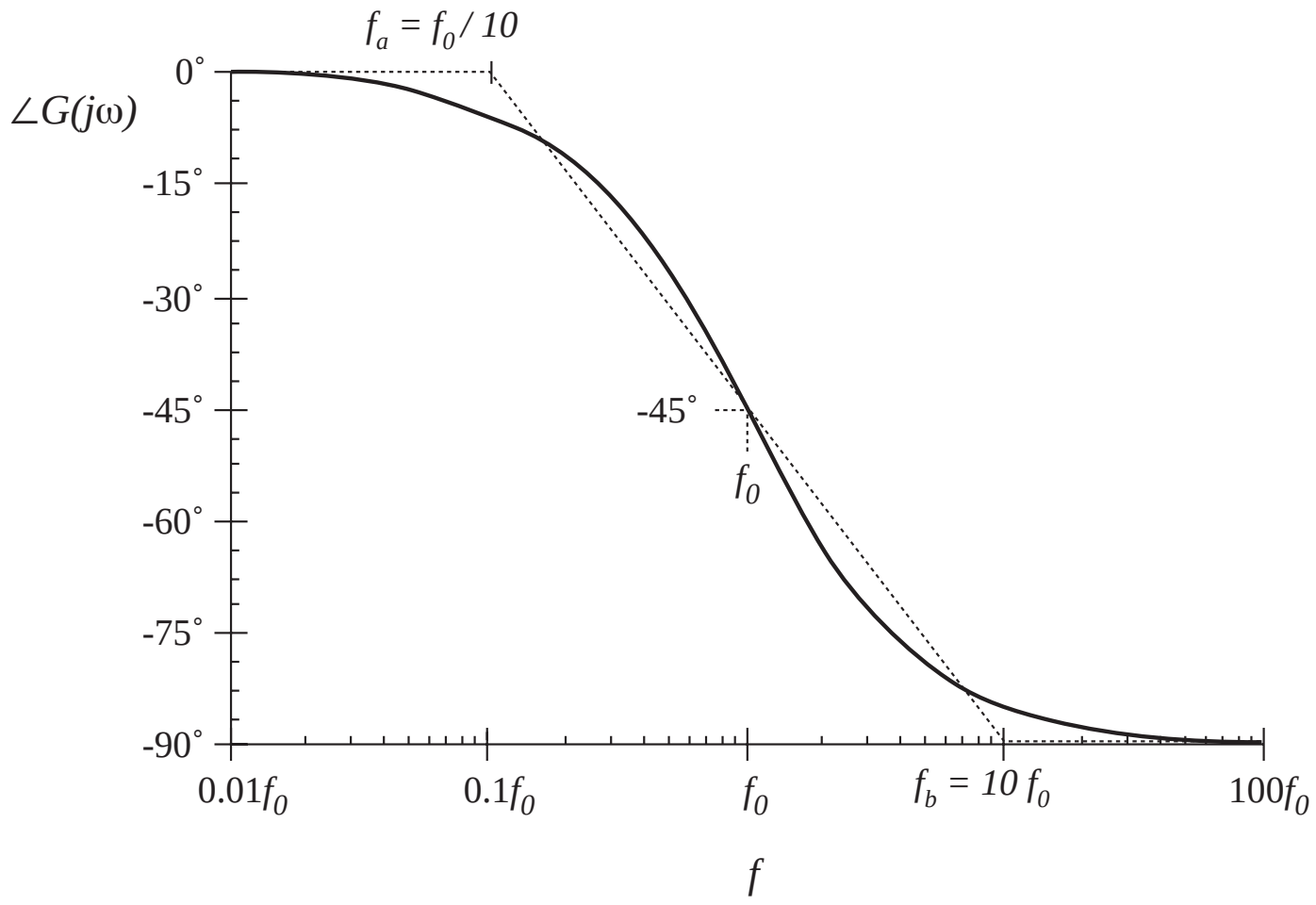
$$f_a = f_0\, e^{-\pi/2} \approx f_0 / 4.81$$
$$f_b = f_0\, e^{\pi/2} \approx 4.81\ f_0$$



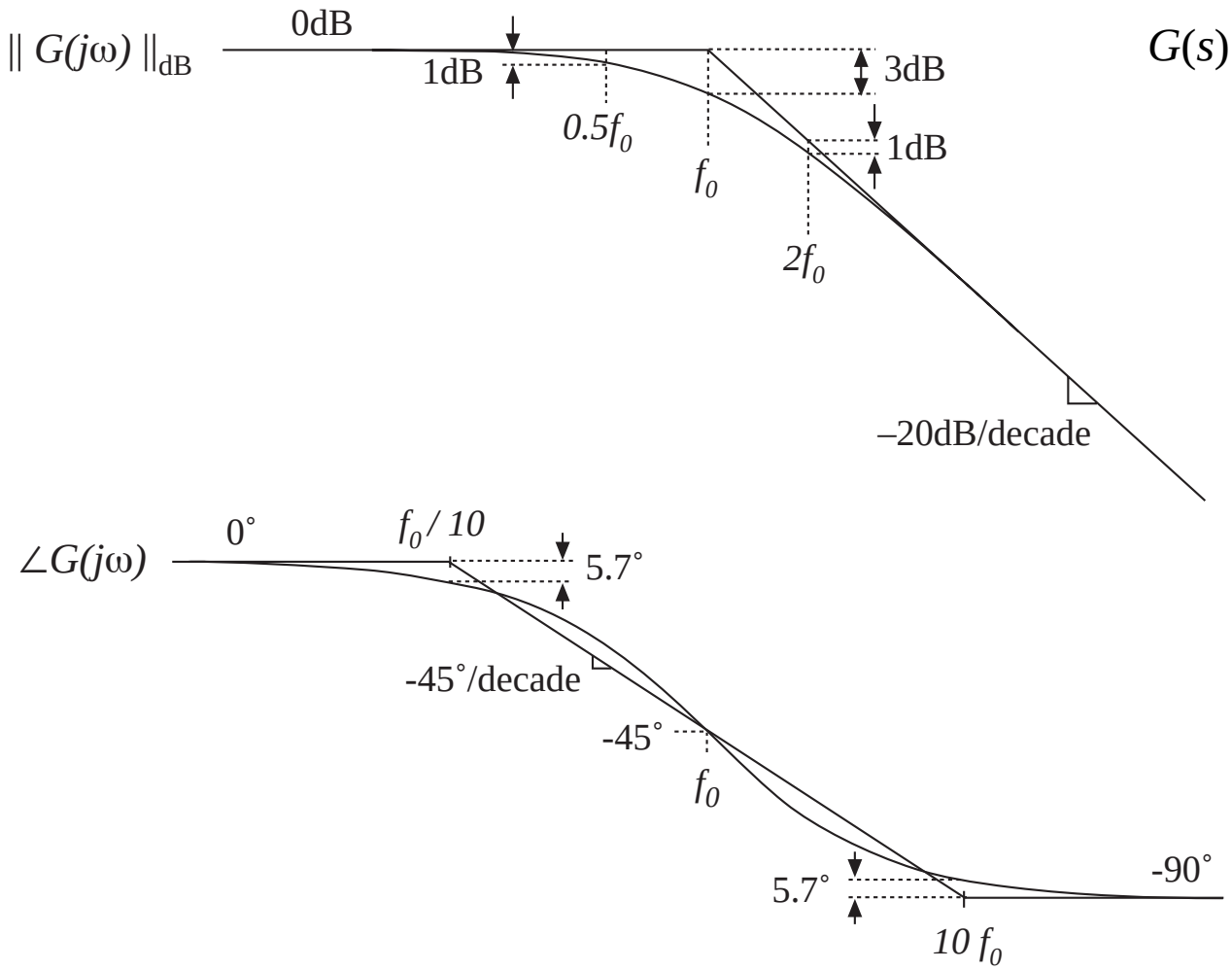
Phase asymptotes: a simpler choice

$f_a = f_0 / 10$

$f_b = 10\ f_0$



Summary: Bode plot of real pole



$$G(s) = \frac{1}{\left(1 + \frac{s}{\omega_0}\right)}$$

8.1.2. Single zero response

Normalized form:

$$G(s) = \left(1 + \frac{s}{\omega_0}\right)$$

Magnitude:

$$\left\| G(j\omega) \right\| = \sqrt{1 + \left(\frac{\omega}{\omega_0}\right)^2}$$

Use arguments similar to those used for the simple pole, to derive asymptotes:

0dB at low frequency, $\omega << \omega_0$

+20dB/decade slope at high frequency, $\omega >> \omega_0$

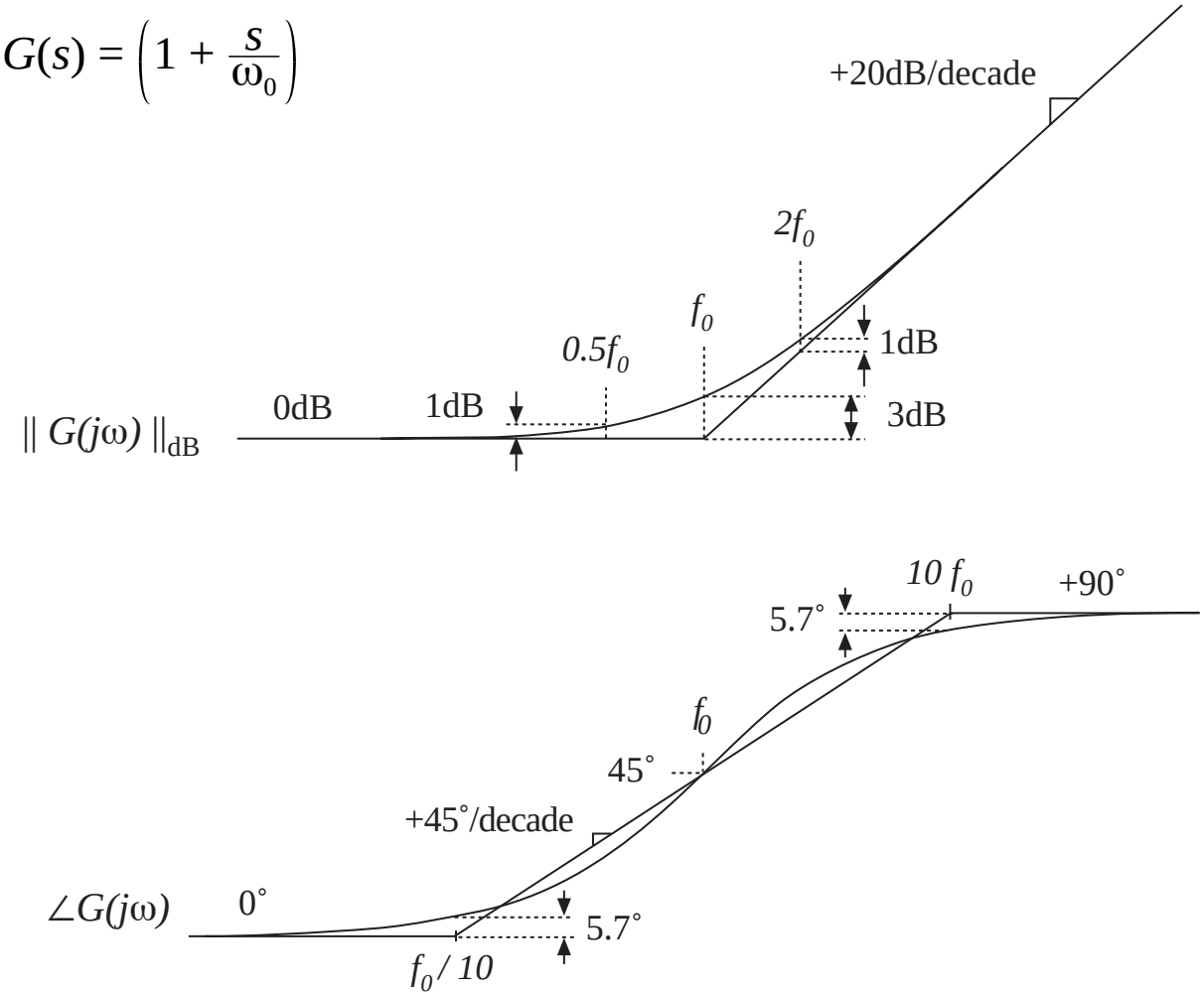
Phase:

$$\angle G(j\omega) = \tan^{-1}\left(\frac{\omega}{\omega_0}\right)$$

—with the exception of a missing minus sign, same as simple pole

Summary: Bode plot, real zero

$$G(s) = \left(1 + \frac{s}{\omega_0}\right)$$



8.1.3. Right half-plane zero

Normalized form:

$$G(s) = \left(1 - \frac{s}{\omega_0}\right)$$

Magnitude:

$$\left\| G(j\omega) \right\| = \sqrt{1 + \left(\frac{\omega}{\omega_0}\right)^2}$$

—same as conventional (left half-plane) zero. Hence, magnitude asymptotes are identical to those of LHP zero.

Phase:

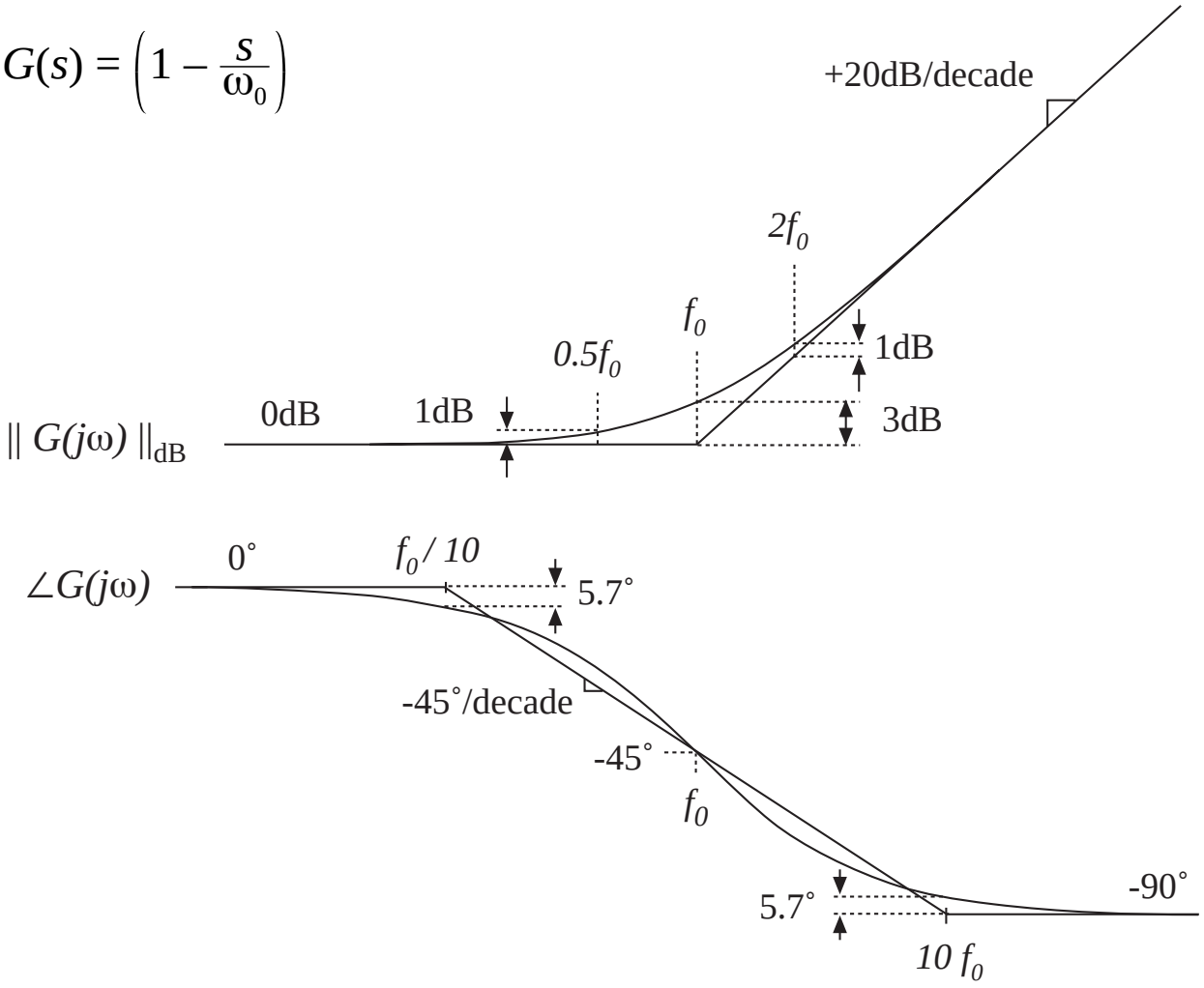
$$\angle G(j\omega) = -\tan^{-1}\left(\frac{\omega}{\omega_0}\right)$$

—same as real pole.

The RHP zero exhibits the magnitude asymptotes of the LHP zero, and the phase asymptotes of the pole

Summary: Bode plot, RHP zero

$$G(s) = \left(1 - \frac{s}{\omega_0}\right)$$



8.1.4. Frequency inversion

Reversal of frequency axis. A useful form when describing mid- or high-frequency flat asymptotes. Normalized form, inverted pole:

$$G(s) = \frac{1}{\left(1 + \frac{\omega_0}{s}\right)}$$

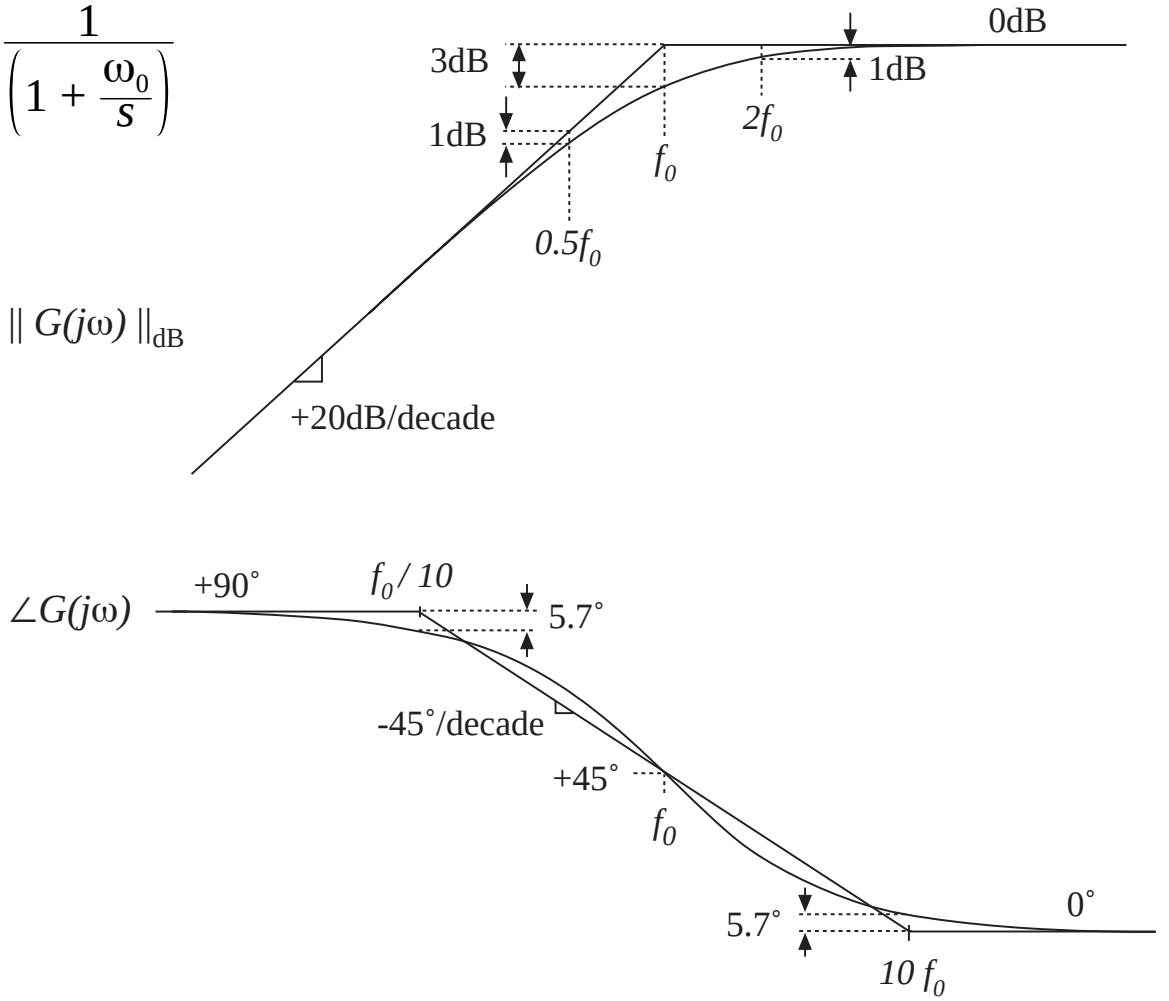
An algebraically equivalent form:

$$G(s) = \frac{\left(\frac{s}{\omega_0}\right)}{\left(1 + \frac{s}{\omega_0}\right)}$$

The inverted-pole format emphasizes the high-frequency gain.

Asymptotes, inverted pole

$$G(s) = \frac{1}{\left(1 + \frac{\omega_0}{s}\right)}$$



Inverted zero

Normalized form, inverted zero:

$$G(s) = \left(1 + \frac{\omega_0}{s}\right)$$

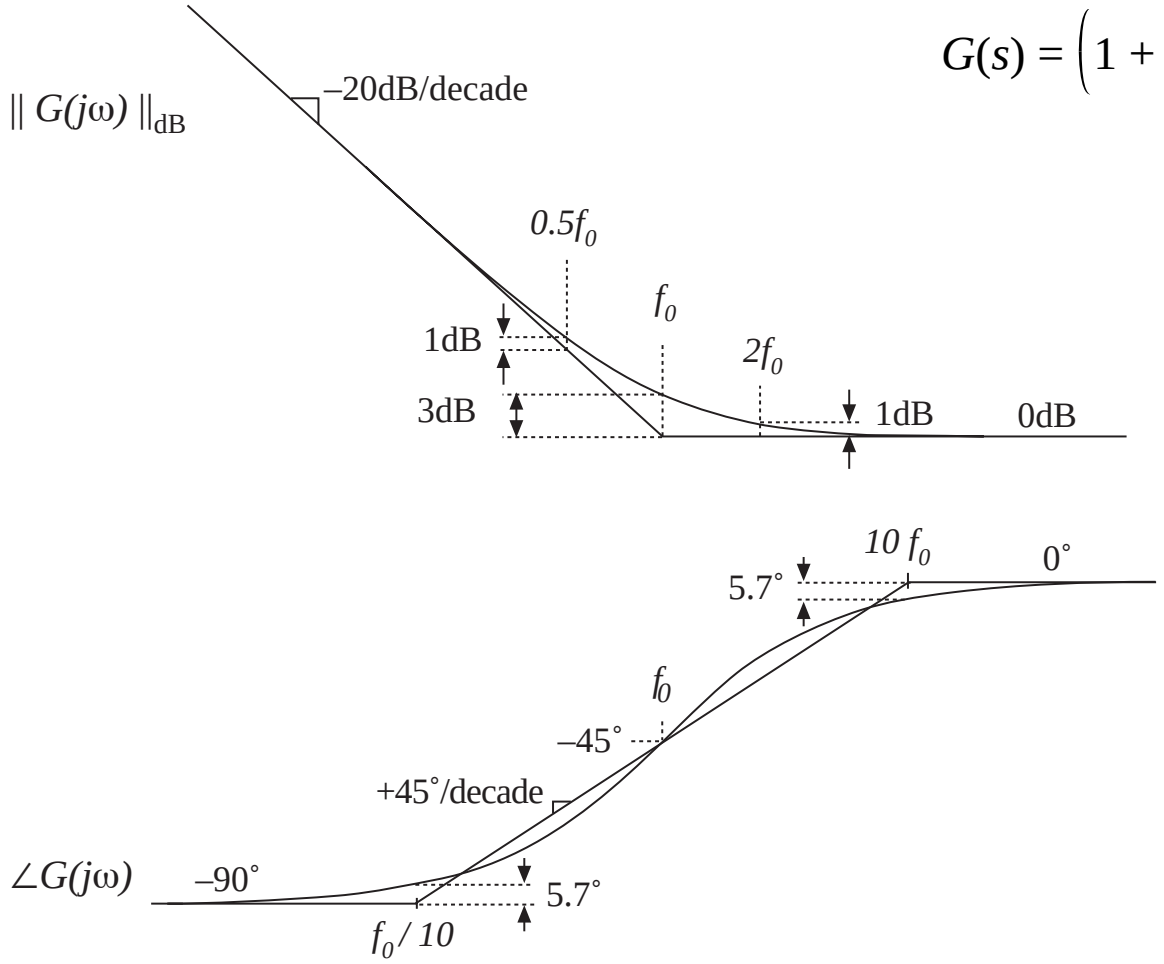
An algebraically equivalent form:

$$G(s) = \frac{\left(1 + \frac{s}{\omega_0}\right)}{\left(\frac{s}{\omega_0}\right)}$$

Again, the inverted-zero format emphasizes the high-frequency gain.

Asymptotes, inverted zero

$$G(s) = \left(1 + \frac{\omega_0}{s}\right)$$



8.1.5. Combinations

Suppose that we have constructed the Bode diagrams of two complex-values functions of frequency, $G_1(\omega)$ and $G_2(\omega)$. It is desired to construct the Bode diagram of the product, $G_3(\omega) = G_1(\omega)\, G_2(\omega)$.

Express the complex-valued functions in polar form:

$$G_1(\omega) = R_1(\omega)\, e^{j\theta_1(\omega)}$$
$$G_2(\omega) = R_2(\omega)\, e^{j\theta_2(\omega)}$$
$$G_3(\omega) = R_3(\omega)\, e^{j\theta_3(\omega)}$$

The product $G_3(\omega)$ can then be written

$$G_3(\omega) = G_1(\omega)\, G_2(\omega) = R_1(\omega)\, e^{j\theta_1(\omega)}\, R_2(\omega)\, e^{j\theta_2(\omega)}$$

$$G_3(\omega) = \left(R_1(\omega)\, R_2(\omega)\right) e^{j(\theta_1(\omega) + \theta_2(\omega))}$$

Combinations

$$G_3(\omega) = \left(R_1(\omega)\, R_2(\omega) \right) e^{j(\theta_1(\omega) + \theta_2(\omega))}$$

The composite phase is

$$\theta_3(\omega) = \theta_1(\omega) + \theta_2(\omega)$$

The composite magnitude is

$$R_3(\omega) = R_1(\omega)\, R_2(\omega)$$

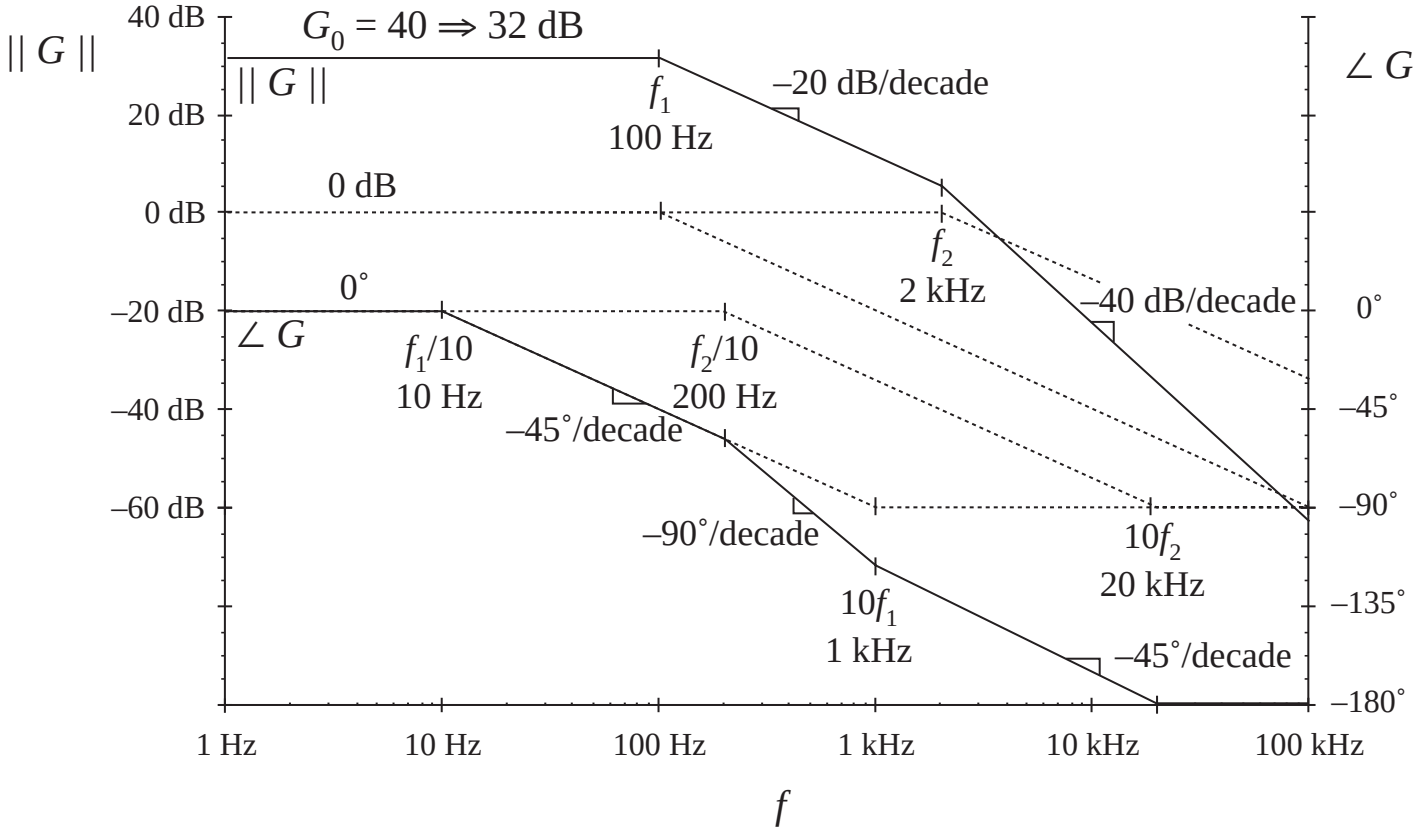
$$\left| R_3(\omega) \right|_{\text{dB}} = \left| R_1(\omega) \right|_{\text{dB}} + \left| R_2(\omega) \right|_{\text{dB}}$$

Composite phase is sum of individual phases.

Composite magnitude, when expressed in dB, is sum of individual magnitudes.

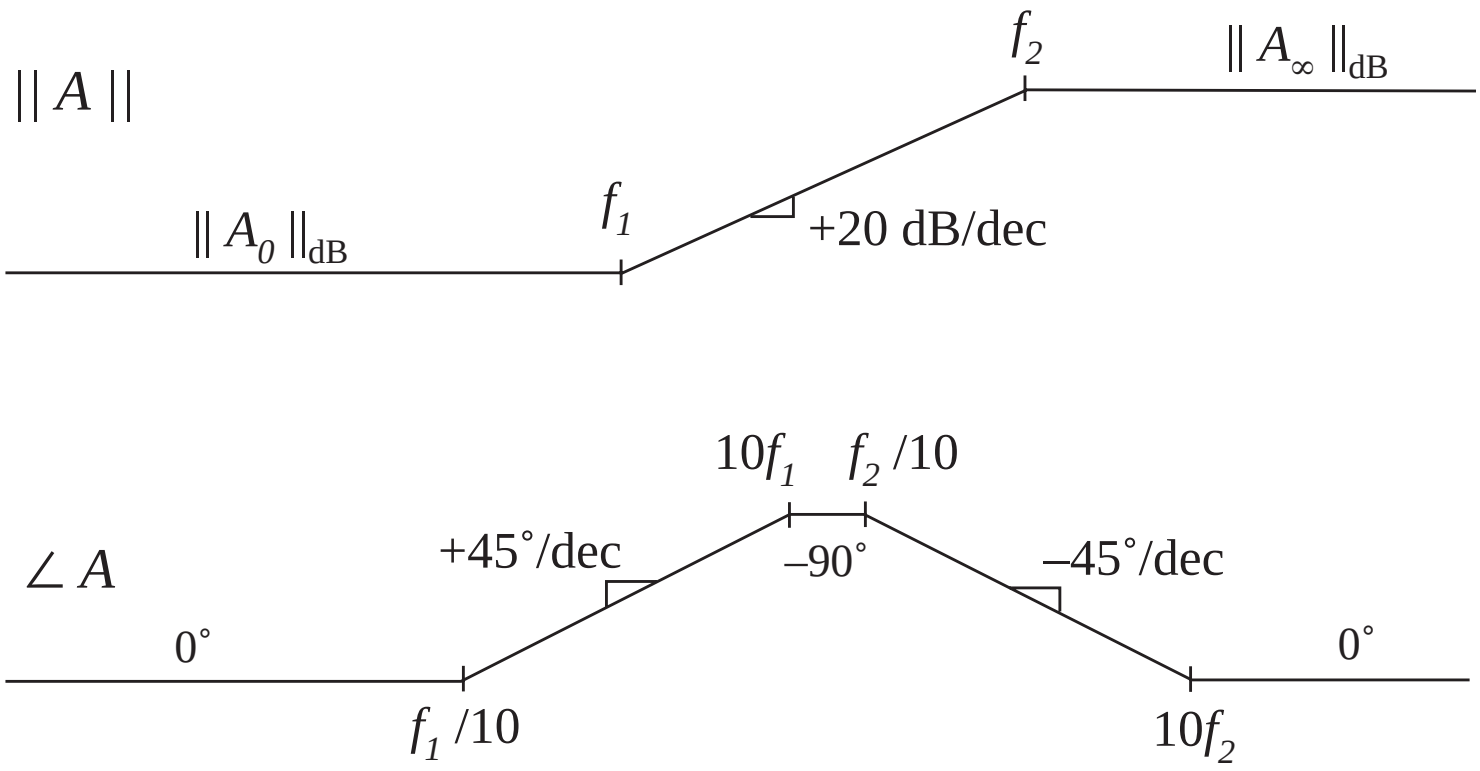
Example 1: $G(s) = \dfrac{G_0}{\left(1 + \dfrac{s}{\omega_1}\right)\left(1 + \dfrac{s}{\omega_2}\right)}$

with $G_0 = 40 \Rightarrow 32$ dB, $f_1 = \omega_1/2\pi = 100$ Hz, $f_2 = \omega_2/2\pi = 2$ kHz



Example 2

Determine the transfer function $A(s)$ corresponding to the following asymptotes:



Example 2, continued

One solution:

$$A(s) = A_0 \frac{\left(1 + \frac{s}{\omega_1}\right)}{\left(1 + \frac{s}{\omega_2}\right)}$$

Analytical expressions for asymptotes:

For $f < f_1$

$$\left\| A_0 \frac{\left(1 + \frac{s}{\omega_1}\right)}{\left(1 + \frac{s}{\omega_2}\right)} \right\|_{s = j\omega} = A_0 \frac{1}{1} = A_0$$

For $f_1 < f < f_2$

$$\left\| A_0 \frac{\left(\frac{s}{\omega_1}\right)}{\left(1 + \frac{s}{\omega_2}\right)} \right\|_{s = j\omega} = A_0 \frac{\left\| \frac{s}{\omega_1} \right\|_{s = j\omega}}{1} = A_0 \frac{\omega}{\omega_1} = A_0 \frac{f}{f_1}$$

Example 2, continued

For $f > f_2$

$$\left\| A_0 \frac{\left(\blacktriangle + \frac{s}{\omega_1} \right)}{\left(\blacktriangle + \frac{s}{\omega_2} \right)} \right\|_{s = j\omega} = A_0 \frac{\left\| \frac{s}{\omega_1} \right\|_{s = j\omega}}{\left\| \frac{s}{\omega_2} \right\|_{s = j\omega}} = A_0 \frac{\omega_2}{\omega_1} = A_0 \frac{f_2}{f_1}$$

So the high-frequency asymptote is

$$A_\infty = A_0 \frac{f_2}{f_1}$$

Another way to express $A(s)$: use inverted poles and zeroes, and express $A(s)$ directly in terms of A_∞

$$A(s) = A_\infty \frac{\left(1 + \frac{\omega_1}{s} \right)}{\left(1 + \frac{\omega_2}{s} \right)}$$

8.1.6 Quadratic pole response: resonance

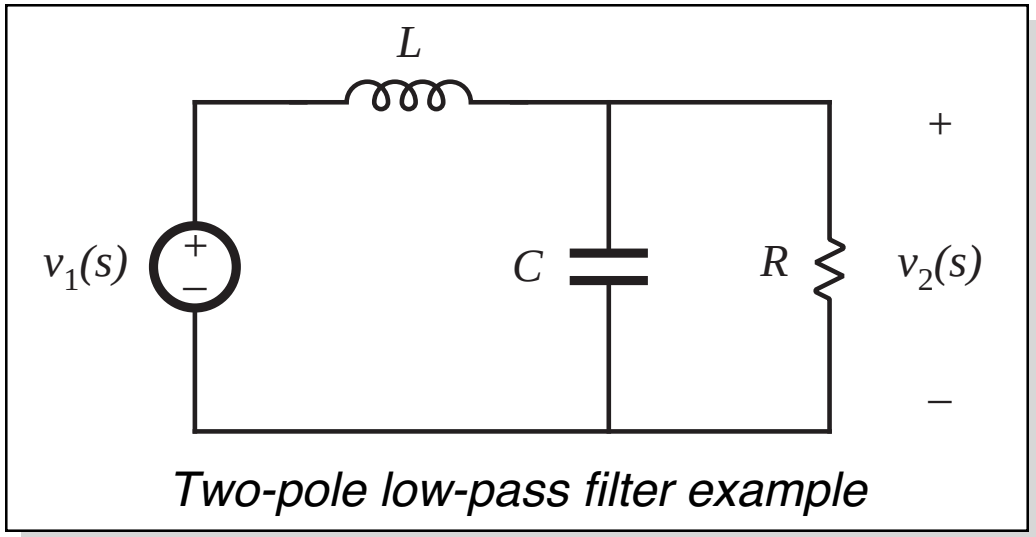
Example

$$G(s) = \frac{v_2(s)}{v_1(s)} = \frac{1}{1 + s\frac{L}{R} + s^2 LC}$$

Second-order denominator, of the form

$$G(s) = \frac{1}{1 + a_1 s + a_2 s^2}$$

with $a_1 = L/R$ and $a_2 = LC$



Two-pole low-pass filter example

How should we construct the Bode diagram?

Approach 1: factor denominator

$$G(s) = \frac{1}{1 + a_1 s + a_2 s^2}$$

We might factor the denominator using the quadratic formula, then construct Bode diagram as the combination of two real poles:

$$G(s) = \frac{1}{\left(1 - \frac{s}{s_1}\right)\left(1 - \frac{s}{s_2}\right)} \quad \text{with} \quad s_1 = -\frac{a_1}{2a_2}\left[1 - \sqrt{1 - \frac{4a_2}{a_1^2}}\right]$$

$$s_2 = -\frac{a_1}{2a_2}\left[1 + \sqrt{1 - \frac{4a_2}{a_1^2}}\right]$$

- If $4a_2 \le a_1^2$, then the roots s_1 and s_2 are real. We can construct Bode diagram as the combination of two real poles.
- If $4a_2 > a_1^2$, then the roots are complex. In Section 8.1.1, the assumption was made that ω_0 is real; hence, the results of that section cannot be applied and we need to do some additional work.

Approach 2: Define a standard normalized form for the quadratic case

$$G(s) = \frac{1}{1 + 2\zeta \frac{s}{\omega_0} + \left(\frac{s}{\omega_0}\right)^2} \qquad \text{or} \qquad G(s) = \frac{1}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2}$$

- When the coefficients of s are real and positive, then the parameters ζ, ω_0, and Q are also real and positive
- The parameters ζ, ω_0, and Q are found by equating the coefficients of s
- The parameter ω_0 is the angular corner frequency, and we can define $f_0 = \omega_0/2\pi$
- The parameter ζ is called the *damping factor.* ζ controls the shape of the exact curve in the vicinity of $f = f_0$. The roots are complex when $\zeta < 1$.
- In the alternative form, the parameter Q is called the *quality factor. Q* also controls the shape of the exact curve in the vicinity of $f = f_0$. The roots are complex when $Q > 0.5$.

The Q-factor

In a second-order system, ζ and Q are related according to

$$Q = \frac{1}{2\zeta}$$

Q is a measure of the dissipation in the system. A more general definition of Q, for sinusoidal excitation of a passive element or system is

$$Q = 2\pi \frac{\text{(peak stored energy)}}{\text{(energy dissipated per cycle)}}$$

For a second-order passive system, the two equations above are equivalent. We will see that Q has a simple interpretation in the Bode diagrams of second-order transfer functions.

Analytical expressions for f_0 and Q

Two-pole low-pass filter example: we found that

$$G(s) = \frac{v_2(s)}{v_1(s)} = \frac{1}{1 + s\frac{L}{R} + s^2 LC}$$

Equate coefficients of like powers of s with the standard form

$$G(s) = \frac{1}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2}$$

Result:

$$f_0 = \frac{\omega_0}{2\pi} = \frac{1}{2\pi\sqrt{LC}}$$

$$Q = R\sqrt{\frac{C}{L}}$$

Magnitude asymptotes, quadratic form

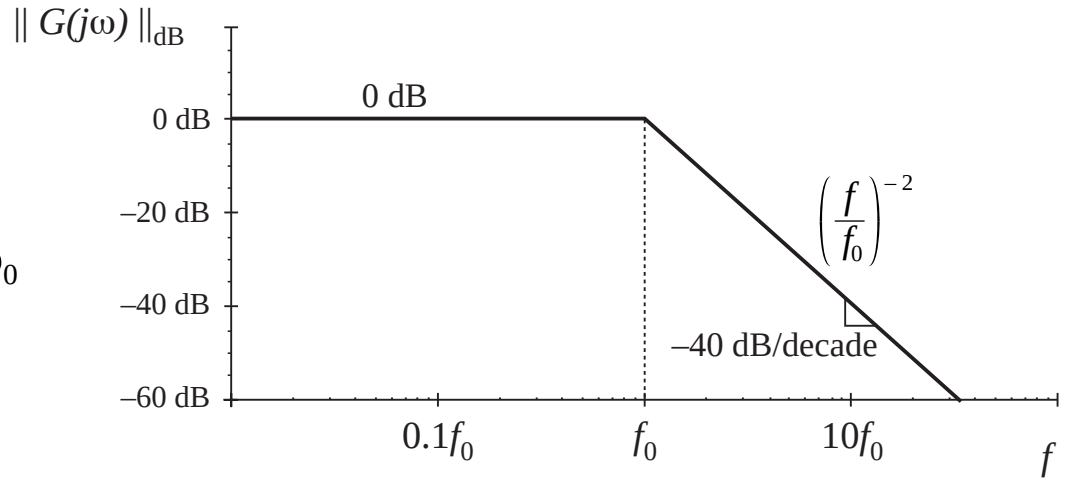
In the form $$G(s) = \frac{1}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2}$$

let $s = j\omega$ and find magnitude: $$\left\| G(j\omega) \right\| = \frac{1}{\sqrt{\left(1 - \left(\frac{\omega}{\omega_0}\right)^2\right)^2 + \frac{1}{Q^2}\left(\frac{\omega}{\omega_0}\right)^2}}$$

Asymptotes are

$$\left\| G \right\| \rightarrow 1 \quad \text{for } \omega << \omega_0$$

$$\left\| G \right\| \rightarrow \left(\frac{f}{f_0}\right)^{-2} \quad \text{for } \omega >> \omega_0$$



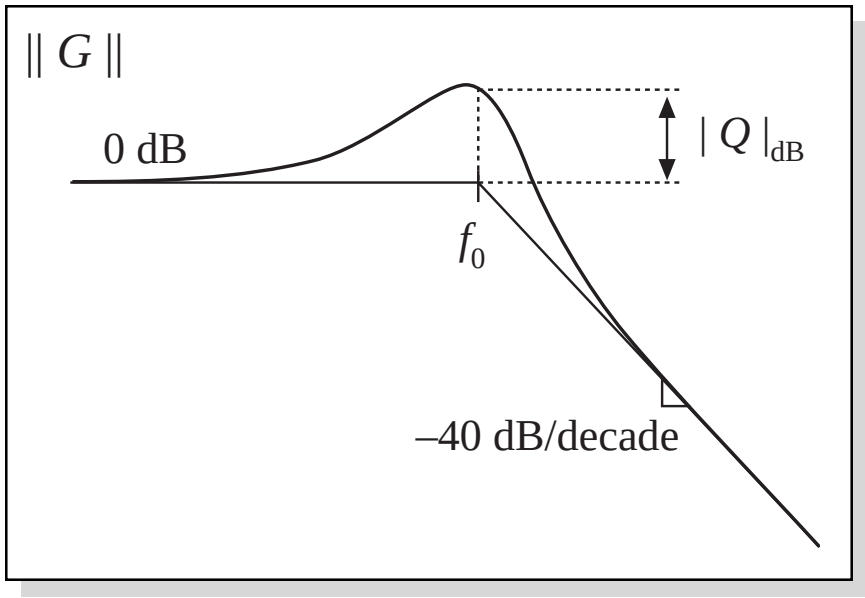
Deviation of exact curve from magnitude asymptotes

$$\left\| G(j\omega) \right\| = \frac{1}{\sqrt{\left(1 - \left(\frac{\omega}{\omega_0}\right)^2\right)^2 + \frac{1}{Q^2}\left(\frac{\omega}{\omega_0}\right)^2}}$$

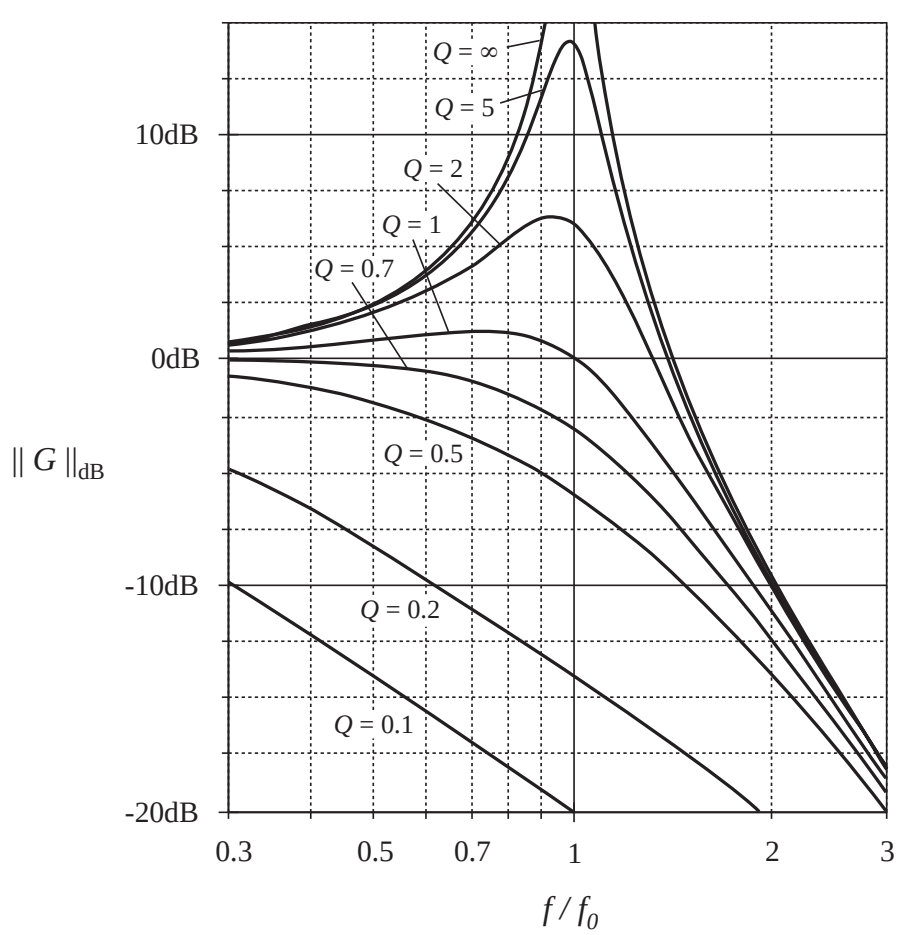
At $\omega = \omega_0$, the exact magnitude is

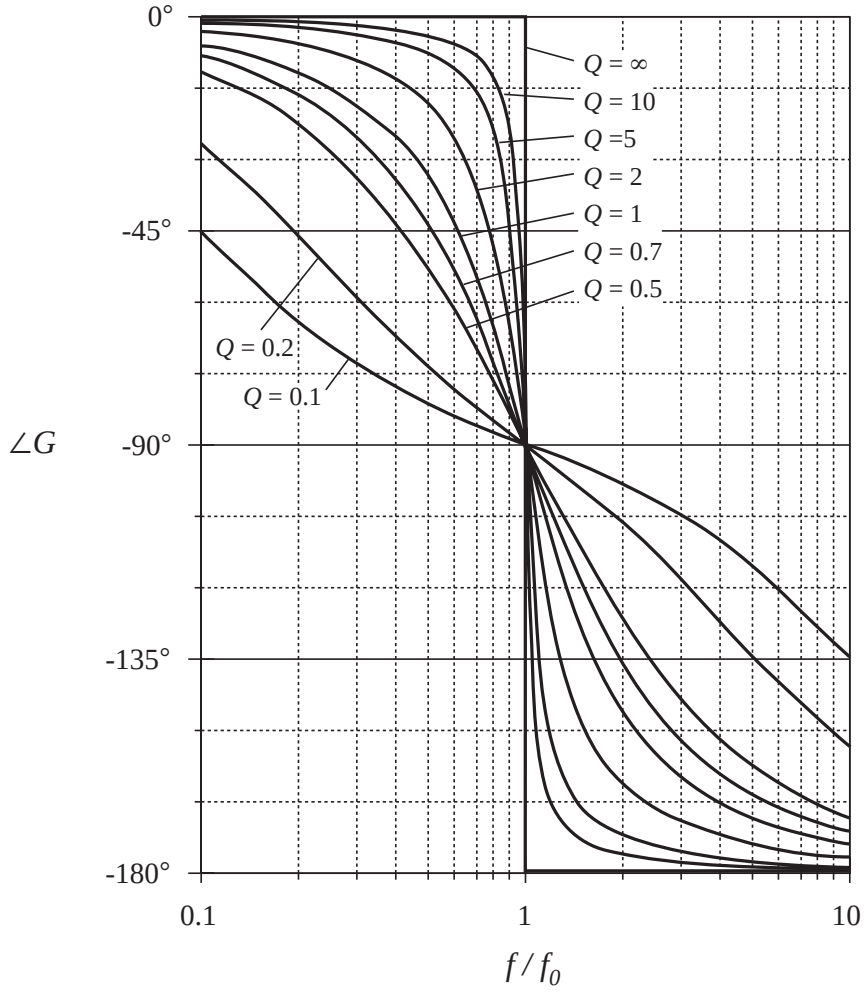
$$\left\| G(j\omega_0) \right\| = Q \qquad \text{or, in dB:} \qquad \left\| G(j\omega_0) \right\|_{\text{dB}} = \left| Q \right|_{\text{dB}}$$

The exact curve has magnitude Q at $f = f_0$. The deviation of the exact curve from the asymptotes is $| Q |_{\text{dB}}$



Two-pole response: exact curves





8.1.7. The low-Q approximation

Given a second-order denominator polynomial, of the form

$$G(s) = \frac{1}{1 + a_1 s + a_2 s^2} \qquad \text{or} \qquad G(s) = \frac{1}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2}$$

When the roots are real, i.e., when $Q < 0.5$, then we can factor the denominator, and construct the Bode diagram using the asymptotes for real poles. We would then use the following normalized form:

$$G(s) = \frac{1}{\left(1 + \frac{s}{\omega_1}\right)\left(1 + \frac{s}{\omega_2}\right)}$$

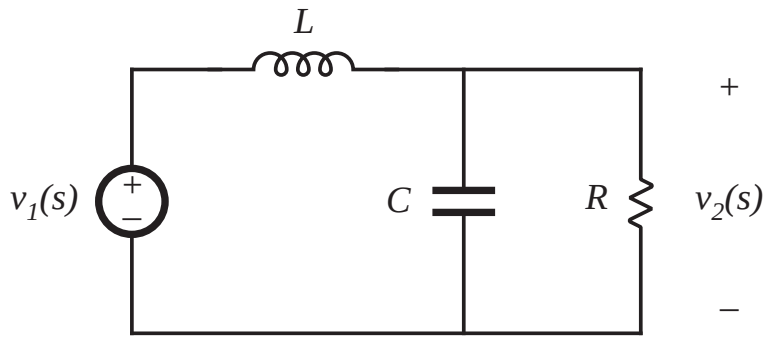
This is a particularly desirable approach when $Q << 0.5$, i.e., when the corner frequencies ω_1 and ω_2 are well separated.

An example

A problem with this procedure is the complexity of the quadratic formula used to find the corner frequencies.

R-L-C network example:

$$G(s) = \frac{v_2(s)}{v_1(s)} = \frac{1}{1 + s\frac{L}{R} + s^2 LC}$$



Use quadratic formula to factor denominator. Corner frequencies are:

$$\omega_1, \omega_2 = \frac{L/R \pm \sqrt{\left(L/R\right)^2 - 4\,LC}}{2\,LC}$$

Factoring the denominator

$$\omega_1, \omega_2 = \frac{L/R \pm \sqrt{\left(L/R\right)^2 - 4\,LC}}{2\,LC}$$

This complicated expression yields little insight into how the corner frequencies ω_1 and ω_2 depend on R, L, and C.

When the corner frequencies are well separated in value, it can be shown that they are given by the much simpler (approximate) expressions

$$\omega_1 \approx \frac{R}{L}, \qquad \omega_2 \approx \frac{1}{RC}$$

ω_1 is then independent of C, and ω_2 is independent of L.

These simpler expressions can be derived via the Low-Q Approximation.

Derivation of the Low-Q Approximation

Given

$$G(s) = \frac{1}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2}$$

Use quadratic formula to express corner frequencies ω_1 and ω_2 in terms of Q and ω_0 as:

$$\omega_1 = \frac{\omega_0}{Q} \frac{1 - \sqrt{1 - 4Q^2}}{2} \qquad \omega_2 = \frac{\omega_0}{Q} \frac{1 + \sqrt{1 - 4Q^2}}{2}$$

Corner frequency ω_2

$$\omega_2 = \frac{\omega_0}{Q} \frac{1 + \sqrt{1 - 4Q^2}}{2}$$

can be written in the form

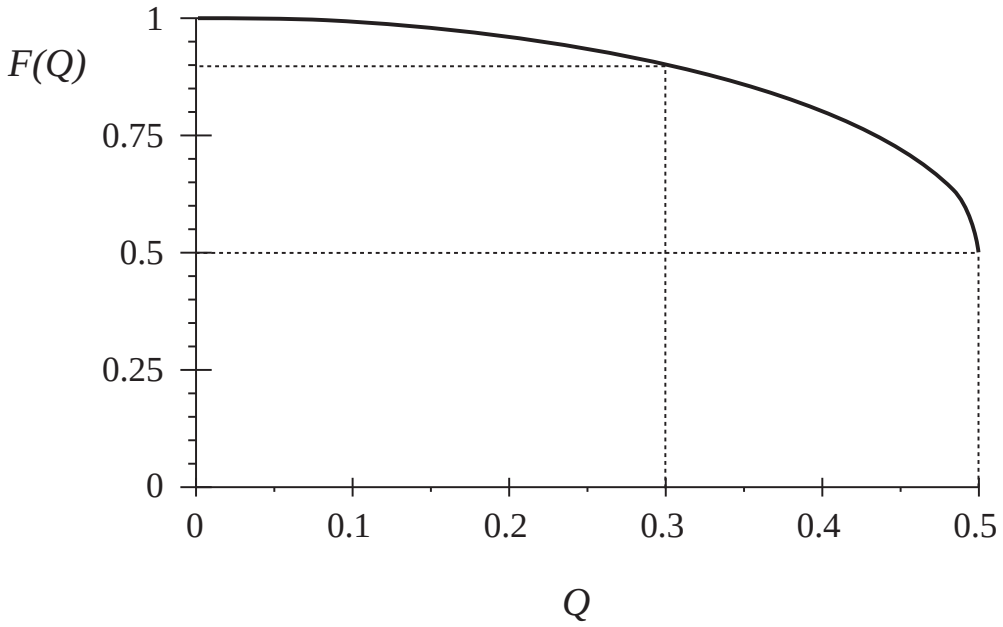
$$\omega_2 = \frac{\omega_0}{Q} F(Q)$$

where

$$F(Q) = \frac{1}{2}\left(1 + \sqrt{1 - 4Q^2}\right)$$

For small Q, $F(Q)$ tends to 1. We then obtain

$$\omega_2 \approx \frac{\omega_0}{Q} \quad \text{for} \quad Q << \frac{1}{2}$$



For $Q < 0.3$, the approximation $F(Q) = 1$ is within 10% of the exact value.

Corner frequency ω_1

$$\omega_1 = \frac{\omega_0}{Q} \frac{1 - \sqrt{1 - 4Q^2}}{2}$$

can be written in the form

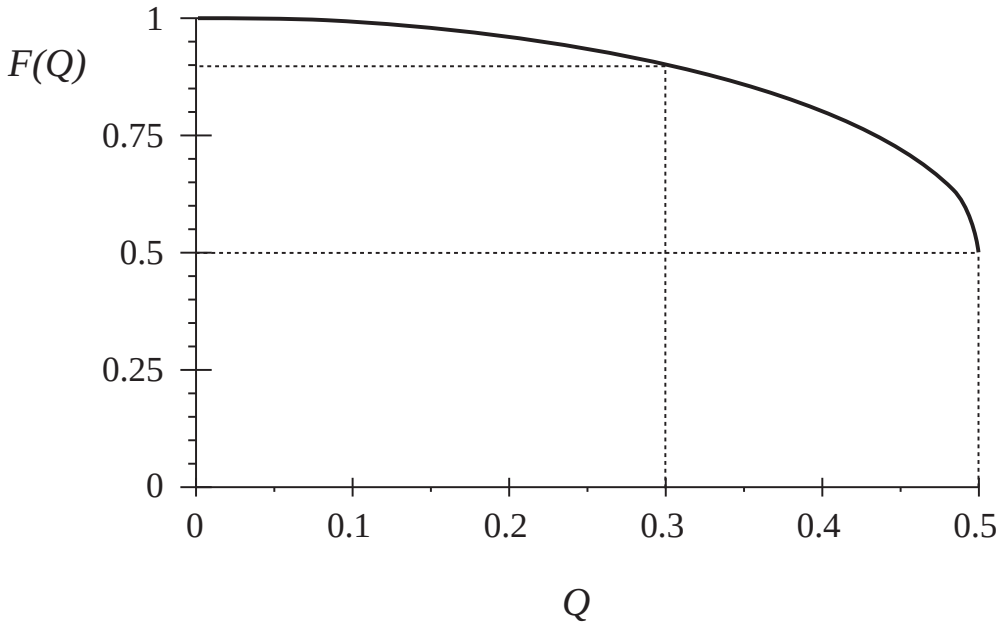
$$\omega_1 = \frac{Q\,\omega_0}{F(Q)}$$

where

$$F(Q) = \frac{1}{2}\left(1 + \sqrt{1 - 4Q^2}\right)$$

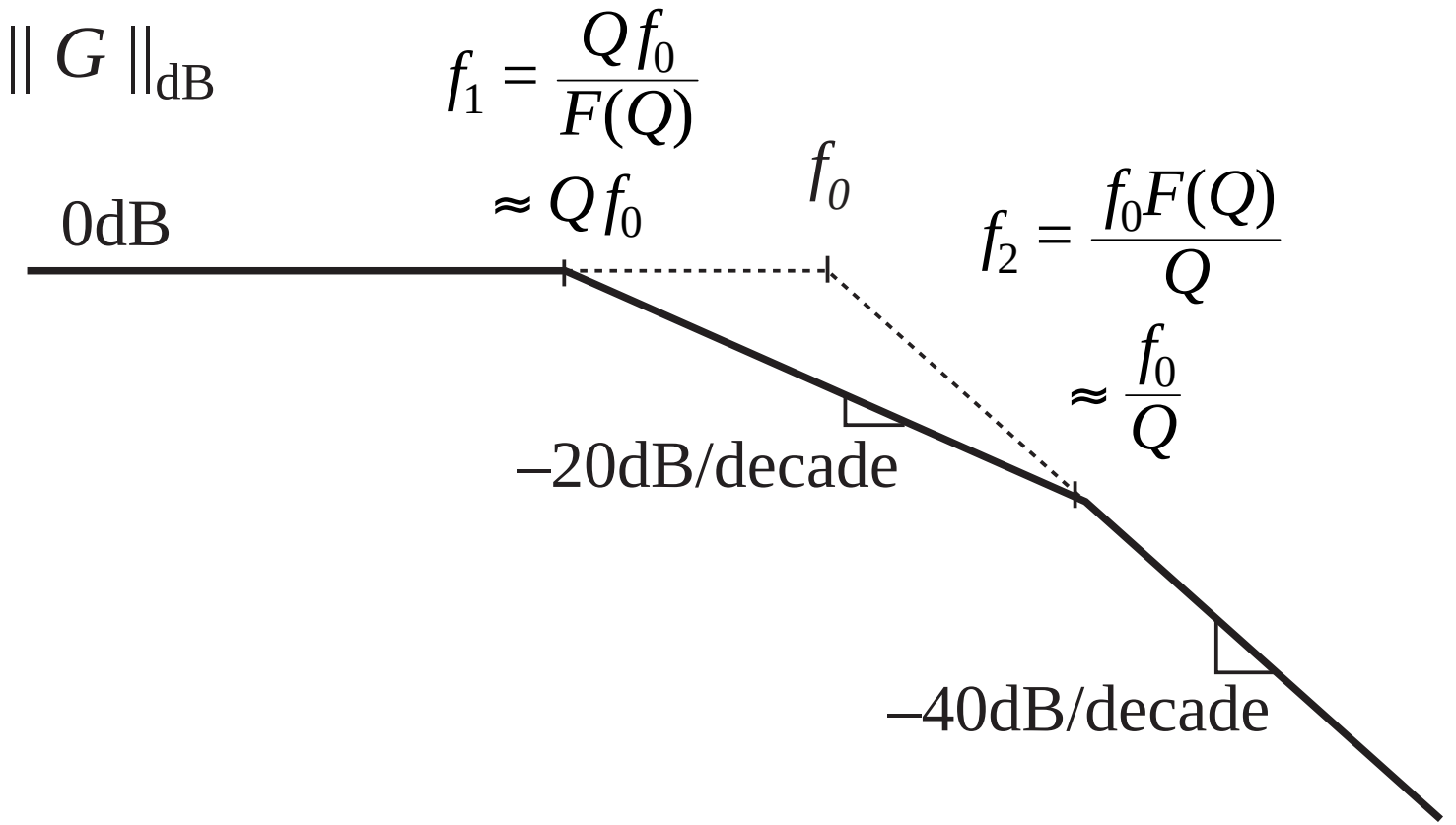
For small Q, $F(Q)$ tends to 1. We then obtain

$$\omega_1 \approx Q\,\omega_0 \quad \text{for} \quad Q << \frac{1}{2}$$



For $Q < 0.3$, the approximation $F(Q) = 1$ is within 10% of the exact value.

The Low-Q Approximation



R-L-C Example

For the previous example:

$$G(s) = \frac{v_2(s)}{v_1(s)} = \frac{1}{1 + s\frac{L}{R} + s^2 LC}$$

$$f_0 = \frac{\omega_0}{2\pi} = \frac{1}{2\pi\sqrt{LC}}$$

$$Q = R\sqrt{\frac{C}{L}}$$

Use of the Low-Q Approximation leads to

$$\omega_1 \approx Q\,\omega_0 = R\sqrt{\frac{C}{L}}\,\frac{1}{\sqrt{LC}} = \frac{R}{L}$$

$$\omega_2 \approx \frac{\omega_0}{Q} = \frac{1}{\sqrt{LC}}\,\frac{1}{R\sqrt{\frac{C}{L}}} = \frac{1}{RC}$$

8.1.8. Approximate Roots of an Arbitrary-Degree Polynomial

Generalize the low-Q approximation to obtain approximate factorization of the n^{th}-order polynomial

$$P(s) = 1 + a_1 s + a_2 s^2 + \cdots + a_n s^n$$

It is desired to factor this polynomial in the form

$$P(s) = \left(1 + \tau_1 s\right)\left(1 + \tau_2 s\right) \cdots \left(1 + \tau_n s\right)$$

When the roots are real and well separated in value, then approximate analytical expressions for the time constants τ_1, τ_2, ... τ_n can be found, that typically are simple functions of the circuit element values.

Objective: find a general method for deriving such expressions. Include the case of complex root pairs.

Derivation of method

Multiply out factored form of polynomial, then equate to original form (equate like powers of s):

$$a_1 = \tau_1 + \tau_2 + \cdots + \tau_n$$

$$a_2 = \tau_1\left(\tau_2 + \cdots + \tau_n\right) + \tau_2\left(\tau_3 + \cdots + \tau_n\right) + \cdots$$

$$a_3 = \tau_1\tau_2\left(\tau_3 + \cdots + \tau_n\right) + \tau_2\tau_3\left(\tau_4 + \cdots + \tau_n\right) + \cdots$$

$$\vdots$$

$$a_n = \tau_1\tau_2\tau_3\cdots\tau_n$$

- Exact system of equations relating roots to original coefficients
- Exact general solution is hopeless
- Under what conditions can solution for time constants be easily approximated?

Approximation of time constants
when roots are real and well separated

System of equations:

(from previous slide)

$$a_1 = \tau_1 + \tau_2 + \cdots + \tau_n$$

$$a_2 = \tau_1\left(\tau_2 + \cdots + \tau_n\right) + \tau_2\left(\tau_3 + \cdots + \tau_n\right) + \cdots$$

$$a_3 = \tau_1\tau_2\left(\tau_3 + \cdots + \tau_n\right) + \tau_2\tau_3\left(\tau_4 + \cdots + \tau_n\right) + \cdots$$

$$\vdots$$

$$a_n = \tau_1\tau_2\tau_3\cdots\tau_n$$

Suppose that roots are real and well-separated, and are arranged in decreasing order of magnitude:

$$\left|\tau_1\right| >> \left|\tau_2\right| >> \cdots >> \left|\tau_n\right|$$

Then the first term of each equation is dominant

$\Rightarrow$ Neglect second and following terms in each equation above

Approximation of time constants
when roots are real and well separated

System of equations:

(only first term in each equation is included)

$$a_1 \approx \tau_1$$
$$a_2 \approx \tau_1 \tau_2$$
$$a_3 \approx \tau_1 \tau_2 \tau_3$$
$$\vdots$$
$$a_n = \tau_1 \tau_2 \tau_3 \cdots \tau_n$$

Solve for the time constants:

$$\tau_1 \approx a_1$$
$$\tau_2 \approx \frac{a_2}{a_1}$$
$$\tau_3 \approx \frac{a_3}{a_2}$$
$$\vdots$$
$$\tau_n \approx \frac{a_n}{a_{n-1}}$$

Result
when roots are real and well separated

If the following inequalities are satisfied

$$\left| a_1 \right| >> \left| \frac{a_2}{a_1} \right| >> \left| \frac{a_3}{a_2} \right| >> \cdots >> \left| \frac{a_n}{a_{n-1}} \right|$$

Then the polynomial $P(s)$ has the following approximate factorization

$$P(s) \approx \left(1 + a_1 s\right) \left(1 + \frac{a_2}{a_1} s\right) \left(1 + \frac{a_3}{a_2} s\right) \cdots \left(1 + \frac{a_n}{a_{n-1}} s\right)$$

- If the a_n coefficients are simple analytical functions of the element values L, C, etc., then the roots are similar simple analytical functions of L, C, etc.
- Numerical values are used to justify the approximation, but analytical expressions for the roots are obtained

When two roots are not well separated
then leave their terms in quadratic form

Suppose inequality k is not satisfied:

$$\left|a_1\right| >> \left|\frac{a_2}{a_1}\right| >> \cdots >> \left|\frac{a_k}{a_{k-1}}\right| \quad \not>> \quad \left|\frac{a_{k+1}}{a_k}\right| >> \cdots >> \left|\frac{a_n}{a_{n-1}}\right|$$

↑
not
satisfied

Then leave the terms corresponding to roots k and $(k+1)$ in quadratic form, as follows:

$$P(s) \approx \left(1 + a_1 s\right)\left(1 + \frac{a_2}{a_1} s\right) \cdots \left(1 + \frac{a_k}{a_{k-1}} s + \frac{a_{k+1}}{a_{k-1}} s^2\right) \cdots \left(1 + \frac{a_n}{a_{n-1}} s\right)$$

This approximation is accurate provided

$$\left|a_1\right| >> \left|\frac{a_2}{a_1}\right| >> \cdots >> \left|\frac{a_k}{a_{k-1}}\right| >> \left|\frac{a_{k-2}\, a_{k+1}}{a_{k-1}^2}\right| >> \left|\frac{a_{k+2}}{a_{k+1}}\right| >> \cdots >> \left|\frac{a_n}{a_{n-1}}\right|$$

When the first inequality is violated

A special case for quadratic roots

When inequality 1 is not satisfied:

$$\left| a_1 \right| \not>> \left| \frac{a_2}{a_1} \right| >> \left| \frac{a_3}{a_2} \right| >> \cdots >> \left| \frac{a_n}{a_{n-1}} \right|$$

↑

not satisfied

Then leave the first two roots in quadratic form, as follows:

$$P(s) \approx \left(1 + a_1 s + a_2 s^2\right) \left(1 + \frac{a_3}{a_2} s\right) \cdots \left(1 + \frac{a_n}{a_{n-1}} s\right)$$

This approximation is justified provided

$$\left| \frac{a_2^2}{a_3} \right| >> \left| a_1 \right| >> \left| \frac{a_3}{a_2} \right| >> \left| \frac{a_4}{a_3} \right| >> \cdots >> \left| \frac{a_n}{a_{n-1}} \right|$$

Other cases

- When several isolated inequalities are violated
  - —Leave the corresponding roots in quadratic form
  - —See next two slides

- When several adjacent inequalities are violated
  - —Then the corresponding roots are close in value
  - —Must use cubic or higher-order roots

Leaving adjacent roots in quadratic form

In the case when inequality *k* is not satisfied:

$$\left|a_1\right| \gg \left|\frac{a_2}{a_1}\right| \gg \cdots \gg \left|\frac{a_k}{a_{k-1}}\right| \not\gg \left|\frac{a_{k+1}}{a_k}\right| \gg \cdots \gg \left|\frac{a_n}{a_{n-1}}\right|$$

Then leave the corresponding roots in quadratic form:

$$P(s) \approx \left(1 + a_1 s\right)\left(1 + \frac{a_2}{a_1} s\right) \cdots \left(1 + \frac{a_k}{a_{k-1}} s + \frac{a_{k+1}}{a_{k-1}} s^2\right) \cdots \left(1 + \frac{a_n}{a_{n-1}} s\right)$$

This approximation is accurate provided that

$$\left|a_1\right| \gg \left|\frac{a_2}{a_1}\right| \gg \cdots \gg \left|\frac{a_k}{a_{k-1}}\right| \gg \left|\frac{a_{k-2}\, a_{k+1}}{a_{k-1}^2}\right| \gg \left|\frac{a_{k+2}}{a_{k+1}}\right| \gg \cdots \gg \left|\frac{a_n}{a_{n-1}}\right|$$

(derivation is similar to the case of well-separated roots)

When the first inequality is not satisfied

The formulas of the previous slide require a special form for the case when the first inequality is not satisfied:

$$\left| a_1 \right| \not\gg \left| \frac{a_2}{a_1} \right| \gg \left| \frac{a_3}{a_2} \right| \gg \cdots \gg \left| \frac{a_n}{a_{n-1}} \right|$$

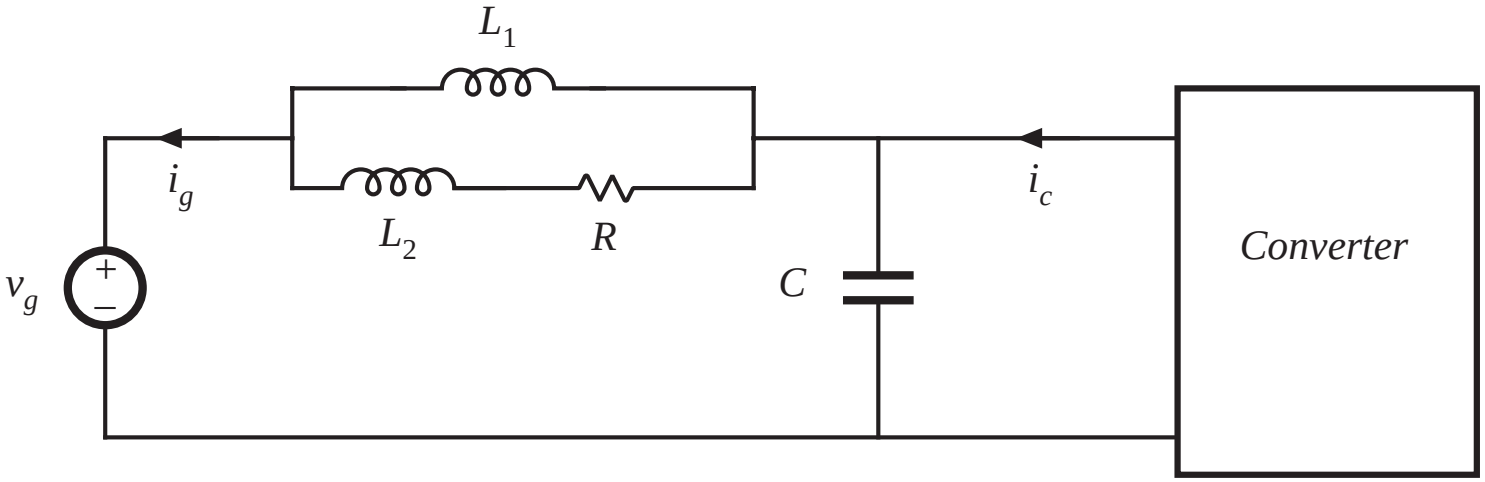
We should then use the following form:

$$P(s) \approx \left(1 + a_1 s + a_2 s^2\right) \left(1 + \frac{a_3}{a_2} s\right) \cdots \left(1 + \frac{a_n}{a_{n-1}} s\right)$$

The conditions for validity of this approximation are:

$$\left| \frac{a_2^2}{a_3} \right| \gg \left| a_1 \right| \gg \left| \frac{a_3}{a_2} \right| \gg \left| \frac{a_4}{a_3} \right| \gg \cdots \gg \left| \frac{a_n}{a_{n-1}} \right|$$

Example
Damped input EMI filter



$$G(s) = \frac{i_g(s)}{i_c(s)} = \frac{1 + s\,\dfrac{L_1 + L_2}{R}}{1 + s\,\dfrac{L_1 + L_2}{R} + s^2 L_1 C + s^3\,\dfrac{L_1 L_2 C}{R}}$$

Example

Approximate factorization of a third-order denominator

The filter transfer function from the previous slide is

$$G(s) = \frac{i_g(s)}{i_c(s)} = \frac{1 + s\,\frac{L_1 + L_2}{R}}{1 + s\,\frac{L_1 + L_2}{R} + s^2 L_1 C + s^3\,\frac{L_1 L_2 C}{R}}$$

—contains a third-order denominator, with the following coefficients:

$$a_1 = \frac{L_1 + L_2}{R}$$

$$a_2 = L_1 C$$

$$a_3 = \frac{L_1 L_2 C}{R}$$

Real roots case

Factorization as three real roots:

$$\left(1 + s\frac{L_1 + L_2}{R}\right)\left(1 + sRC\frac{L_1}{L_1 + L_2}\right)\left(1 + s\frac{L_2}{R}\right)$$

This approximate analytical factorization is justified provided

$$\frac{L_1 + L_2}{R} >> RC\frac{L_1}{L_1 + L_2} >> \frac{L_2}{R}$$

Note that these inequalities cannot be satisfied unless $L_1 >> L_2$. The above inequalities can then be further simplified to

$$\frac{L_1}{R} >> RC >> \frac{L_2}{R}$$

And the factored polynomial reduces to

$$\left(1 + s\frac{L_1}{R}\right)\left(1 + sRC\right)\left(1 + s\frac{L_2}{R}\right)$$

- *Illustrates in a simple way how the roots depend on the element values*

When the second inequality is violated

$$\frac{L_1 + L_2}{R} >> RC \frac{L_1}{L_1 + L_2} \quad \not\gg \quad \frac{L_2}{R}$$

↑

not satisfied

Then leave the second and third roots in quadratic form:

$$P(s) = \left(1 + a_1 s\right)\left(1 + \frac{a_2}{a_1} s + \frac{a_3}{a_1} s^2\right)$$

which is

$$\left(1 + s \frac{L_1 + L_2}{R}\right)\left(1 + sRC \frac{L_1}{L_1 + L_2} + s^2 L_1 || L_2 C\right)$$

Validity of the approximation

This is valid provided

$$\frac{L_1 + L_2}{R} >> RC \quad \frac{L_1}{L_1 + L_2} >> \frac{L_1 || L_2}{L_1 + L_2} RC \qquad \text{(use } a_0 = 1\text{)}$$

These inequalities are equivalent to

$$L_1 >> L_2, \quad \text{and} \quad \frac{L_1}{R} >> RC$$

It is no longer required that $RC >> L_2/R$

The polynomial can therefore be written in the simplified form

$$\left(1 + s\frac{L_1}{R}\right)\left(1 + sRC + s^2 L_2 C\right)$$

When the first inequality is violated

$$\frac{L_1 + L_2}{R} \not\gg RC\frac{L_1}{L_1 + L_2} >> \frac{L_2}{R}$$

↑

not satisfied

Then leave the first and second roots in quadratic form:

$$P(s) = \left(1 + a_1 s + a_2 s^2\right)\left(1 + \frac{a_3}{a_2} s\right)$$

which is

$$\left(1 + s\frac{L_1 + L_2}{R} + s^2 L_1 C\right)\left(1 + s\frac{L_2}{R}\right)$$

Validity of the approximation

This is valid provided

$$\frac{L_1 RC}{L_2} >> \frac{L_1 + L_2}{R} >> \frac{L_2}{R}$$

These inequalities are equivalent to

$$L_1 >> L_2, \quad \text{and} \quad RC >> \frac{L_2}{R}$$

It is no longer required that $L_1/R >> RC$

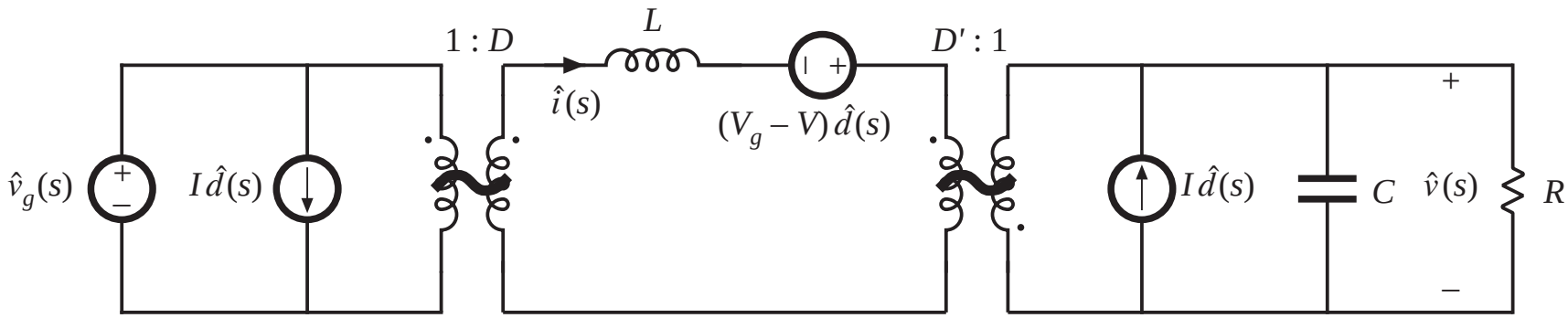
The polynomial can therefore be written in the simplified form

$$\left(1 + s\frac{L_1}{R} + s^2 L_1 C\right)\left(1 + s\frac{L_2}{R}\right)$$

8.2. Analysis of converter transfer functions

8.2.1. Example: transfer functions of the buck-boost converter

Small-signal ac model of the buck-boost converter, derived in Chapter 7:



Definition of transfer functions

The converter contains two inputs, $\hat{d}(s)$ and $\hat{v}_g(s)$ and one output, $\hat{v}(s)$

Hence, the ac output voltage variations can be expressed as the superposition of terms arising from the two inputs:

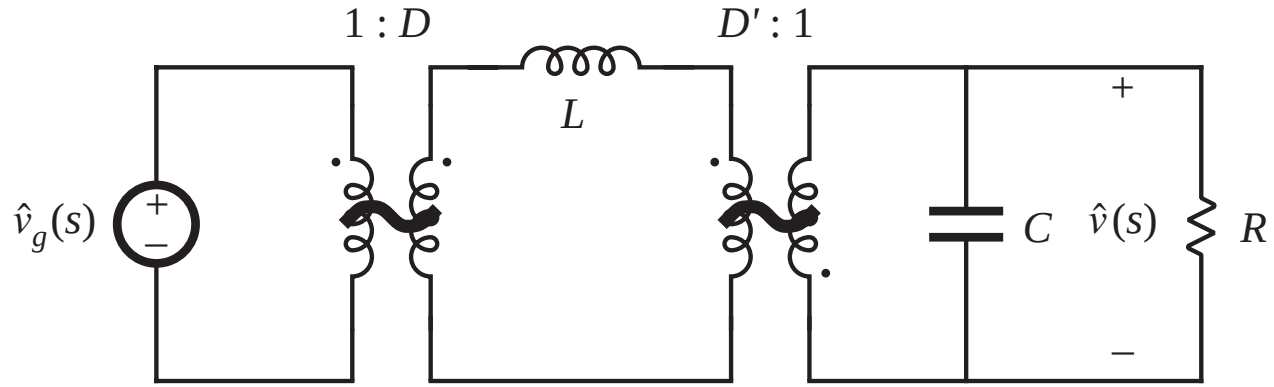
$$\hat{v}(s) = G_{vd}(s)\,\hat{d}(s) + G_{vg}(s)\,\hat{v}_g(s)$$

The control-to-output and line-to-output transfer functions can be defined as

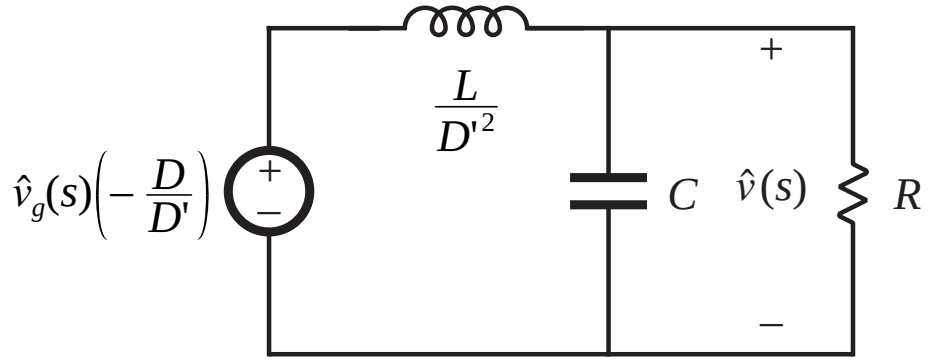
$$G_{vd}(s) = \left.\frac{\hat{v}(s)}{\hat{d}(s)}\right|_{\hat{v}_g(s) = 0} \quad \text{and} \quad G_{vg}(s) = \left.\frac{\hat{v}(s)}{\hat{v}_g(s)}\right|_{\hat{d}(s) = 0}$$

Derivation of line-to-output transfer function $G_{vg}(s)$

Set $\hat{d}$ sources to zero:



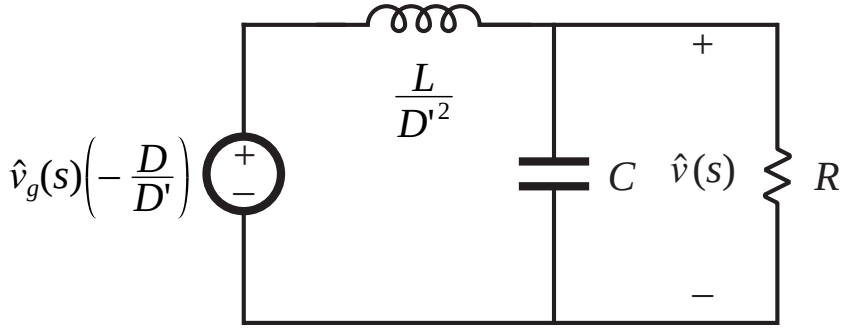
Push elements through transformers to output side:



Derivation of transfer functions

Use voltage divider formula to solve for transfer function:

$$G_{vg}(s) = \left.\frac{\hat{v}(s)}{\hat{v}_g(s)}\right|_{\hat{d}(s)=0} = -\frac{D}{D'}\,\frac{\left(R \parallel \frac{1}{sC}\right)}{\frac{sL}{D'^2} + \left(R \parallel \frac{1}{sC}\right)}$$



Expand parallel combination and express as a rational fraction:

$$G_{vg}(s) = \left(-\frac{D}{D'}\right)\frac{\left(\frac{R}{1+sRC}\right)}{\frac{sL}{D'^2} + \left(\frac{R}{1+sRC}\right)}$$

$$= \left(-\frac{D}{D'}\right)\frac{R}{R + \frac{sL}{D'^2} + \frac{s^2RLC}{D'^2}}$$

We aren't done yet! Need to write in normalized form, where the coefficient of s^0 is 1, and then identify salient features

Derivation of transfer functions

Divide numerator and denominator by R. Result: the line-to-output transfer function is

$$G_{vg}(s) = \left. \frac{\hat{v}(s)}{\hat{v}_g(s)} \right|_{\hat{d}(s) = 0} = \left(-\frac{D}{D'} \right) \frac{1}{1 + s \frac{L}{D'^2 R} + s^2 \frac{LC}{D'^2}}$$

which is of the following standard form:

$$G_{vg}(s) = G_{g0} \frac{1}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0} \right)^2}$$

Salient features of the line-to-output transfer function

Equate standard form to derived transfer function, to determine expressions for the salient features:

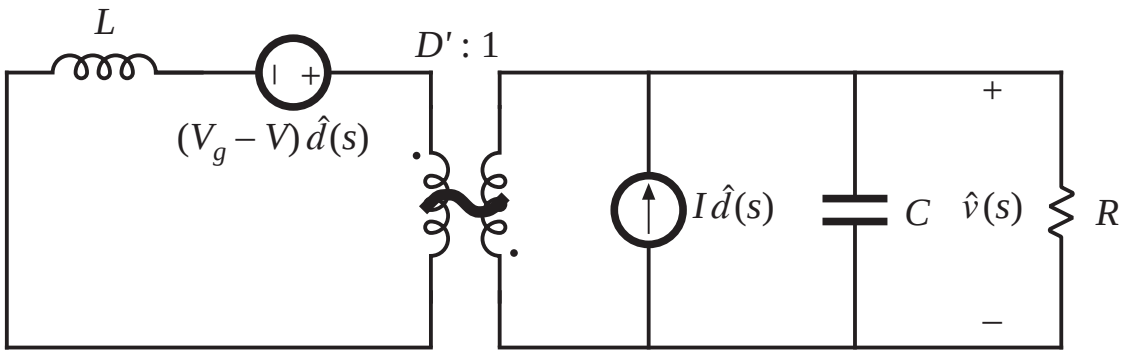
$$G_{g0} = -\frac{D}{D'}$$

$$\frac{1}{\omega_0^2} = \frac{LC}{D'^2} \qquad \omega_0 = \frac{D'}{\sqrt{LC}}$$

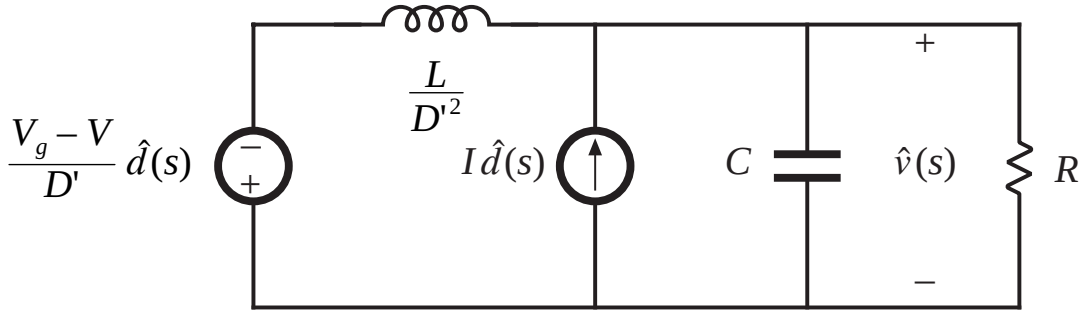
$$\frac{1}{Q\omega_0} = \frac{L}{D'^2 R} \qquad Q = D'R\sqrt{\frac{C}{L}}$$

Derivation of control-to-output transfer function $G_{vd}(s)$

In small-signal model, set $\hat{v}_g$ source to zero:



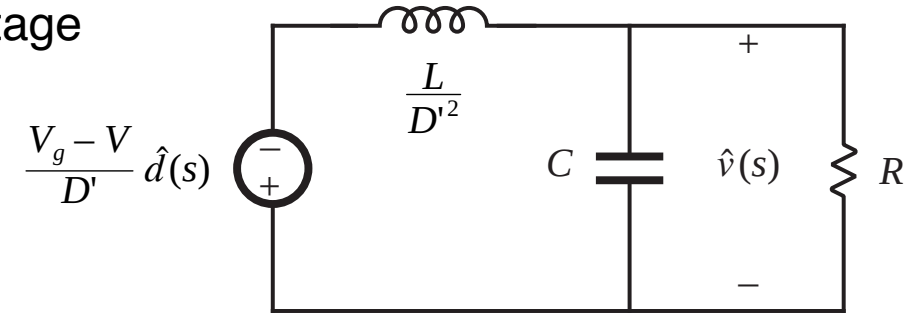
Push all elements to output side of transformer:



There are two $\hat{d}$ sources. One way to solve the model is to use superposition, expressing the output $\hat{v}$ as a sum of terms arising from the two sources.

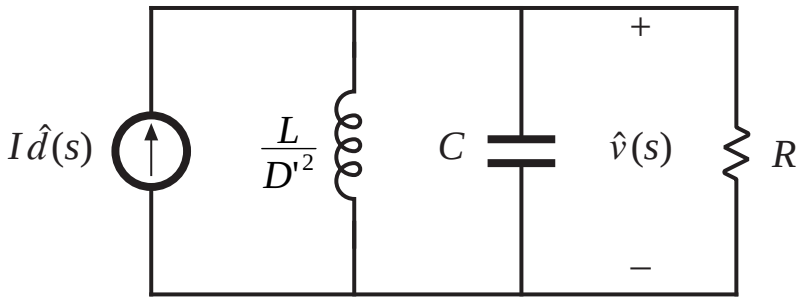
Superposition

With the voltage source only:



$$\frac{\hat{v}(s)}{\hat{d}(s)} = \left(-\frac{V_g - V}{D'}\right) \frac{\left(R \parallel \frac{1}{sC}\right)}{\frac{sL}{D'^2} + \left(R \parallel \frac{1}{sC}\right)}$$

With the current source alone:



$$\frac{\hat{v}(s)}{\hat{d}(s)} = I\left(\frac{sL}{D'^2} \parallel R \parallel \frac{1}{sC}\right)$$

Total:

$$G_{vd}(s) = \left(-\frac{V_g - V}{D'}\right) \frac{\left(R \parallel \frac{1}{sC}\right)}{\frac{sL}{D'^2} + \left(R \parallel \frac{1}{sC}\right)} + I\left(\frac{sL}{D'^2} \parallel R \parallel \frac{1}{sC}\right)$$

Control-to-output transfer function

Express in normalized form:

$$G_{vd}(s) = \left.\frac{\hat{v}(s)}{\hat{d}(s)}\right|_{\hat{v}_g(s)=0} = \left(-\frac{V_g - V}{D'^2}\right) \frac{\left(1 - s\,\frac{LI}{V_g - V}\right)}{\left(1 + s\,\frac{L}{D'^2 R} + s^2\,\frac{LC}{D'^2}\right)}$$

This is of the following standard form:

$$G_{vd}(s) = G_{d0}\,\frac{\left(1 - \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2\right)}$$

Salient features of control-to-output transfer function

$$G_{d0} = -\frac{V_g - V}{D'} = -\frac{V_g}{D'^2} = \frac{V}{DD'}$$

$$\omega_z = \frac{V_g - V}{L\,I} = \frac{D'\,R}{D\,L} \qquad \text{(RHP)}$$

$$\omega_0 = \frac{D'}{\sqrt{LC}}$$

$$Q = D'R\sqrt{\frac{C}{L}}$$

— Simplified using the dc relations: $V = -\frac{D}{D'}\,V_g$

$$I = -\frac{V}{D'\,R}$$

Plug in numerical values

Suppose we are given the following numerical values:

$D = 0.6$

$R = 10\Omega$

$V_g = 30\text{V}$

$L = 160\mu\text{H}$

$C = 160\mu\text{F}$

Then the salient features have the following numerical values:

$$\left| G_{g0} \right| = \frac{D}{D'} = 1.5 \Rightarrow 3.5 \text{ dB}$$

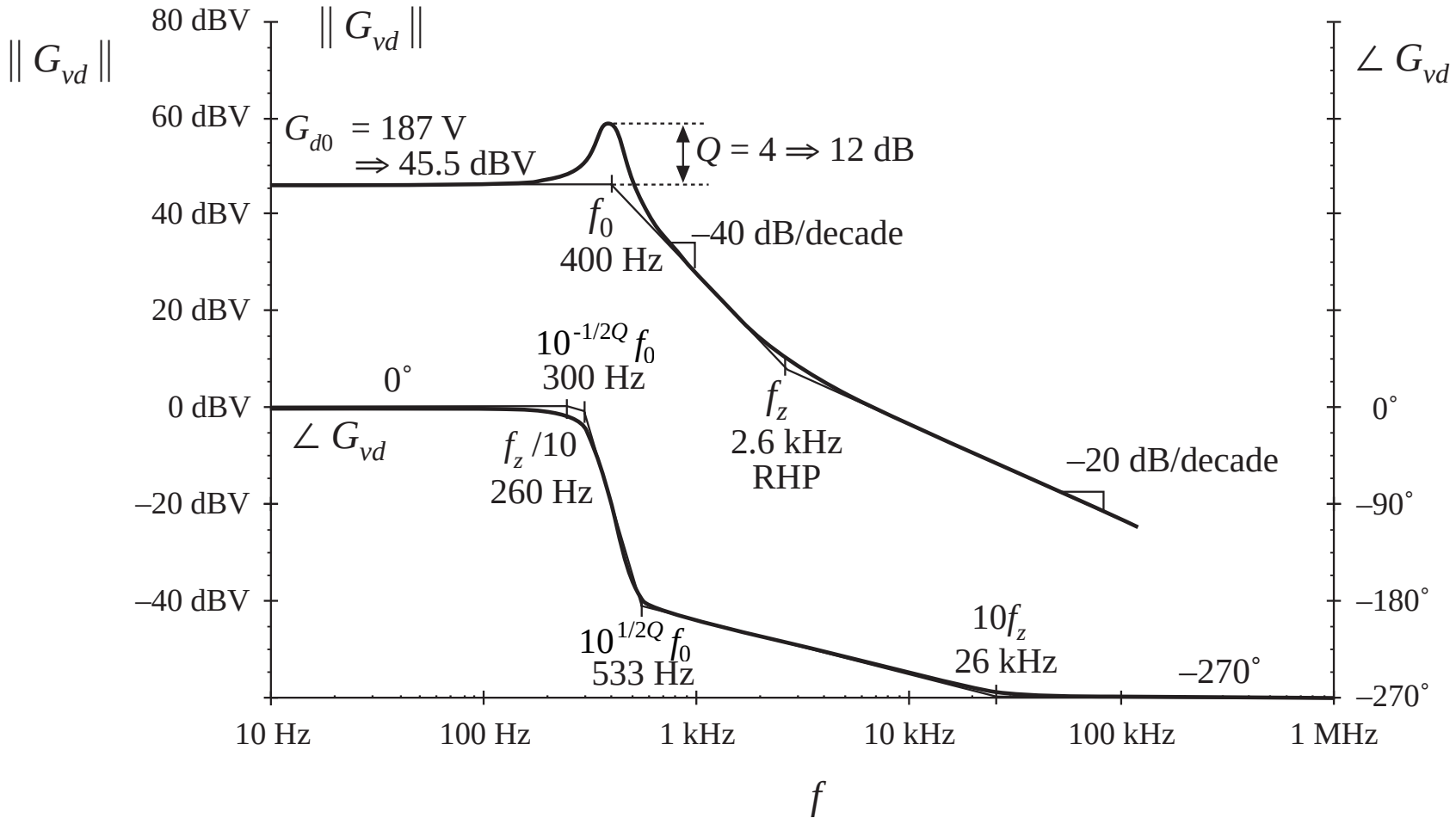
$$\left| G_{d0} \right| = \frac{\left| V \right|}{DD'} = 187.5 \text{ V} \Rightarrow 45.5 \text{ dBV}$$

$$f_0 = \frac{\omega_0}{2\pi} = \frac{D'}{2\pi\sqrt{LC}} = 400 \text{ Hz}$$

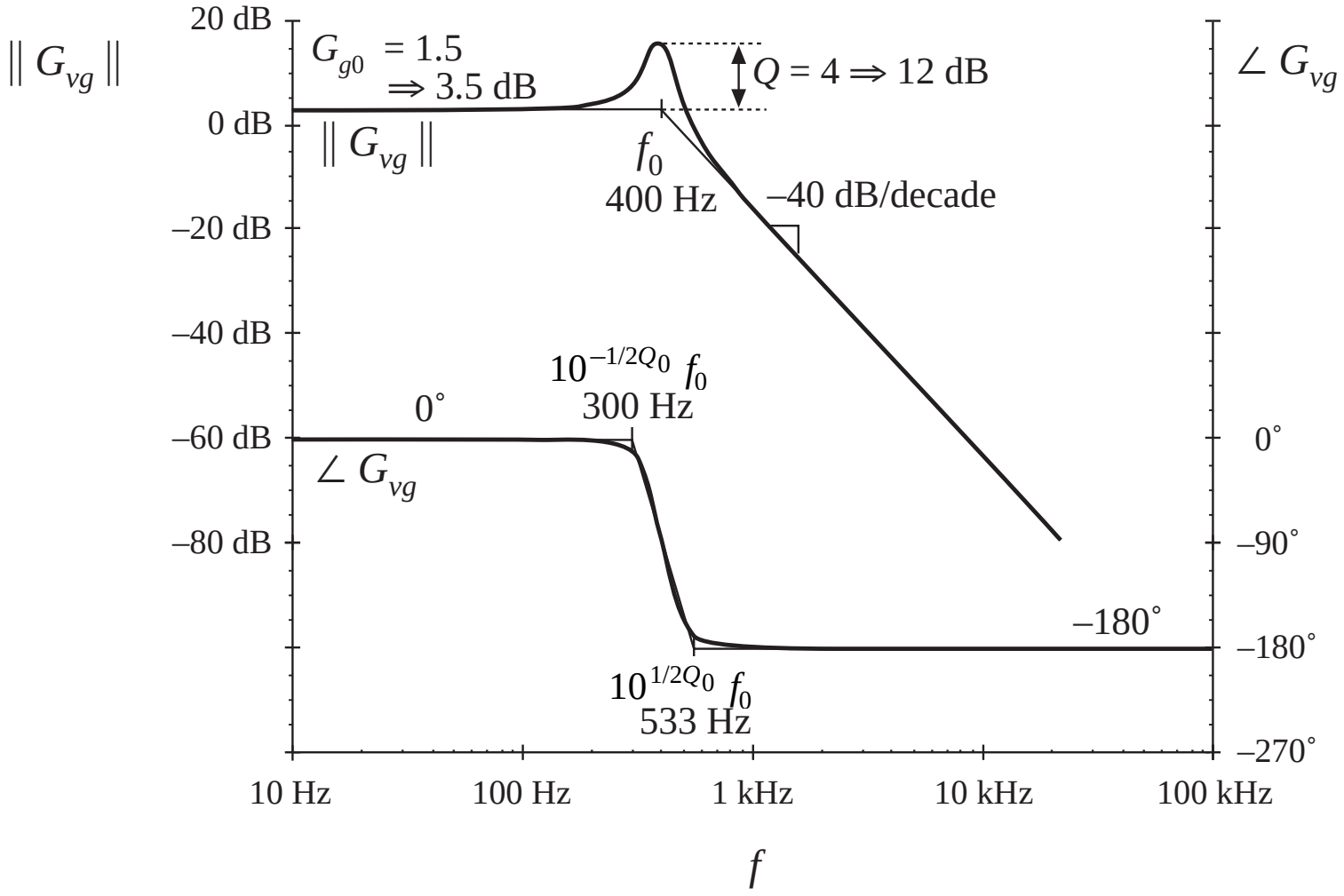
$$Q = D'R\sqrt{\frac{C}{L}} = 4 \Rightarrow 12 \text{ dB}$$

$$f_z = \frac{\omega_z}{2\pi} = \frac{D'^2 R}{2\pi DL} = 2.65 \text{ kHz}$$

Bode plot: control-to-output transfer function



Bode plot: line-to-output transfer function



8.2.2. Transfer functions of some basic CCM converters

Table 8.2. Salient features of the small-signal CCM transfer functions of some basic dc-dc converters

Converter	G_{g0}	G_{d0}	ω_0	Q	ω_z
buck	D	$\frac{V}{D}$	$\frac{1}{\sqrt{LC}}$	$R\sqrt{\frac{C}{L}}$	∞
boost	$\frac{1}{D'}$	$\frac{V}{D'}$	$\frac{D'}{\sqrt{LC}}$	$D'R\sqrt{\frac{C}{L}}$	$\frac{D'^2 R}{L}$
buck-boost	$-\frac{D}{D'}$	$\frac{V}{D\,D'^2}$	$\frac{D'}{\sqrt{LC}}$	$D'R\sqrt{\frac{C}{L}}$	$\frac{D'^2 R}{D\,L}$

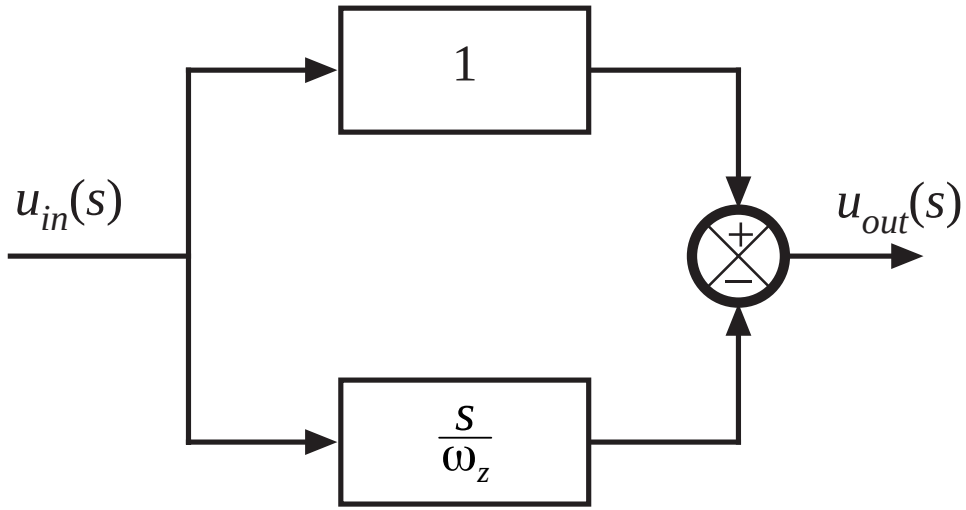
where the transfer functions are written in the standard forms

$$G_{vd}(s) = G_{d0}\,\frac{\left(1 - \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2\right)}$$

$$G_{vg}(s) = G_{g0}\,\frac{1}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2}$$

8.2.3. Physical origins of the right half-plane zero

$$G(s) = \left(1 - \frac{s}{\omega_0}\right)$$

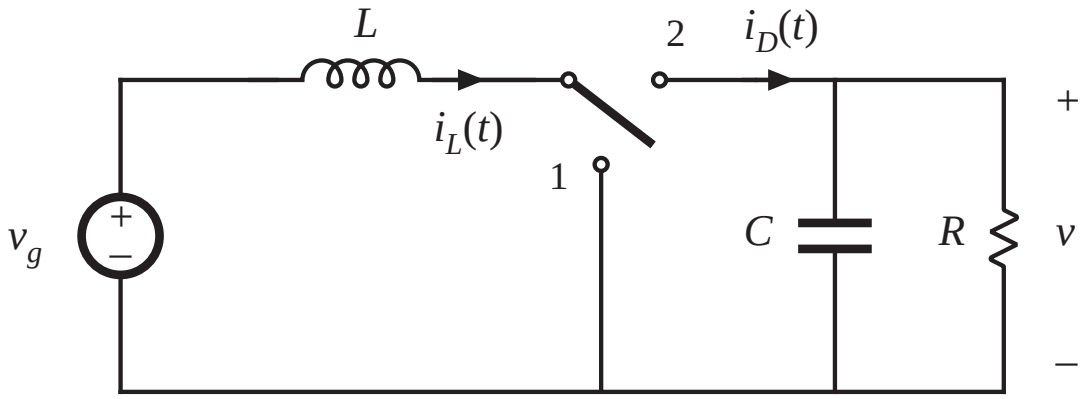


- *phase reversal at high frequency*
- *transient response: output initially tends in wrong direction*

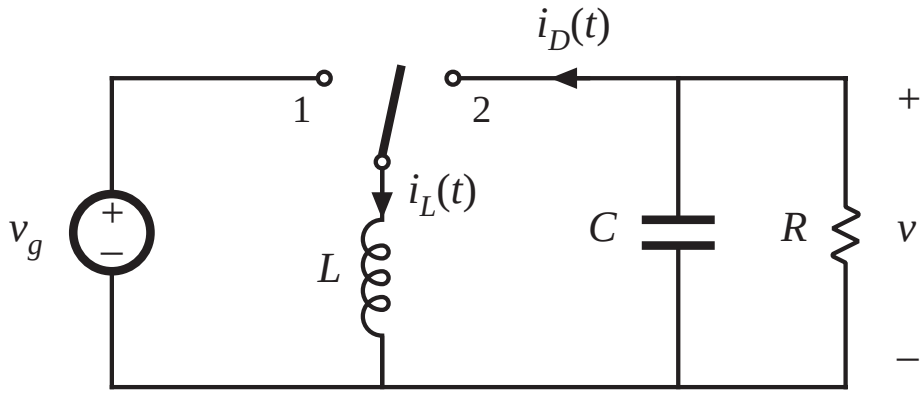
Two converters whose CCM control-to-output transfer functions exhibit RHP zeroes

$$\left\langle i_D \right\rangle_{T_s} = d' \left\langle i_L \right\rangle_{T_s}$$

Boost



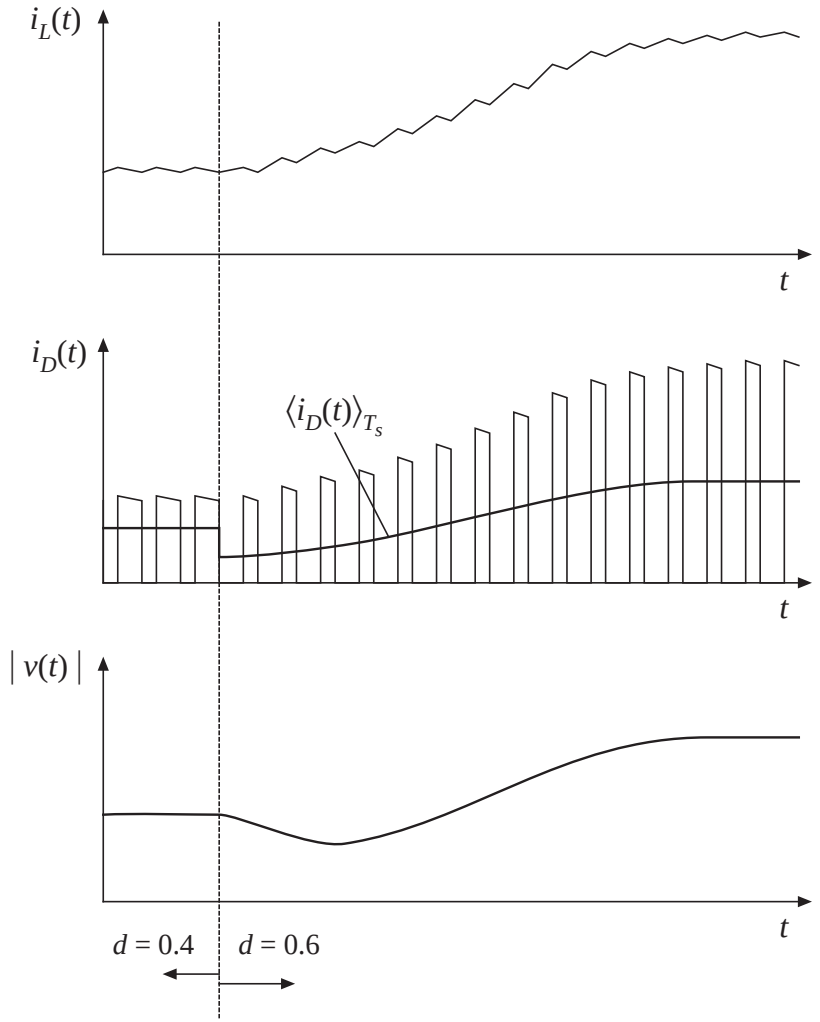
Buck-boost



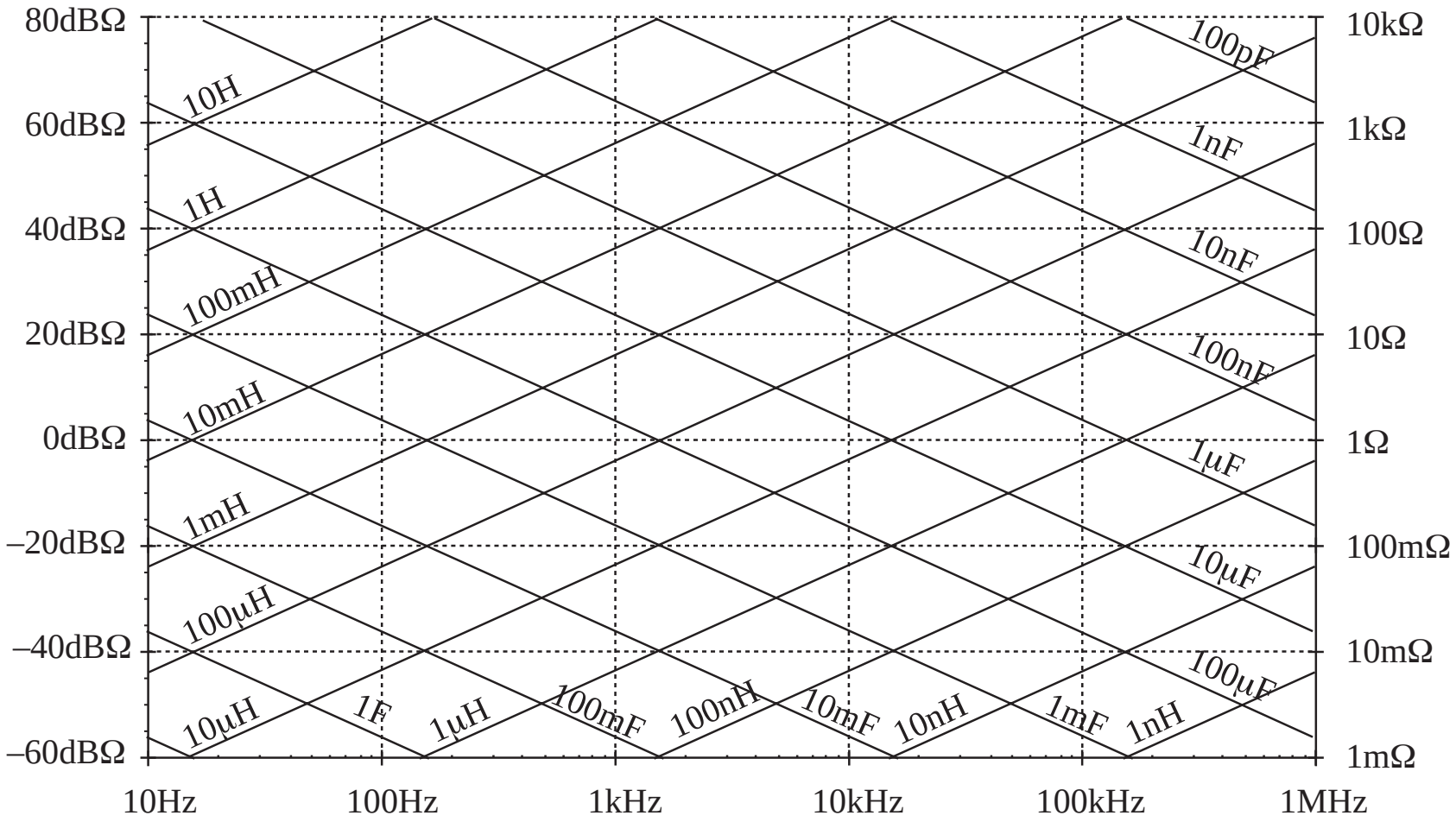
Waveforms, step increase in duty cycle

$$\left\langle i_D \right\rangle_{T_s} = d' \left\langle i_L \right\rangle_{T_s}$$

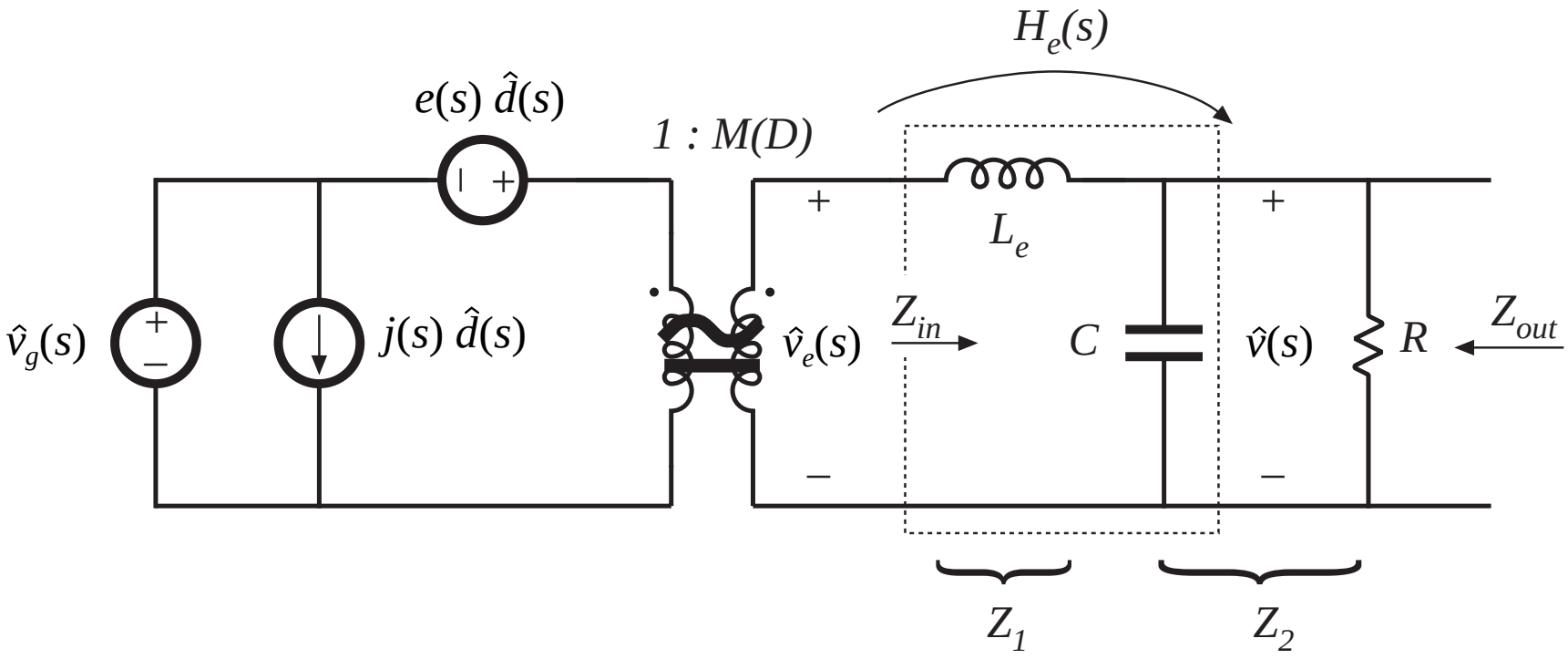
- Increasing $d(t)$ causes the average diode current to initially decrease
- As inductor current increases to its new equilibrium value, average diode current eventually increases



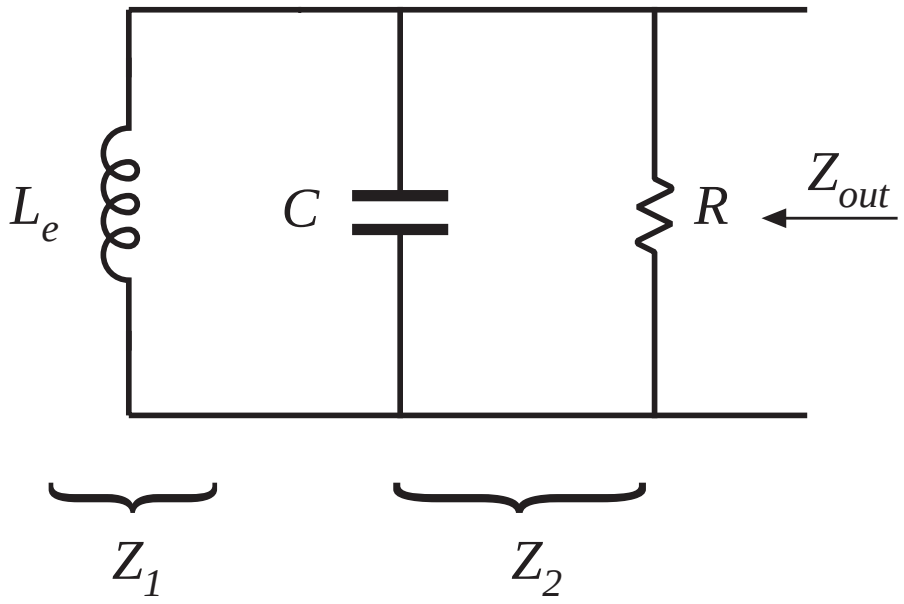
Impedance graph paper



Transfer functions predicted by canonical model

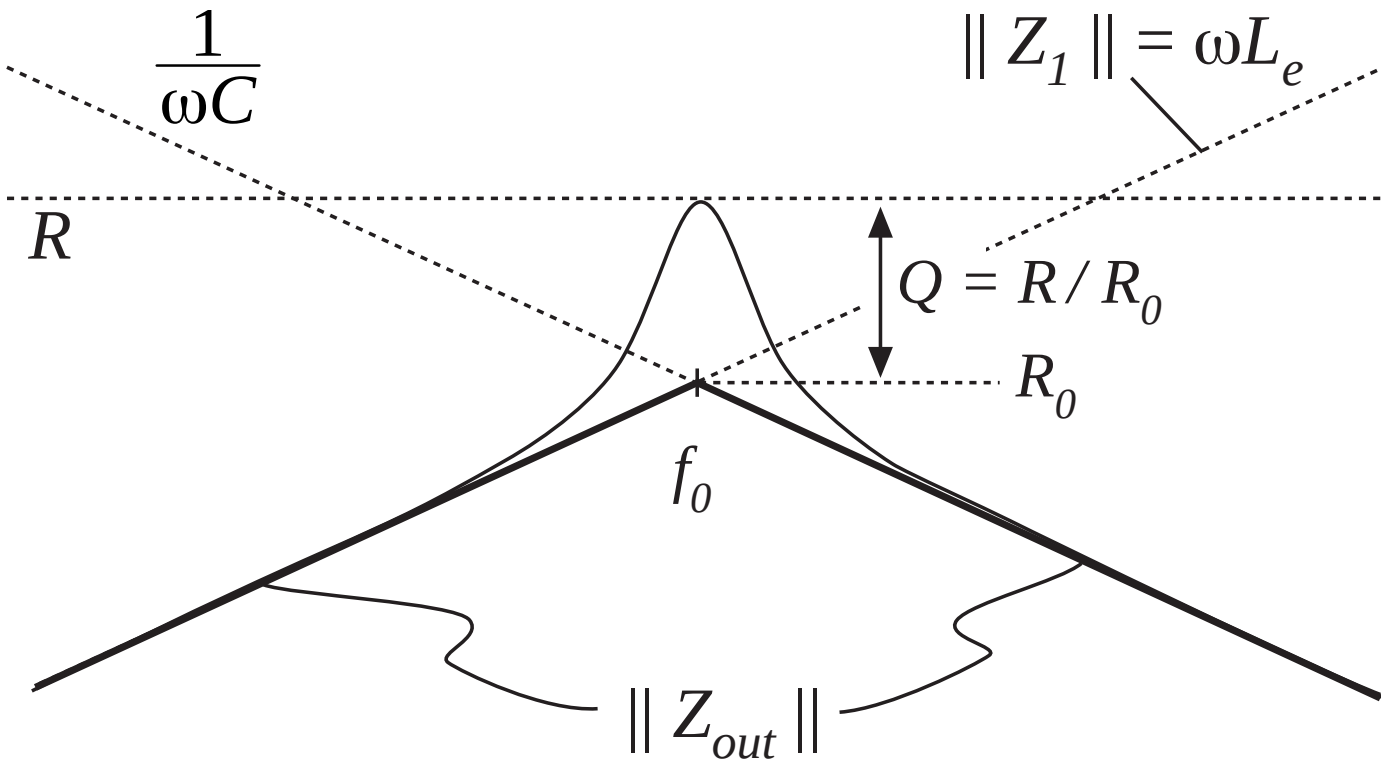


Output impedance Z_{out}: set sources to zero

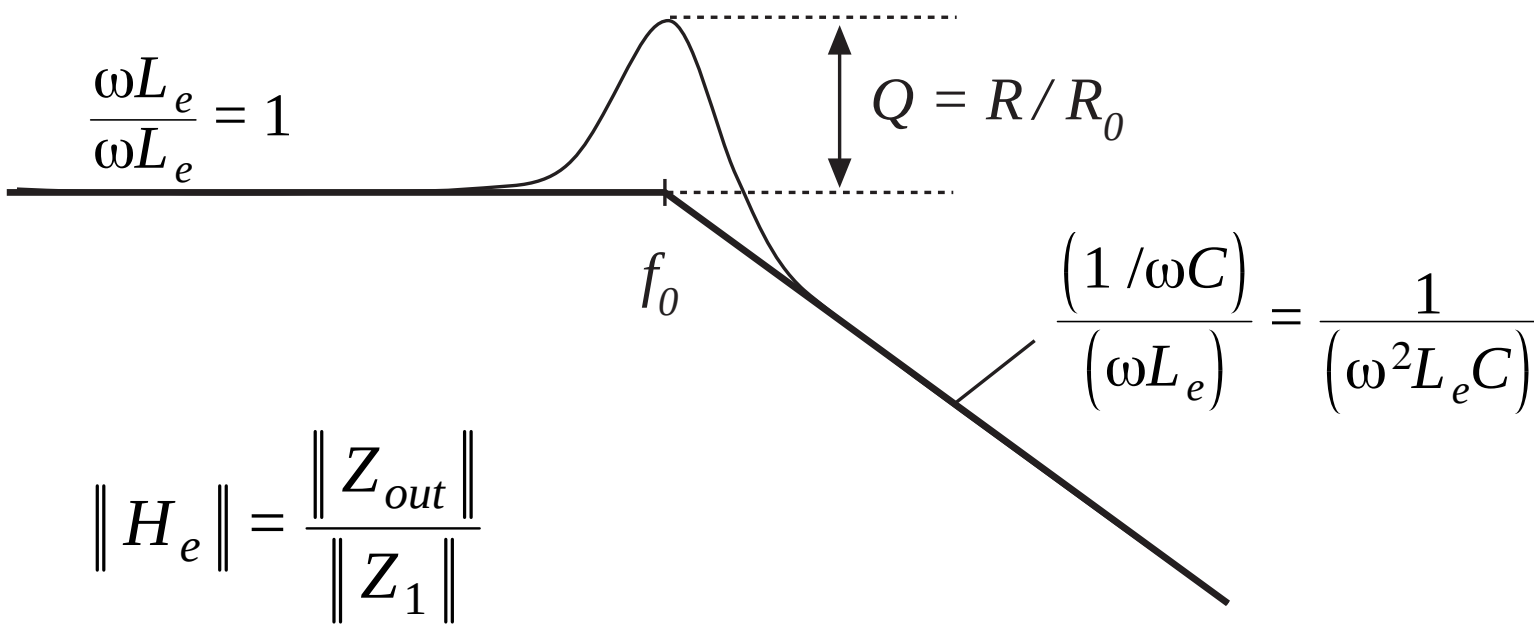


$$Z_{out} = Z_1 \parallel Z_2$$

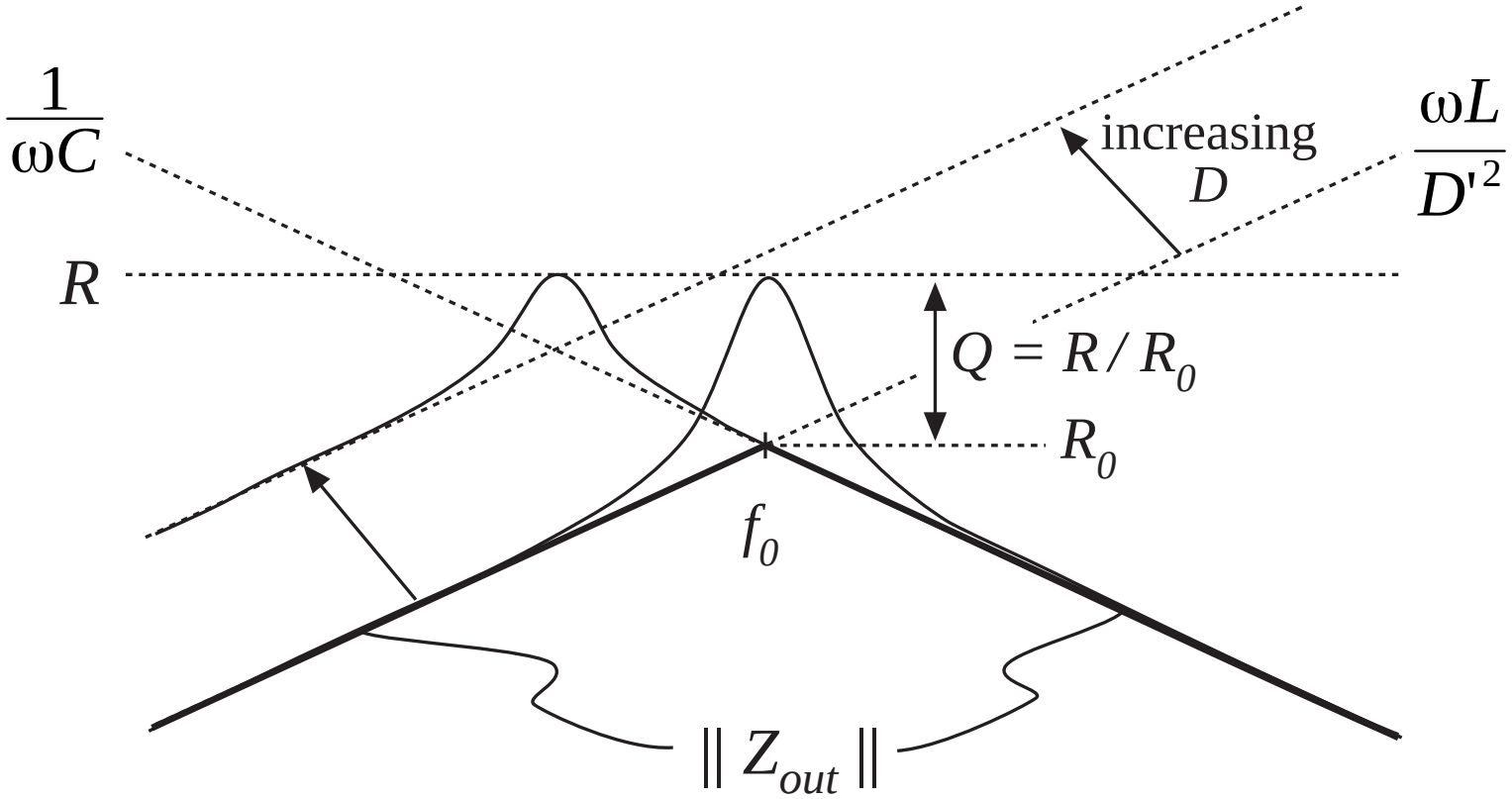
Graphical construction of output impedance



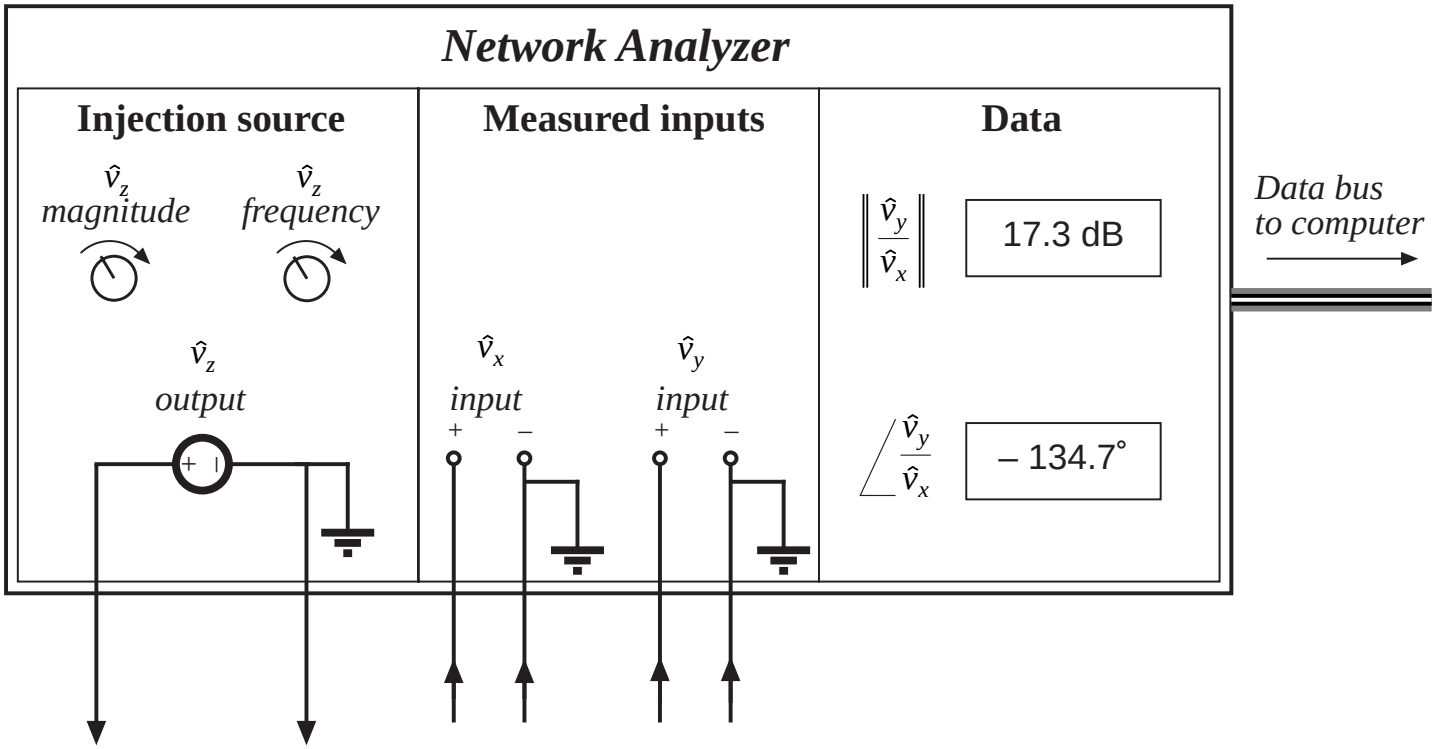
Graphical construction of filter effective transfer function



Boost and buck-boost converters: $L_e = L / D'^2$



8.4. Measurement of ac transfer functions and impedances



Swept sinusoidal measurements

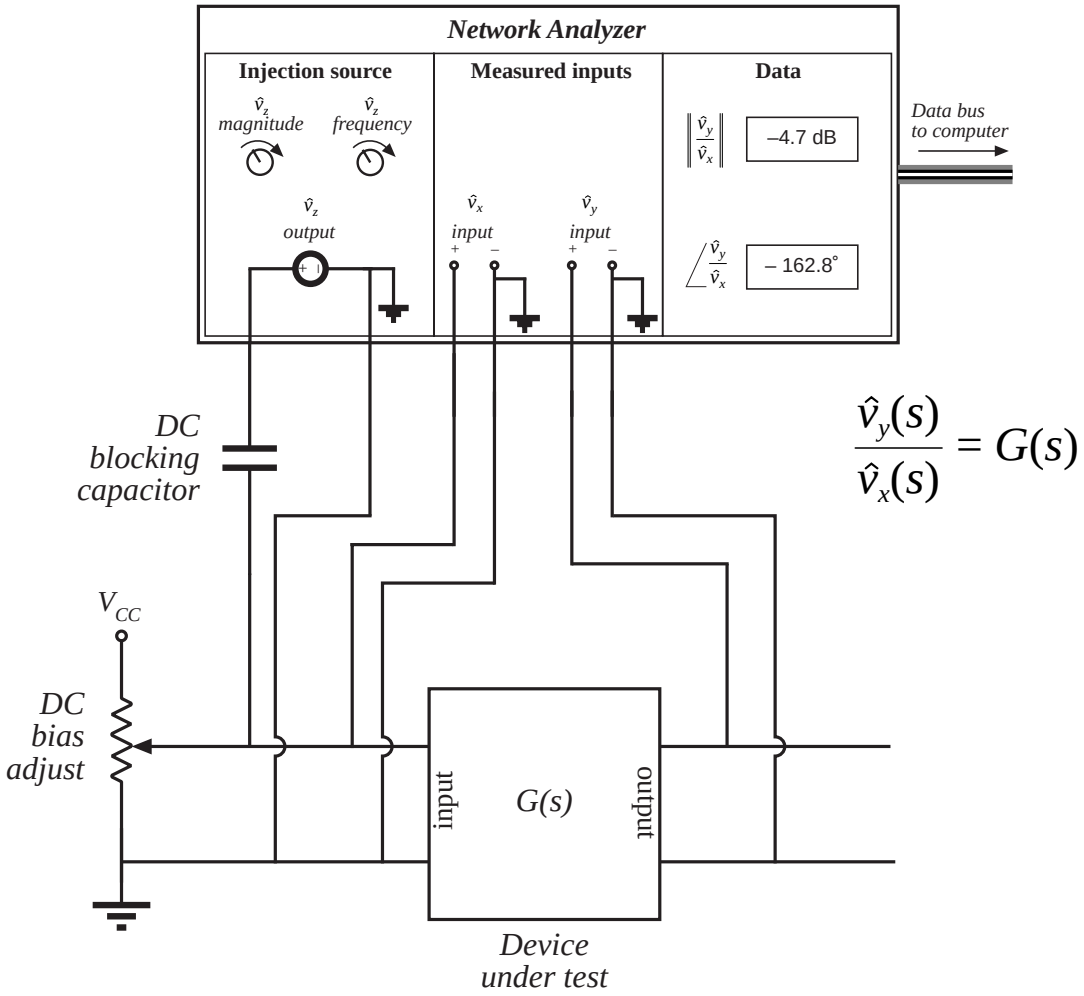
- Injection source produces sinusoid $\hat{v}_z$ of controllable amplitude and frequency
- Signal inputs $\hat{v}_x$ and $\hat{v}_y$ perform function of narrowband tracking voltmeter:

  Component of input at injection source frequency is measured

  Narrowband function is essential: switching harmonics and other noise components are removed
- Network analyzer measures

$$\left\| \frac{\hat{v}_y}{\hat{v}_x} \right\| \quad \text{and} \quad \angle \frac{\hat{v}_y}{\hat{v}_x}$$

Measurement of an ac transfer function

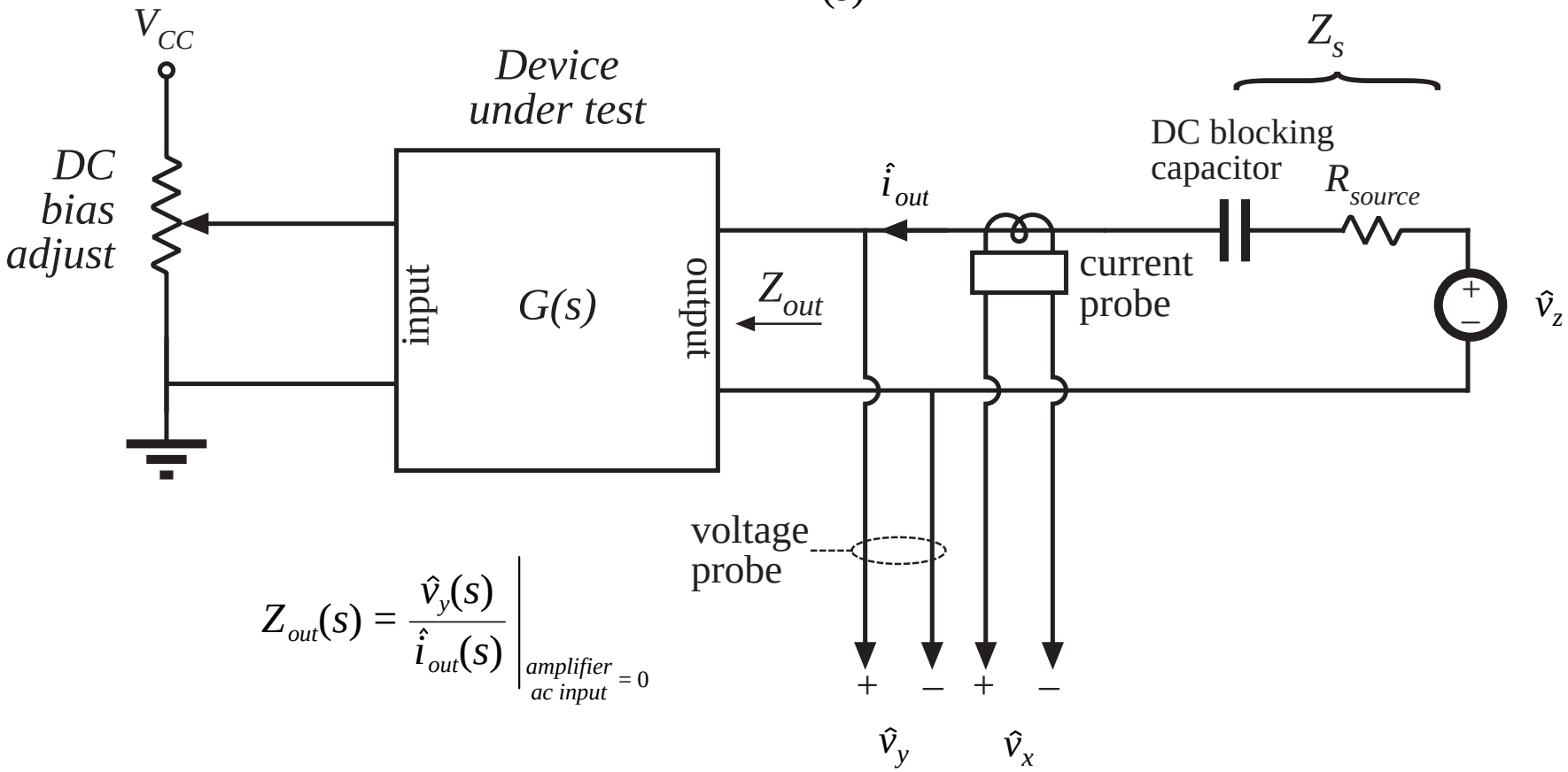


$$\frac{\hat{v}_y(s)}{\hat{v}_x(s)} = G(s)$$

- Potentiometer establishes correct quiescent operating point
- Injection sinusoid coupled to device input via dc blocking capacitor
- Actual device input and output voltages are measured as $\hat{v}_x$ and $\hat{v}_y$
- Dynamics of blocking capacitor are irrelevant

Measurement of an output impedance

$$Z(s) = \frac{\hat{v}(s)}{\hat{i}(s)}$$



$$Z_{out}(s) = \left.\frac{\hat{v}_y(s)}{\hat{i}_{out}(s)}\right|_{\substack{amplifier\\ ac\ input}=0}$$

Measurement of output impedance

- Treat output impedance as transfer function from output current to output voltage:

$$Z(s) = \frac{\hat{v}(s)}{\hat{i}(s)} \qquad Z_{out}(s) = \left. \frac{\hat{v}_y(s)}{\hat{i}_{out}(s)} \right|_{\substack{amplifier \\ ac\ input}} = 0$$

- Potentiometer at device input port establishes correct quiescent operating point
- Current probe produces voltage proportional to current; this voltage is connected to network analyzer channel $\hat{v}_x$
- Network analyzer result must be multiplied by appropriate factor, to account for scale factors of current and voltage probes

Measurement of small impedances

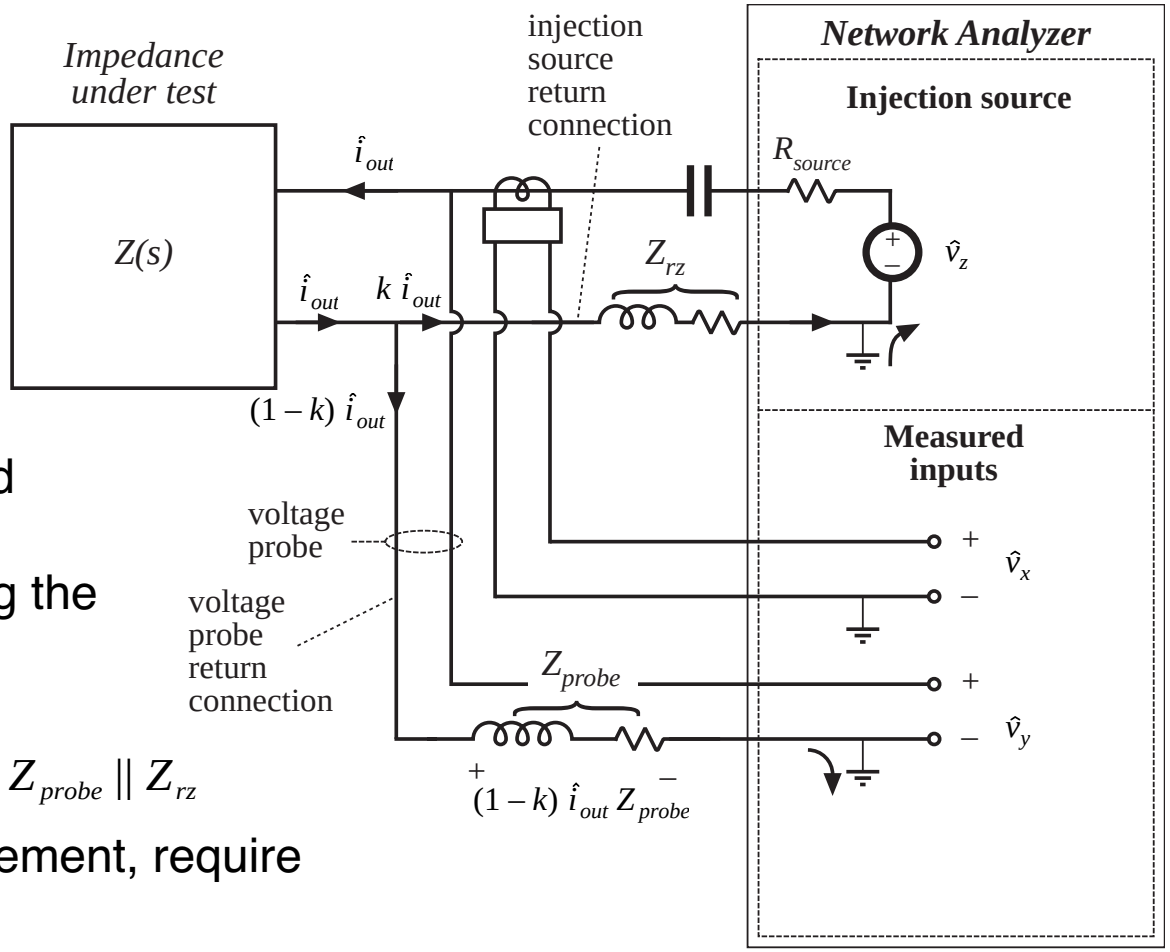
Grounding problems cause measurement to fail:

Injection current can return to analyzer via two paths. Injection current which returns via voltage probe ground induces voltage drop in voltage probe, corrupting the measurement. Network analyzer measures

$$Z + (1 - k)\, Z_{probe} = Z + Z_{probe} \parallel Z_{rz}$$

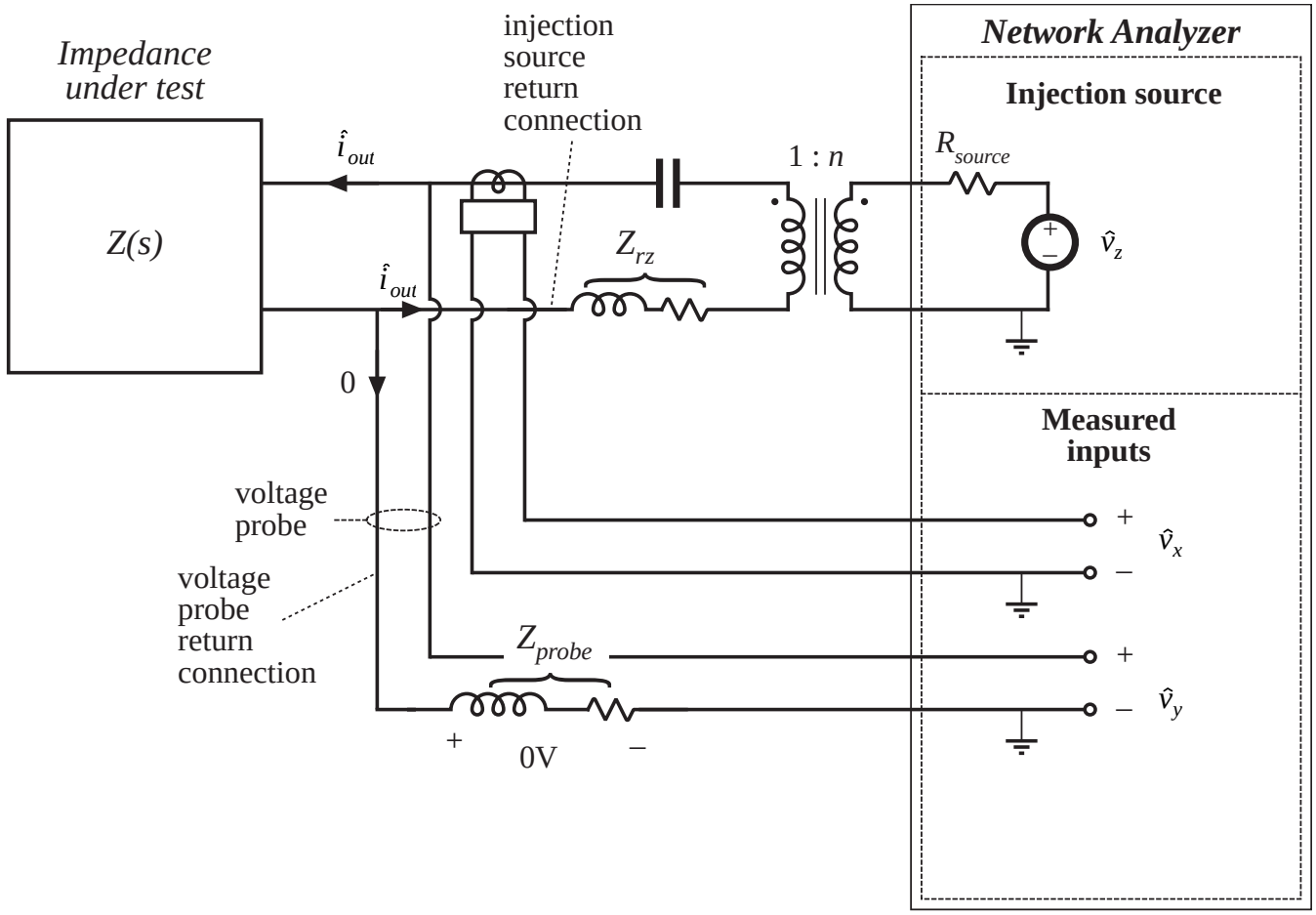
For an accurate measurement, require

$$\| Z \| >> \left\| \left(Z_{probe} \parallel Z_{rz} \right) \right\|$$



Improved measurement: add isolation transformer

Injection current must now return entirely through transformer. No additional voltage is induced in voltage probe ground connection



8.5. Summary of key points

1. The magnitude Bode diagrams of functions which vary as $(f / f_0)n$ have slopes equal to $20n$ dB per decade, and pass through 0dB at $f = f_0$.
2. It is good practice to express transfer functions in normalized pole-zero form; this form directly exposes expressions for the salient features of the response, i.e., the corner frequencies, reference gain, etc.
3. The right half-plane zero exhibits the magnitude response of the left half-plane zero, but the phase response of the pole.
4. Poles and zeroes can be expressed in frequency-inverted form, when it is desirable to refer the gain to a high-frequency asymptote.

Summary of key points

5. A two-pole response can be written in the standard normalized form of Eq. (8-53). When $Q > 0.5$, the poles are complex conjugates. The magnitude response then exhibits peaking in the vicinity of the corner frequency, with an exact value of Q at $f = f_0$. High Q also causes the phase to change sharply near the corner frequency.

6. When the Q is less than 0.5, the two pole response can be plotted as two real poles. The low- Q approximation predicts that the two poles occur at frequencies f_0 / Q and Qf_0. These frequencies are within 10% of the exact values for $Q \leq 0.3$.

7. The low- Q approximation can be extended to find approximate roots of an arbitrary degree polynomial. Approximate analytical expressions for the salient features can be derived. Numerical values are used to justify the approximations.

Summary of key points

8. Salient features of the transfer functions of the buck, boost, and buck-boost converters are tabulated in section 8.2.2. The line-to-output transfer functions of these converters contain two poles. Their control-to-output transfer functions contain two poles, and may additionally contain a right half-pland zero.

9. Approximate magnitude asymptotes of impedances and transfer functions can be easily derived by graphical construction. This approach is a useful supplement to conventional analysis, because it yields physical insight into the circuit behavior, and because it exposes suitable approximations. Several examples, including the impedances of basic series and parallel resonant circuits and the transfer function $H_e(s)$ of the boost and buck-boost converters, are worked in section 8.3.

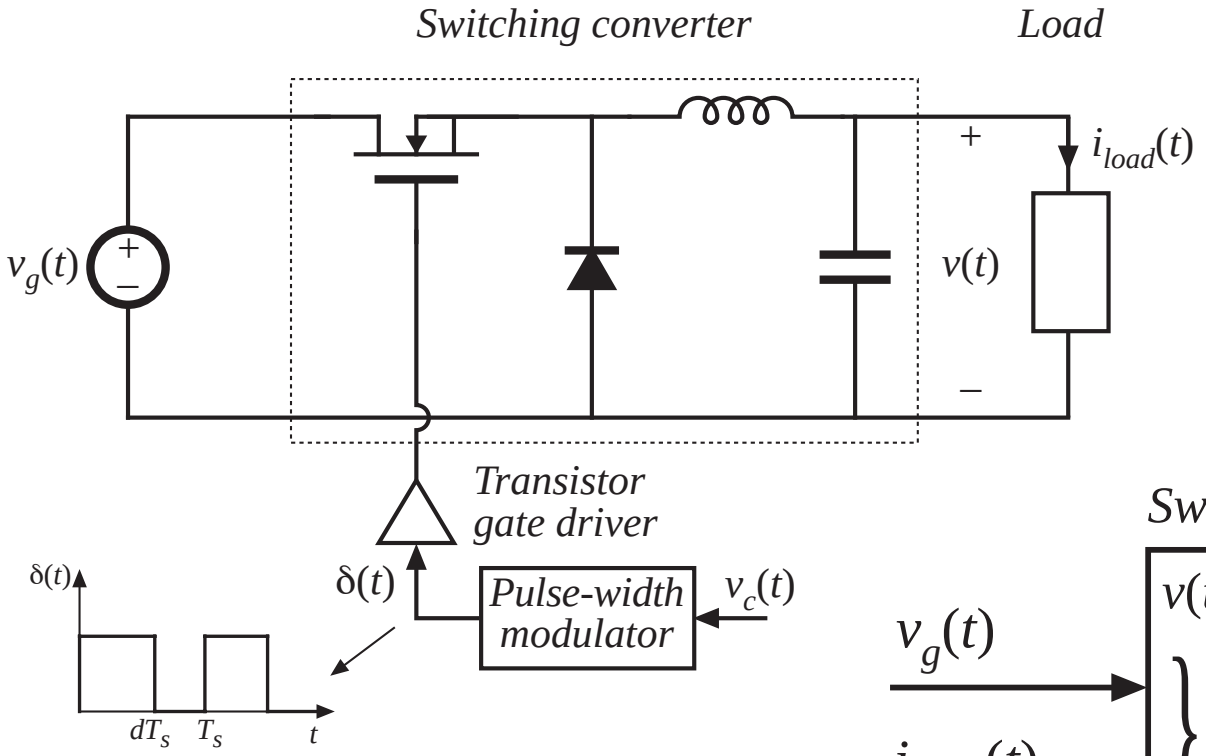
10. Measurement of transfer functions and impedances using a network analyzer is discussed in section 8.4. Careful attention to ground connections is important when measuring small impedances.

Chapter 9. Controller Design

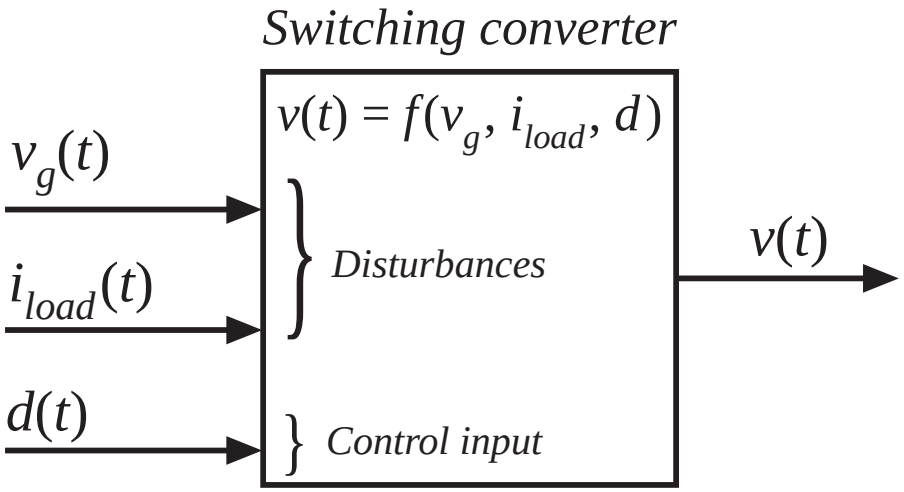
Controller design

Controller design

9.1. Introduction



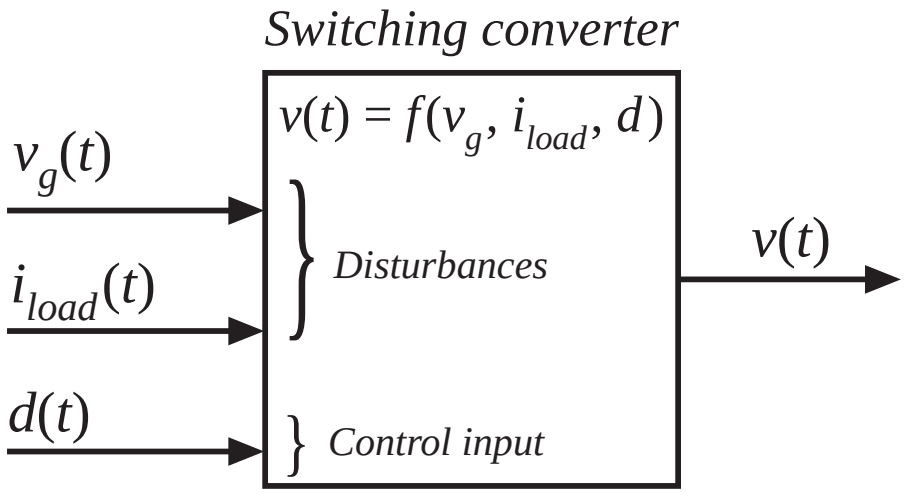
Output voltage of a switching converter depends on duty cycle d, input voltage v_g, and load current i_{load}.



The dc regulator application

Objective: maintain constant output voltage $v(t) = V$, in spite of disturbances in $v_g(t)$ and $i_{load}(t)$.

Typical variation in $v_g(t)$: 100Hz or 120Hz ripple, produced by rectifier circuit.



Load current variations: a significant step-change in load current, such as from 50% to 100% of rated value, may be applied.

A typical output voltage regulation specification: $5\text{V} \pm 0.1\text{V}$.

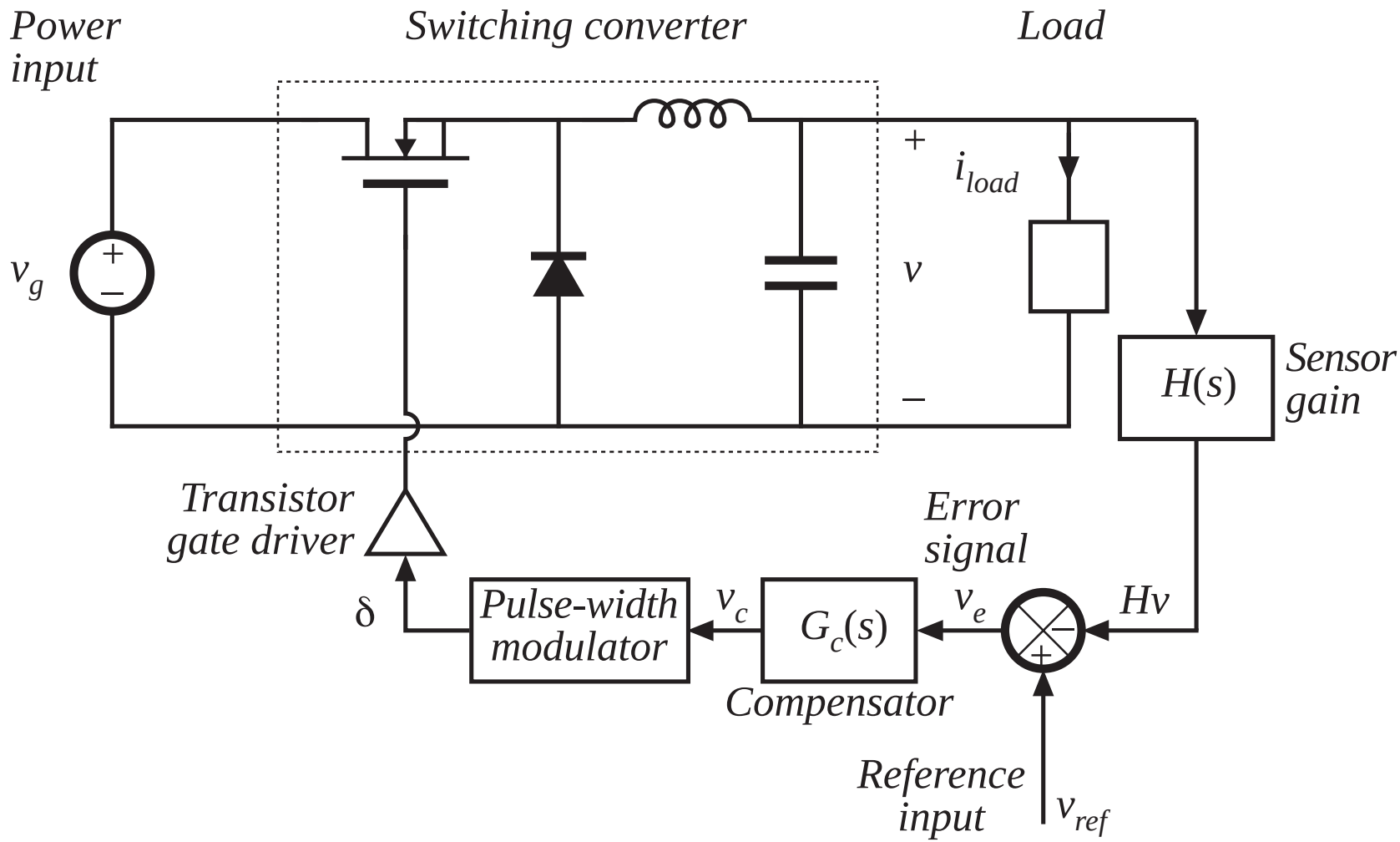
Circuit elements are constructed to some specified tolerance. In high volume manufacturing of converters, all output voltages must meet specifications.

The dc regulator application

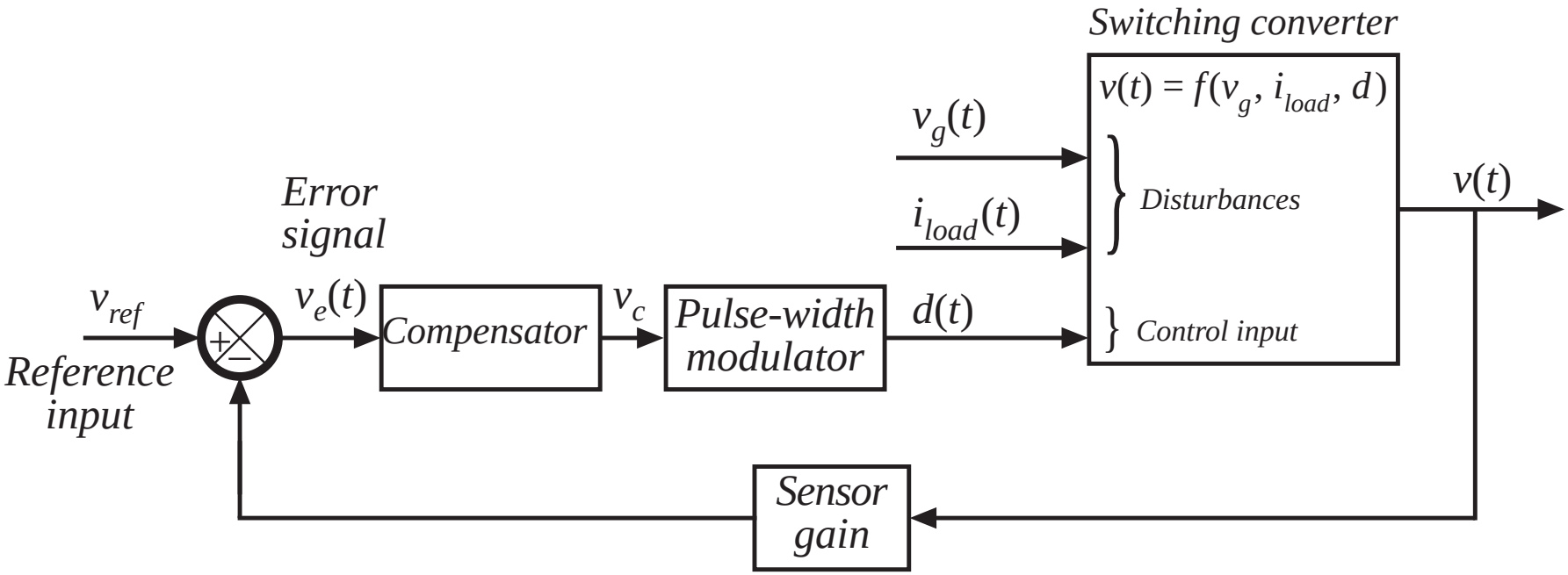
So we cannot expect to set the duty cycle to a single value, and obtain a given constant output voltage under all conditions.

Negative feedback: build a circuit that automatically adjusts the duty cycle as necessary, to obtain the specified output voltage with high accuracy, regardless of disturbances or component tolerances.

Negative feedback:
a switching regulator system

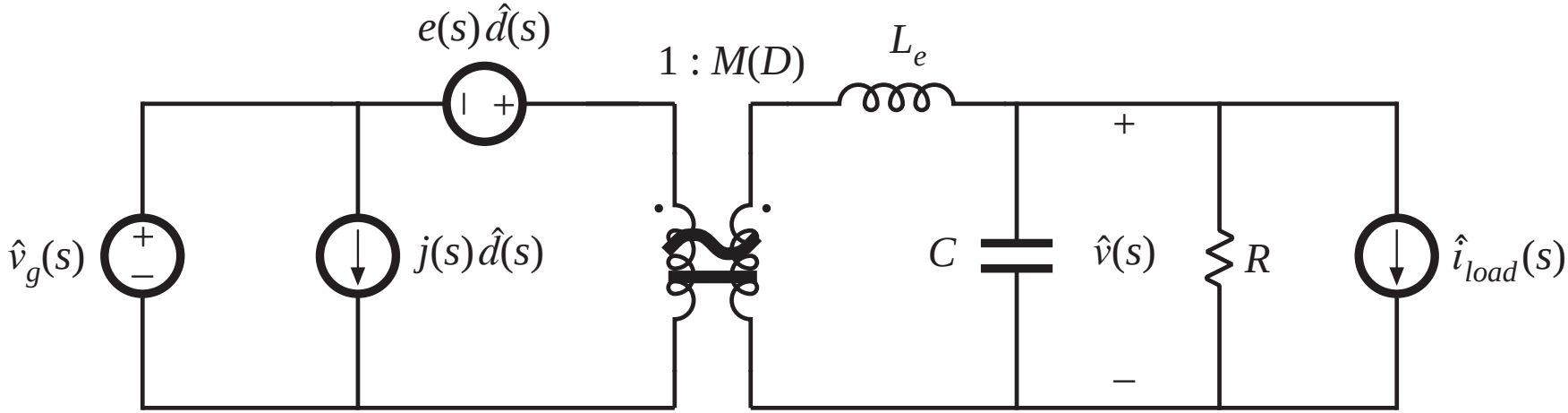


Negative feedback



9.2. Effect of negative feedback on the network transfer functions

Small signal model: open-loop converter



Output voltage can be expressed as

$$\hat{v}(s) = G_{vd}(s)\,\hat{d}(s) + G_{vg}(s)\,\hat{v}_g(s) - Z_{out}(s)\,\hat{i}_{load}(s)$$

where

$$G_{vd}(s) = \left.\frac{\hat{v}(s)}{\hat{d}(s)}\right|_{\substack{\hat{v}_g = 0 \\ \hat{i}_{load} = 0}} \qquad G_{vg}(s) = \left.\frac{\hat{v}(s)}{\hat{v}_g(s)}\right|_{\substack{\hat{d} = 0 \\ \hat{i}_{load} = 0}} \qquad Z_{out}(s) = -\left.\frac{\hat{v}(s)}{\hat{i}_{load}(s)}\right|_{\substack{\hat{d} = 0 \\ \hat{v}_g = 0}}$$

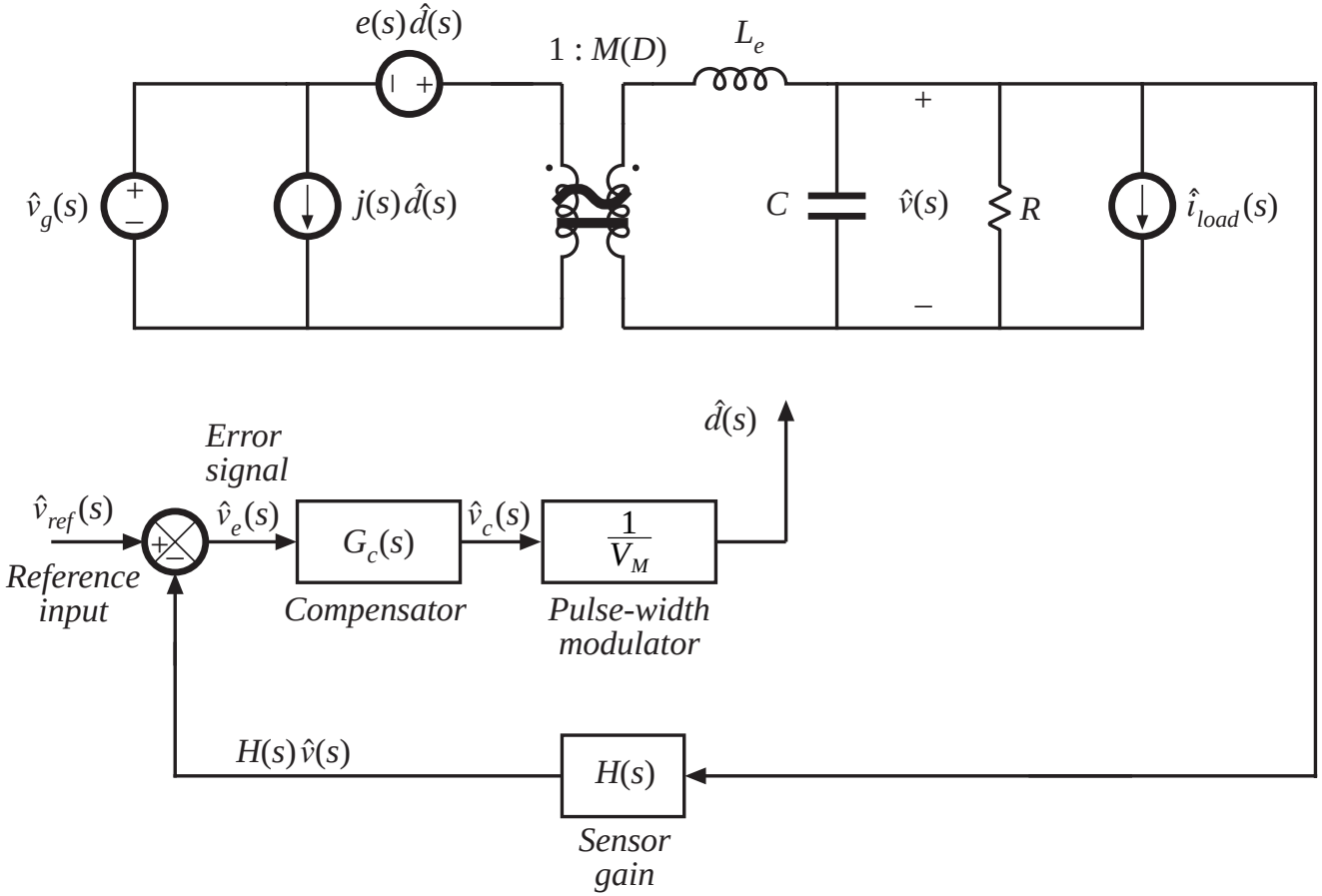
Voltage regulator system small-signal model

- *Use small-signal converter model*
- *Perturb and linearize remainder of feedback loop:*

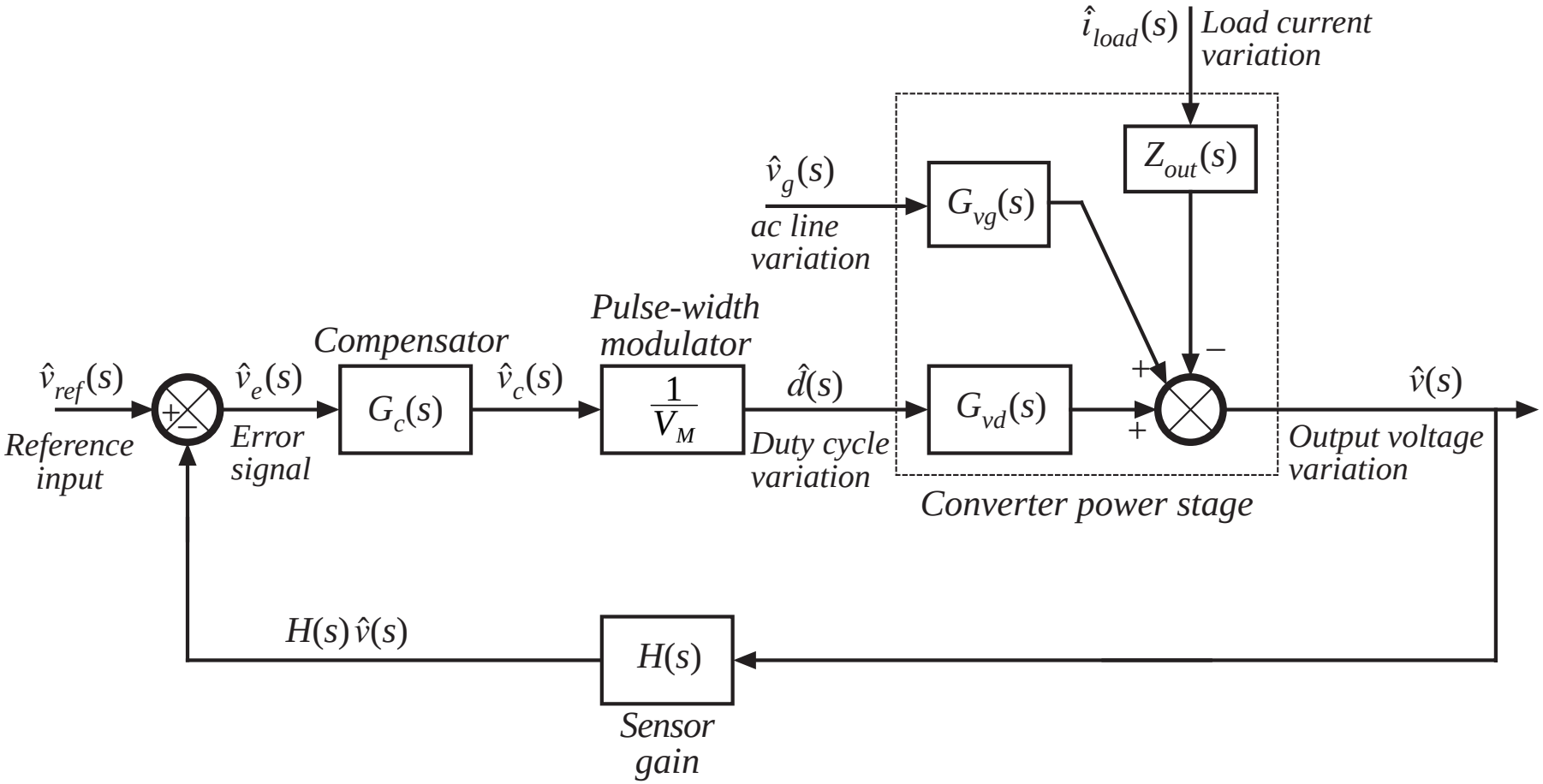
$$v_{ref}(t) = V_{ref} + \hat{v}_{ref}(t)$$

$$v_e(t) = V_e + \hat{v}_e(t)$$

etc.



Regulator system small-signal block diagram



Solution of block diagram

Manipulate block diagram to solve for $\hat{v}(s)$. Result is

$$\hat{v} = \hat{v}_{ref} \frac{G_c G_{vd} / V_M}{1 + H G_c G_{vd} / V_M} + \hat{v}_g \frac{G_{vg}}{1 + H G_c G_{vd} / V_M} - \hat{i}_{load} \frac{Z_{out}}{1 + H G_c G_{vd} / V_M}$$

which is of the form

$$\hat{v} = \hat{v}_{ref} \frac{1}{H} \frac{T}{1 + T} + \hat{v}_g \frac{G_{vg}}{1 + T} - \hat{i}_{load} \frac{Z_{out}}{1 + T}$$

$$with \quad T(s) = H(s)\, G_c(s)\, G_{vd}(s) / V_M \quad = "loop\ gain"$$

Loop gain $T(s)$ = products of the gains around the negative feedback loop.

9.2.1. Feedback reduces the transfer functions from disturbances to the output

Original (open-loop) line-to-output transfer function:

$$G_{vg}(s) = \left. \frac{\hat{v}(s)}{\hat{v}_g(s)} \right|_{\substack{\hat{d} = 0 \\ \hat{i}_{load} = 0}}$$

With addition of negative feedback, the line-to-output transfer function becomes:

$$\left. \frac{\hat{v}(s)}{\hat{v}_g(s)} \right|_{\substack{\hat{v}_{ref} = 0 \\ \hat{i}_{load} = 0}} = \frac{G_{vg}(s)}{1 + T(s)}$$

Feedback reduces the line-to-output transfer function by a factor of

$$\frac{1}{1 + T(s)}$$

If $T(s)$ is large in magnitude, then the line-to-output transfer function becomes small.

Closed-loop output impedance

Original (open-loop) output impedance:

$$Z_{out}(s) = - \left. \frac{\hat{v}(s)}{\hat{i}_{load}(s)} \right|_{\substack{\hat{d} = 0 \\ \hat{v}_g = 0}}$$

With addition of negative feedback, the output impedance becomes:

$$\left. \frac{\hat{v}(s)}{- \hat{i}_{load}(s)} \right|_{\substack{\hat{v}_{ref} = 0 \\ \hat{v}_g = 0}} = \frac{Z_{out}(s)}{1 + T(s)}$$

Feedback reduces the output impedance by a factor of

$$\frac{1}{1 + T(s)}$$

If $T(s)$ is large in magnitude, then the output impedance is greatly reduced in magnitude.

9.2.2. Feedback causes the transfer function from the reference input to the output to be insensitive to variations in the gains in the forward path of the loop

Closed-loop transfer function from $\hat{v}_{ref}$ to $\hat{v}(s)$ is:

$$\left.\frac{\hat{v}(s)}{\hat{v}_{ref}(s)}\right|_{\substack{\hat{v}_g = 0 \\ \hat{i}_{load} = 0}} = \frac{1}{H(s)} \frac{T(s)}{1 + T(s)}$$

If the loop gain is large in magnitude, i.e., $\| T \| >> 1$, then $(1+T) \approx T$ and $T/(1+T) \approx T/T = 1$. The transfer function then becomes

$$\frac{\hat{v}(s)}{\hat{v}_{ref}(s)} \approx \frac{1}{H(s)}$$

which is independent of the gains in the forward path of the loop.

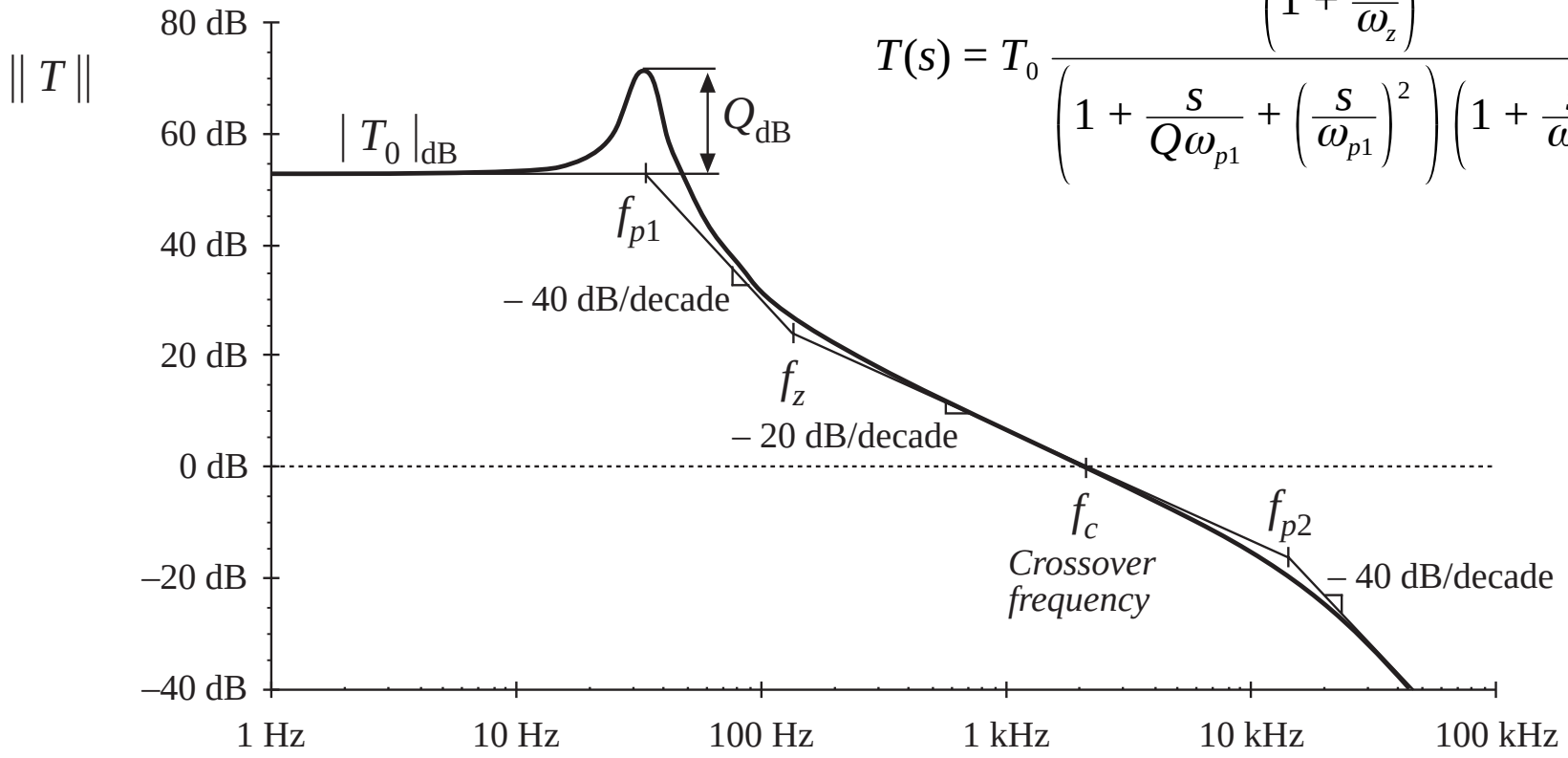
This result applies equally well to dc values:

$$\frac{V}{V_{ref}} = \frac{1}{H(0)} \frac{T(0)}{1 + T(0)} \approx \frac{1}{H(0)}$$

9.3. Construction of the important quantities $1/(1+T)$ and $T/(1+T)$

Example

$$T(s) = T_0 \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{Q\omega_{p1}} + \left(\frac{s}{\omega_{p1}}\right)^2\right)\left(1 + \frac{s}{\omega_{p2}}\right)}$$



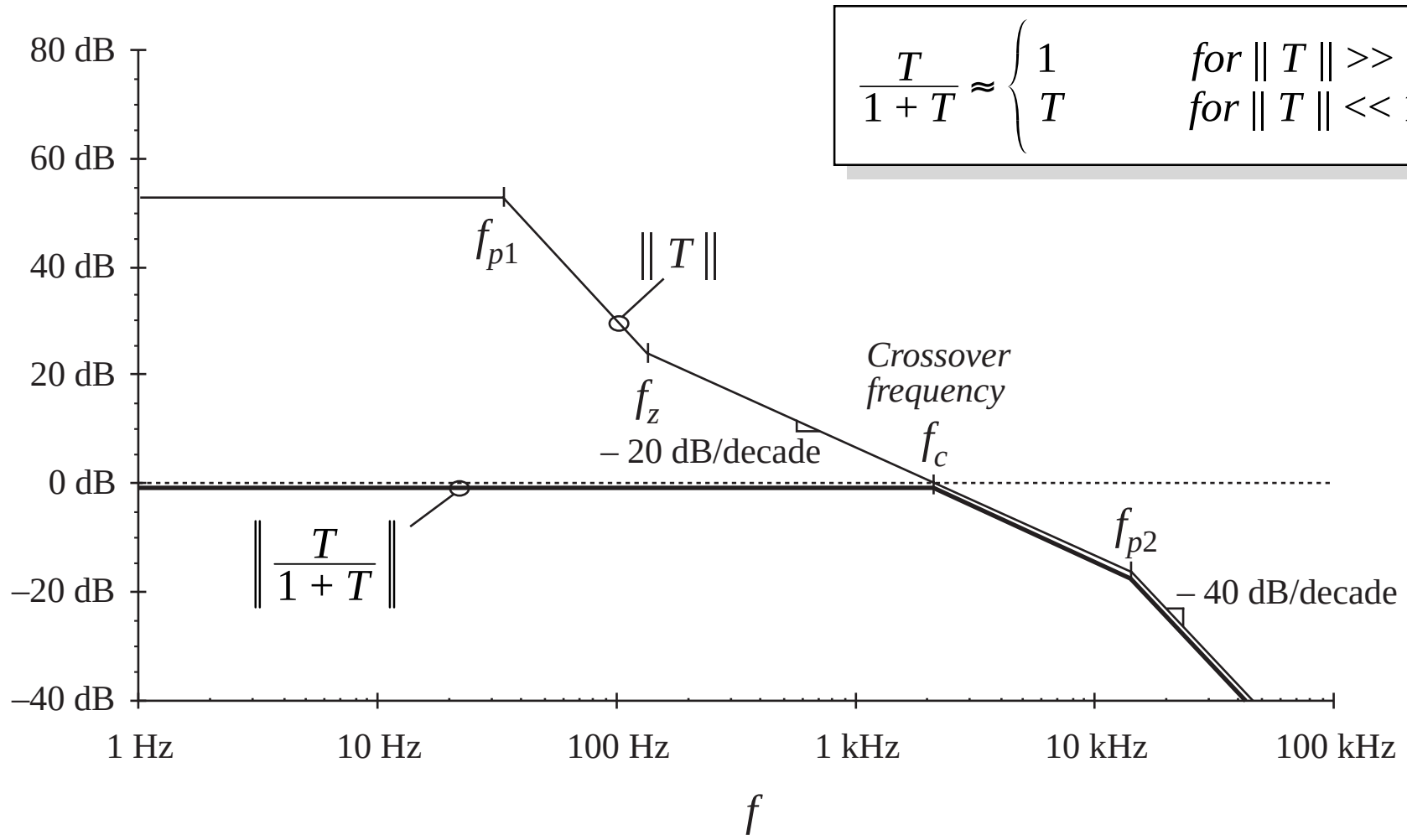
At the crossover frequency f_c, $\| T \| = 1$

Approximating $1/(1+T)$ and $T/(1+T)$

$$\frac{T}{1+T} \approx \begin{cases} 1 & \text{for } \| T \| >> 1 \\ T & \text{for } \| T \| << 1 \end{cases}$$

$$\frac{1}{1+T(s)} \approx \begin{cases} \dfrac{1}{T(s)} & \text{for } \| T \| >> 1 \\ 1 & \text{for } \| T \| << 1 \end{cases}$$

Example: construction of $T/(1+T)$



Example: analytical expressions for approximate reference to output transfer function

At frequencies sufficiently less that the crossover frequency, the loop gain $T(s)$ has large magnitude. The transfer function from the reference to the output becomes

$$\frac{\hat{v}(s)}{\hat{v}_{ref}(s)} = \frac{1}{H(s)} \frac{T(s)}{1 + T(s)} \approx \frac{1}{H(s)}$$

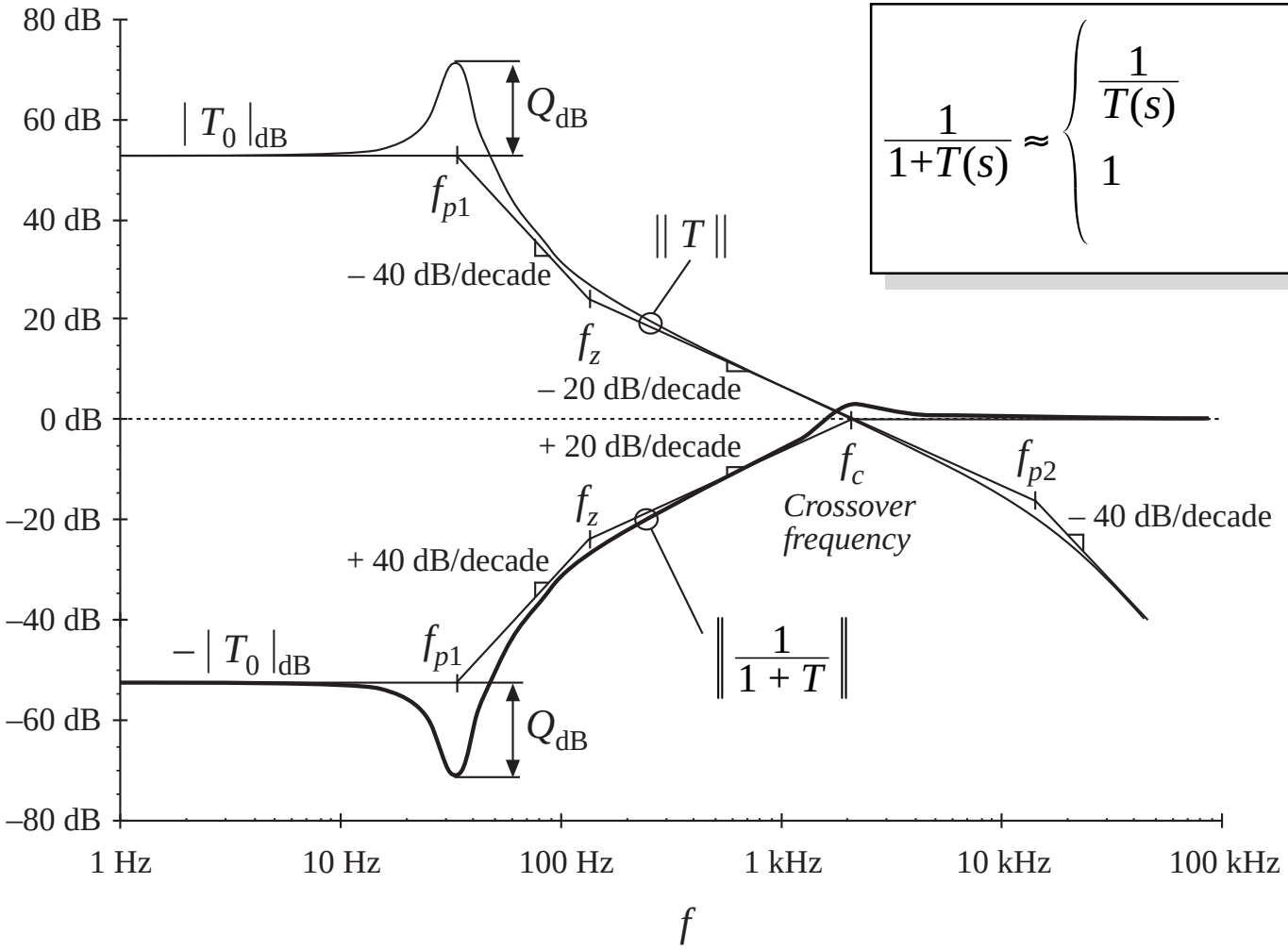
This is the desired behavior: the output follows the reference according to the ideal gain $1/H(s)$. The feedback loop works well at frequencies where the loop gain $T(s)$ has large magnitude.

At frequencies above the crossover frequency, $\| T \| < 1$. The quantity $T/(1+T)$ then has magnitude approximately equal to 1, and we obtain

$$\frac{\hat{v}(s)}{\hat{v}_{ref}(s)} = \frac{1}{H(s)} \frac{T(s)}{1 + T(s)} \approx \frac{T(s)}{H(s)} = \frac{G_c(s) G_{vd}(s)}{V_M}$$

This coincides with the open-loop transfer function from the reference to the output. At frequencies where $\| T \| < 1$, the loop has essentially no effect on the transfer function from the reference to the output.

Same example: construction of 1/(1+T)



$$\frac{1}{1+T(s)} \approx \begin{cases} \frac{1}{T(s)} & \text{for } \|T\| >> 1 \\ 1 & \text{for } \|T\| << 1 \end{cases}$$

Interpretation: how the loop rejects disturbances

Below the crossover frequency: $f < f_c$ and $\| T \| > 1$

Then $1/(1+T) \approx 1/T$, and disturbances are reduced in magnitude by $1/\| T \|$

Above the crossover frequency: $f > f_c$ and $\| T \| < 1$

Then $1/(1+T) \approx 1$, and the feedback loop has essentially no effect on disturbances

$$\frac{1}{1+T(s)} \approx \begin{cases} \frac{1}{T(s)} & \text{for } \| T \| >> 1 \\ 1 & \text{for } \| T \| << 1 \end{cases}$$

Terminology: open-loop vs. closed-loop

Original transfer functions, before introduction of feedback ("open-loop transfer functions"):

$$G_{vd}(s) \qquad G_{vg}(s) \qquad Z_{out}(s)$$

Upon introduction of feedback, these transfer functions become ("closed-loop transfer functions"):

$$\frac{1}{H(s)}\,\frac{T(s)}{1+T(s)} \qquad \frac{G_{vg}(s)}{1+T(s)} \qquad \frac{Z_{out}(s)}{1+T(s)}$$

The loop gain:

$$T(s)$$

9.4. Stability

Even though the original open-loop system is stable, the closed-loop transfer functions can be unstable and contain right half-plane poles. Even when the closed-loop system is stable, the transient response can exhibit undesirable ringing and overshoot, due to the high Q -factor of the closed-loop poles in the vicinity of the crossover frequency.

When feedback destabilizes the system, the denominator $(1+T(s))$ terms in the closed-loop transfer functions contain roots in the right half-plane (i.e., with positive real parts). If $T(s)$ is a rational fraction of the form $N(s) / D(s)$, where $N(s)$ and $D(s)$ are polynomials, then we can write

$$\frac{T(s)}{1+T(s)} = \frac{\frac{N(s)}{D(s)}}{1+\frac{N(s)}{D(s)}} = \frac{N(s)}{N(s)+D(s)}$$

$$\frac{1}{1+T(s)} = \frac{1}{1+\frac{N(s)}{D(s)}} = \frac{D(s)}{N(s)+D(s)}$$

- Could evaluate stability by evaluating $N(s) + D(s)$, then factoring to evaluate roots. This is a lot of work, and is not very illuminating.

Determination of stability directly from $T(s)$

- Nyquist stability theorem: general result.
- A special case of the Nyquist stability theorem: the phase margin test

  Allows determination of closed-loop stability (i.e., whether $1/(1+T(s))$ contains RHP poles) directly from the magnitude and phase of $T(s)$.

  A good design tool: yields insight into how $T(s)$ should be shaped, to obtain good performance in transfer functions containing $1/(1+T(s))$ terms.

9.4.1. The phase margin test

A test on $T(s)$, to determine whether $1/(1+T(s))$ contains RHP poles.

The crossover frequency f_c is defined as the frequency where

$$\| T(j2\pi f_c) \| = 1 \Rightarrow 0\text{dB}$$

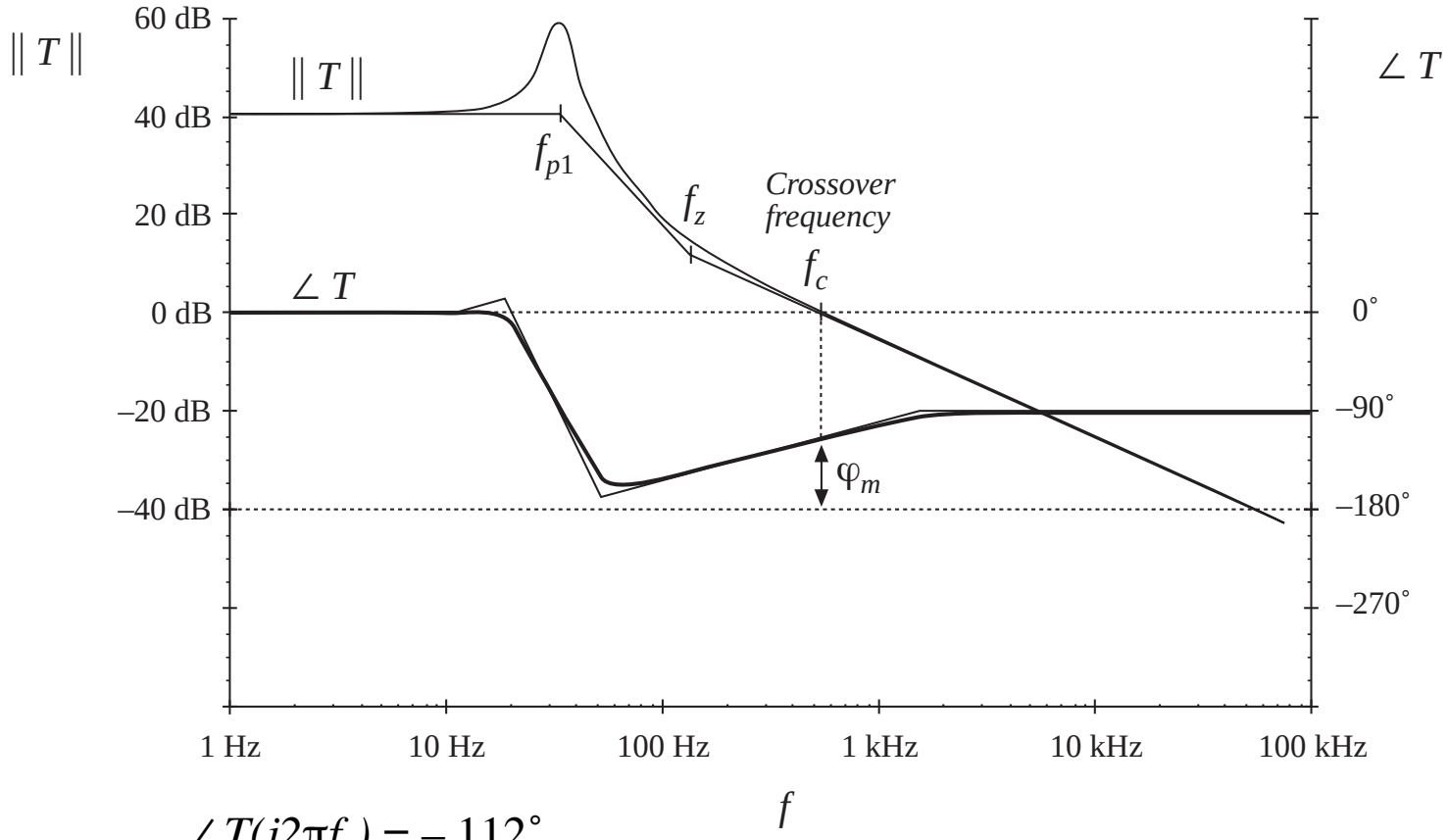
The phase margin φ_m is determined from the phase of $T(s)$ at f_c , as follows:

$$\varphi_m = 180^\circ + \angle T(j2\pi f_c)$$

If there is exactly one crossover frequency, and if $T(s)$ contains no RHP poles, then

the quantities $T(s)/(1+T(s))$ and $1/(1+T(s))$ contain no RHP poles whenever the phase margin φ_m is positive.

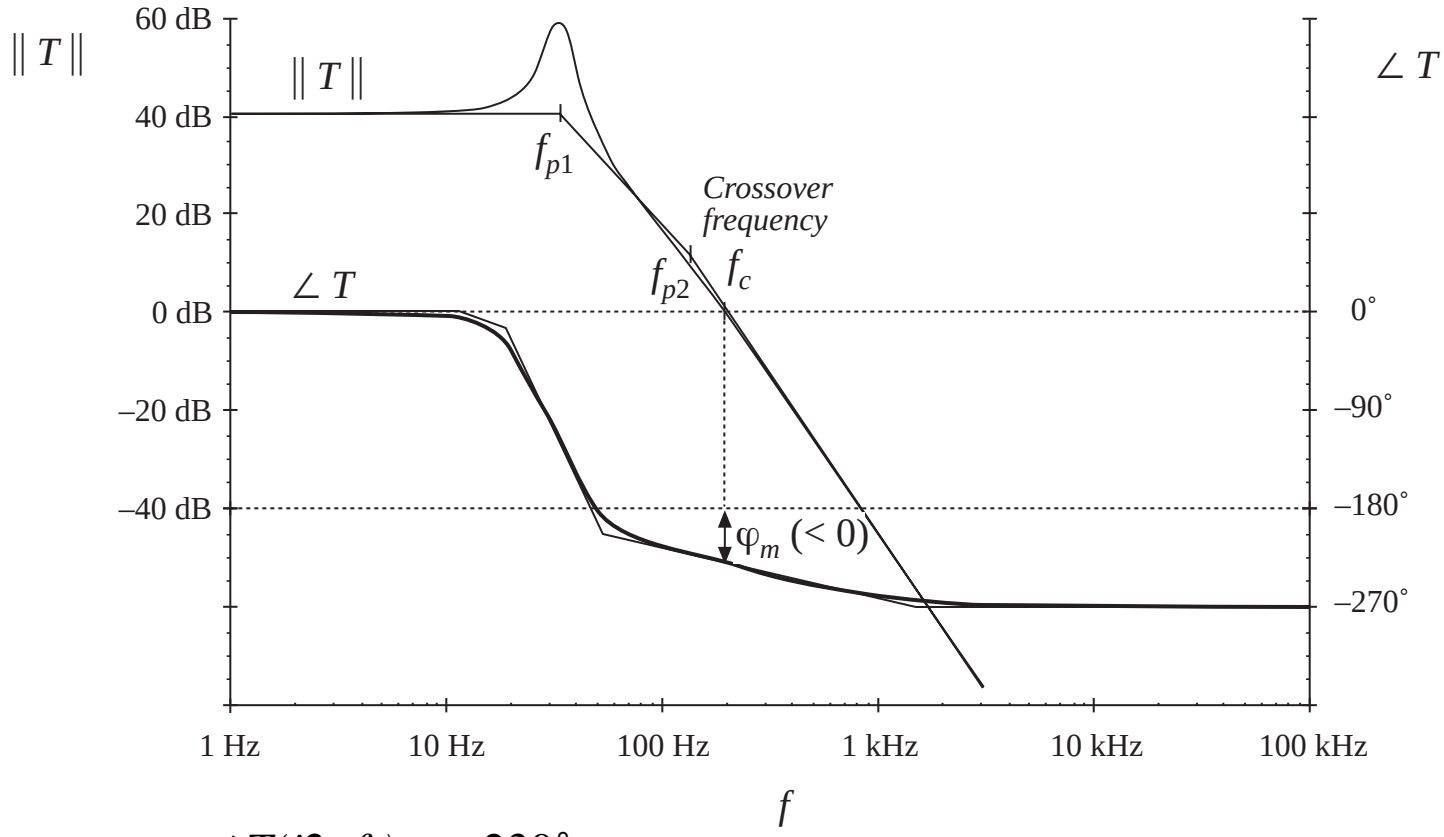
Example: a loop gain leading to a stable closed-loop system



$$\angle T(j2\pi f_c) = -112^\circ$$

$$\varphi_m = 180^\circ - 112^\circ = +68^\circ$$

Example: a loop gain leading to an unstable closed-loop system



$$\angle T(j2\pi f_c) = -230^\circ$$

$$\varphi_m = 180^\circ - 230^\circ = -50^\circ$$

9.4.2. The relation between phase margin and closed-loop damping factor

How much phase margin is required?

A small positive phase margin leads to a stable closed-loop system having complex poles near the crossover frequency with high Q. The transient response exhibits overshoot and ringing.

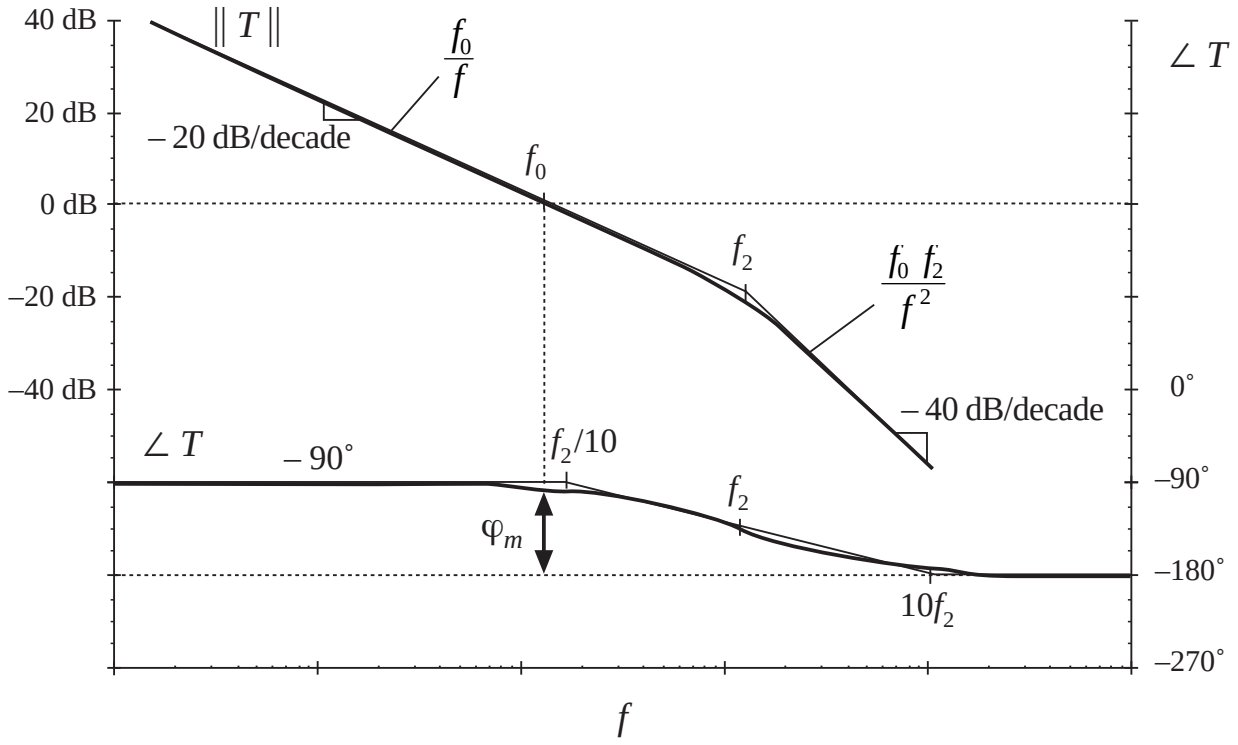
Increasing the phase margin reduces the Q. Obtaining real poles, with no overshoot and ringing, requires a large phase margin.

The relation between phase margin and closed-loop Q is quantified in this section.

A simple second-order system

Consider the case where $T(s)$ can be well-approximated in the vicinity of the crossover frequency as

$$T(s) = \frac{1}{\left(\frac{s}{\omega_0}\right)\left(1 + \frac{s}{\omega_2}\right)}$$



Closed-loop response

If

$$T(s) = \frac{1}{\left(\frac{s}{\omega_0}\right)\left(1 + \frac{s}{\omega_2}\right)}$$

Then

$$\frac{T(s)}{1 + T(s)} = \frac{1}{1 + \frac{1}{T(s)}} = \frac{1}{1 + \frac{s}{\omega_0} + \frac{s^2}{\omega_0 \omega_2}}$$

or,

$$\frac{T(s)}{1 + T(s)} = \frac{1}{1 + \frac{s}{Q\omega_c} + \left(\frac{s}{\omega_c}\right)^2}$$

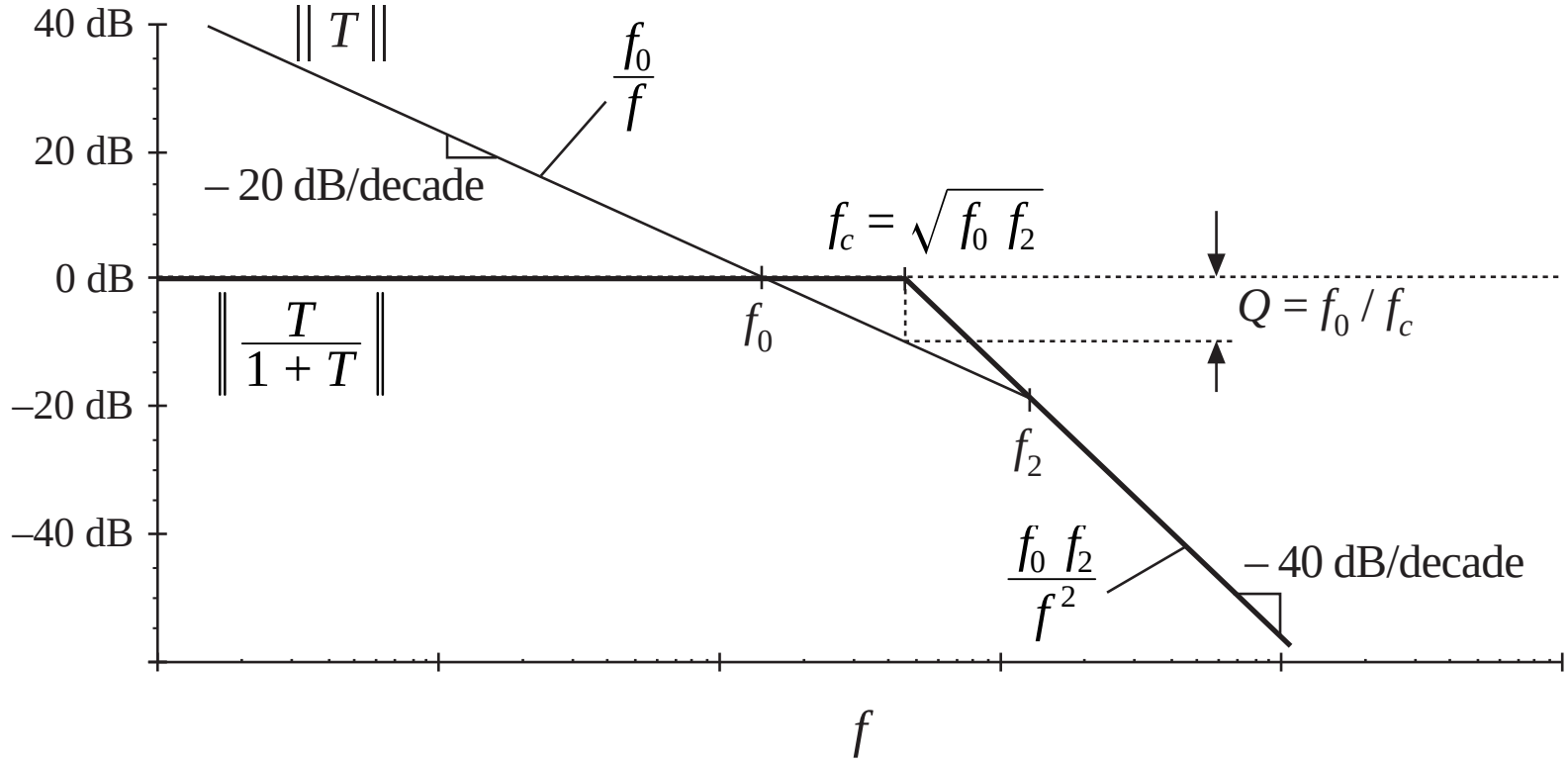
where

$$\omega_c = \sqrt{\omega_0 \omega_2} = 2\pi f_c \qquad Q = \frac{\omega_0}{\omega_c} = \sqrt{\frac{\omega_0}{\omega_2}}$$

Low-Q case

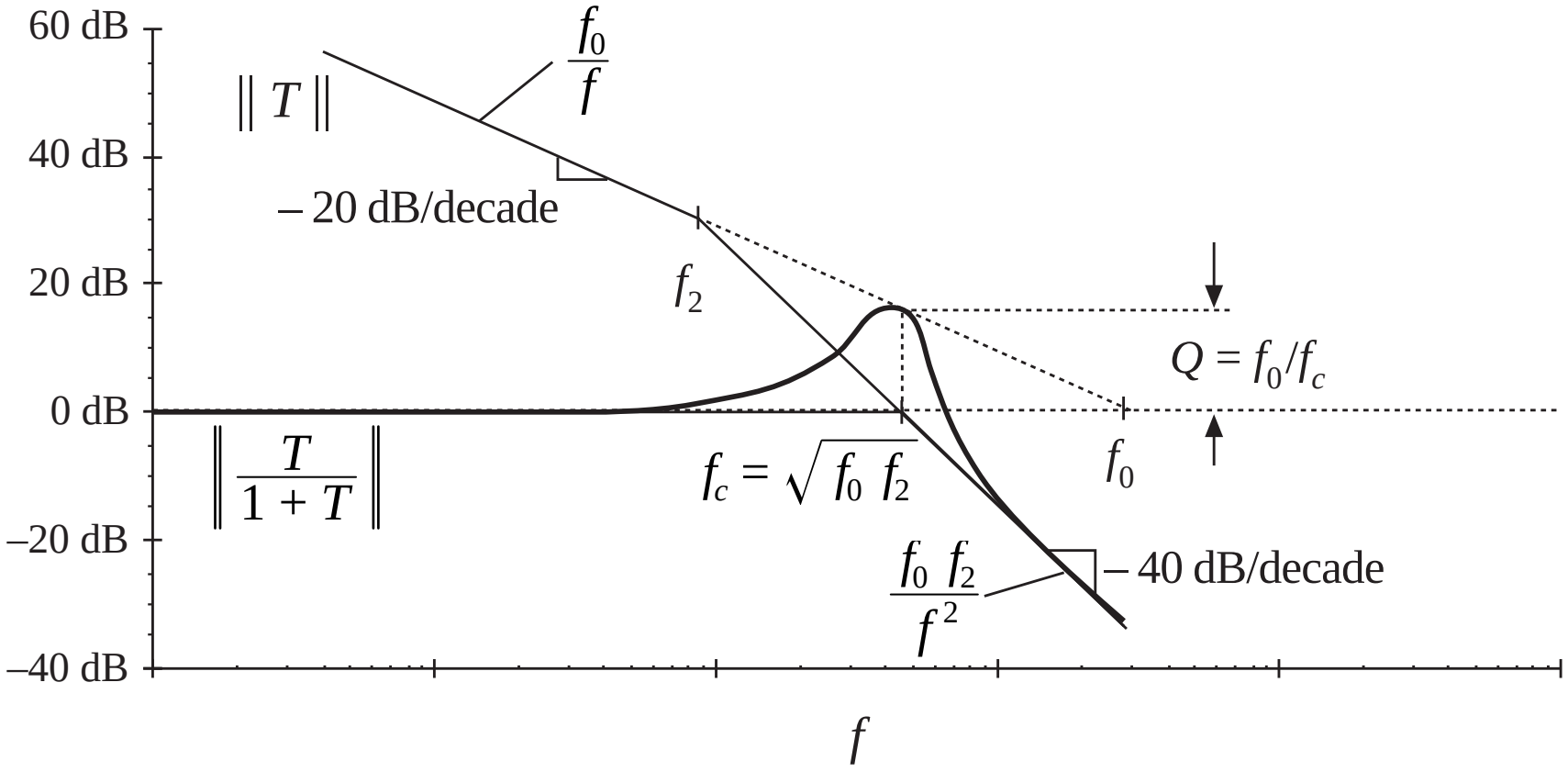
$$Q = \frac{\omega_0}{\omega_c} = \sqrt{\frac{\omega_0}{\omega_2}}$$

low-Q approximation: $Q\,\omega_c = \omega_0$ $\qquad \frac{\omega_c}{Q} = \omega_2$



High-Q case

$$\omega_c = \sqrt{\omega_0 \omega_2} = 2\pi f_c \qquad Q = \frac{\omega_0}{\omega_c} = \sqrt{\frac{\omega_0}{\omega_2}}$$



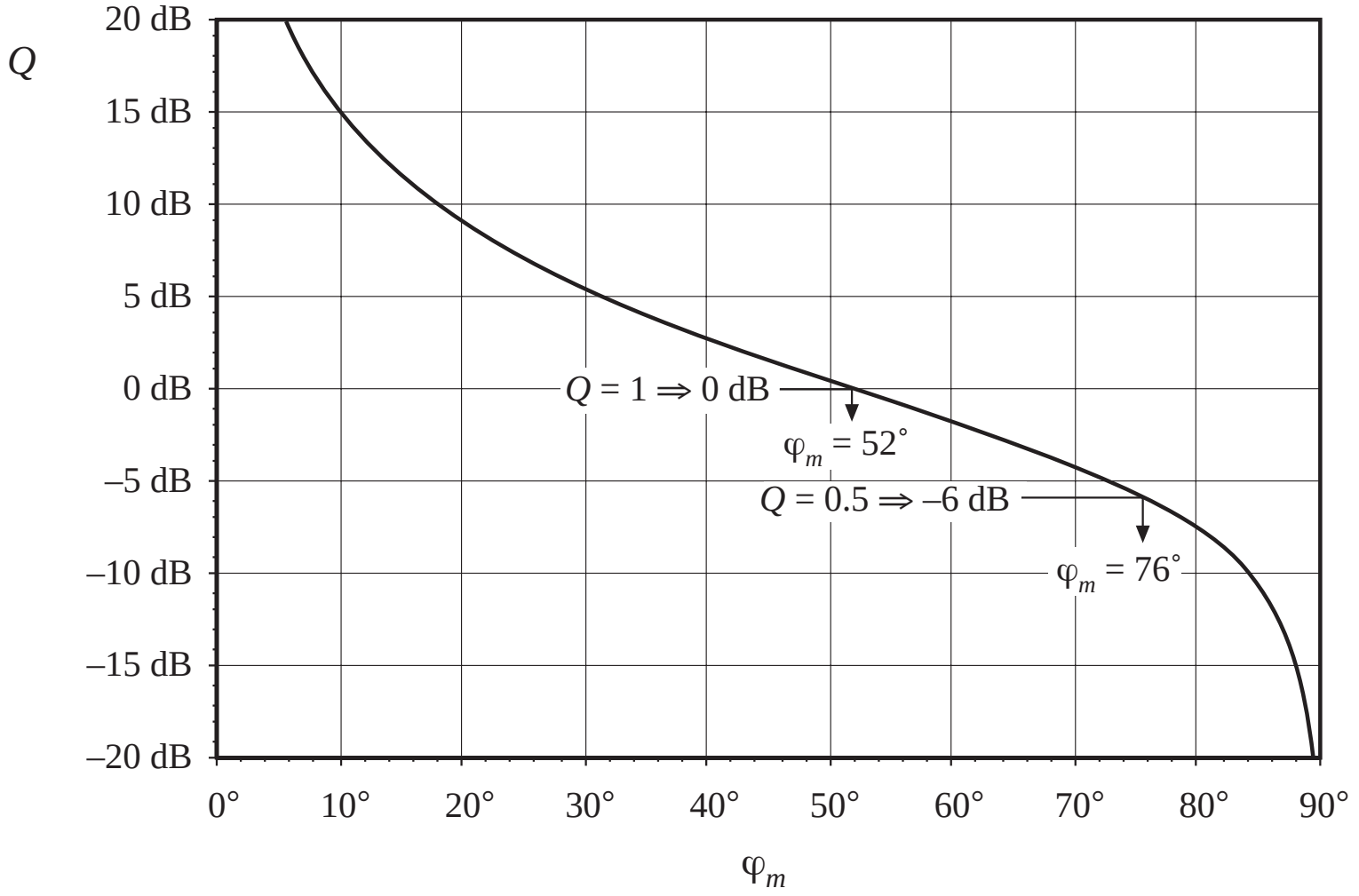
Q vs. φ_m

Solve for exact crossover frequency, evaluate phase margin, express as function of φ_m. Result is:

$$Q = \frac{\sqrt{\cos \varphi_m}}{\sin \varphi_m}$$

$$\varphi_m = \tan^{-1} \sqrt{\frac{1 + \sqrt{1 + 4Q^4}}{2Q^4}}$$

Q vs. φ_m


Q
20 dB
15 dB
10 dB
5 dB
0 dB
–5 dB
–10 dB
–15 dB
–20 dB
Q = 1 ⇒ 0 dB
φm = 52˚
Q = 0.5 ⇒ –6 dB
φm = 76˚
0°
10°
20°
30°
40°
50°
60°
70°
80°
90°
φm

9.4.3. Transient response vs. damping factor

Unit-step response of second-order system $T(s)/(1+T(s))$

$$\hat{v}(t) = 1 + \frac{2Q\, e^{-\omega_c t/2Q}}{\sqrt{4Q^2-1}} \sin\left[\frac{\sqrt{4Q^2-1}}{2Q}\,\omega_c\, t + \tan^{-1}\left(\sqrt{4Q^2-1}\right)\right] \qquad Q > 0.5$$

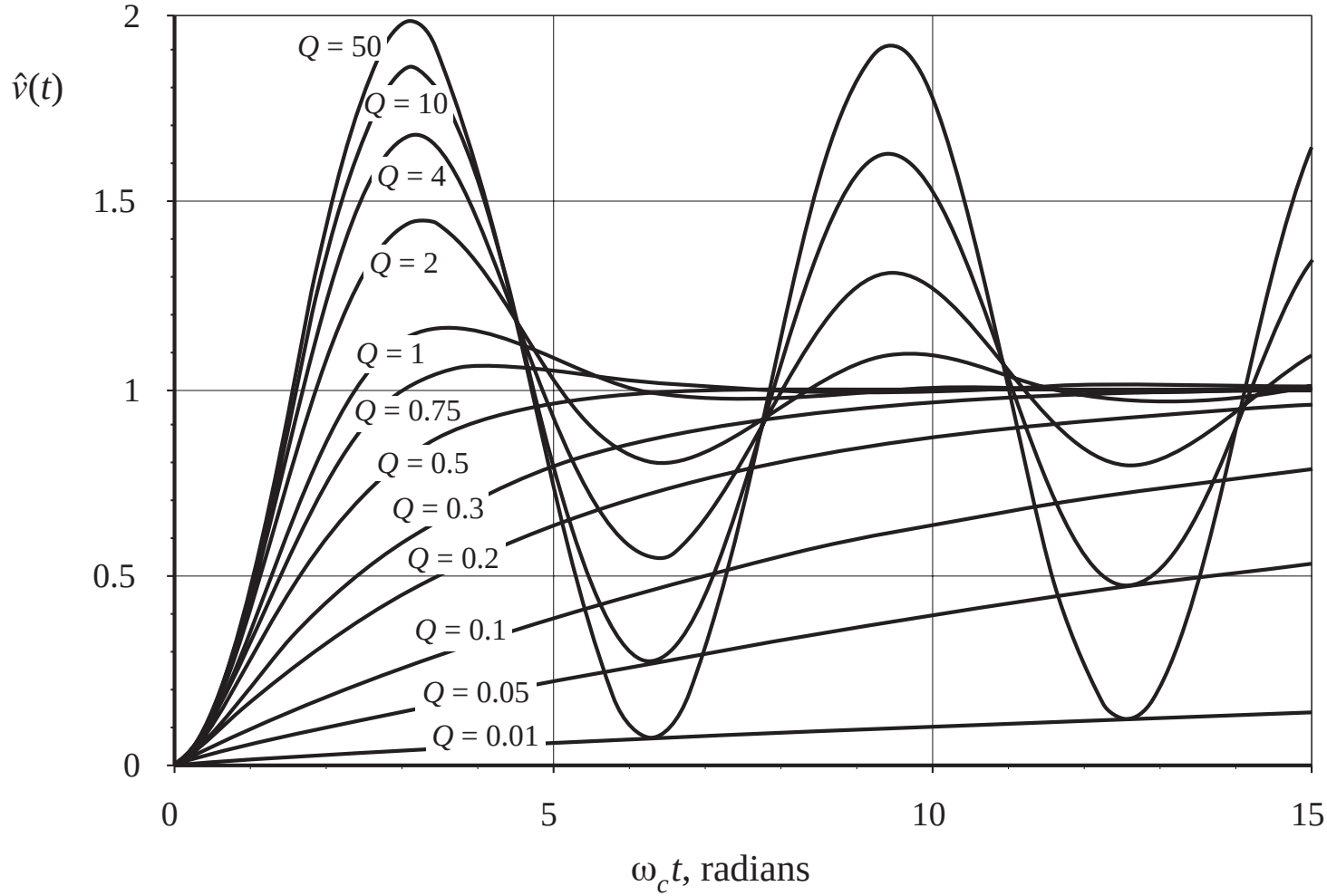
$$\hat{v}(t) = 1 - \frac{\omega_2}{\omega_2-\omega_1}\, e^{-\omega_1 t} - \frac{\omega_1}{\omega_1-\omega_2}\, e^{-\omega_2 t} \qquad Q < 0.5$$

$$\omega_1,\ \omega_2 = \frac{\omega_c}{2Q}\left(1 \pm \sqrt{1-4Q^2}\right)$$

For $Q > 0.5$, the peak value is

$$peak\ \hat{v}(t) = 1 + e^{-\pi/\sqrt{4Q^2-1}}$$

Transient response vs. damping factor



9.5. Regulator design

Typical specifications:

- Effect of load current variations on output voltage regulation

  This is a limit on the maximum allowable output impedance

- Effect of input voltage variations on the output voltage regulation

  This limits the maximum allowable line-to-output transfer function

- Transient response time

  This requires a sufficiently high crossover frequency

- Overshoot and ringing

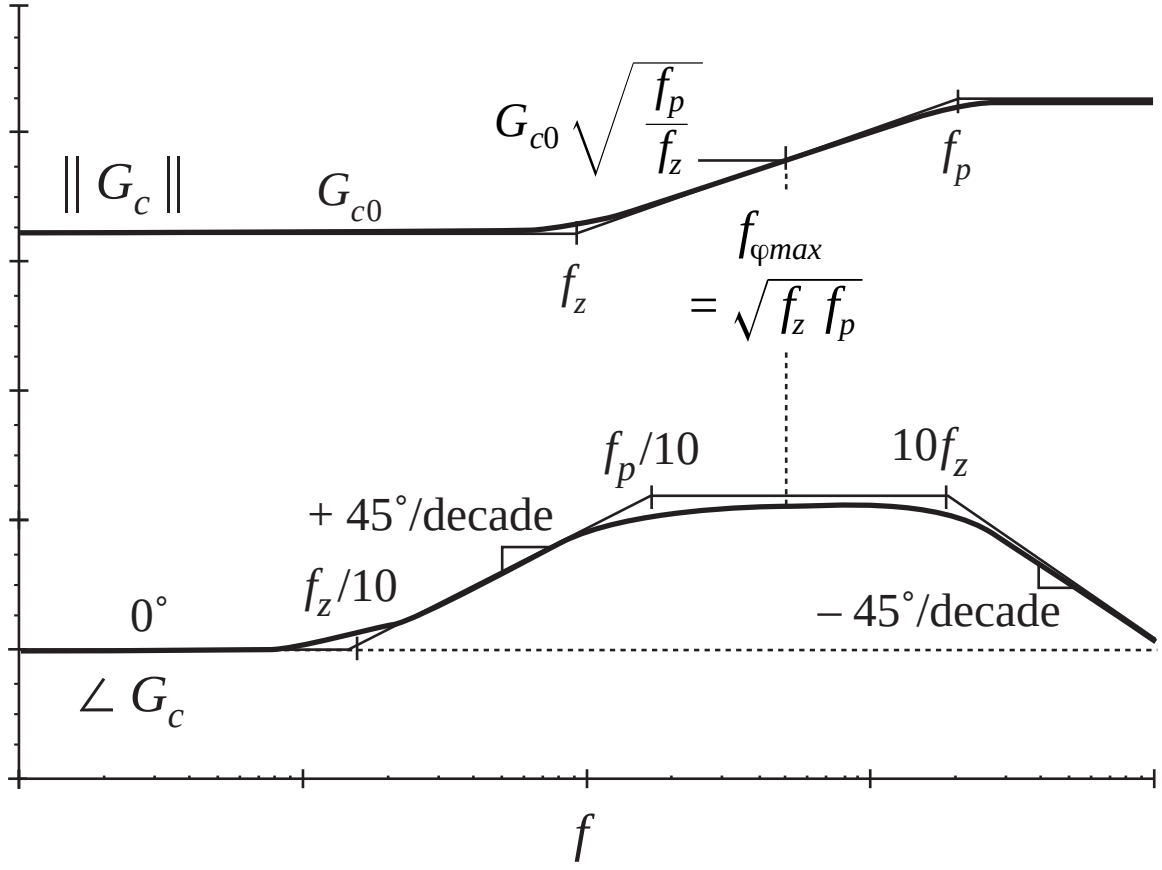
  An adequate phase margin must be obtained

The regulator design problem: add compensator network $G_c(s)$ to modify $T(s)$ such that all specifications are met.

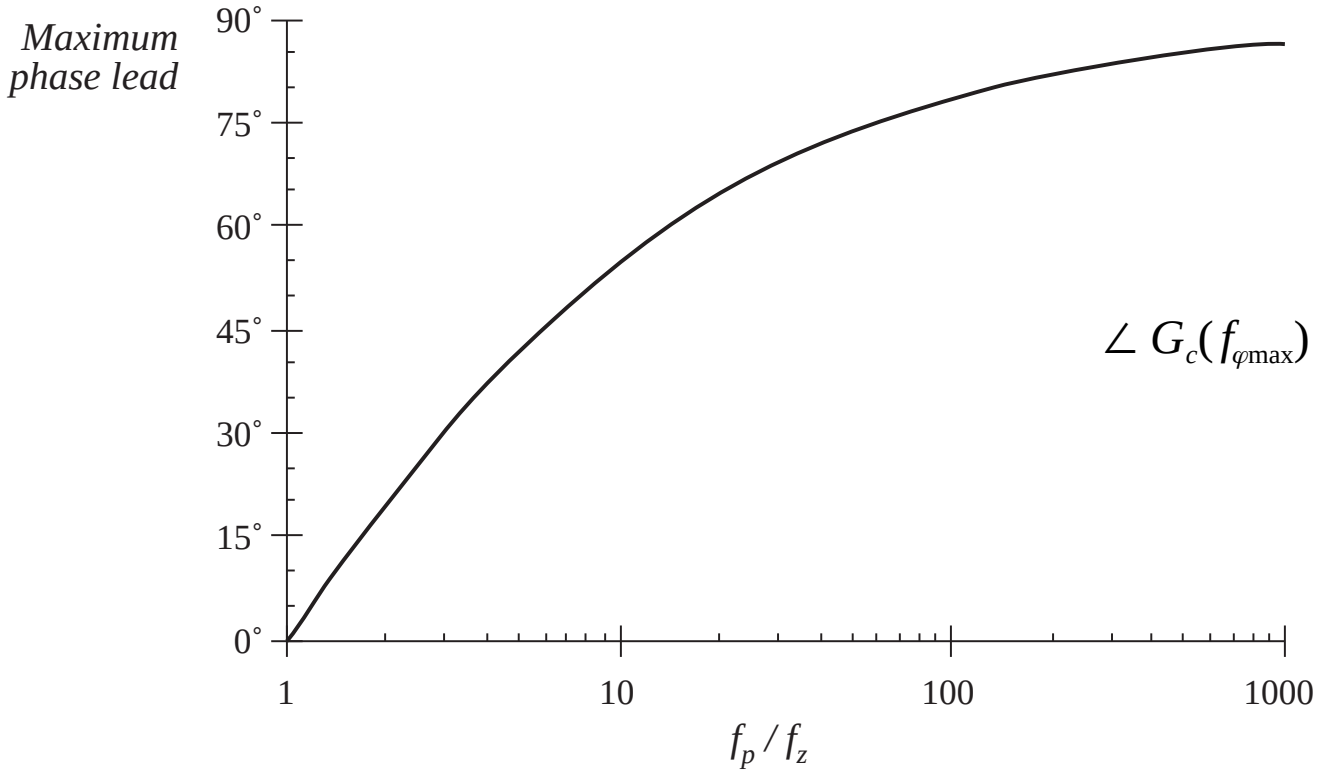
9.5.1. Lead (PD) compensator

$$G_c(s) = G_{c0} \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_p}\right)}$$

Improves phase margin



Lead compensator: maximum phase lead



$$f_{\varphi\max} = \sqrt{f_z f_p}$$

$$\angle G_c(f_{\varphi\max}) = \tan^{-1}\left(\frac{\sqrt{\frac{f_p}{f_z}} - \sqrt{\frac{f_z}{f_p}}}{2} \right)$$

$$\frac{f_p}{f_z} = \frac{1 + \sin\left(\theta\right)}{1 - \sin\left(\theta\right)}$$

Lead compensator design

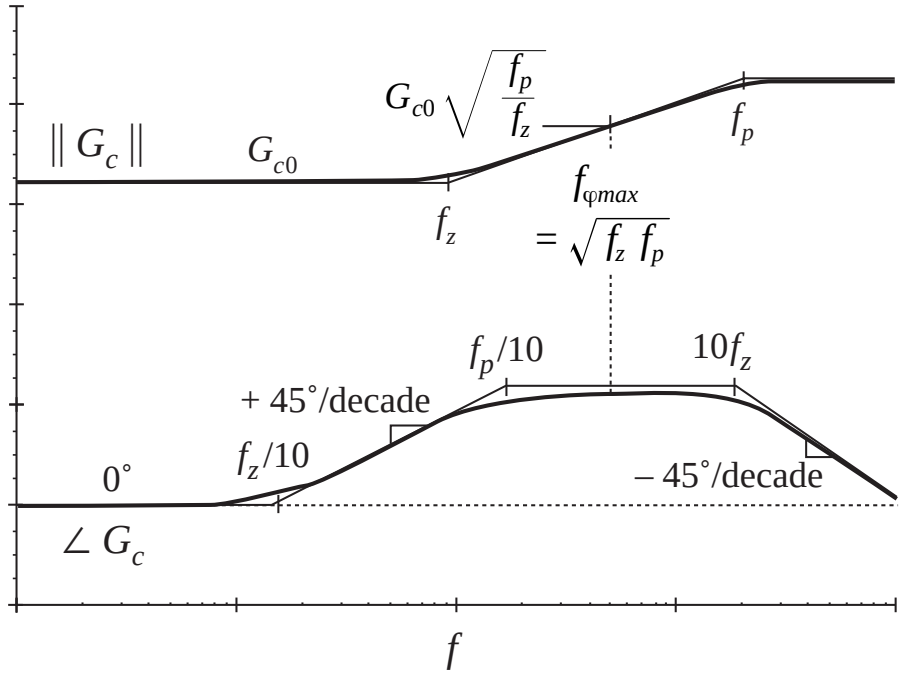
To optimally obtain a compensator phase lead of θ at frequency f_c, the pole and zero frequencies should be chosen as follows:

$$f_z = f_c \sqrt{\frac{1 - \sin(\theta)}{1 + \sin(\theta)}}$$

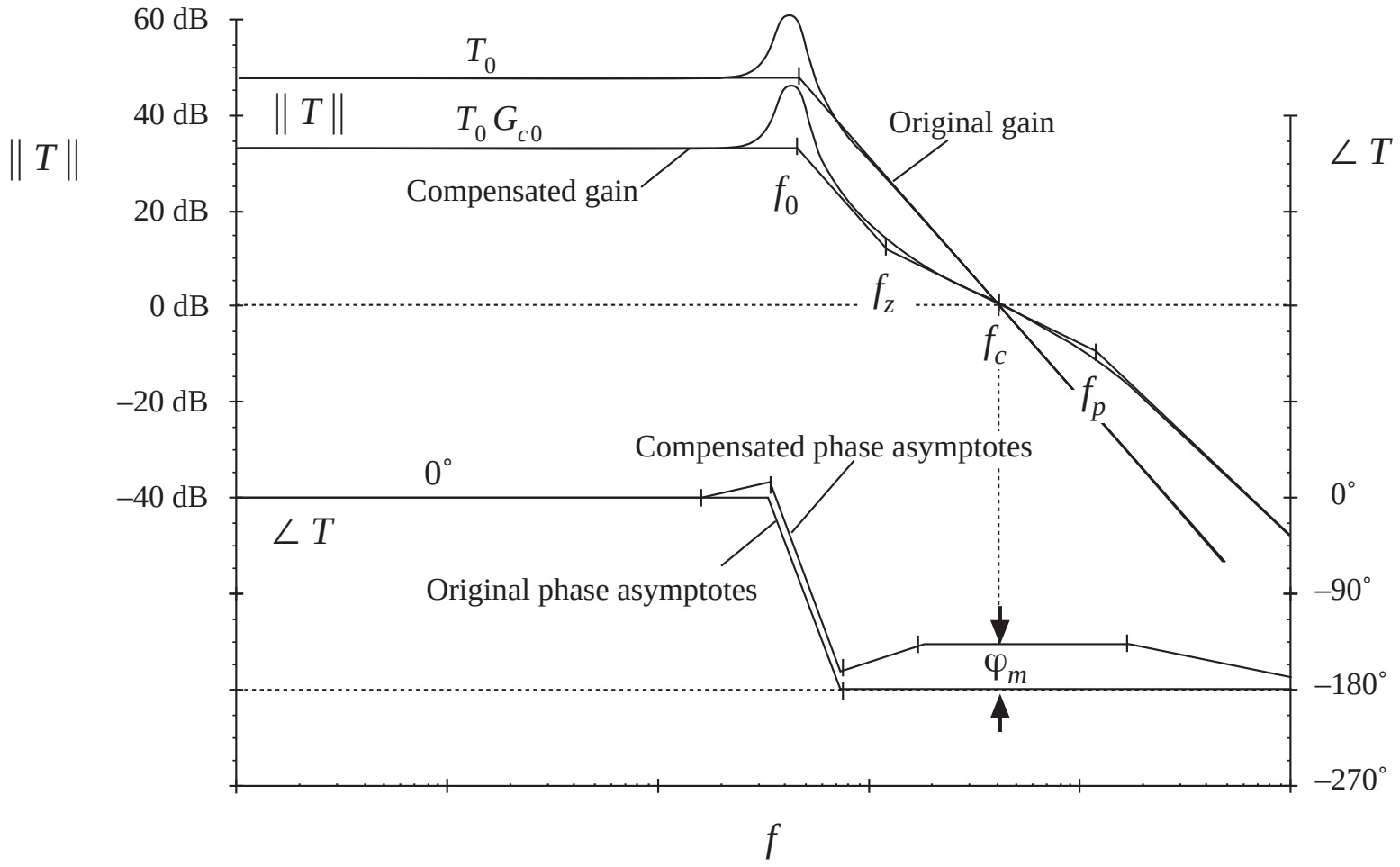
$$f_p = f_c \sqrt{\frac{1 + \sin(\theta)}{1 - \sin(\theta)}}$$

If it is desired that the magnitude of the compensator gain at f_c be unity, then G_{c0} should be chosen as

$$G_{c0} = \sqrt{\frac{f_z}{f_p}}$$



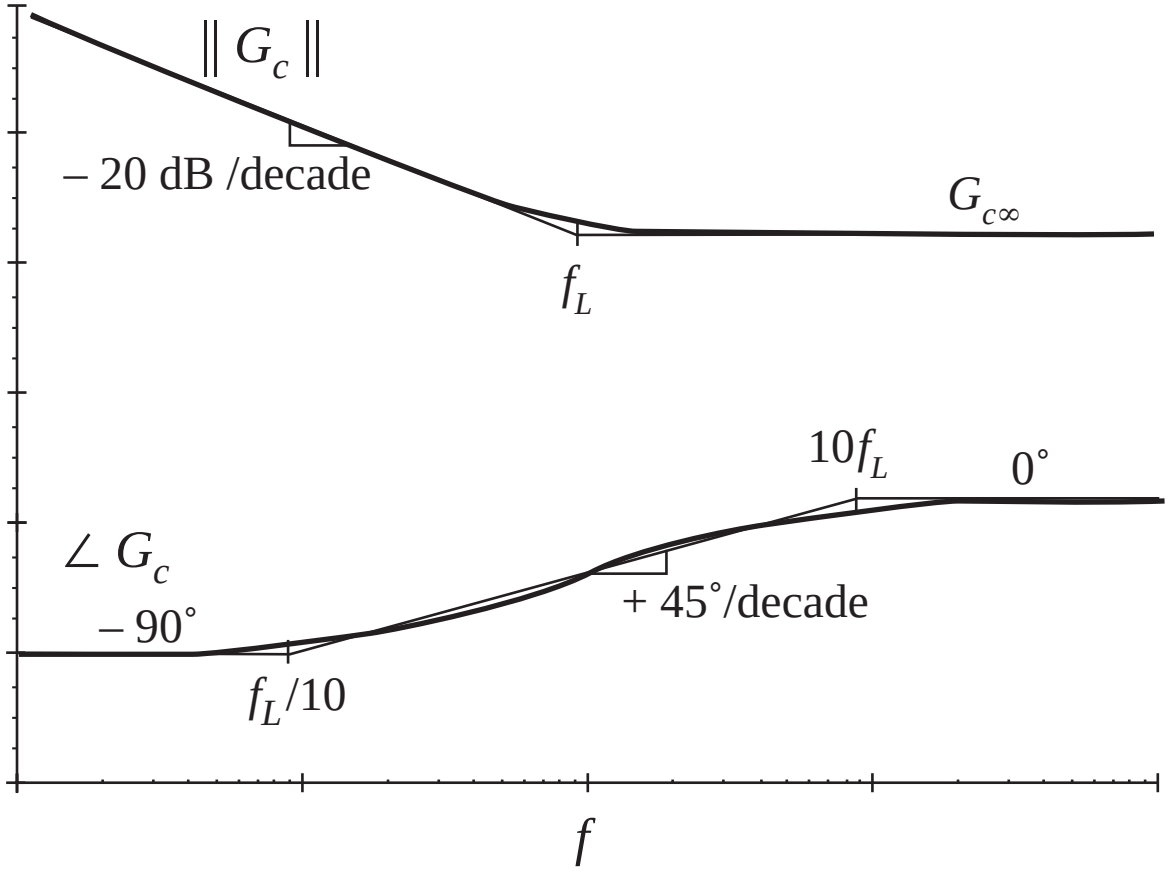
Example: lead compensation



9.5.2. Lag (PI) compensation

$$G_c(s) = G_{c\infty}\left(1 + \frac{\omega_L}{s}\right)$$

Improves low-frequency loop gain and regulation



Example: lag compensation

original (uncompensated) loop gain is

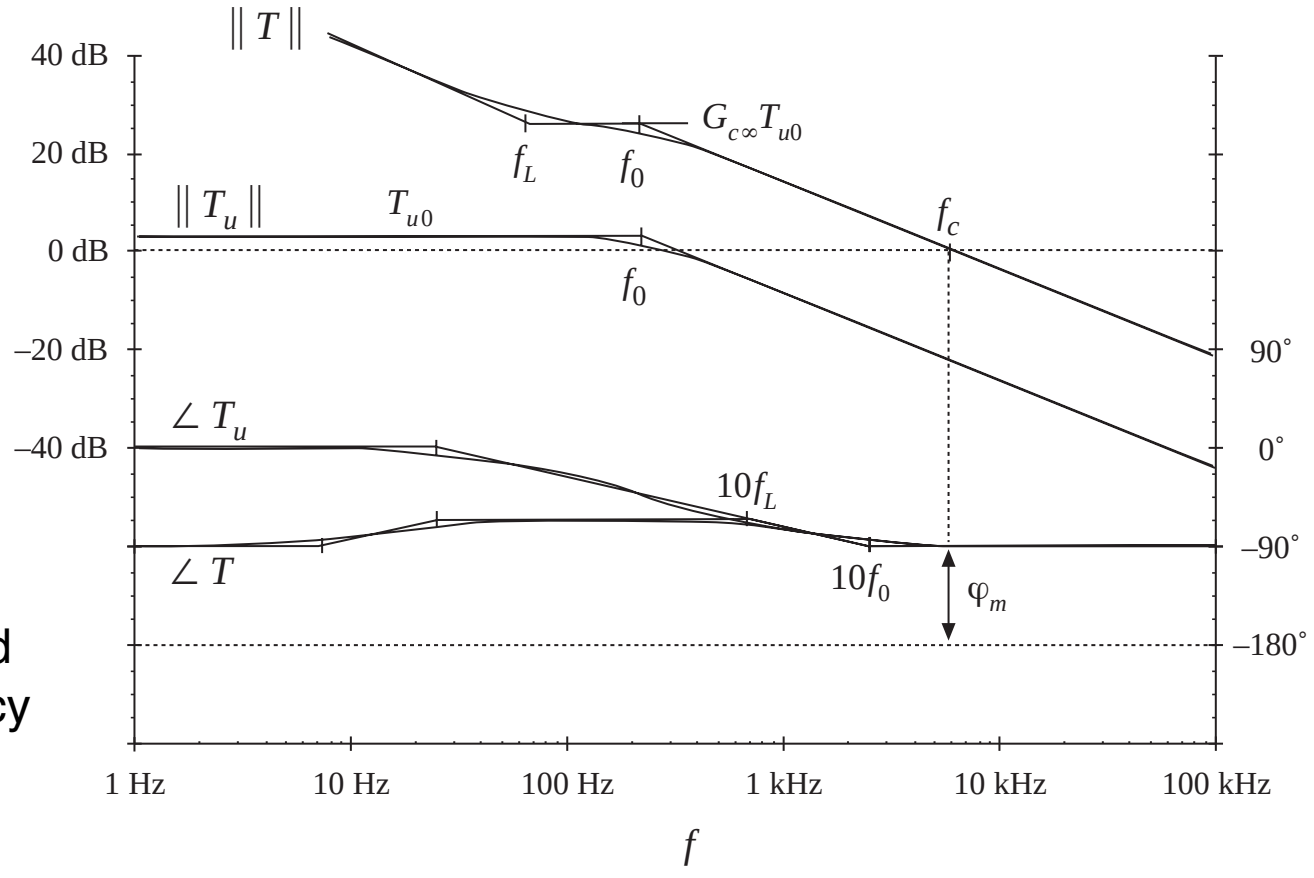
$$T_u(s) = \frac{T_{u0}}{\left(1 + \frac{s}{\omega_0}\right)}$$

compensator:

$$G_c(s) = G_{c\infty}\left(1 + \frac{\omega_L}{s}\right)$$

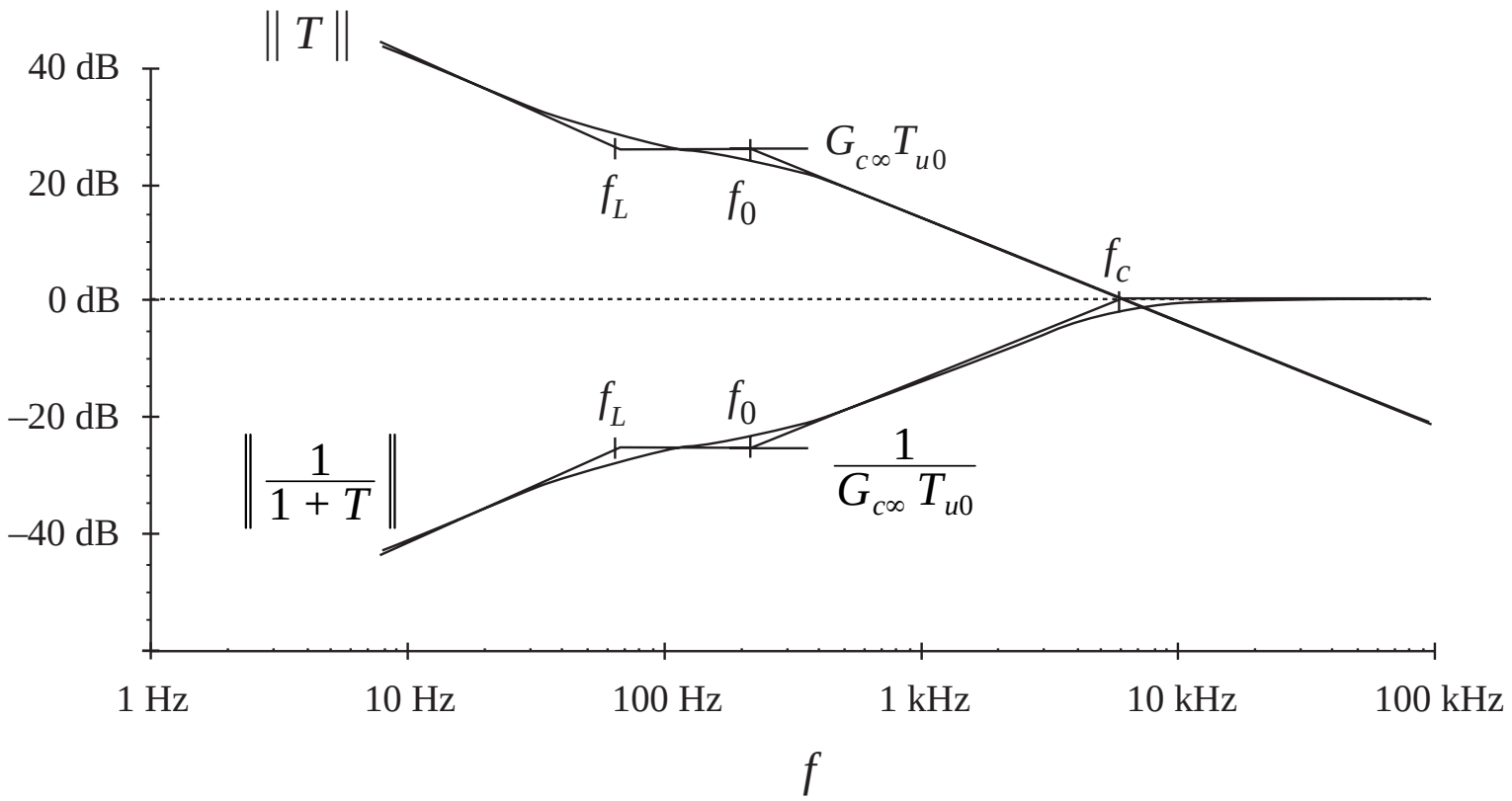
Design strategy: choose

- $G_{c\infty}$ to obtain desired crossover frequency
- ω_L sufficiently low to maintain adequate phase margin



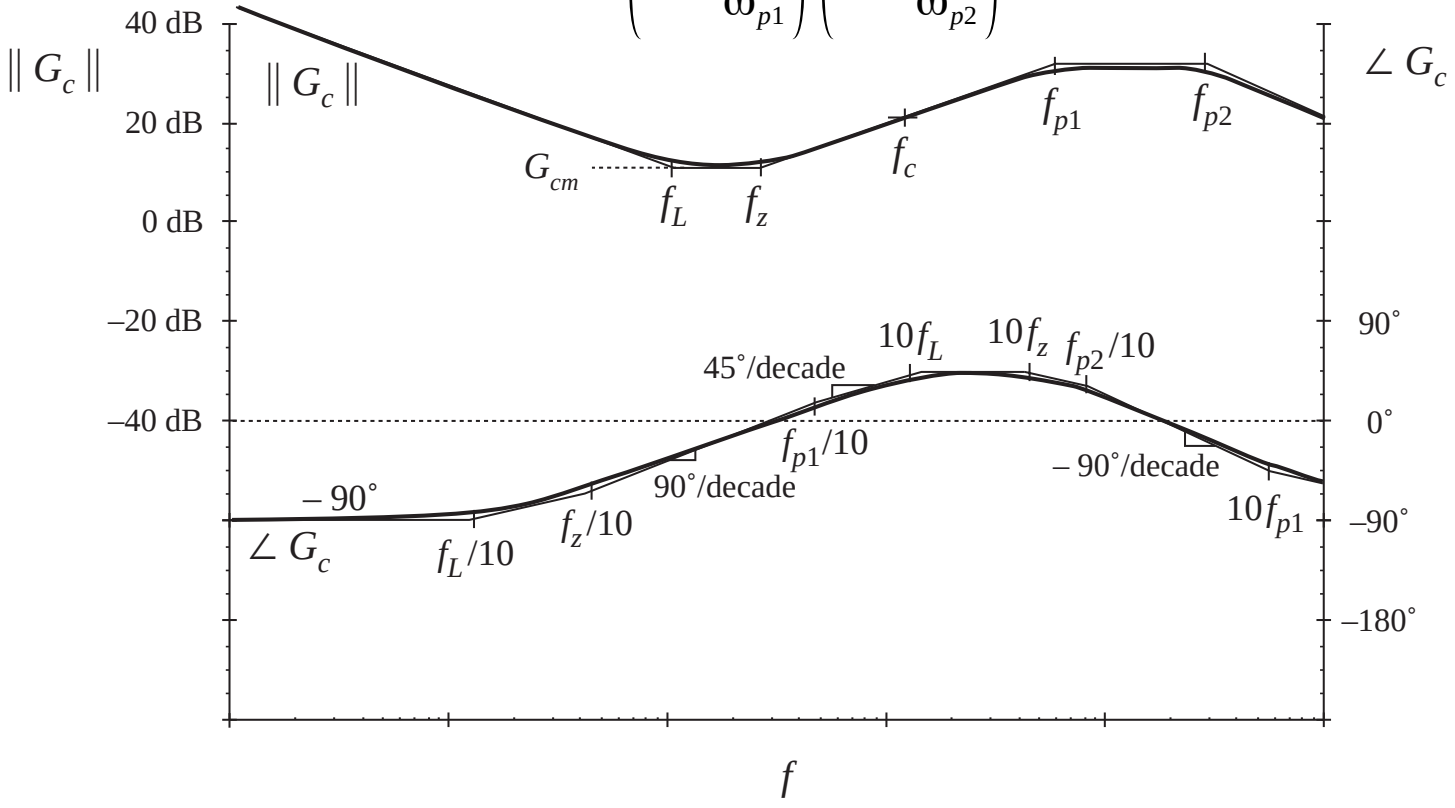
Example, continued

Construction of $1/(1+T)$*, lag compensator example:*

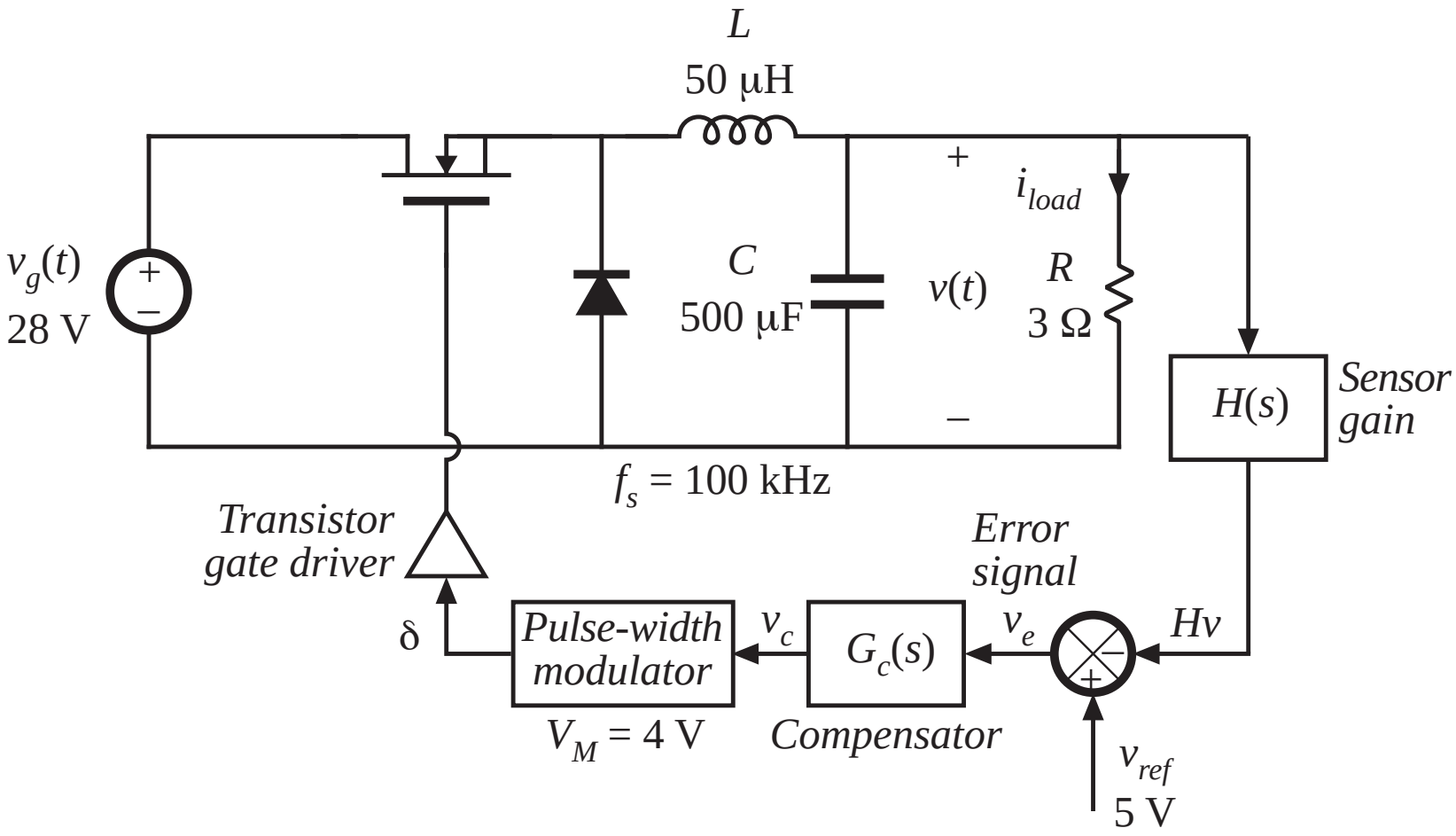


9.5.3. Combined (PID) compensator

$$G_c(s) = G_{cm} \frac{\left(1 + \frac{\omega_L}{s}\right)\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)}$$



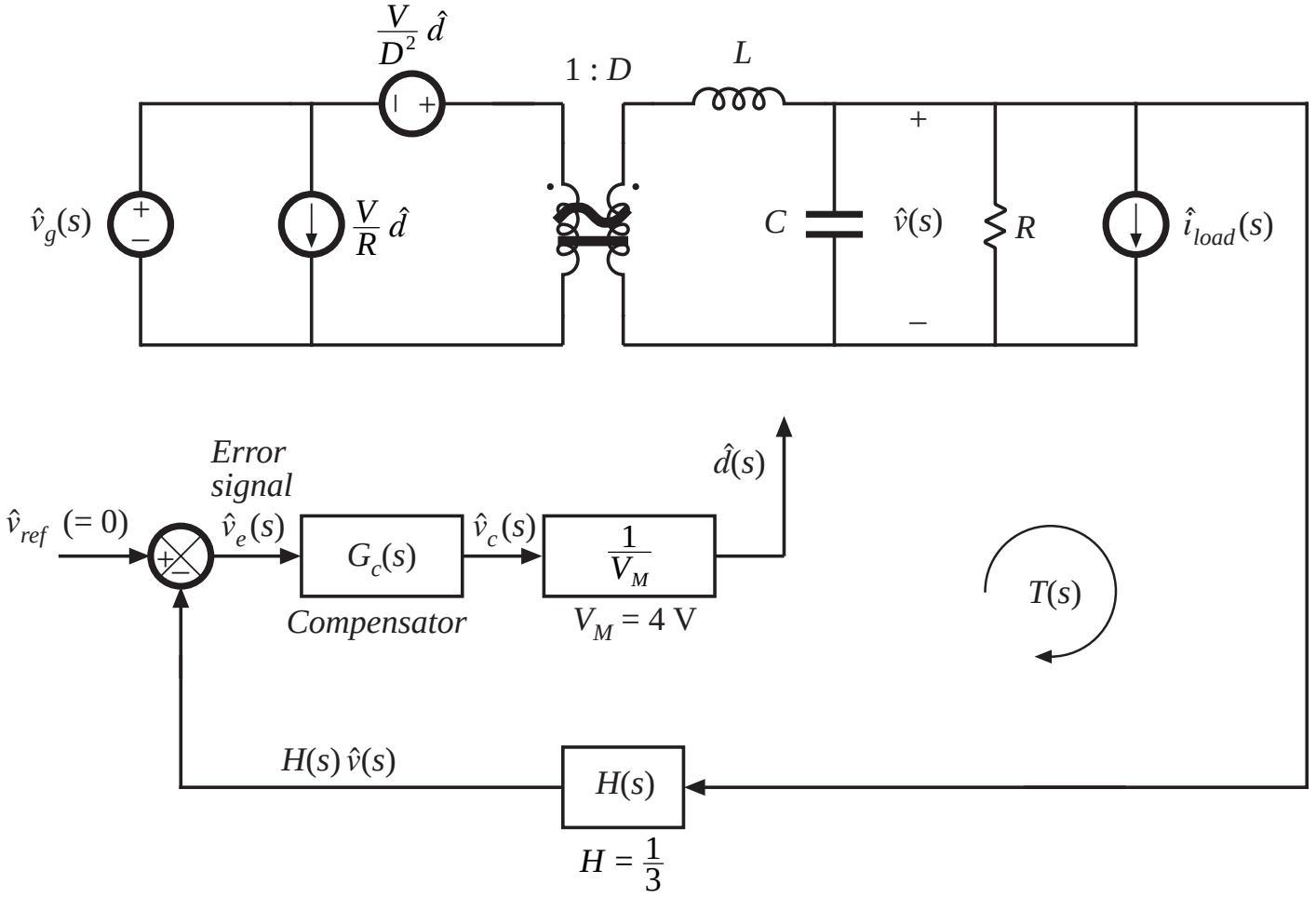
9.5.4. Design example



Quiescent operating point

Input voltage	$V_g = 28\text{V}$
Output	$V = 15\text{V}, I_{load} = 5\text{A}, R = 3\Omega$
Quiescent duty cycle	$D = 15/28 = 0.536$
Reference voltage	$V_{ref} = 5\text{V}$
Quiescent value of control voltage	$V_c = DV_M = 2.14\text{V}$
Gain $H(s)$	$H = V_{ref}/V = 5/15 = 1/3$

Small-signal model



Open-loop control-to-output transfer function $G_{vd}(s)$

$$G_{vd}(s) = \frac{V}{D} \frac{1}{1 + s\frac{L}{R} + s^2 LC}$$

standard form:

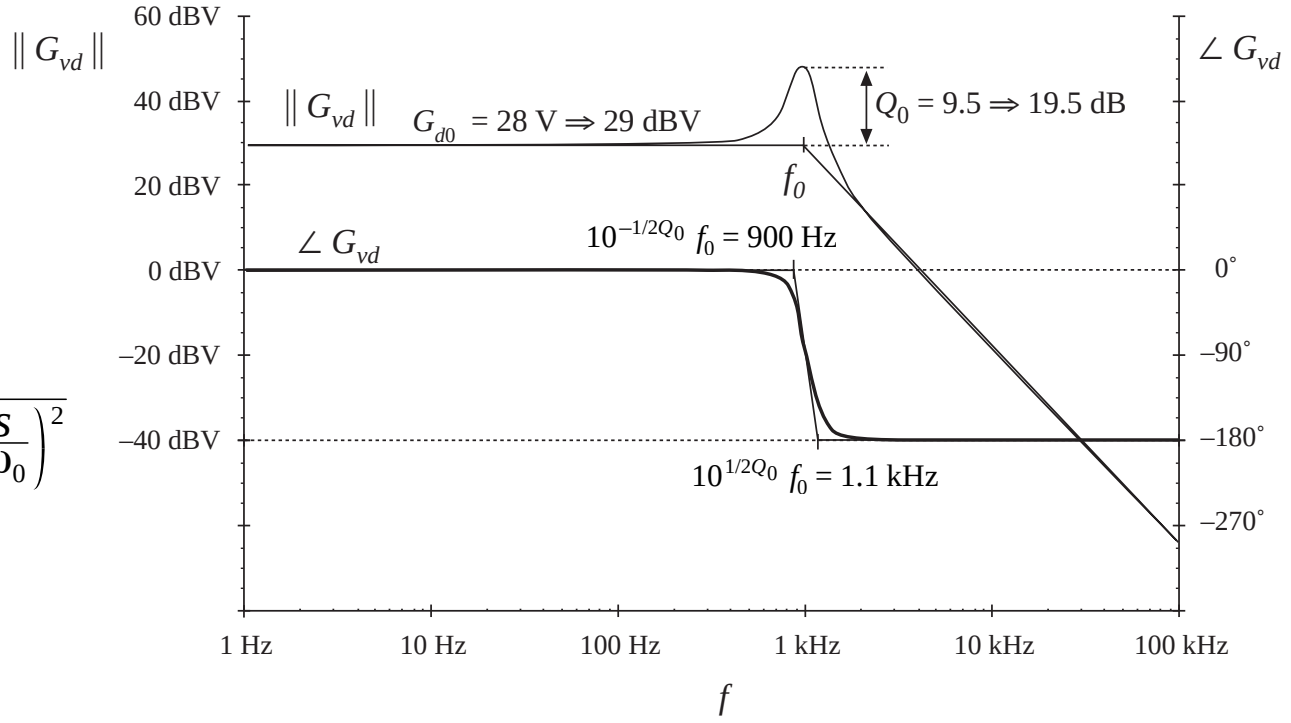
$$G_{vd}(s) = G_{d0} \frac{1}{1 + \frac{s}{Q_0 \omega_0} + \left(\frac{s}{\omega_0}\right)^2}$$

salient features:

$$G_{d0} = \frac{V}{D} = 28\text{V}$$

$$f_0 = \frac{\omega_0}{2\pi} = \frac{1}{2\pi\sqrt{LC}} = 1\text{kHz}$$

$$Q_0 = R\sqrt{\frac{C}{L}} = 9.5 \Rightarrow 19.5\text{dB}$$



Open-loop line-to-output transfer function and output impedance

$$G_{vg}(s) = D \frac{1}{1 + s\frac{L}{R} + s^2 LC}$$

—same poles as control-to-output transfer function

standard form:

$$G_{vg}(s) = G_{g0} \frac{1}{1 + \frac{s}{Q_0 \omega_0} + \left(\frac{s}{\omega_0}\right)^2}$$

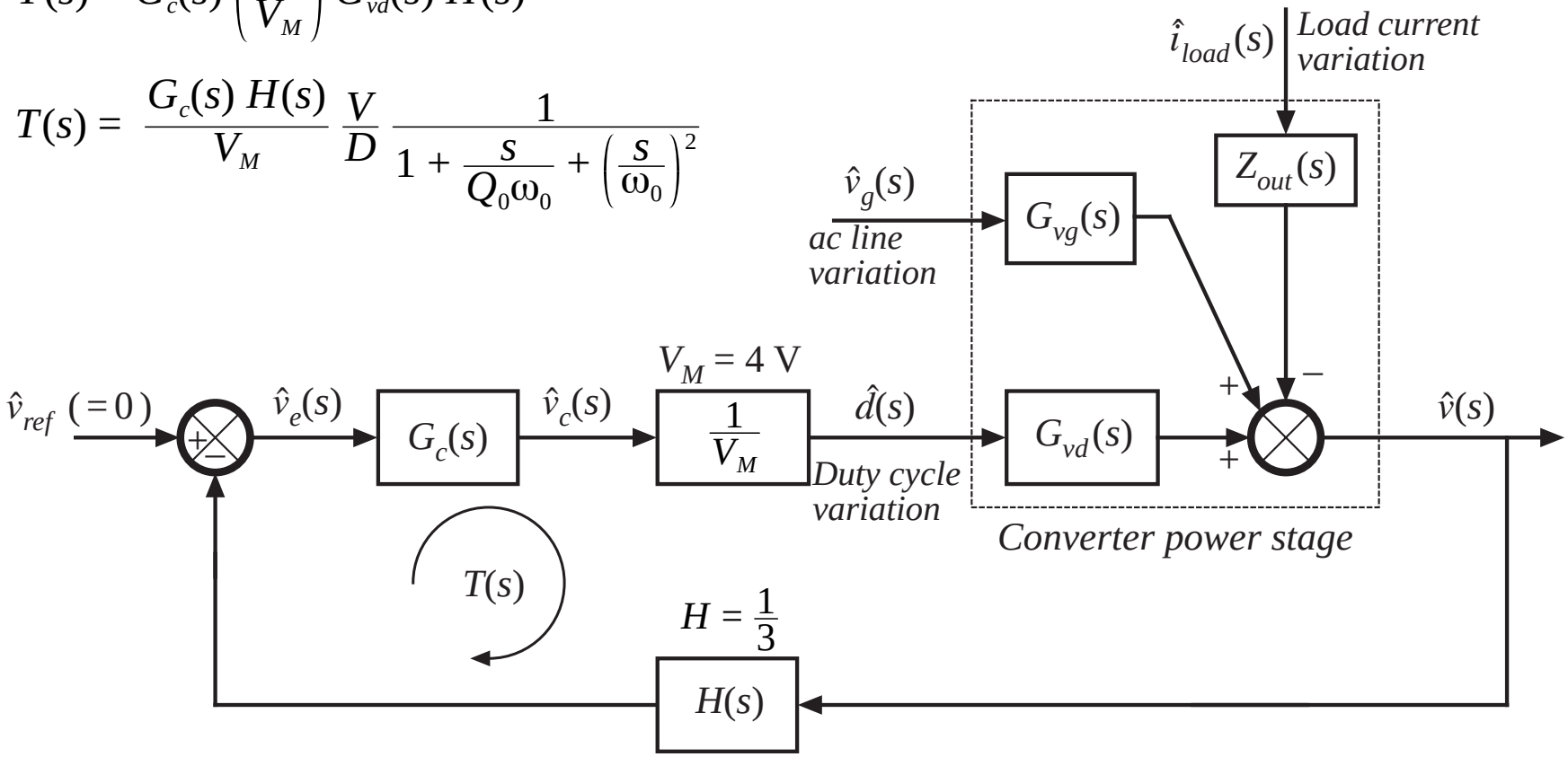
Output impedance:

$$Z_{out}(s) = R \parallel \frac{1}{sC} \parallel sL = \frac{sL}{1 + s\frac{L}{R} + s^2 LC}$$

System block diagram

$$T(s) = G_c(s) \left(\frac{1}{V_M} \right) G_{vd}(s)\, H(s)$$

$$T(s) = \frac{G_c(s)\, H(s)}{V_M} \frac{V}{D} \frac{1}{1 + \frac{s}{Q_0 \omega_0} + \left(\frac{s}{\omega_0} \right)^2}$$

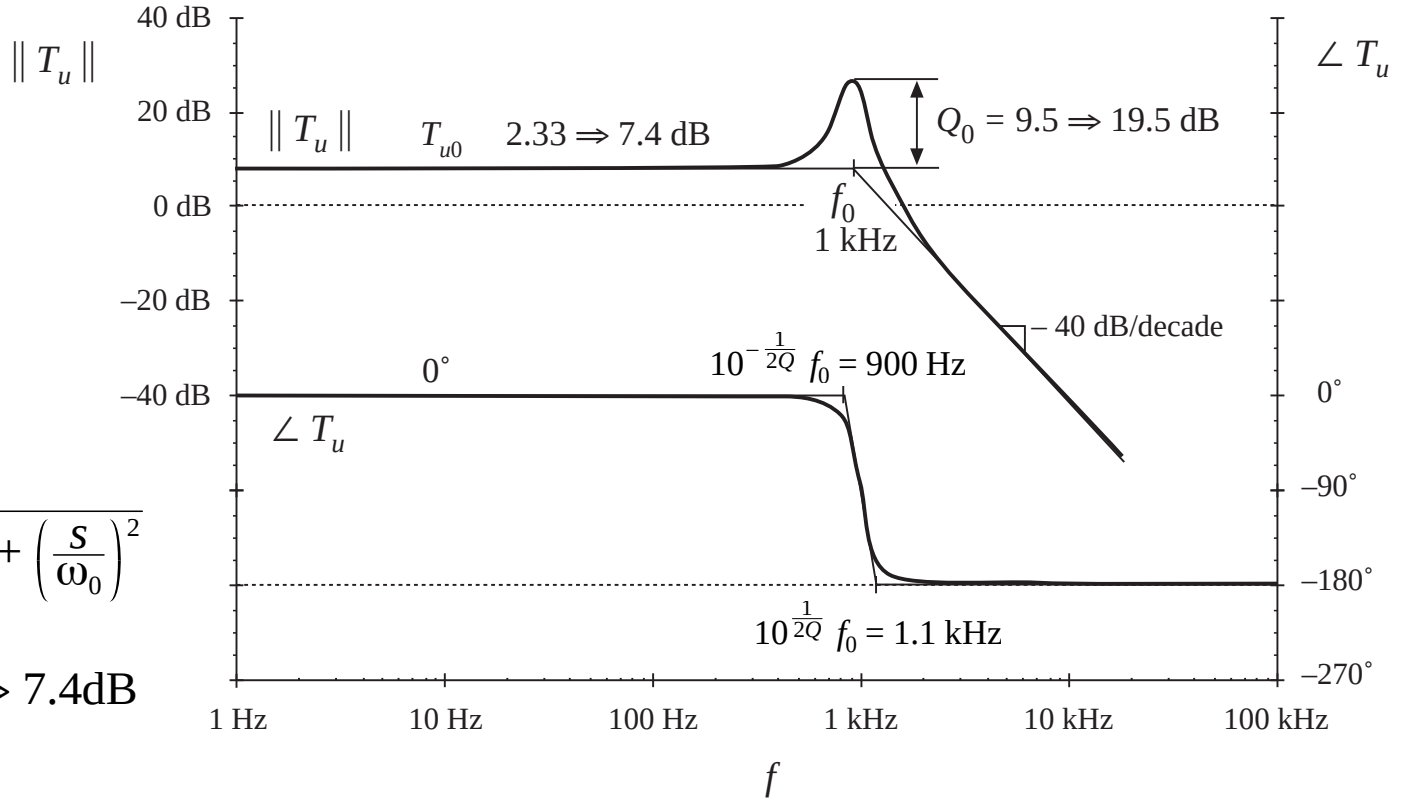


Uncompensated loop gain (with $G_c = 1$)

With $G_c = 1$, the loop gain is

$$T_u(s) = T_{u0} \frac{1}{1 + \frac{s}{Q_0 \omega_0} + \left(\frac{s}{\omega_0}\right)^2}$$

$$T_{u0} = \frac{H\,V}{D\,V_M} = 2.33 \Rightarrow 7.4\text{dB}$$



$f_c = 1.8$ kHz, $\varphi_m = 5^\circ$

Lead compensator design

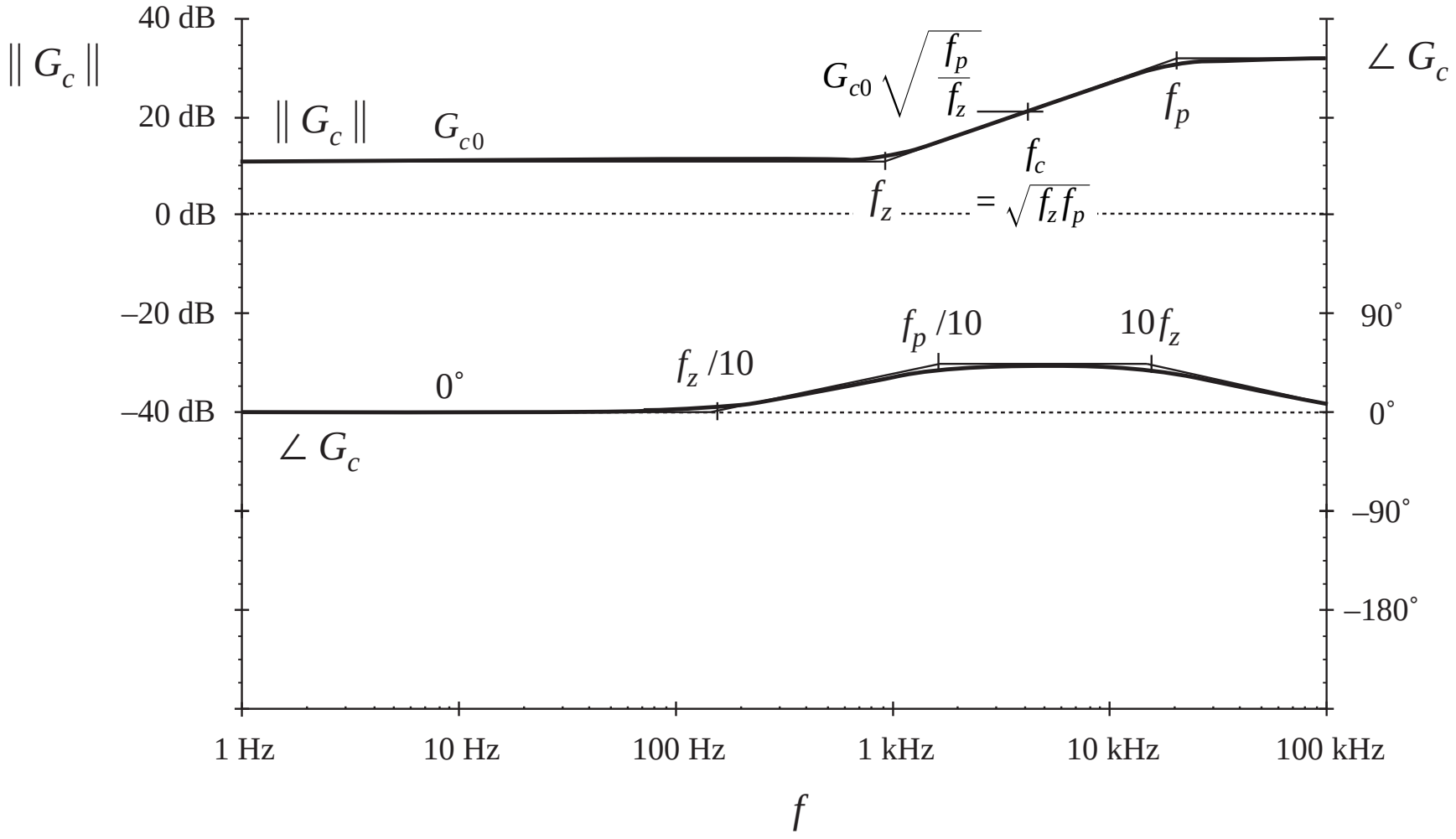
- Obtain a crossover frequency of $5\ \text{kHz}$, with phase margin of 52°
- T_u has phase of approximately -180° at $5\ \text{kHz}$, hence lead (PD) compensator is needed to increase phase margin.
- Lead compensator should have phase of $+52^\circ$ at $5\ \text{kHz}$
- T_u has magnitude of $-20.6\ \text{dB}$ at $5\ \text{kHz}$
- Lead compensator gain should have magnitude of $+20.6\ \text{dB}$ at $5\ \text{kHz}$
- Lead compensator pole and zero frequencies should be

$$f_z = (5\text{kHz}) \sqrt{\frac{1 - \sin(52^\circ)}{1 + \sin(52^\circ)}} = 1.7\text{kHz}$$

$$f_p = (5\text{kHz}) \sqrt{\frac{1 + \sin(52^\circ)}{1 - \sin(52^\circ)}} = 14.5\text{kHz}$$

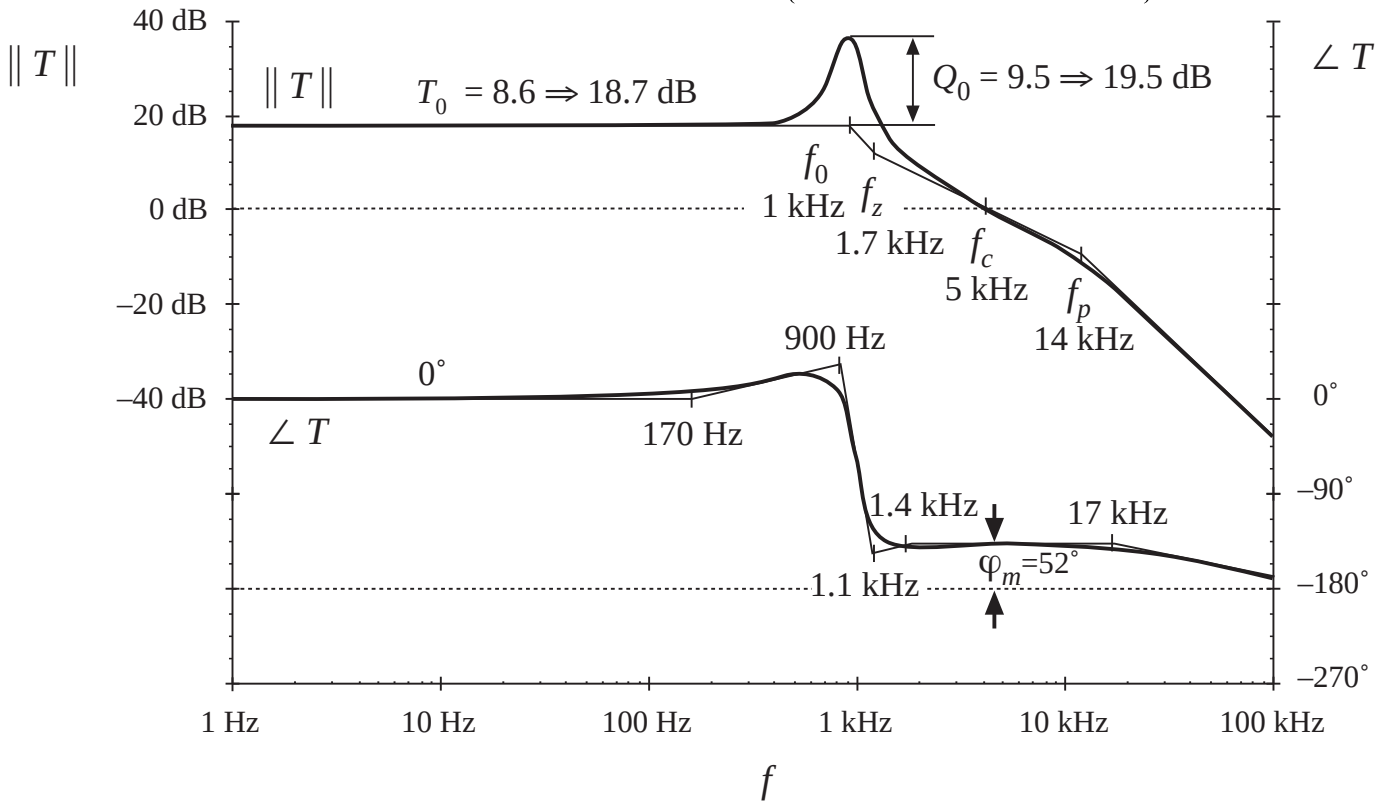
- Compensator dc gain should be $G_{c0} = \left(\frac{f_c}{f_0}\right)^2 \frac{1}{T_{u0}} \sqrt{\frac{f_z}{f_p}} = 3.7 \Rightarrow 11.3\text{dB}$

Lead compensator Bode plot

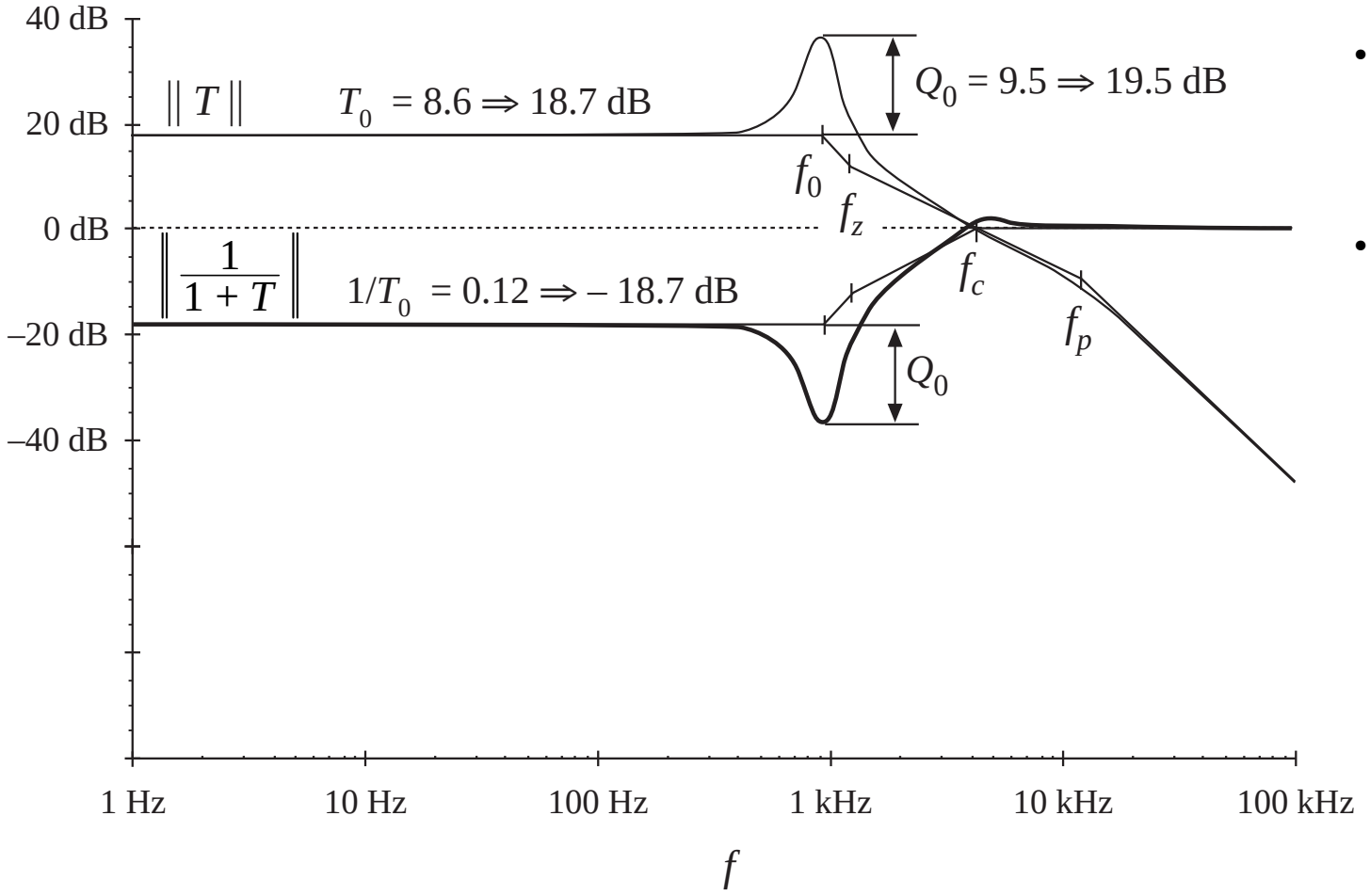


Loop gain, with lead compensator

$$T(s) = T_{u0}\, G_{c0}\, \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_p}\right)\left(1 + \frac{s}{Q_0\omega_0} + \left(\frac{s}{\omega_0}\right)^2\right)}$$



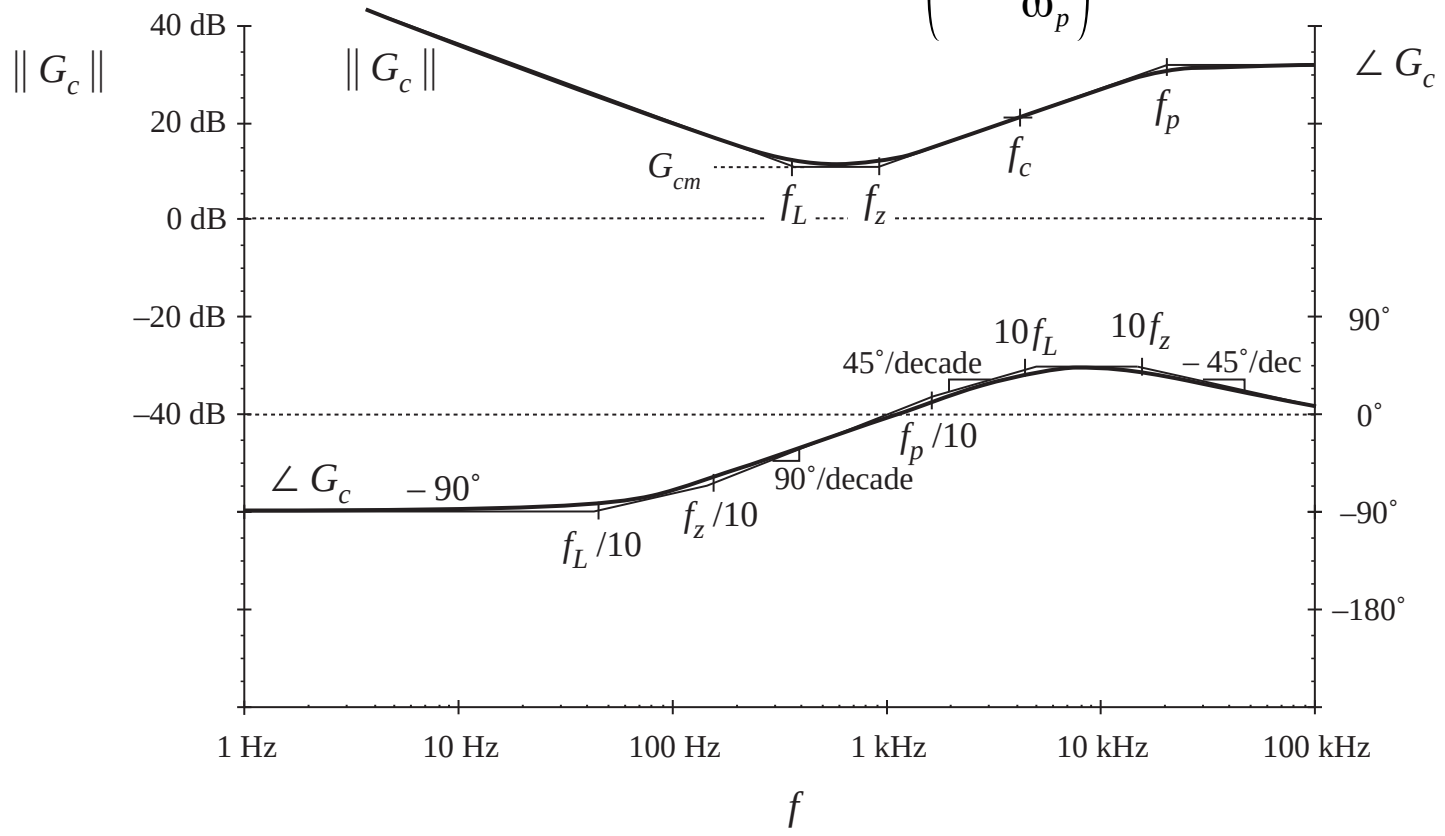
1/(1+T), with lead compensator



- need more low-frequency loop gain
- hence, add inverted zero (PID controller)

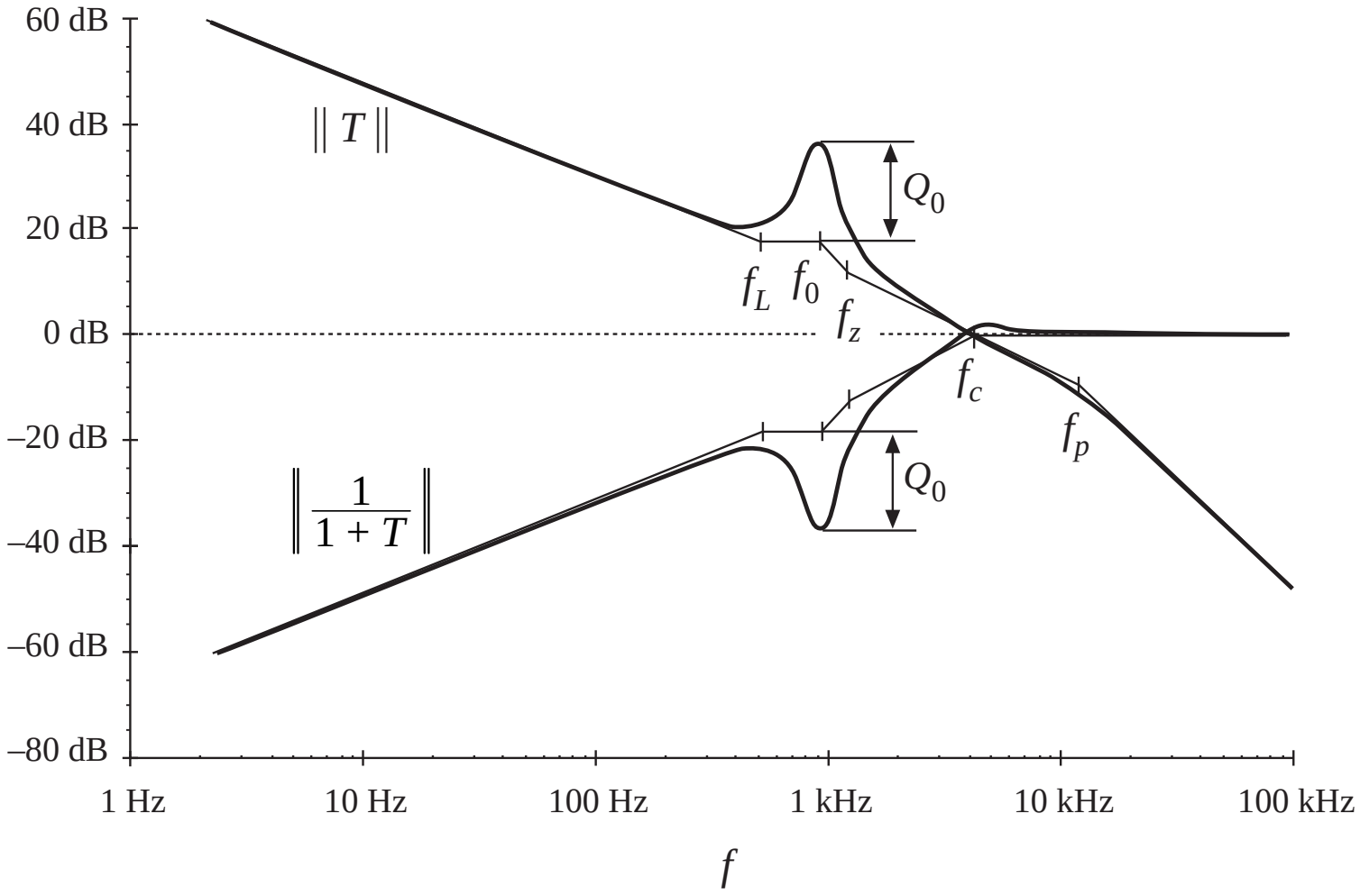
Improved compensator (PID)

$$G_c(s) = G_{cm} \frac{\left(1 + \frac{s}{\omega_z}\right)\left(1 + \frac{\omega_L}{s}\right)}{\left(1 + \frac{s}{\omega_p}\right)}$$

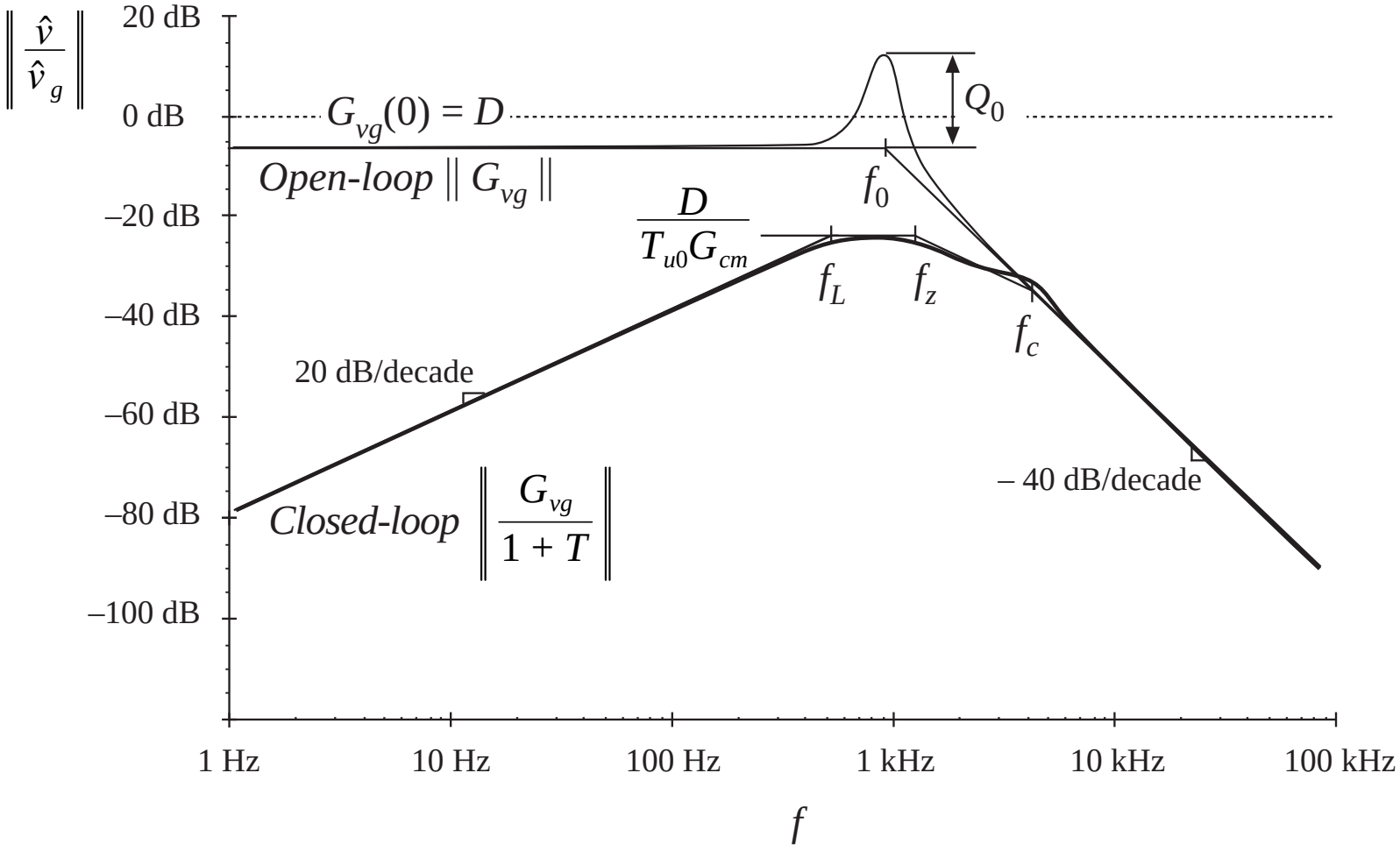


- add inverted zero to PD compensator, without changing dc gain or corner frequencies
- choose f_L to be $f_c/10$, so that phase margin is unchanged

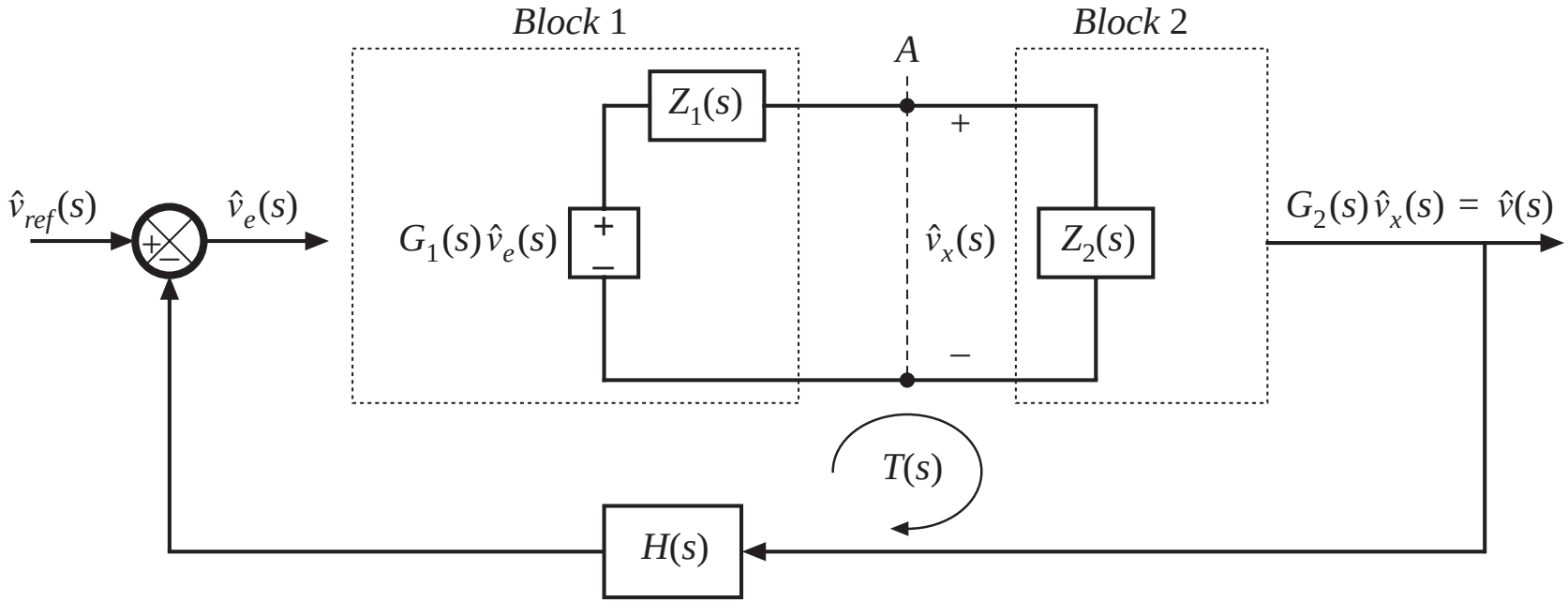
$T(s)$ and $1/(1+T(s))$, with PID compensator



Line-to-output transfer function



9.6. Measurement of loop gains

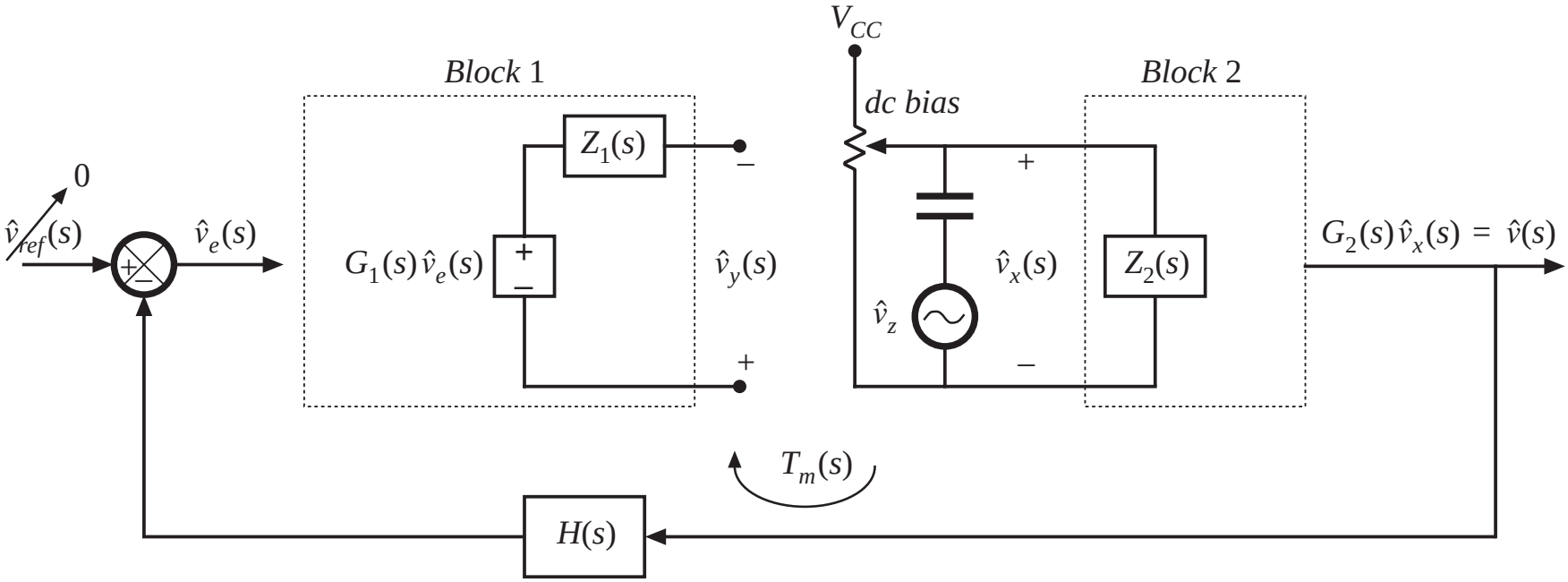


Objective: experimentally determine loop gain $T(s)$, by making measurements at point *A*

Correct result is

$$T(s) = G_1(s) \left(\frac{Z_2(s)}{Z_1(s) + Z_2(s)} \right) G_2(s)\, H(s)$$

Conventional approach: break loop, measure $T(s)$ as conventional transfer function



measured gain is

$$T_m(s) = \left. \frac{\hat{v}_y(s)}{\hat{v}_x(s)} \right|_{\substack{\hat{v}_{ref} = 0 \\ \hat{v}_g = 0}}$$

$$T_m(s) = G_1(s)\, G_2(s)\, H(s)$$

Measured vs. actual loop gain

Actual loop gain:

$$T(s) = G_1(s) \left(\frac{Z_2(s)}{Z_1(s) + Z_2(s)} \right) G_2(s)\, H(s)$$

Measured loop gain:

$$T_m(s) = G_1(s)\, G_2(s)\, H(s)$$

Express T_m as function of T:

$$T_m(s) = T(s) \left(1 + \frac{Z_1(s)}{Z_2(s)} \right)$$

$$T_m(s) \approx T(s) \quad \text{provided that} \quad \| Z_2 \| >> \| Z_1 \|$$

Discussion

- Breaking the loop disrupts the loading of block 2 on block 1.

  A suitable injection point must be found, where loading is not significant.

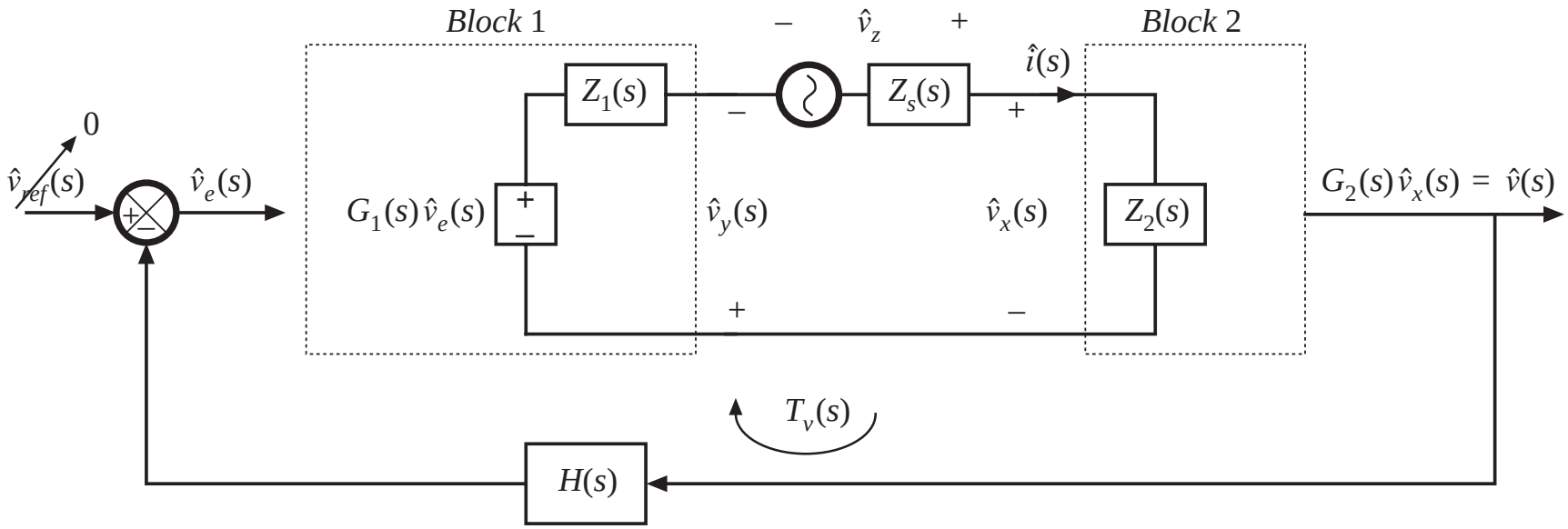
- Breaking the loop disrupts the dc biasing and quiescent operating point.

  A potentiometer must be used, to correctly bias the input to block 2.

  In the common case where the dc loop gain is large, it is very difficult to correctly set the dc bias.

- It would be desirable to avoid breaking the loop, such that the biasing circuits of the system itself set the quiescent operating point.

9.6.1. Voltage injection

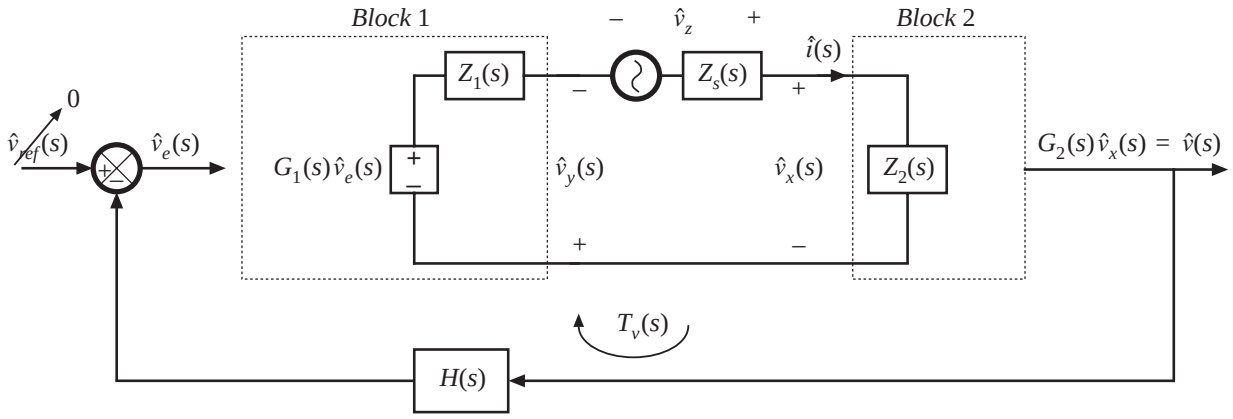


- Ac injection source v_z is connected between blocks 1 and 2
- Dc bias is determined by biasing circuits of the system itself
- Injection source does modify loading of block 2 on block 1

Voltage injection: measured transfer function $T_v(s)$

Network analyzer measures

$$T_v(s) = \left. \frac{\hat{v}_y(s)}{\hat{v}_x(s)} \right|_{\substack{\hat{v}_{ref} = 0 \\ \hat{v}_g = 0}}$$



Solve block diagram:

$$\hat{v}_e(s) = -H(s)\, G_2(s)\, \hat{v}_x(s)$$

$$-\hat{v}_y(s) = G_1(s)\, \hat{v}_e(s) - \hat{i}(s)\, Z_1(s)$$

Hence

$$-\hat{v}_y(s) = -\hat{v}_x(s)\, G_2(s)\, H(s)\, G_1(s) - \hat{i}(s)\, Z_1(s)$$

with

$$\hat{i}(s) = \frac{\hat{v}_x(s)}{Z_2(s)}$$

Substitute:

$$\hat{v}_y(s) = \hat{v}_x(s) \left(G_1(s)\, G_2(s)\, H(s) + \frac{Z_1(s)}{Z_2(s)} \right)$$

which leads to the measured gain

$$T_v(s) = G_1(s)\, G_2(s)\, H(s) + \frac{Z_1(s)}{Z_2(s)}$$

Comparison of $T_v(s)$ with $T(s)$

Actual loop gain is

$$T(s) = G_1(s) \left(\frac{Z_2(s)}{Z_1(s) + Z_2(s)} \right) G_2(s)\, H(s)$$

Gain measured via voltage injection:

$$T_v(s) = G_1(s)\, G_2(s)\, H(s) + \frac{Z_1(s)}{Z_2(s)}$$

Express $Tv(s)$ in terms of $T(s)$:

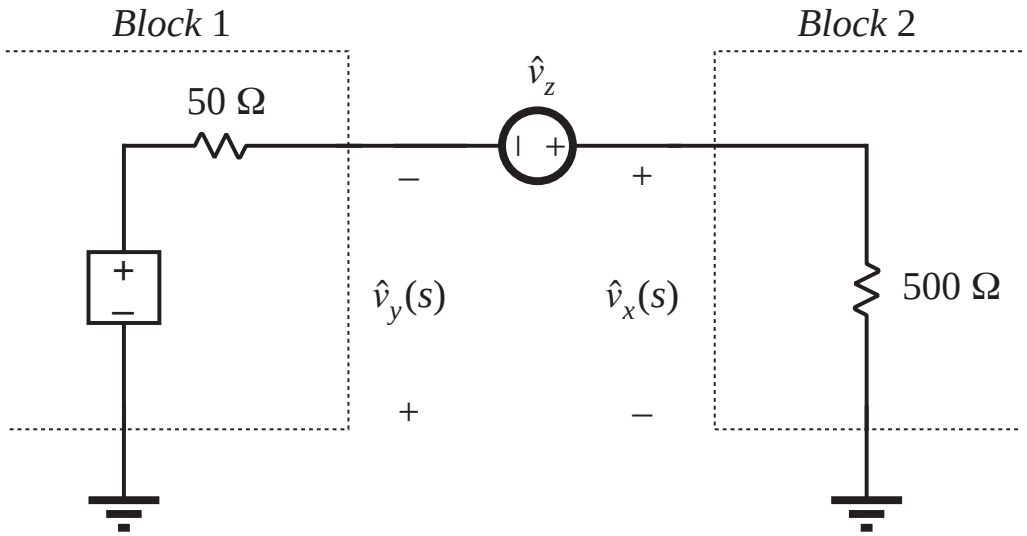
$$T_v(s) = T(s) \left(1 + \frac{Z_1(s)}{Z_2(s)} \right) + \frac{Z_1(s)}{Z_2(s)}$$

Condition for accurate measurement:

$$T_v(s) \approx T(s) \quad \text{provided} \quad (i) \quad \left\| Z_1(s) \right\| << \left\| Z_2(s) \right\|, \quad \text{and}$$

$$(ii) \quad \left\| T(s) \right\| >> \left\| \frac{Z_1(s)}{Z_2(s)} \right\|$$

Example: voltage injection



$$Z_1(s) = 50\Omega$$

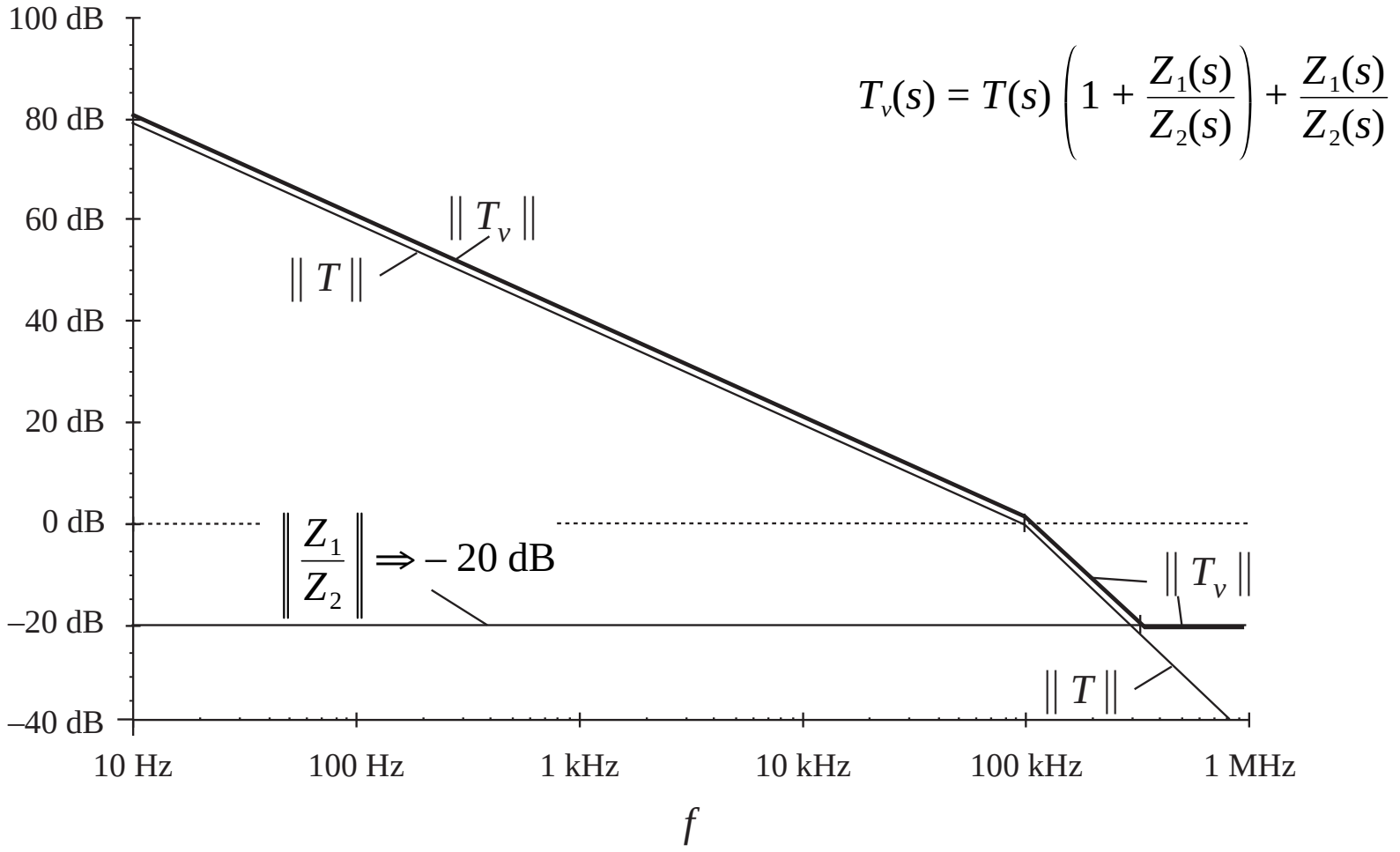
$$Z_2(s) = 500\Omega$$

$$\frac{Z_1(s)}{Z_2(s)} = 0.1 \Rightarrow -20\text{dB}$$

$$\left(1 + \frac{Z_1(s)}{Z_2(s)}\right) = 1.1 \Rightarrow 0.83\text{dB}$$

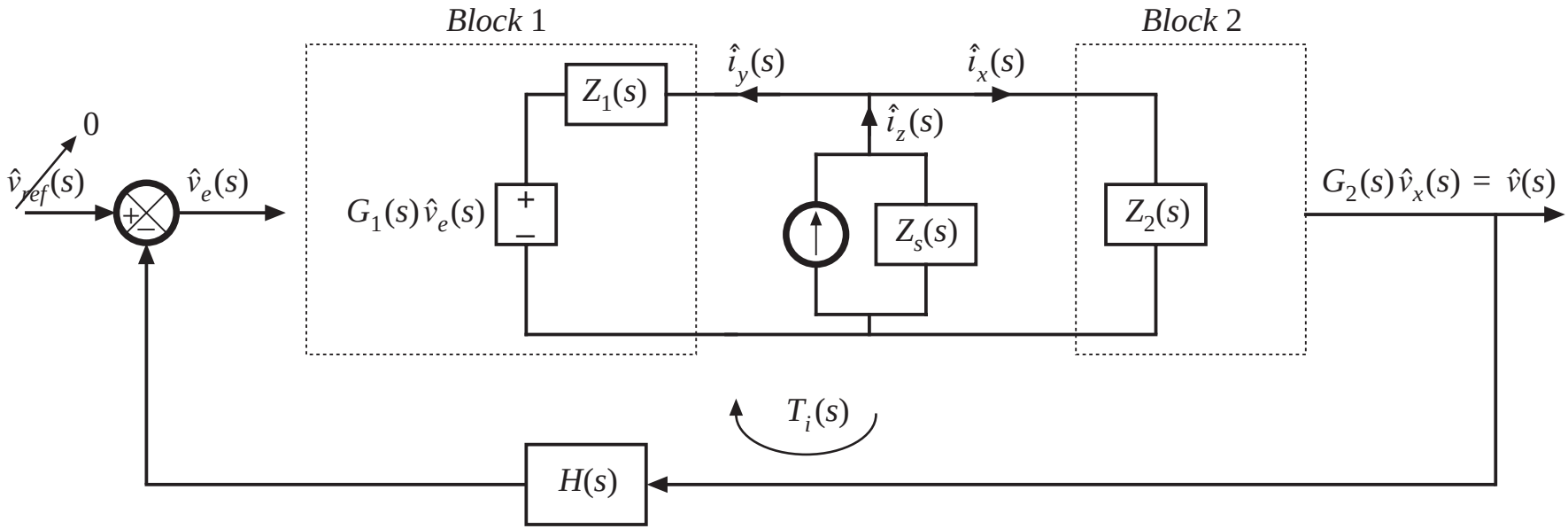
$$\text{suppose actual } T(s) = \frac{10^4}{\left(1 + \frac{s}{2\pi\ 10\text{Hz}}\right)\left(1 + \frac{s}{2\pi\ 100\text{kHz}}\right)}$$

Example: measured $T_v(s)$ and actual $T(s)$



9.6.2. Current injection

$$T_i(s) = \left. \frac{\hat{i}_y(s)}{\hat{i}_x(s)} \right|_{\substack{\hat{v}_{ref} = 0 \\ \hat{v}_g = 0}}$$



Current injection

It can be shown that

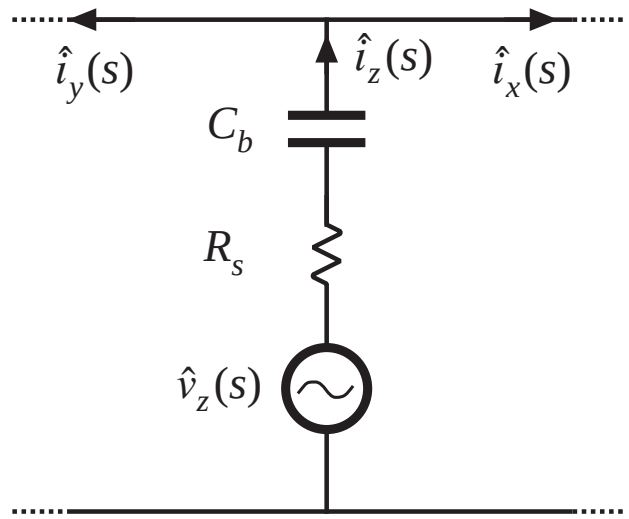
$$T_i(s) = T(s)\left(1 + \frac{Z_2(s)}{Z_1(s)}\right) + \frac{Z_2(s)}{Z_1(s)}$$

Conditions for obtaining accurate measurement:

$$(i) \quad \| Z_2(s) \| << \| Z_1(s) \|, \quad \text{and}$$

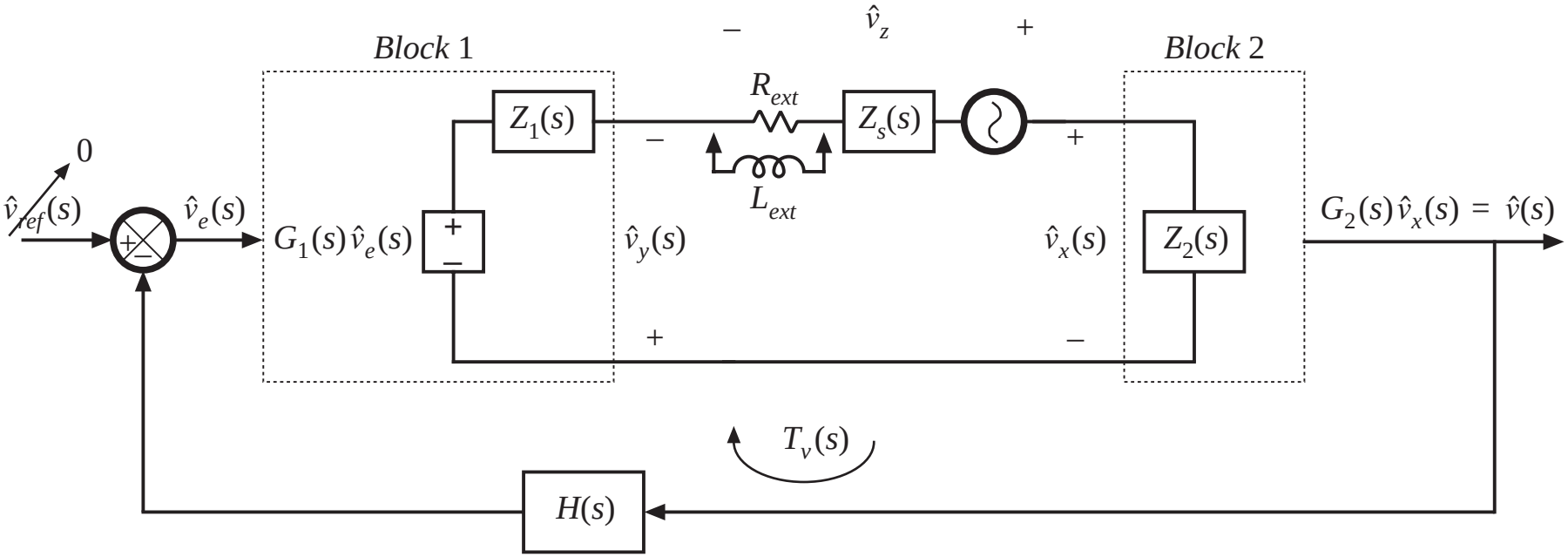
$$(ii) \quad \| T(s) \| >> \left\| \frac{Z_2(s)}{Z_1(s)} \right\|$$

Injection source impedance Z_s is irrelevant. We could inject using a Thevenin-equivalent voltage source:



9.6.3. Measurement of unstable systems

- Injection source impedance Z_s does not affect measurement
- Increasing Z_s reduces loop gain of circuit, tending to stabilize system
- Original (unstable) loop gain is measured (not including Z_s), while circuit operates stably



9.7. Summary of key points

1. Negative feedback causes the system output to closely follow the reference input, according to the gain $1/H(s)$. The influence on the output of disturbances and variation of gains in the forward path is reduced.

2. The loop gain $T(s)$ is equal to the products of the gains in the forward and feedback paths. The loop gain is a measure of how well the feedback system works: a large loop gain leads to better regulation of the output. The crossover frequency f_c is the frequency at which the loop gain T has unity magnitude, and is a measure of the bandwidth of the control system.

Summary of key points

3. The introduction of feedback causes the transfer functions from disturbances to the output to be multiplied by the factor $1/(1+T(s))$. At frequencies where T is large in magnitude (i.e., below the crossover frequency), this factor is approximately equal to $1/T(s)$. Hence, the influence of low-frequency disturbances on the output is reduced by a factor of $1/T(s)$. At frequencies where T is small in magnitude (i.e., above the crossover frequency), the factor is approximately equal to 1. The feedback loop then has no effect. Closed-loop disturbance-to-output transfer functions, such as the line-to-output transfer function or the output impedance, can easily be constructed using the algebra-on-the-graph method.

4. Stability can be assessed using the phase margin test. The phase of T is evaluated at the crossover frequency, and the stability of the important closed-loop quantities $T/(1+T)$ and $1/(1+T)$ is then deduced. Inadequate phase margin leads to ringing and overshoot in the system transient response, and peaking in the closed-loop transfer functions.

Summary of key points

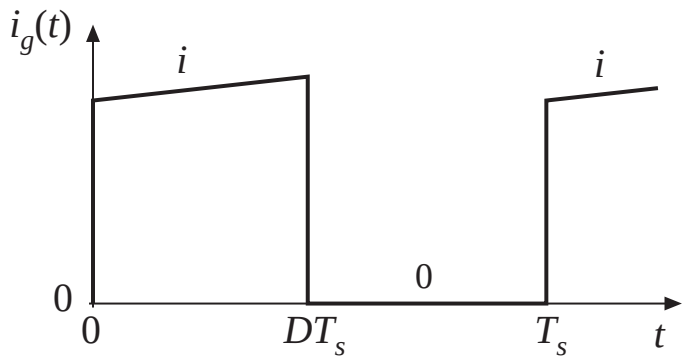
5. Compensators are added in the forward paths of feedback loops to shape the loop gain, such that desired performance is obtained. Lead compensators, or *PD* controllers, are added to improve the phase margin and extend the control system bandwidth. *PI* controllers are used to increase the low-frequency loop gain, to improve the rejection of low-frequency disturbances and reduce the steady-state error.

6. Loop gains can be experimentally measured by use of voltage or current injection. This approach avoids the problem of establishing the correct quiescent operating conditions in the system, a common difficulty in systems having a large dc loop gain. An injection point must be found where interstage loading is not significant. Unstable loop gains can also be measured.

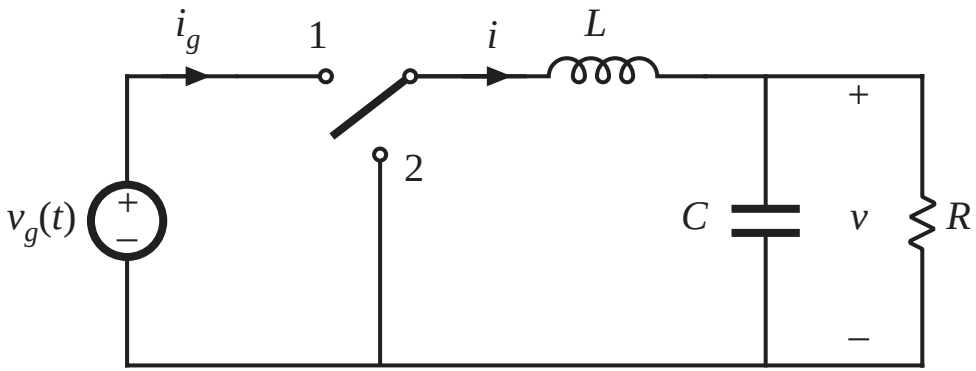
Chapter 10
Input Filter Design

10.1.1 Conducted Electromagnetic Interference (EMI)

Input current $i_g(t)$ is *pulsating*:



Buck converter example

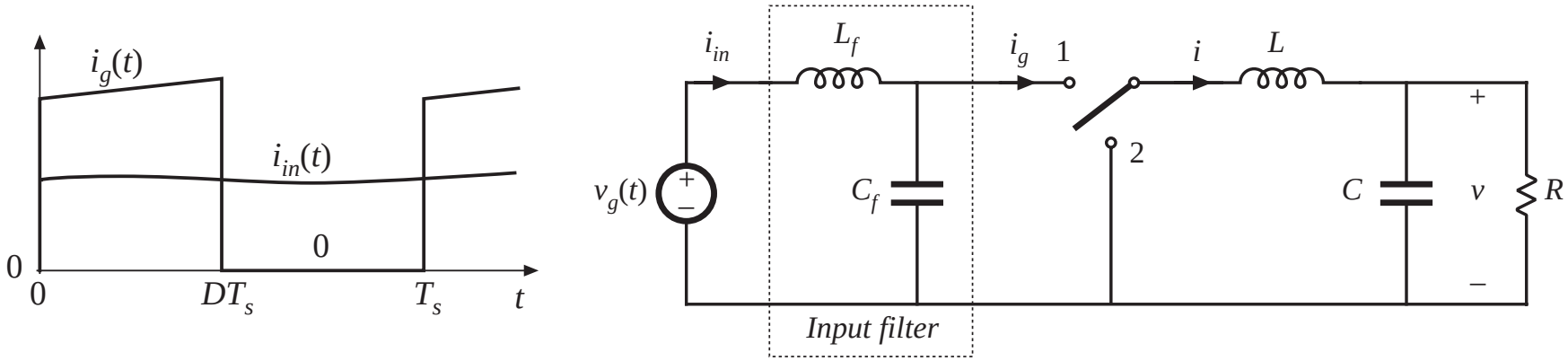


Approximate Fourier series of $i_g(t)$:

$$i_g(t) = DI + \sum_{k=1}^{\infty} \frac{2I}{k\pi} \sin\left(k\pi D\right) \cos\left(k\omega t\right)$$

High frequency current harmonics of substantial amplitude are injected back into $v_g(t)$ source. These harmonics can interfere with operation of nearby equipment. Regulations limit their amplitude, typically to values of 10 μA to 100 μA.

Addition of Low-Pass Filter



Magnitudes and phases of input current harmonics are modified by input filter transfer function $H(s)$:

$$i_{in}(t) = H(0)DI + \sum_{k=1}^{\infty} \| H(kj\omega) \| \frac{2I}{k\pi} \sin\left(k\pi D\right) \cos\left(k\omega t + \angle H(kj\omega)\right)$$

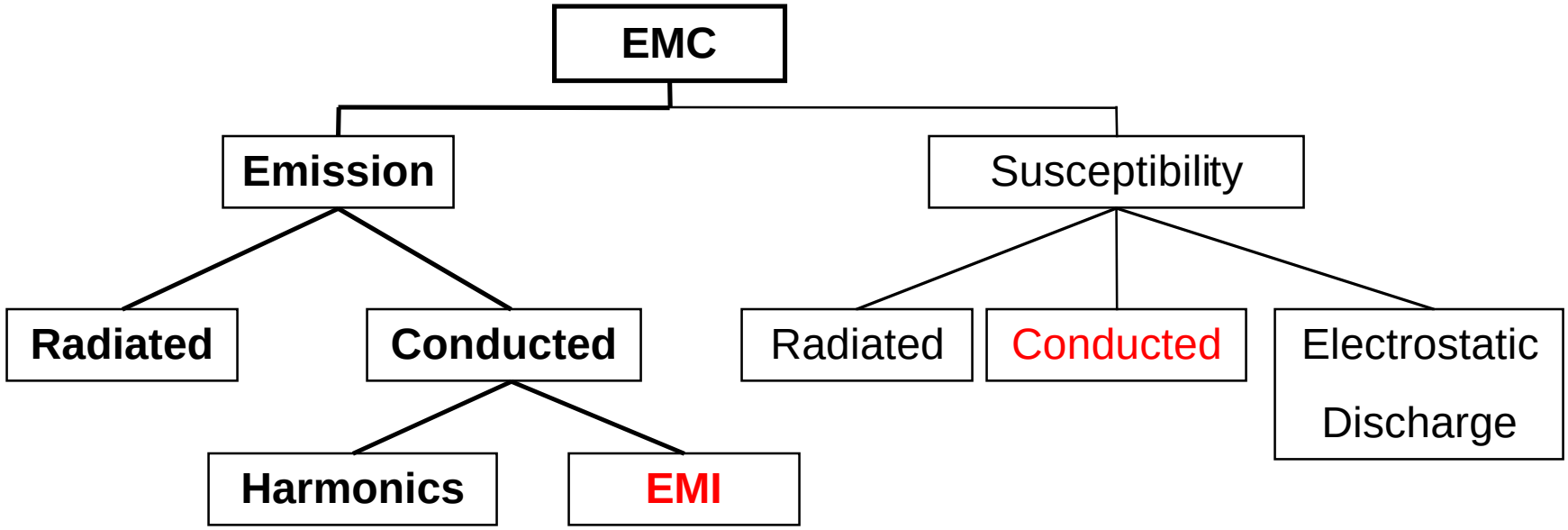
The input filter may be required to attenuate the current harmonics by factors of 80 dB or more.

Electromagnetic Compatibility

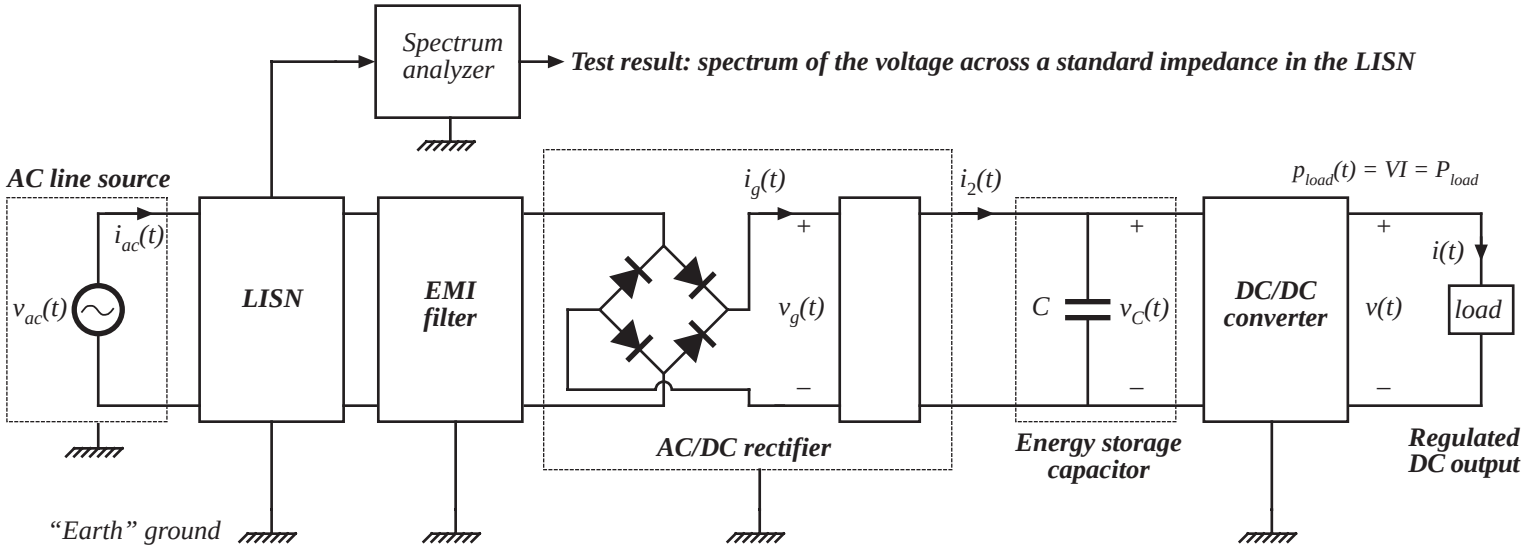
Ability of the device (e.g. power supply) to:

function satisfactorily in its electromagnetic environment (susceptibility or immunity aspect)

without introducing intolerable electromagnetic disturbances (**emission** aspect)



Conducted EMI

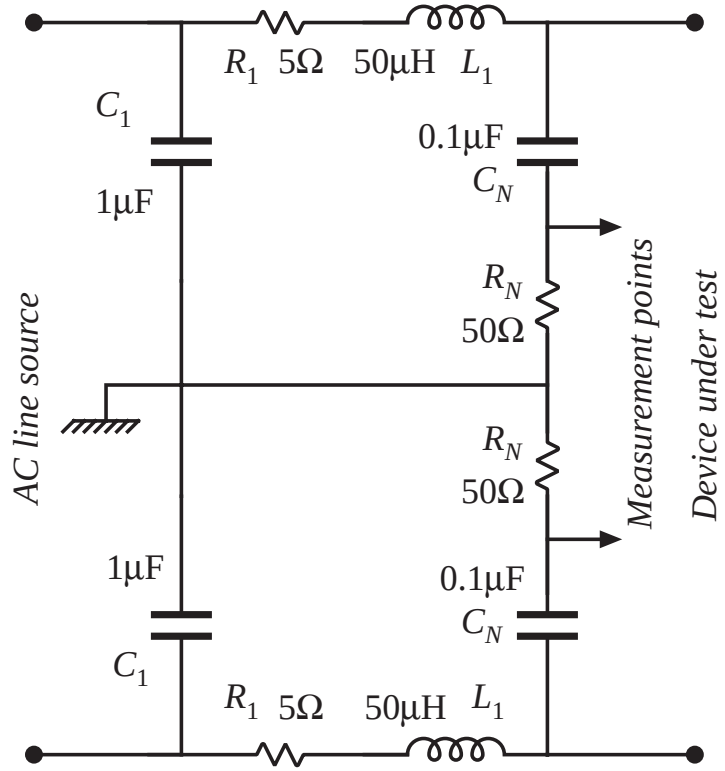


Sample of EMC regulations that include limits on radio-frequency emissions:

European Community Directive on EMC: Euro-Norm EN 55022 or 55081, earlier known as CISPR 22

National standards: VDE (German), FCC (US)

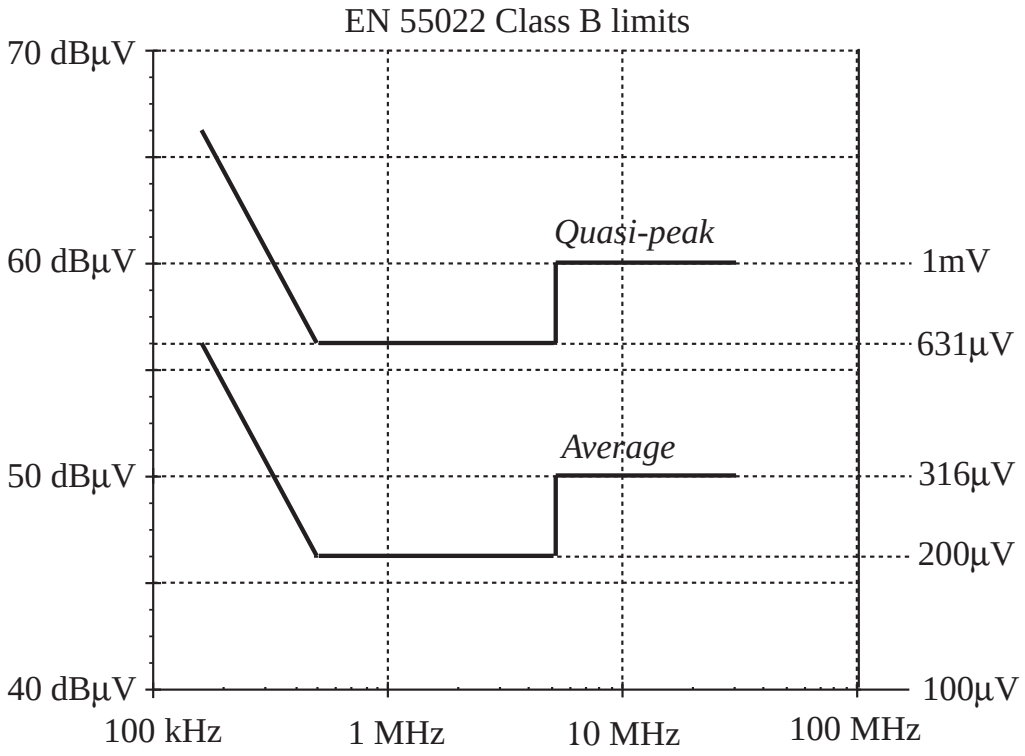
LISN



LISN example

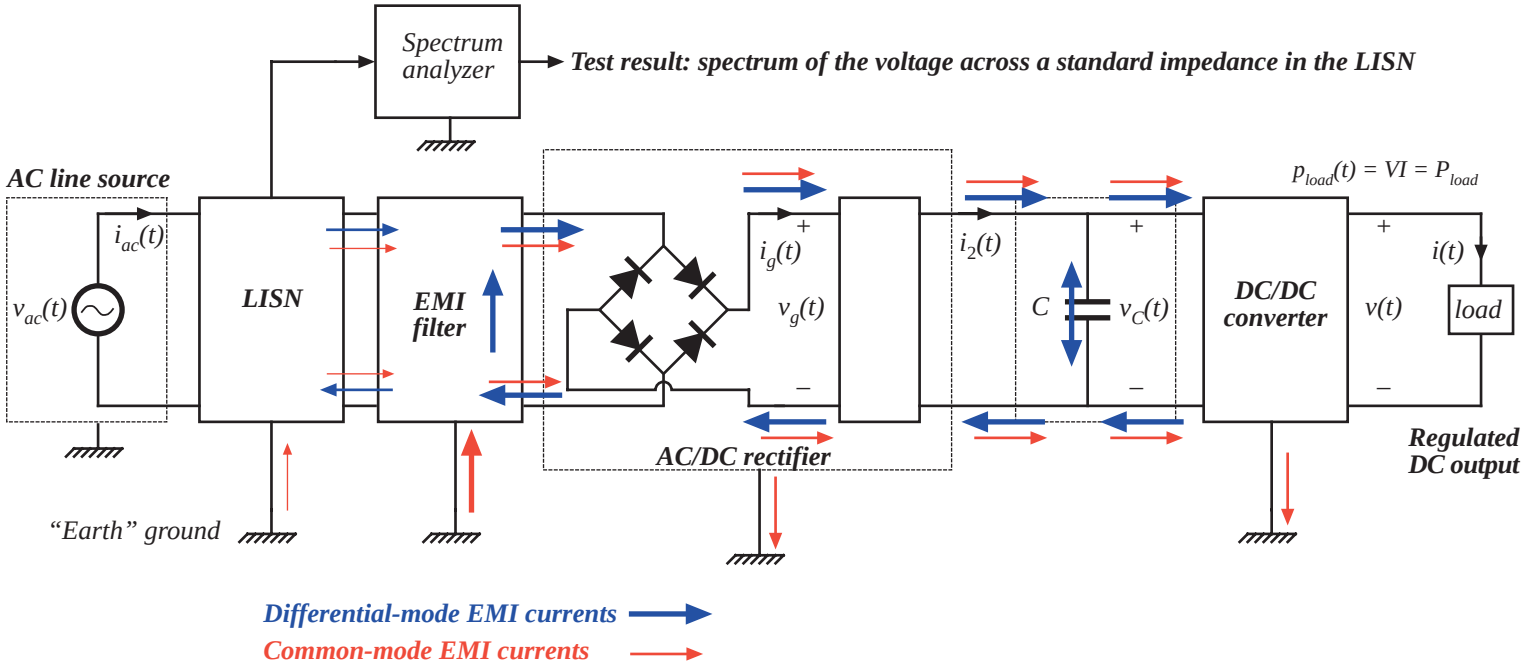
- **LISN:** "Line Impedance Stabilization Network," or "artificial mains network"
- **Purpose:** to standardize impedance of the power source used to supply the device under test
- Spectrum of conducted emissions is measured across the standard impedance (50Ω above 150kHz)

An Example of EMI Limits



- Frequency range: 150kHz-30MHz
- Class B: residential environment
- Quasi-peak/Average: two different setups of the measurement device (such as narrow-band voltmeter or spectrum analyzer)
- Measurement bandwidth: 9kHz

Differential and Common-Mode EMI



- **Differential mode EMI**: input current waveform of the PFC. Differential-mode noise depends on the PFC realization and circuit parameters.
- **Common-mode EMI**: currents through parasitic capacitances between high *dv/dt* points and earth ground (such as from transistor drain to transistor heat sink). Common-mode noise depends on: *dv/dt*, circuit and mechanical layout.

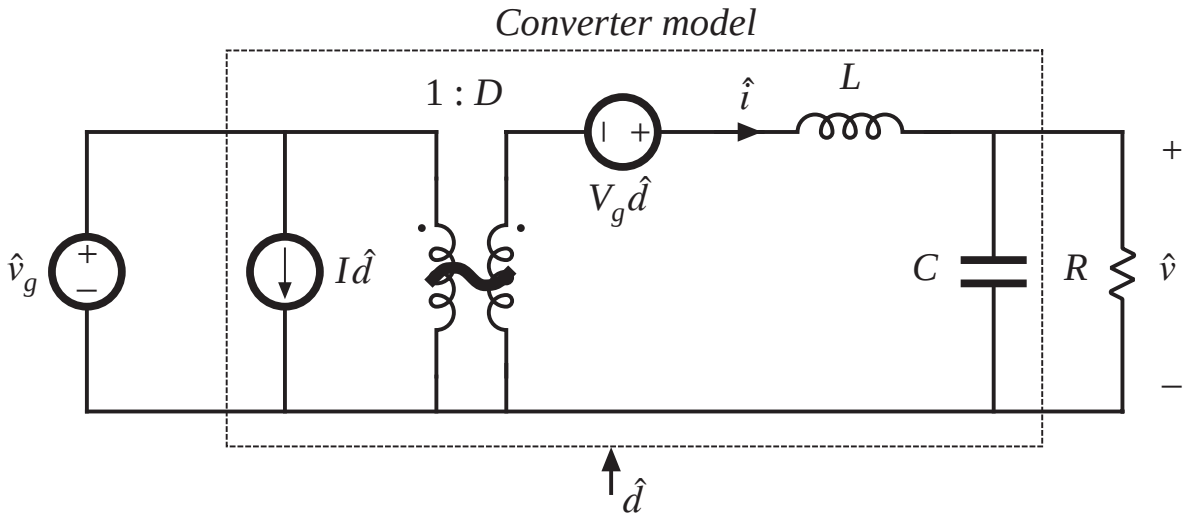
10.1.2 The Input Filter Design Problem

A typical design approach:

1. Engineer designs switching regulator that meets specifications (stability, transient response, output impedance, etc.). In performing this design, a basic converter model is employed, such as the one below:

(no input filter)

(buck converter example)

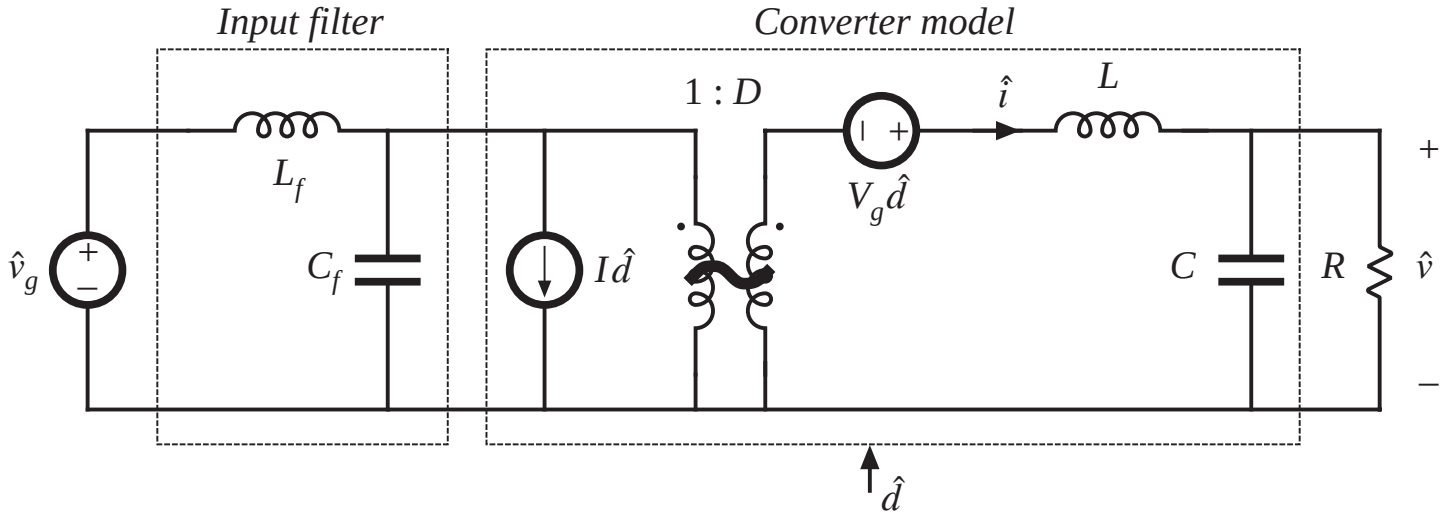


Input Filter Design Problem, p. 2

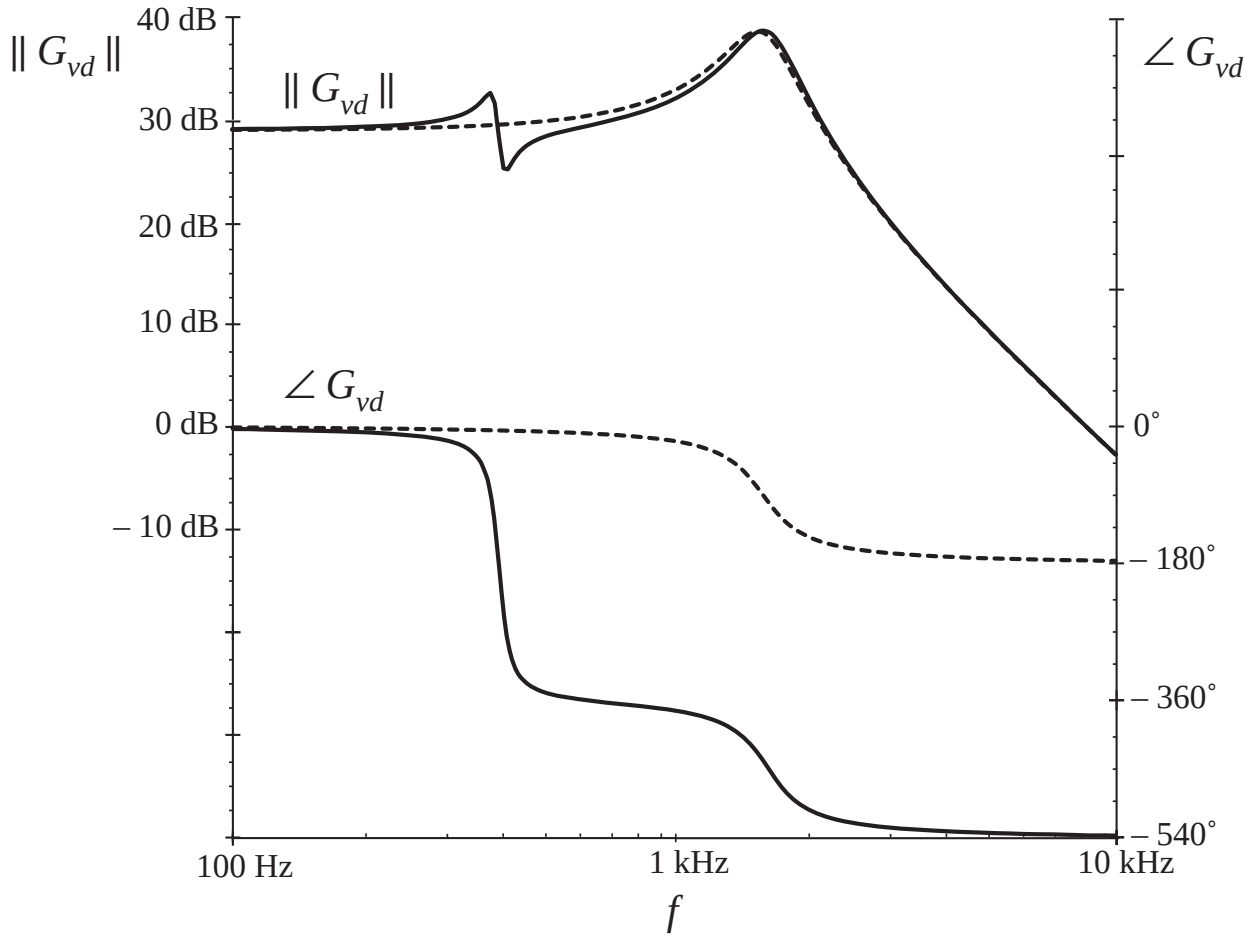
2. Later, the problem of conducted EMI is addressed. An input filter is added, that attenuates harmonics sufficiently to meet regulations.
3. A new problem arises: the controller no longer meets dynamic response specifications. The controller may even become unstable.

Reason: input filter changes converter transfer functions

Converter ac model is modified by input filter



Input Filter Design Problem, p. 3

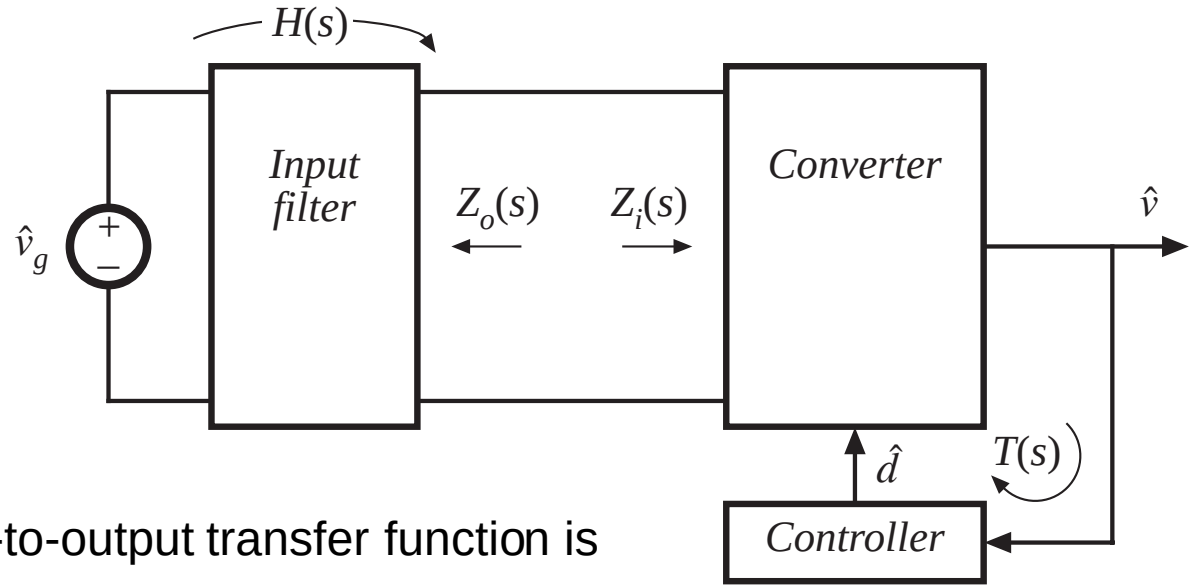


Effect of L-C input filter on control-to-output transfer function $G_{vd}(s)$, buck converter example.

Dashed lines: original magnitude and phase

Solid lines: with addition of input filter

10.2 Effect of an Input Filter on Converter Transfer Functions



Control-to-output transfer function is

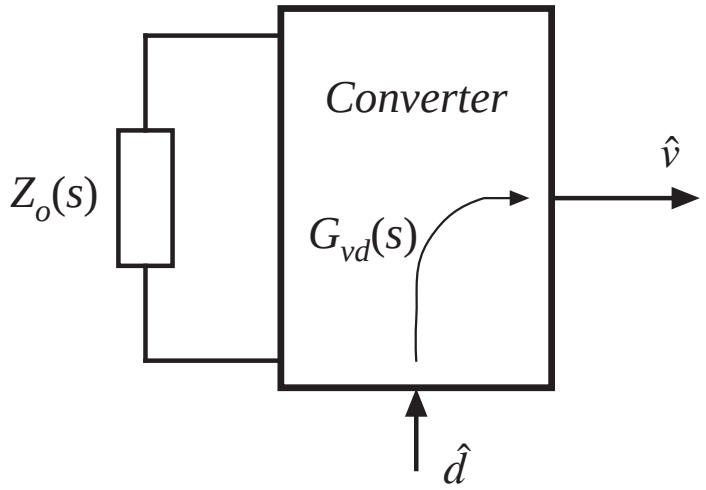
$$G_{vd}(s) = \left. \frac{\hat{v}(s)}{\hat{d}(s)} \right|_{\hat{v}_g(s) = 0}$$

Determination of $G_{vd}(s)$

$$G_{vd}(s) = \left. \frac{\hat{v}(s)}{\hat{d}(s)} \right|_{\hat{v}_g(s) = 0}$$

$\hat{v}_g(s)$ source → short circuit

$Z_o(s)$ = output impedance of input filter



We will use Middlebrook's Extra Element Theorem to show that the input filter modifies $G_{vd}(s)$ as follows:

$$G_{vd}(s) = \left(G_{vd}(s) \Big|_{Z_o(s) = 0} \right) \frac{\left(1 + \frac{Z_o(s)}{Z_N(s)} \right)}{\left(1 + \frac{Z_o(s)}{Z_D(s)} \right)}$$

How an input filter changes $G_{vd}(s)$
Summary of result

$$G_{vd}(s) = \left(G_{vd}(s)\Big|_{Z_o(s)=0} \right) \frac{\left(1 + \frac{Z_o(s)}{Z_N(s)}\right)}{\left(1 + \frac{Z_o(s)}{Z_D(s)}\right)}$$

$G_{vd}(s)\Big|_{Z_o(s)=0}$ is the original transfer function, before addition of input filter

$Z_D(s) = Z_i(s)\Big|_{\hat{d}(s)=0}$ is the converter input impedance, with $\hat{d}$ set to zero

$Z_N(s) = Z_i(s)\Big|_{\hat{v}(s) \xrightarrow[\text{null}]{} 0}$ is the converter input impedance, with the output $\hat{v}$ nulled to zero

(see Appendix C for proof using EET)

Design criteria for basic converters

Table 10.1 Input filter design criteria for basic converters

Converter	$Z_N(s)$	$Z_D(s)$	$Z_e(s)$
Buck	$-\frac{R}{D^2}$	$\frac{R}{D^2}\frac{\left(1+s\frac{L}{R}+s^2LC\right)}{\left(1+sRC\right)}$	$\frac{sL}{D^2}$
Boost	$-D'^2R\left(1-\frac{sL}{D'^2R}\right)$	$D'^2R\frac{\left(1+s\frac{L}{D'^2R}+s^2\frac{LC}{D'^2}\right)}{\left(1+sRC\right)}$	sL
Buck–boost	$-\frac{D'^2R}{D^2}\left(1-\frac{sDL}{D'^2R}\right)$	$\frac{D'^2R}{D^2}\frac{\left(1+s\frac{L}{D'^2R}+s^2\frac{LC}{D'^2}\right)}{\left(1+sRC\right)}$	$\frac{sL}{D^2}$

10.2.2 Impedance Inequalities

$$G_{vd}(s) = \left(G_{vd}(s) \Big|_{Z_o(s) = 0} \right) \frac{\left(1 + \dfrac{Z_o(s)}{Z_N(s)} \right)}{\left(1 + \dfrac{Z_o(s)}{Z_D(s)} \right)}$$

The *correction factor* $\dfrac{\left(1 + \dfrac{Z_o(s)}{Z_N(s)} \right)}{\left(1 + \dfrac{Z_o(s)}{Z_D(s)} \right)}$ shows how the input filter modifies the transfer function $G_{vd}(s)$.

The correction factor has a magnitude of approximately unity provided that the following inequalities are satisfied:

$$\| Z_o \| \ll \| Z_N \|, \quad \text{and}$$
$$\| Z_o \| \ll \| Z_D \|$$

These provide design criteria, which are relatively easy to apply.

Effect of input filter on converter output impedance

A similar analysis leads to the following inequalities, which guarantee that the converter output impedance is not substantially affected by the input filter:

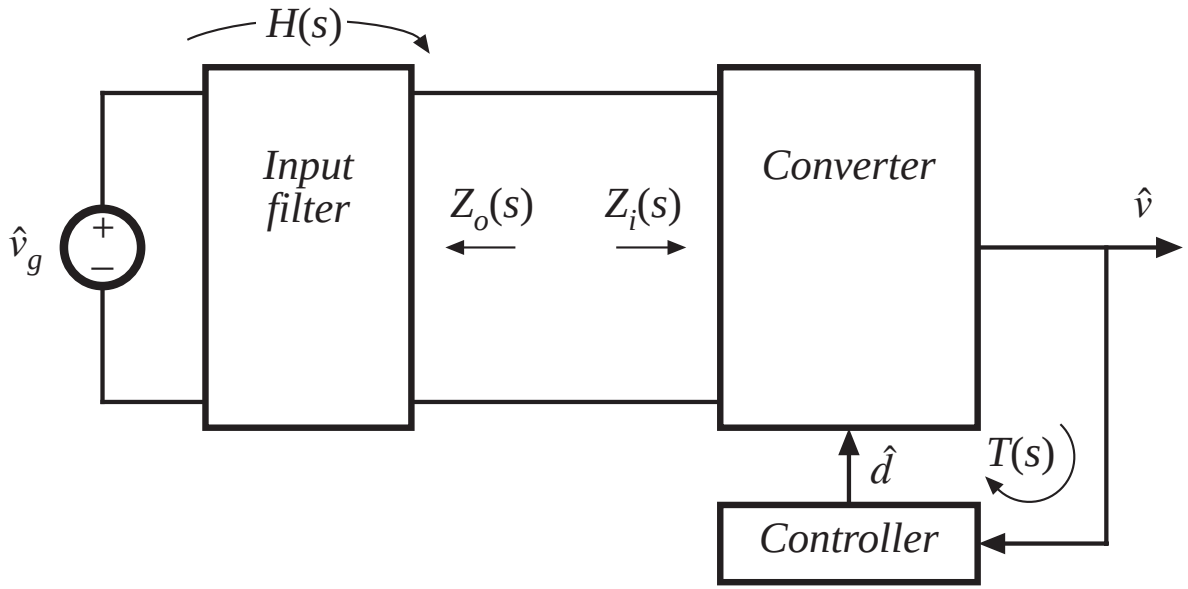
$$\| Z_o \| \ll \| Z_e \|, \quad \text{and}$$
$$\| Z_o \| \ll \| Z_D \|$$

The quantity Z_e is given by:

$$Z_e = Z_i \Big|_{\hat{v} = 0}$$

(converter input impedance when the output is shorted)

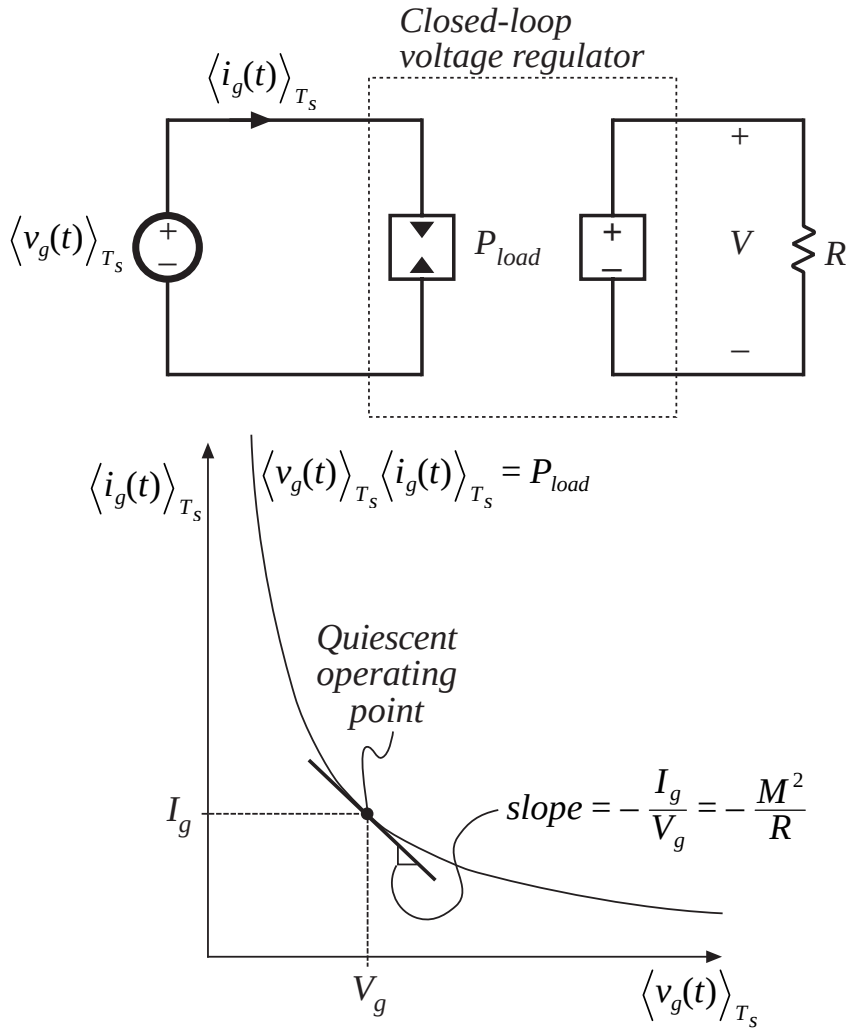
10.2.1 Discussion



$Z_N(s) = Z_i(s)\big|_{\hat{v}(s) \xrightarrow[\text{null}]{} 0}$ is the converter input impedance, with the output $\hat{v}$ nulled to zero

Note that this is the same as the function performed by an ideal controller, which varies the duty cycle as necessary to maintain zero error of the output voltage. So Z_N coincides with the input impedance when an ideal feedback loop perfectly regulates the output voltage.

When the output voltage is perfectly regulated



- For a given load characteristic, the output power P_{load} is independent of the converter input voltage
- If losses are negligible, then the input port *i-v* characteristic is a power sink characteristic, equal to P_{load}:

$$\langle v_g(t) \rangle_{T_s} \langle i_g(t) \rangle_{T_s} = P_{load}$$

- Incremental input resistance is negative, and is equal to:

$$-\frac{R}{M^2}$$

(same as dc asymptote of Z_N)

Negative resistance oscillator

It can be shown that the closed-loop converter input impedance is given by:

$$\frac{1}{Z_i(s)} = \frac{1}{Z_N(s)} \frac{T(s)}{1 + T(s)} + \frac{1}{Z_D(s)} \frac{1}{1 + T(s)}$$

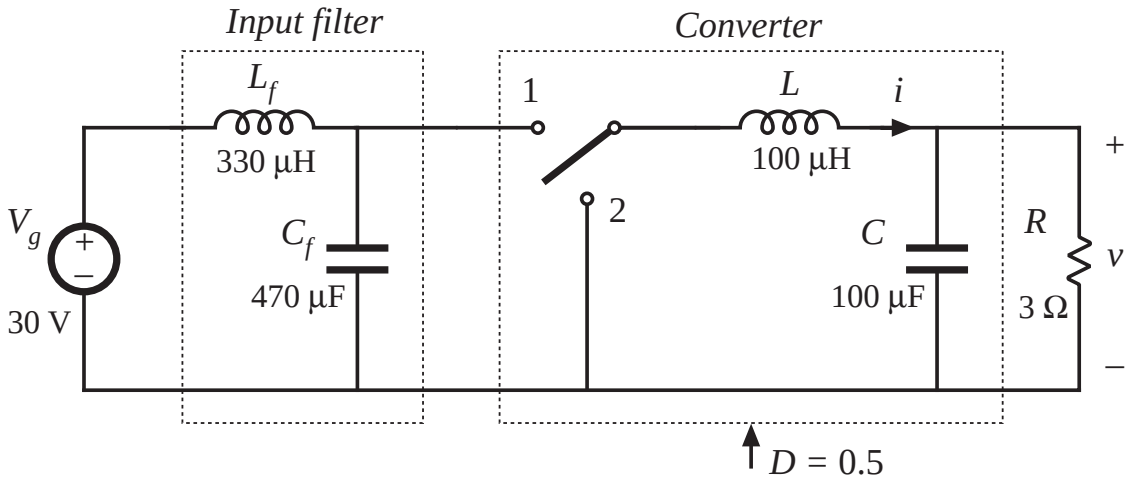
where $T(s)$ is the converter loop gain.

At frequencies below the loop crossover frequency, the input impedance is approximately equal to Z_N, which is a negative resistance.

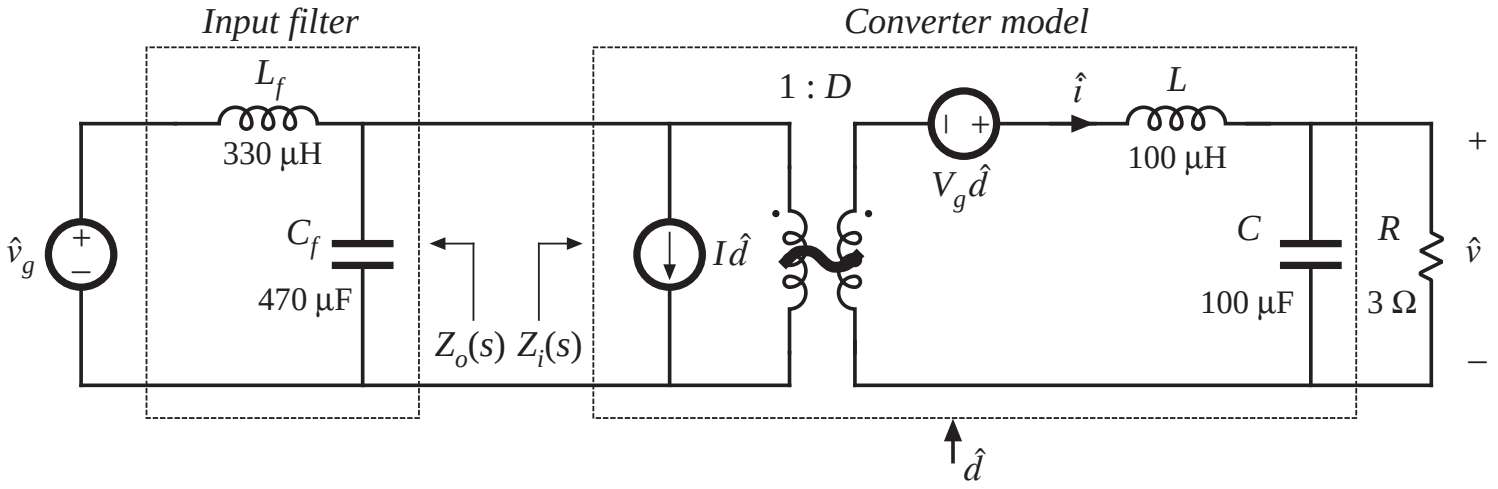
When an undamped or lightly damped input filter is connected to the regulator input port, the input filter can interact with Z_N to form a *negative resistance oscillator*.

10.3 Buck Converter Example
10.3.1 Effect of undamped input filter

Buck converter with input filter

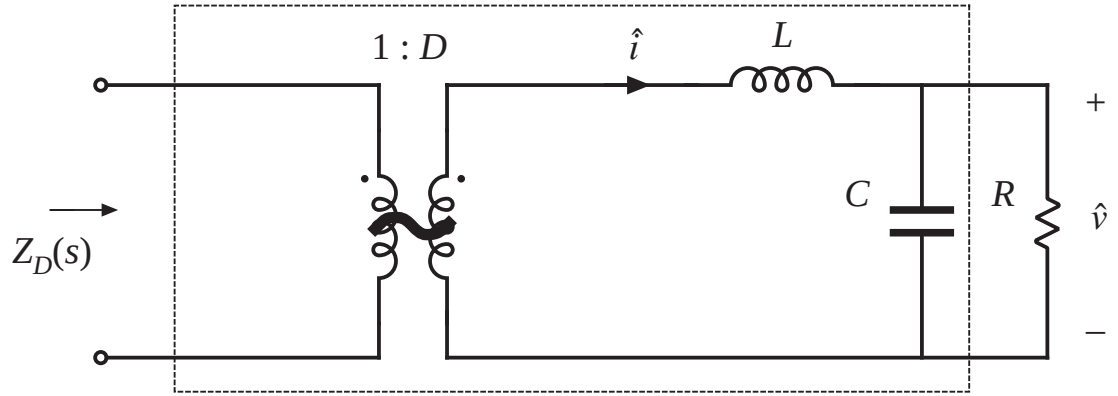


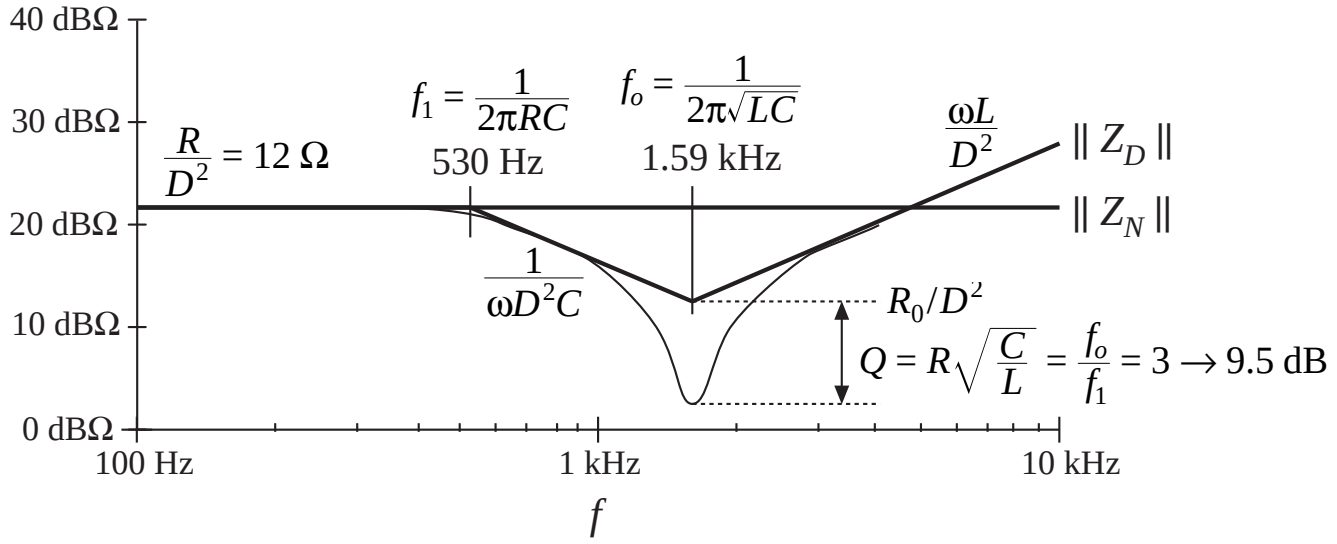
Small-signal model



Determination of Z_D

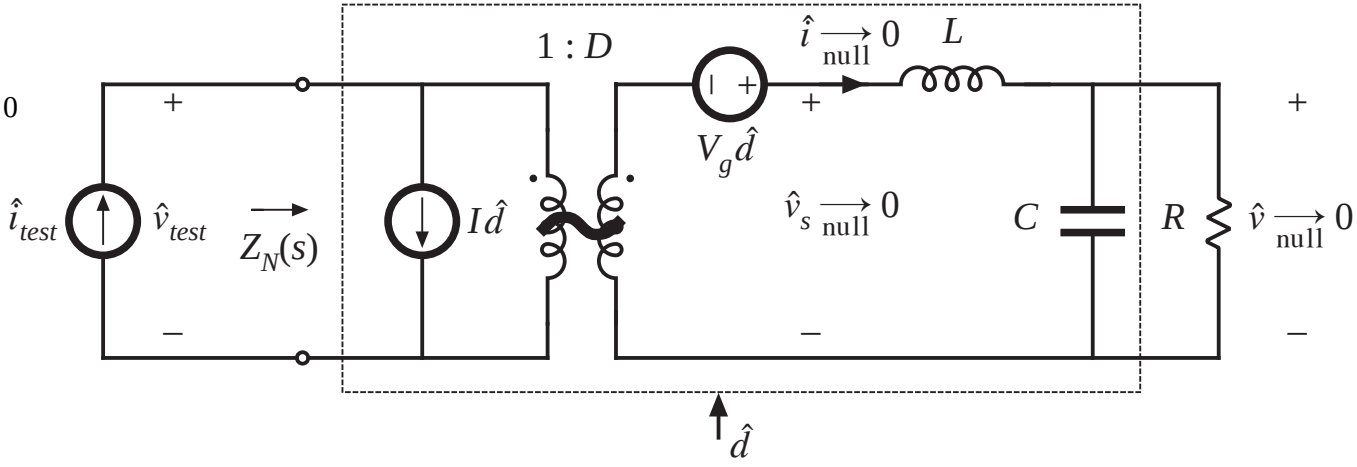
$$Z_D(s) = \frac{1}{D^2}\left(sL + R \| \frac{1}{sC}\right)$$





Determination of Z_N

$$Z_N(s) = \left. \frac{\hat{v}_{test}(s)}{\hat{i}_{test}(s)} \right|_{\hat{v} \xrightarrow[\text{null}]{} 0}$$



Solution:

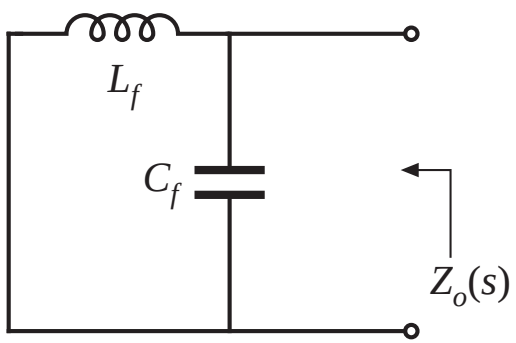
$$\hat{i}_{test}(s) = I\hat{d}(s)$$

$$\hat{v}_{test}(s) = -\frac{V_g\hat{d}(s)}{D}$$

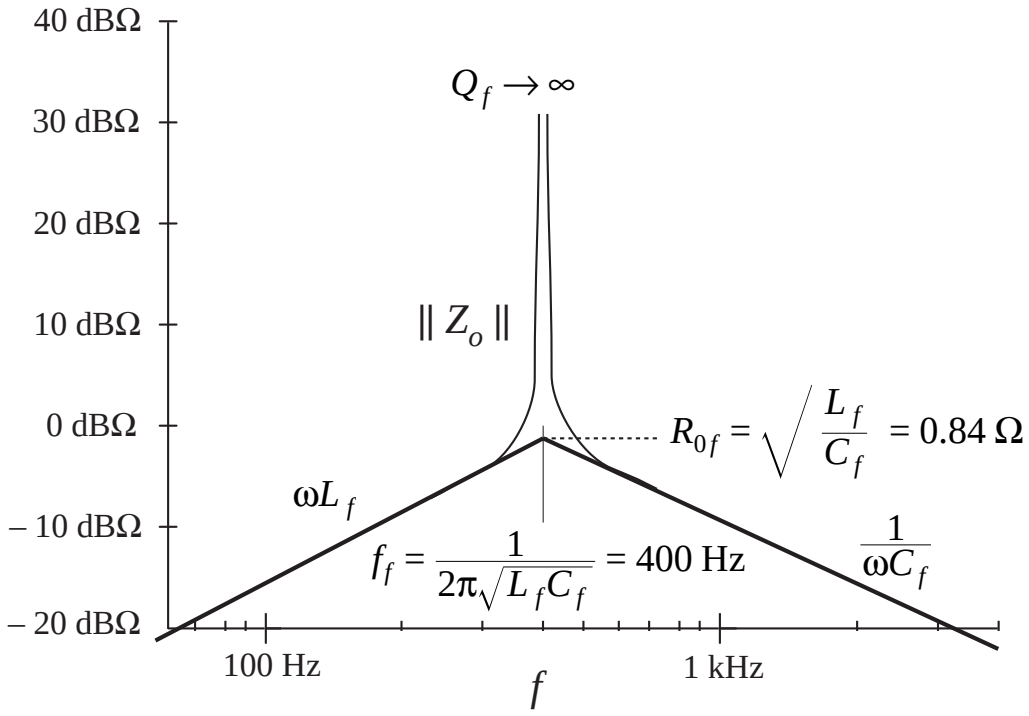
Hence,

$$Z_N(s) = \frac{\left(-\frac{V_g\hat{d}(s)}{D}\right)}{\left(I\hat{d}(s)\right)} = -\frac{R}{D^2}$$

Z_o of undamped input filter



$$Z_o(s) = sL_f \| \frac{1}{sC_f}$$

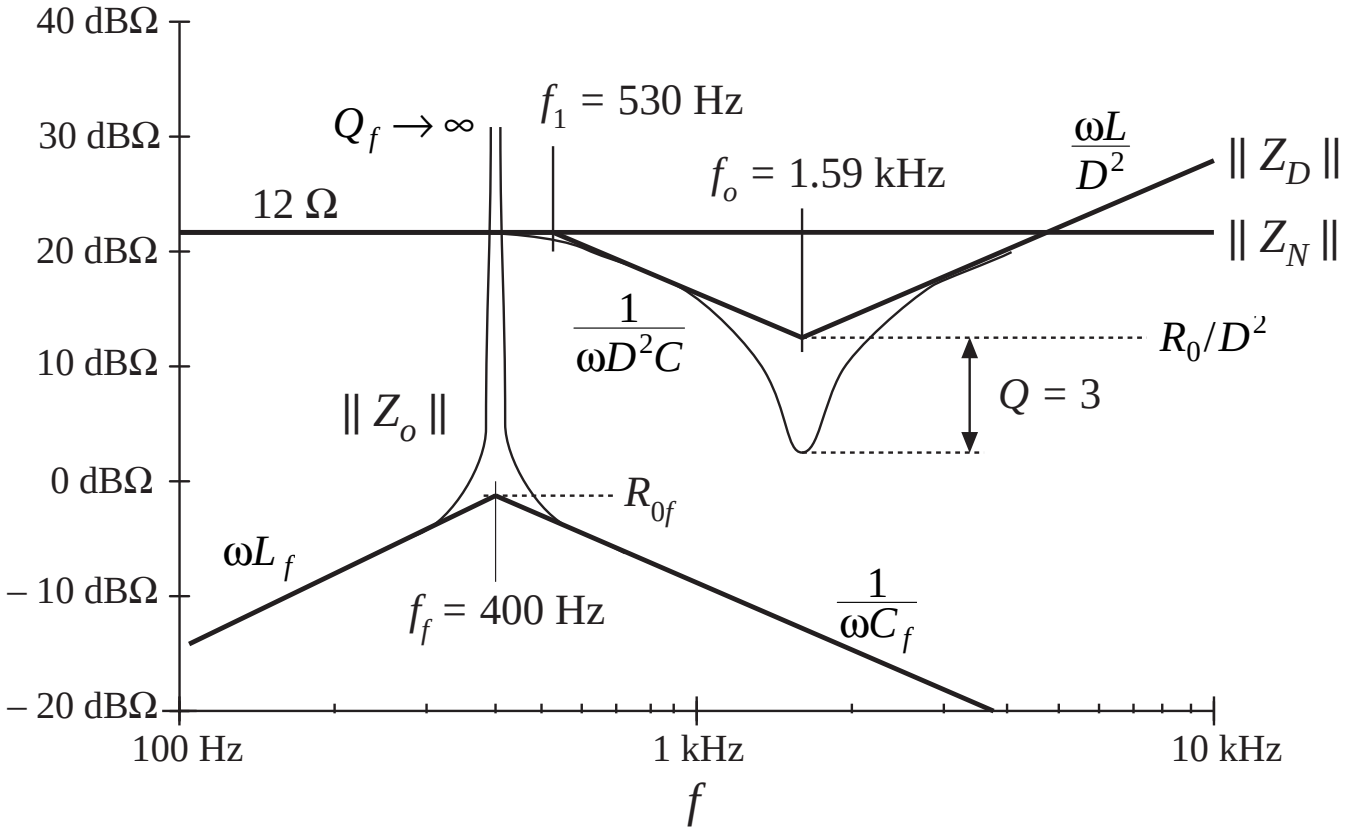


No resistance, hence poles are undamped (infinite Q-factor).

In practice, losses limit Q-factor; nonetheless, Q_f may be very large.

Design criteria

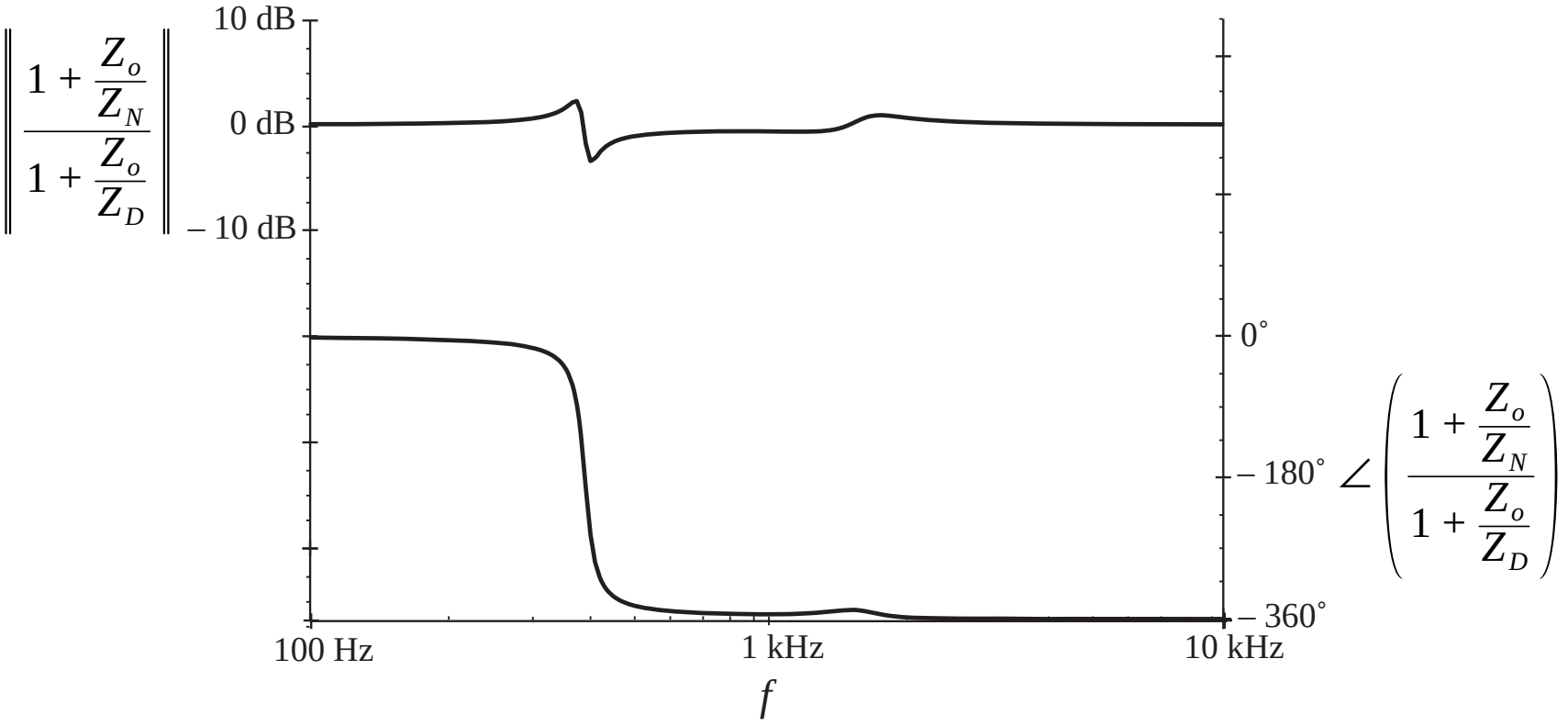
$$\| Z_o \| \ll \| Z_N \|, \quad \text{and}$$
$$\| Z_o \| \ll \| Z_D \|$$



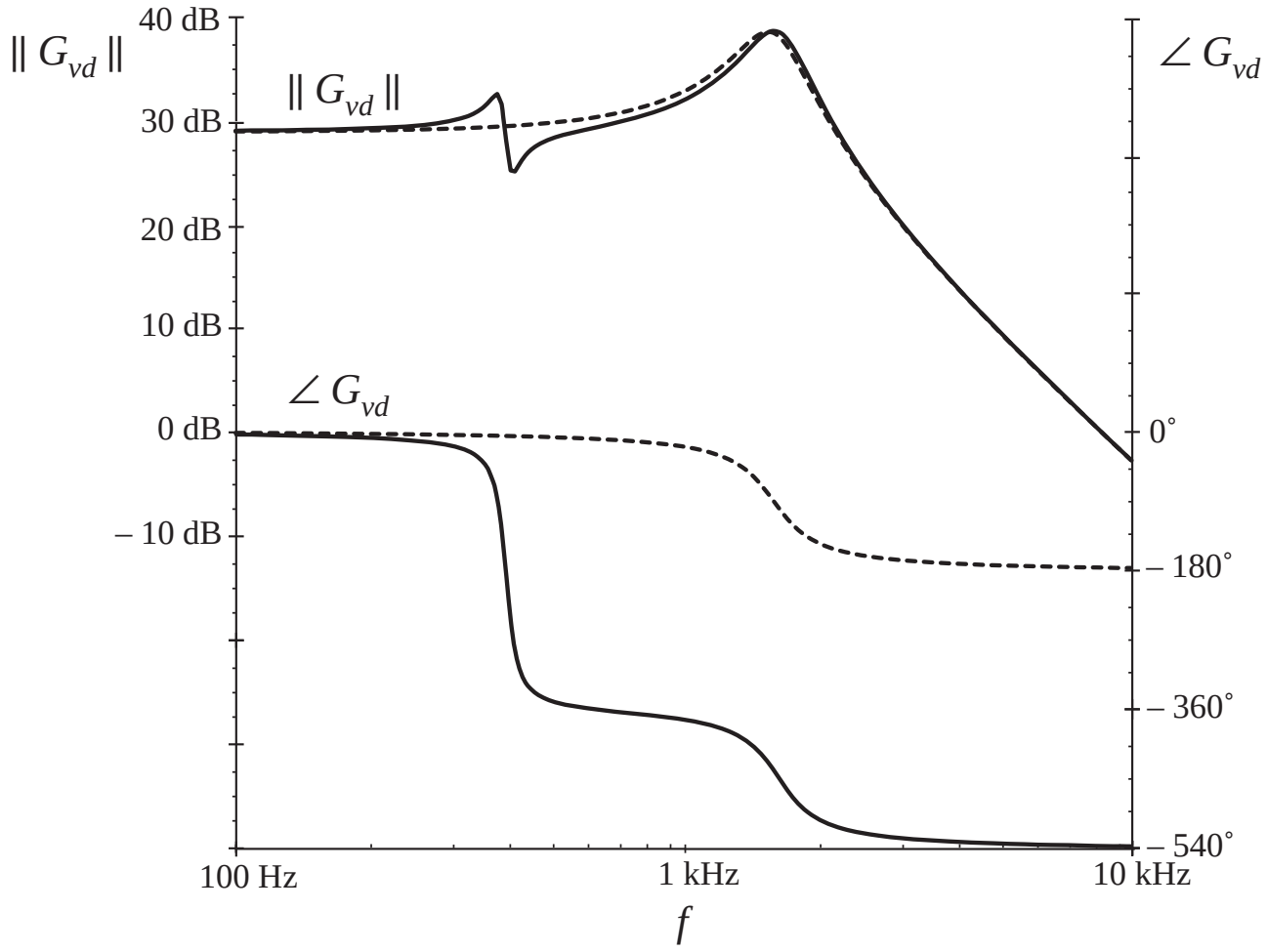
Can meet inequalities everywhere except at resonant frequency f_f.

Need to damp input filter!

Resulting correction factor



Resulting transfer function

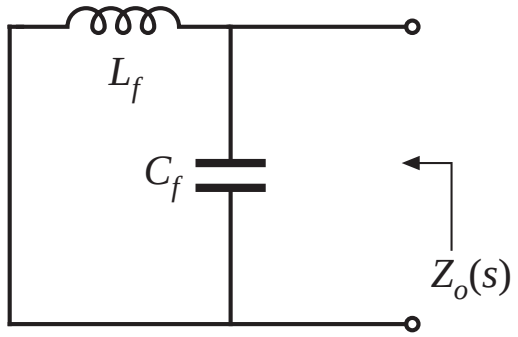


Dashed lines: no input filter

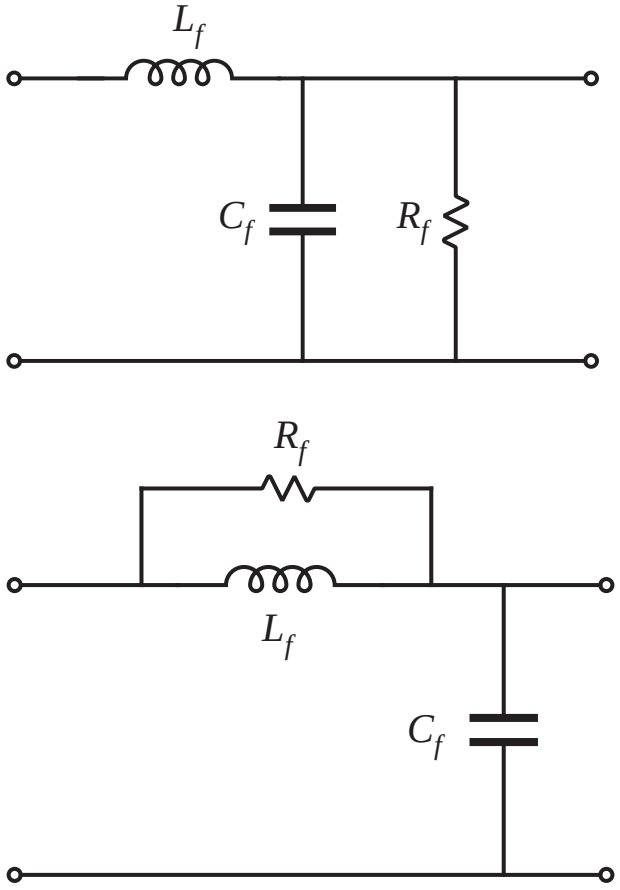
Solid lines: including effect of input filter

10.3.2 Damping the input filter

Undamped filter:



Two possible approaches:

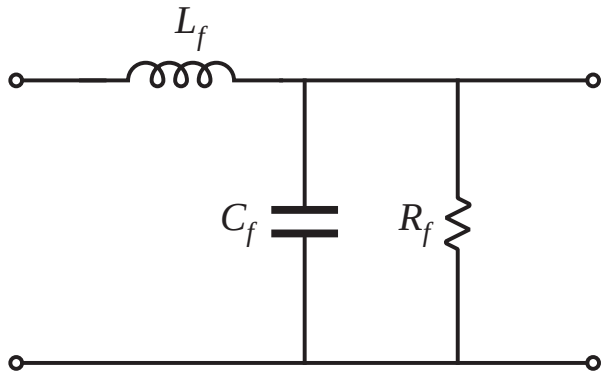


Addition of R_f across C_f

To meet the requirement $R_f \ll \| Z_N \|$:

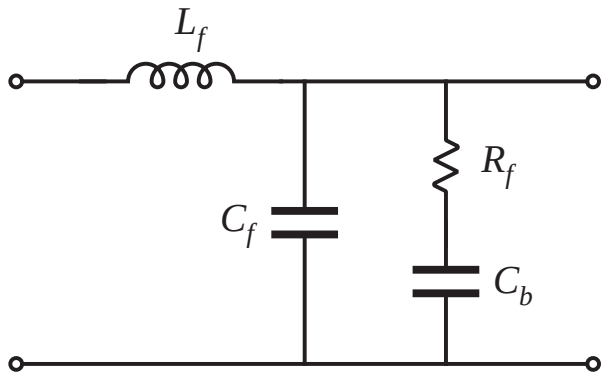
$$R_f \ll \frac{R}{D^2}$$

The power loss in R_f is V_g^2 / R_f, which is larger than the load power!

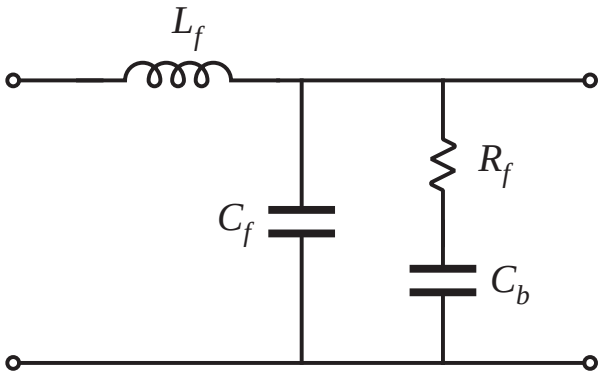


A solution: add dc blocking capacitor C_b.

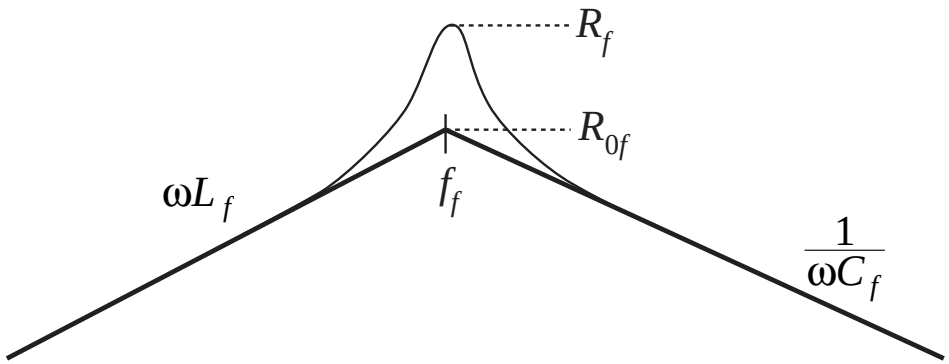
Choose C_b so that its impedance is sufficiently smaller than R_f at the filter resonant frequency.



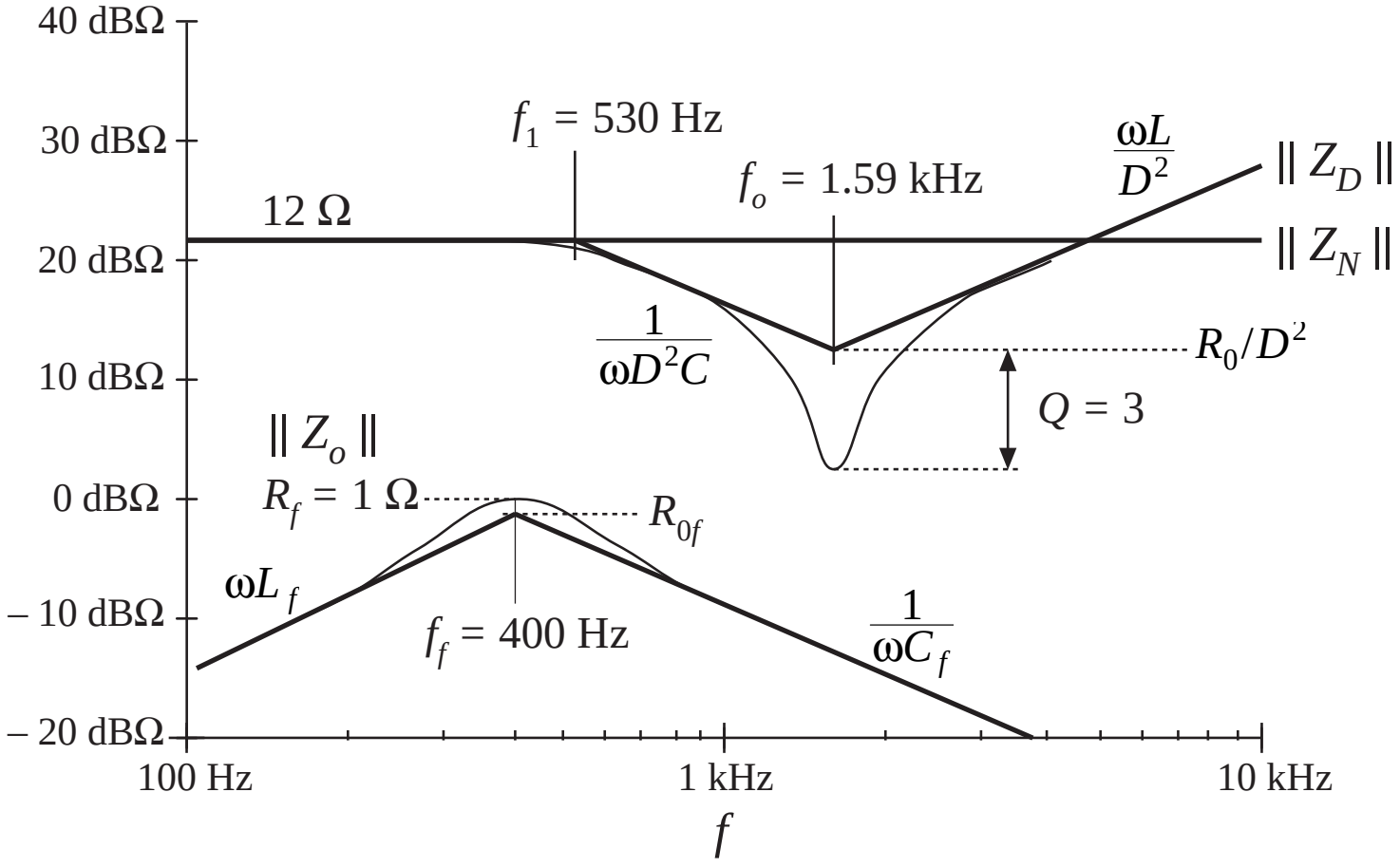
Damped input filter



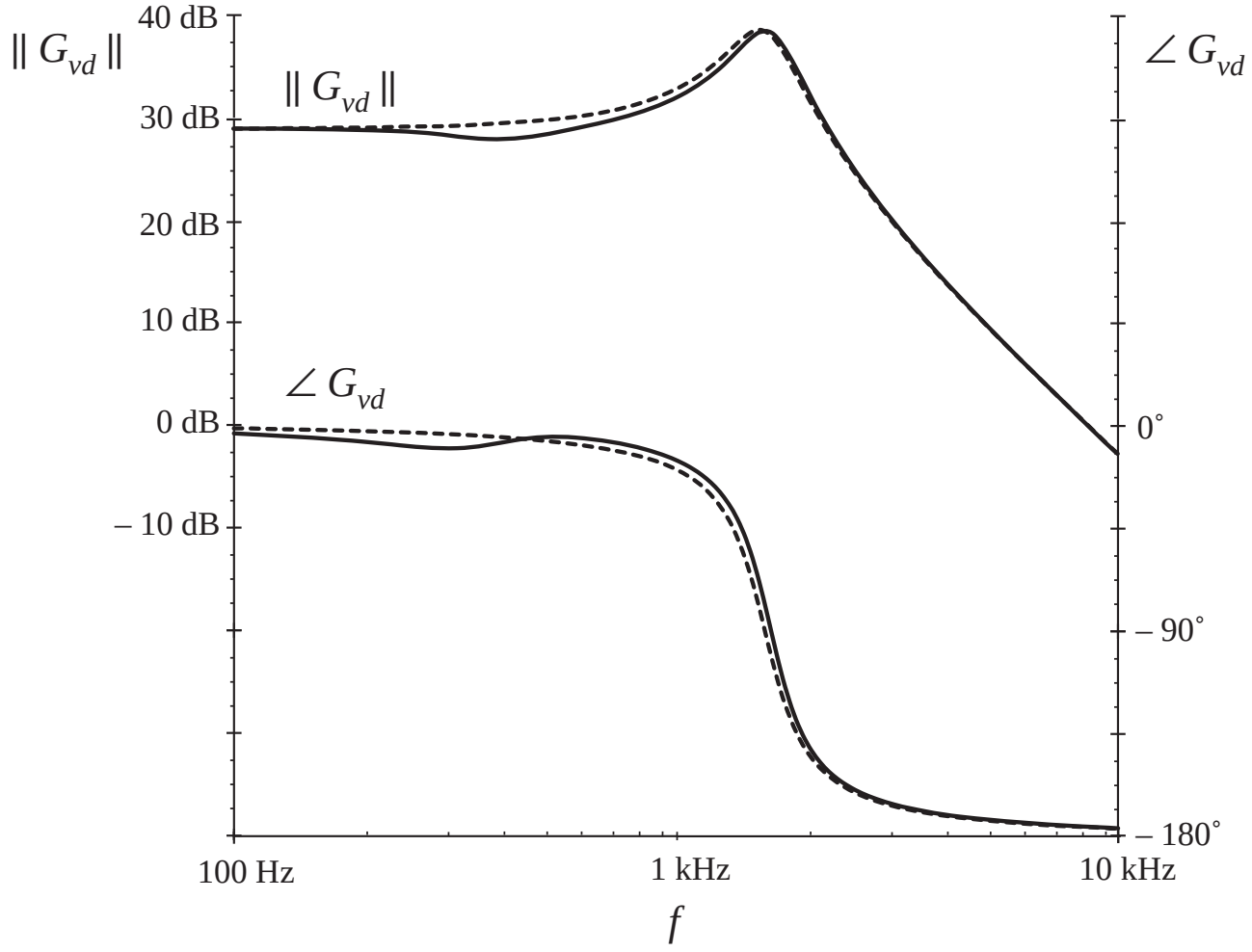
$\| Z_o \|$, with large C_b



Design criteria, with damped input filter



Resulting transfer function

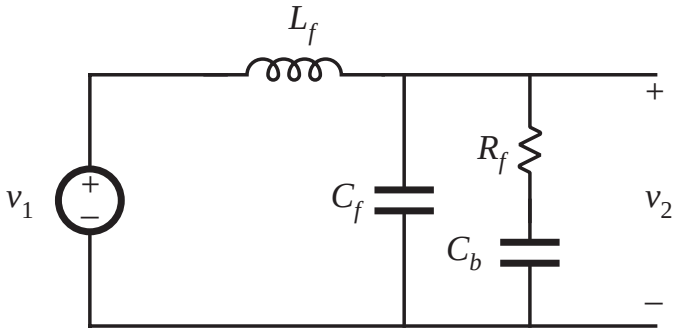


Dashed lines: no input filter

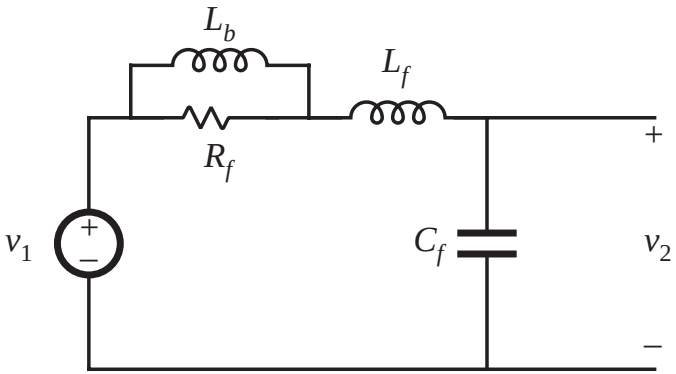
Solid lines: including effect of input filter

10.4 Design of a Damped Input Filter

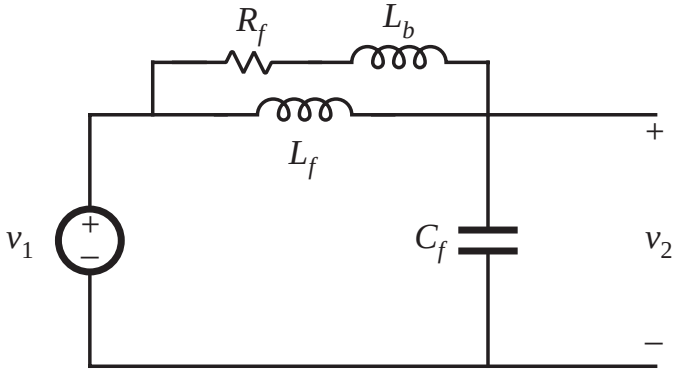
R_f–C_b Parallel Damping



R_f–L_b Series Damping

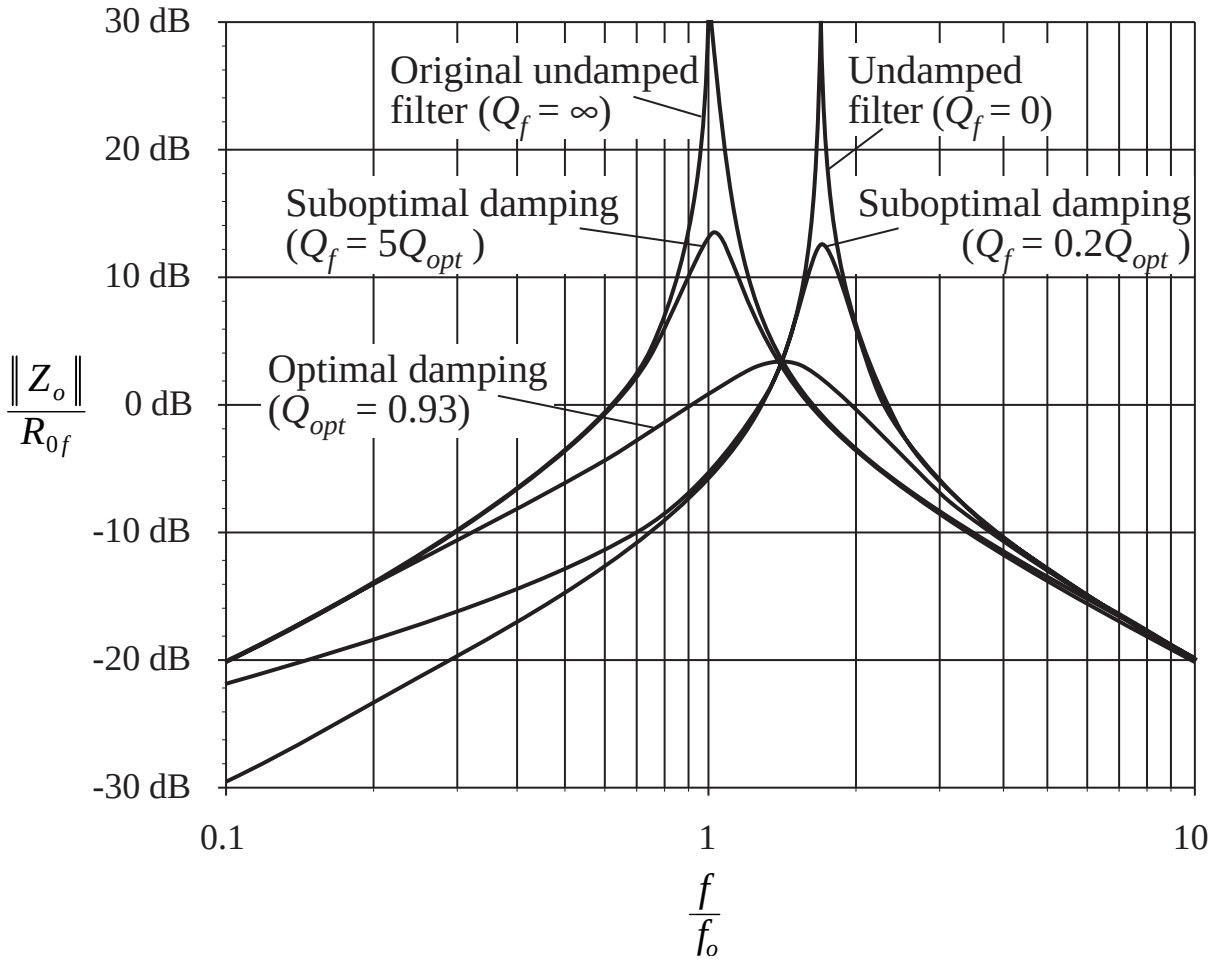


R_f–L_b Parallel Damping



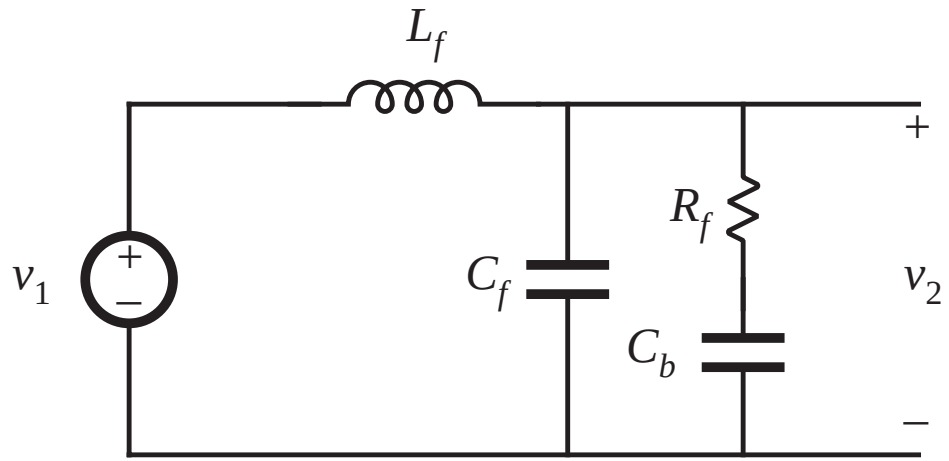
- Size of C_b or L_b can become very large
- Need to optimize design

Dependence of $\| Z_o \|$ on R_f
R_f–L_b Parallel Damping



For this example, $n = L_b/L = 0.516$

10.4.1 R_f–C_b Parallel Damping



- Filter is damped by R_f
- C_b blocks dc current from flowing through R_f
- C_b can be large in value, and is an element to be optimized

Optimal design equations
R_f–C_b Parallel Damping

Define $n = \dfrac{C_b}{C_f}$

The value of the peak output impedance for the optimum design is

$$\| Z_o \|_{\text{mm}} = R_{0f} \frac{\sqrt{2\left(2+n\right)}}{n}$$

where R_{0f} = characteristic impedance of original undamped input filter

Given a desired value of the peak output impedance, can solve above equation for n. The required value of damping resistance R_f can then be found from:

$$Q_{opt} = \frac{R_f}{R_{0f}} = \sqrt{\frac{\left(2+n\right)\left(4+3n\right)}{2n^2\left(4+n\right)}}$$

The peak occurs at the frequency

$$f_m = f_f \sqrt{\frac{2}{2+n}}$$

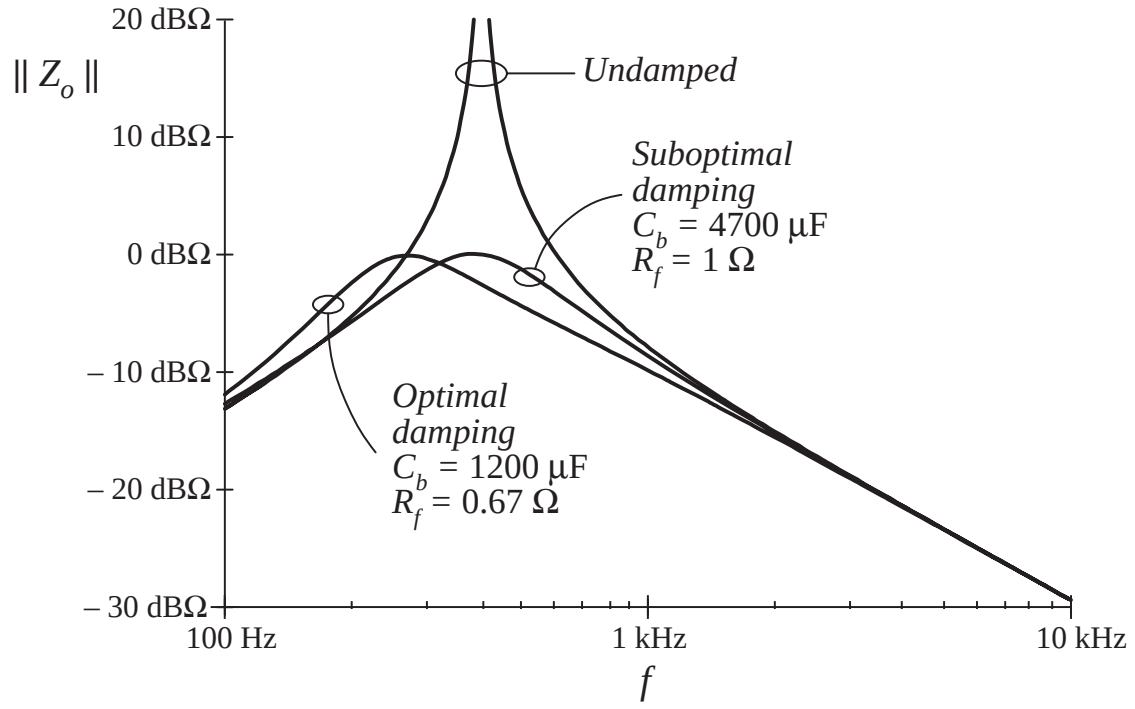
Example
Buck converter of Section 10.3.2

$$n = \frac{R_{0f}^2}{\left\| Z_o \right\|_{\text{mm}}^2} \left(1 + \sqrt{1 + 4 \frac{\left\| Z_o \right\|_{\text{mm}}^2}{R_{0f}^2}} \right) = 2.5$$

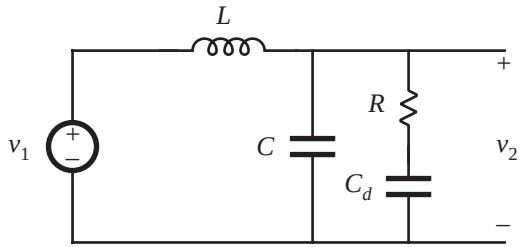
$$R_f = R_{0f} \sqrt{\frac{(2+n)(4+3n)}{2n^2(4+n)}} = 0.67\ \Omega$$

Comparison of designs

Optimal damping achieves same peak output impedance, with much smaller C_b.



Summary
Optimal R-C_d damping



Basic results

$$Q_{opt} = \frac{R}{R_0} = \sqrt{\frac{\left(2+n\right)\left(4+3n\right)}{2n^2\left(4+n\right)}}$$

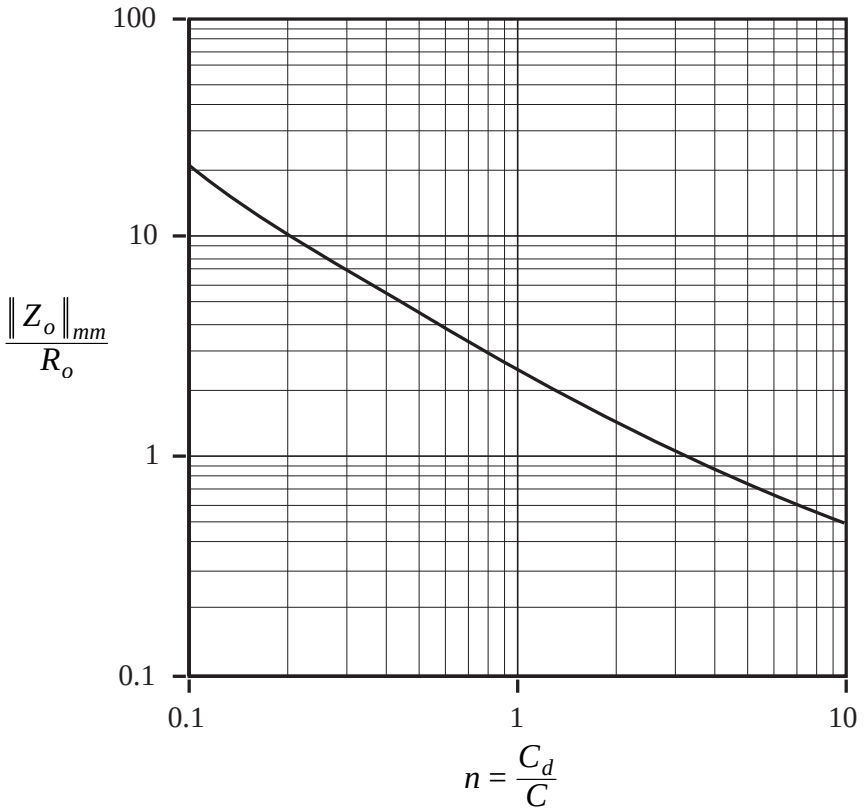
$$\frac{\left\| Z \right\|_{mm}}{R_0} = \frac{\sqrt{2\left(2+n\right)}}{n}$$

with

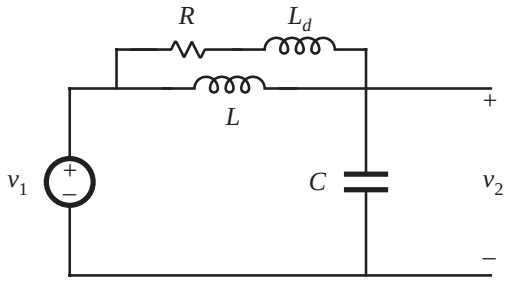
$$n = \frac{C_d}{C}$$

$$R_0 = \sqrt{\frac{L}{C}}$$

- Does not degrade HF attenuation
- No limit on $\| Z \|_{mm}$
- C_d is typically larger than C



Optimal R-L_d damping



Basic results

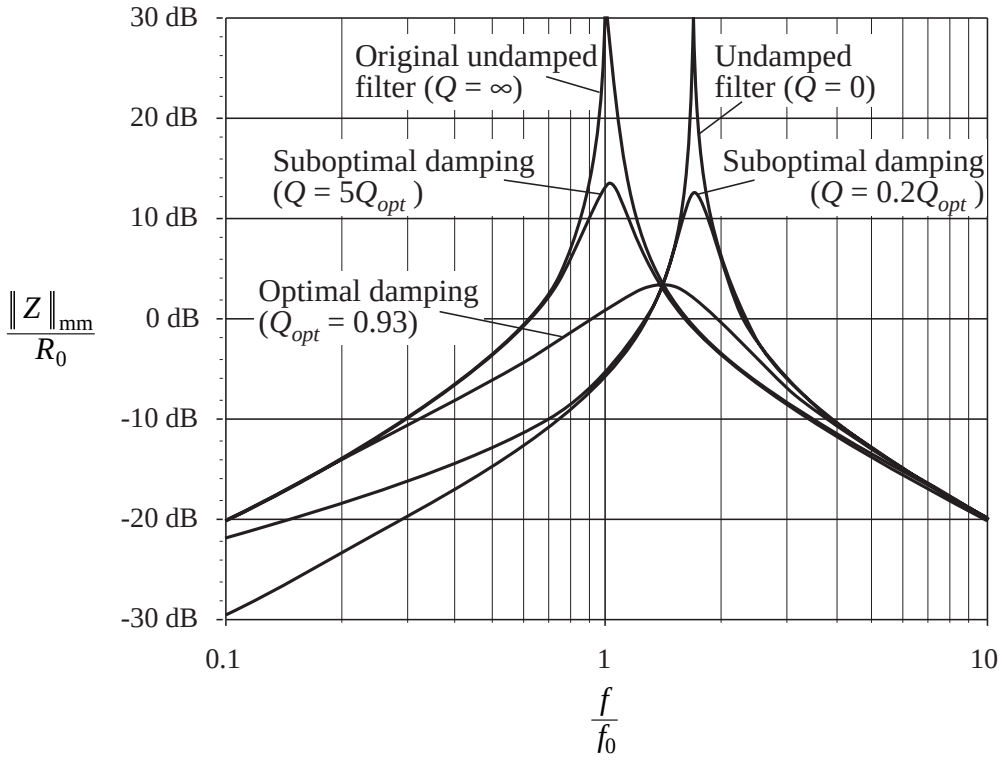
$$Q_{opt} = \sqrt{\frac{n\left(3+4n\right)\left(1+2n\right)}{2\left(1+4n\right)}}$$

$$\frac{\left\| Z \right\|_{mm}}{R_0} = \sqrt{2n\left(1+2n\right)}$$

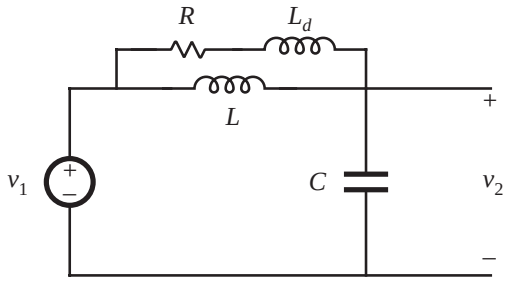
with

$$Q_{opt} = \frac{optimum\ value\ of\ R}{R_0}$$

$$n = \frac{L_d}{L} \qquad R_0 = \sqrt{\frac{L}{C}}$$



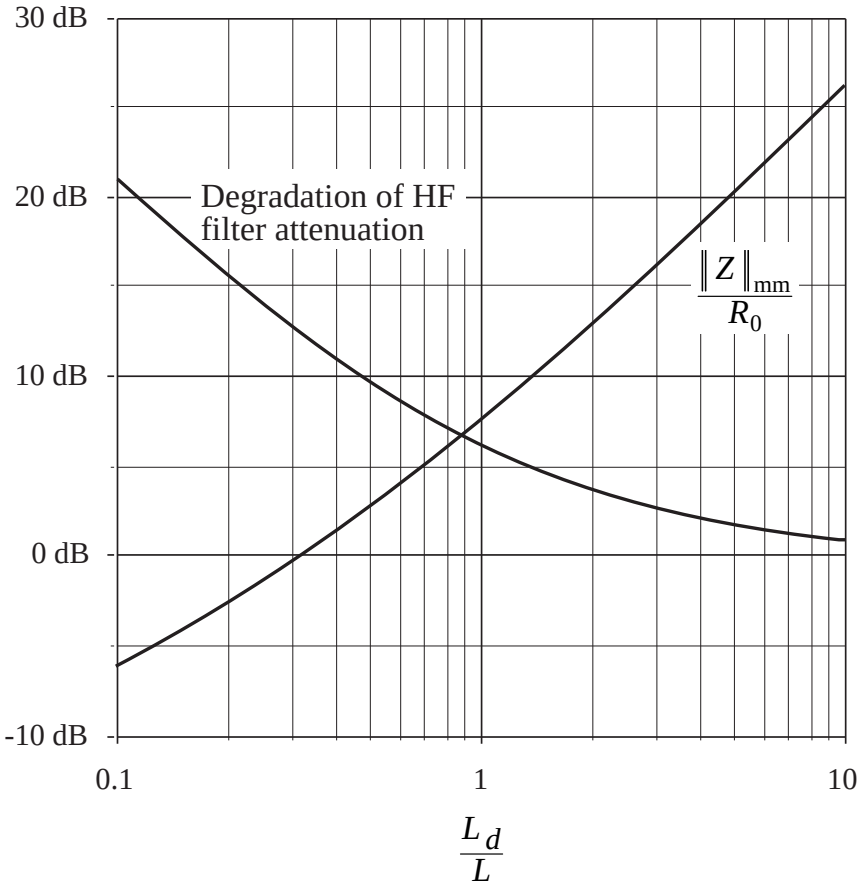
Discussion: Optimal R-L_d damping



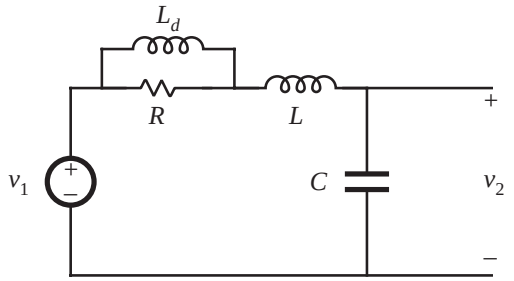
- L_d is physically very small
- A simple low-cost approach to damping the input filter
- Disadvantage: L_d degrades high-frequency attenuation of filter, by the factor

$$\frac{L}{L \| L_d} = 1 + \frac{1}{n}$$

- Basic tradeoff: peak output impedance vs. high-frequency attenuation
- Example: the choice $n = 1$ ($L_d = L$) degrades the HF attenuation by 6 dB, an leads to peak output impedance of $\| Z \|_{mm} = \sqrt{6}\ R_0$



Optimal R-L_d series damping



Basic results

$$Q_{opt} = \frac{R_0}{R} = \left(\frac{1+n}{n}\right)\sqrt{\frac{2\left(1+n\right)\left(4+n\right)}{\left(2+n\right)\left(4+3n\right)}}$$

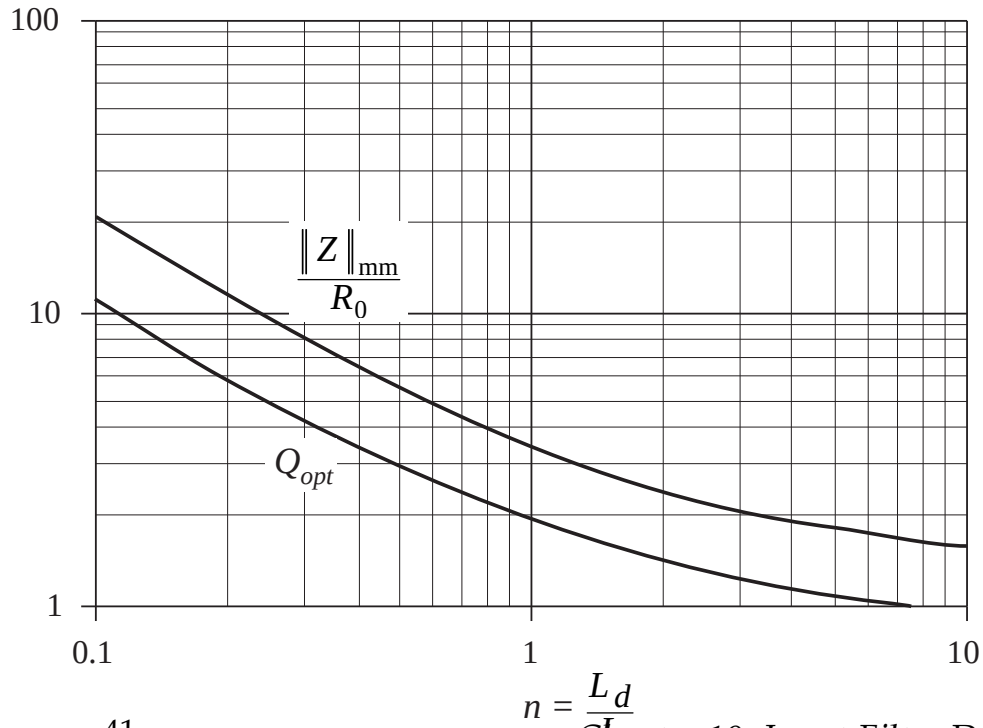
$$\frac{\| Z \|_{mm}}{R_0} = \frac{\sqrt{2\left(1+n\right)\left(2+n\right)}}{n}$$

with

$$n = \frac{L_d}{L}$$

$$R_0 = \sqrt{\frac{L}{C}}$$

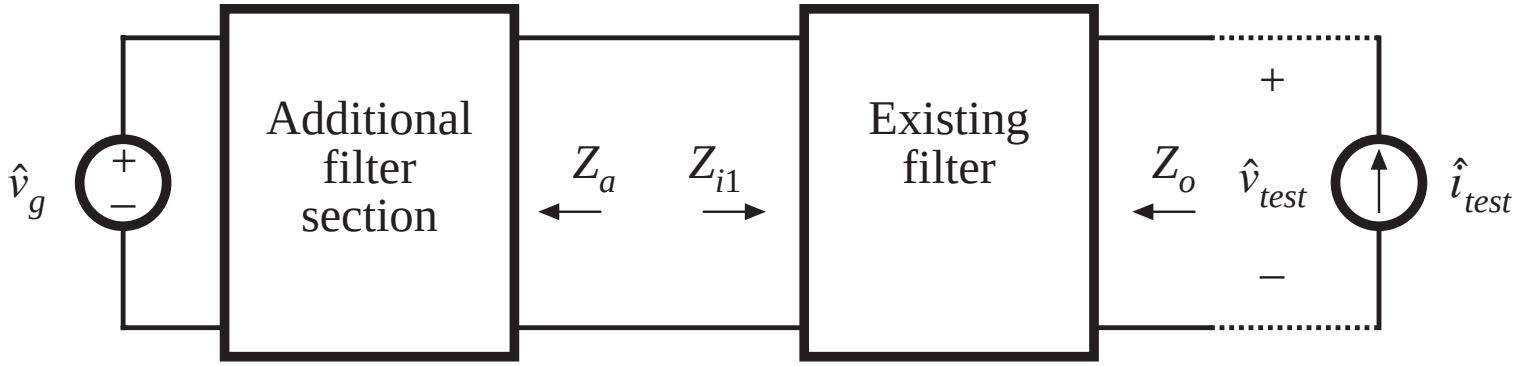
- Does not degrade HF attenuation
- L_d must conduct entire dc current
- Peak output impedance cannot be reduced below $\sqrt{2}\ R_0$



10.4.4 Cascading Filter Sections

- Cascade connection of multiple *L*-*C* filter sections can achieve a given high-frequency attenuation with much smaller volume and weight
- Need to damp each section of the filter
- One approach: add new filter section to an existing filter, using new design criteria
- Stagger-tuning of filter sections

Addition of filter section

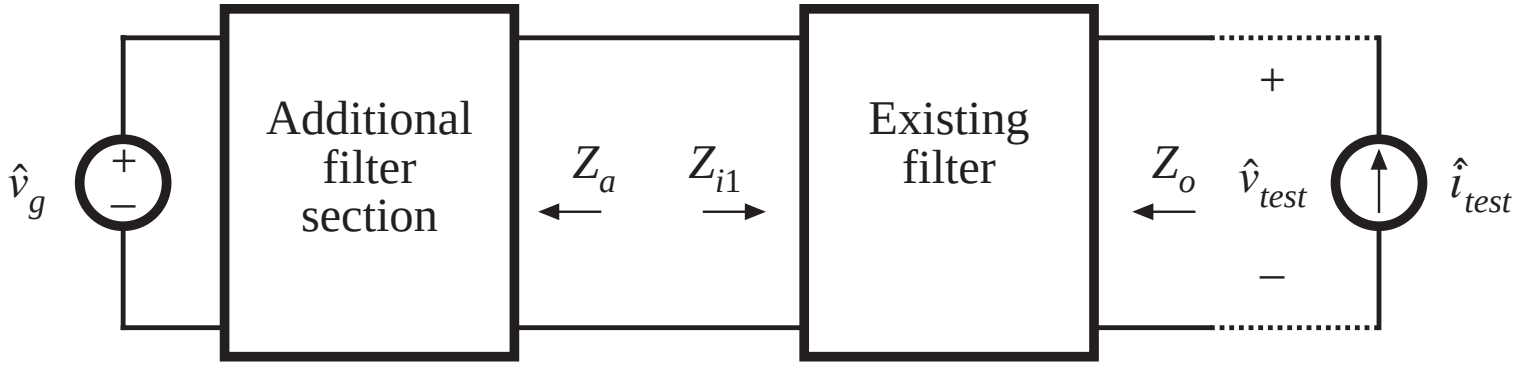


How the additional filter section changes the output impedance of the existing filter:

$$\text{modified } Z_o(s) = \left[Z_o(s) \right]_{Z_a(s) = 0} \frac{\left(1 + \dfrac{Z_a(s)}{Z_{N1}(s)} \right)}{\left(1 + \dfrac{Z_a(s)}{Z_{D1}(s)} \right)}$$

$$Z_{N1}(s) = Z_{i1}(s) \Big|_{\hat{v}_{test}(s) \xrightarrow[\text{null}]{} 0} \qquad Z_{D1}(s) = Z_{i1}(s) \Big|_{\hat{i}_{test}(s) = 0}$$

Design criteria



$$Z_{N1}(s) = Z_{i1}(s)\Big|_{\hat{v}_{test}(s) \xrightarrow[\text{null}]{} 0}$$ (with filter output port short-circuited)

$$Z_{D1}(s) = Z_{i1}(s)\Big|_{\hat{i}_{test}(s) = 0}$$ (with filter output port open-circuited)

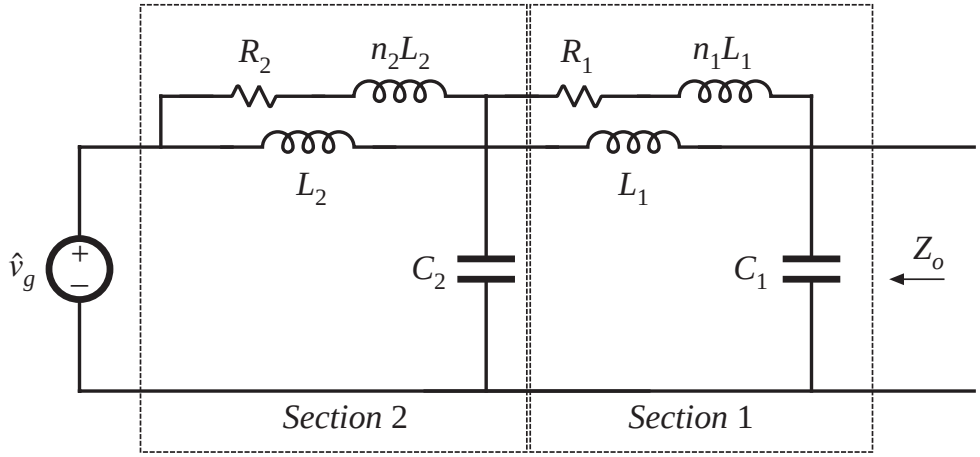
The presence of the additional filter section does not substantially alter the output impedance Z_o of the existing filter provided that

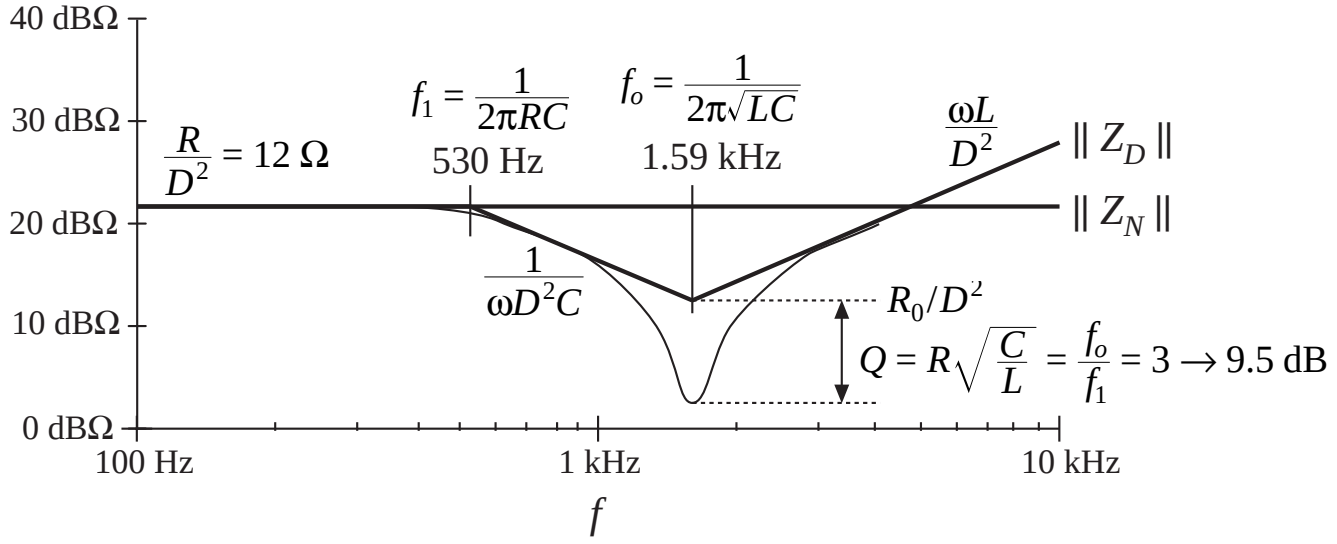
$$\|Z_a\| \ll \|Z_{N1}\| \quad \text{and}$$
$$\|Z_a\| \ll \|Z_{D1}\|$$

10.4.5 Example
Two-Stage Input Filter

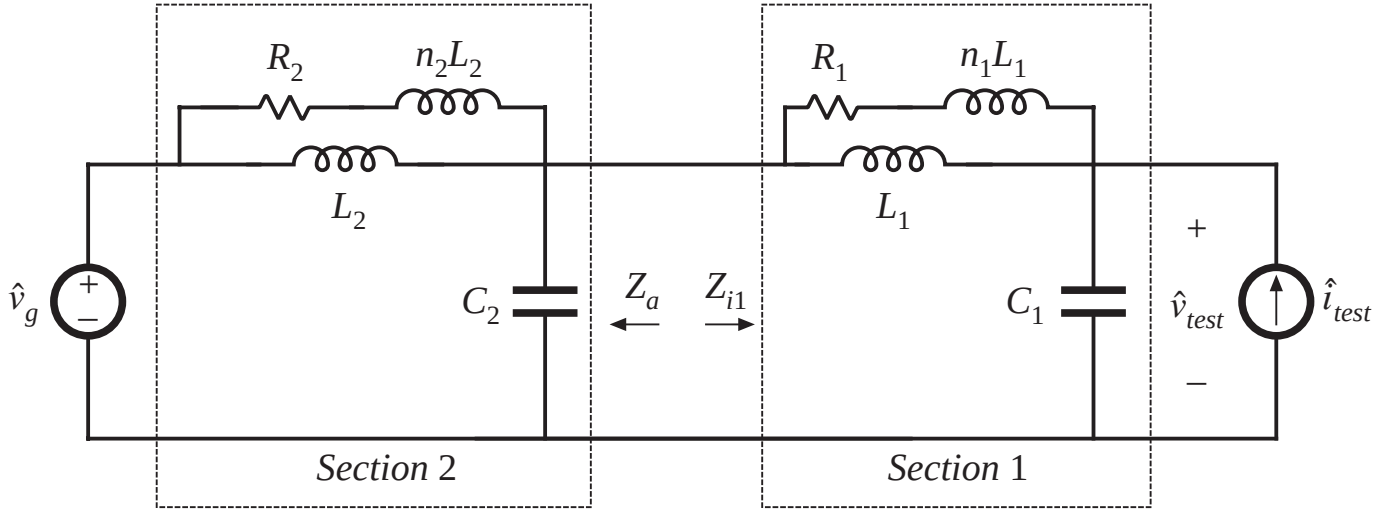
Requirements: For the same buck converter example, achieve the following:

- 80 dB of attenuation at 250 kHz
- Section 1 to satisfy Z_o impedance inequalities as before:





Section 2 impedance inequalities

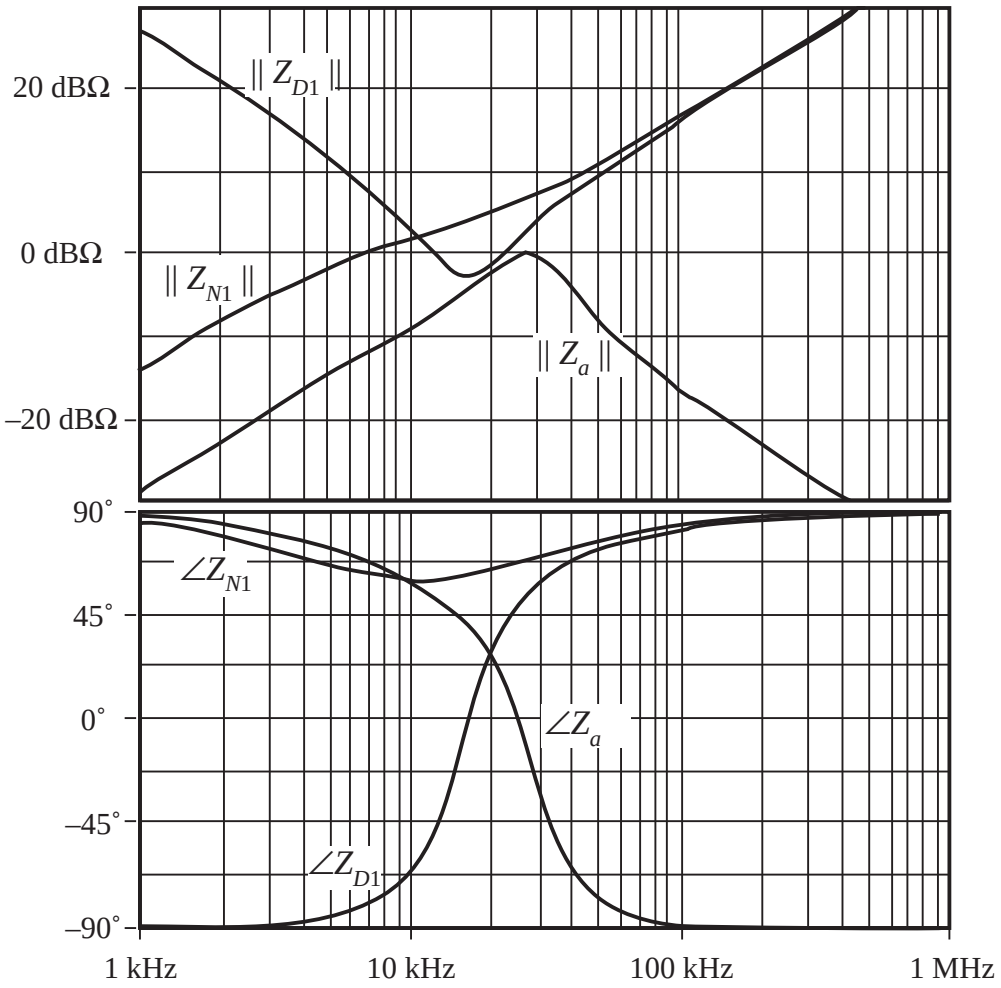


To avoid disrupting the output impedance Z_o of section 1, section 2 should satisfy the following inequalities:

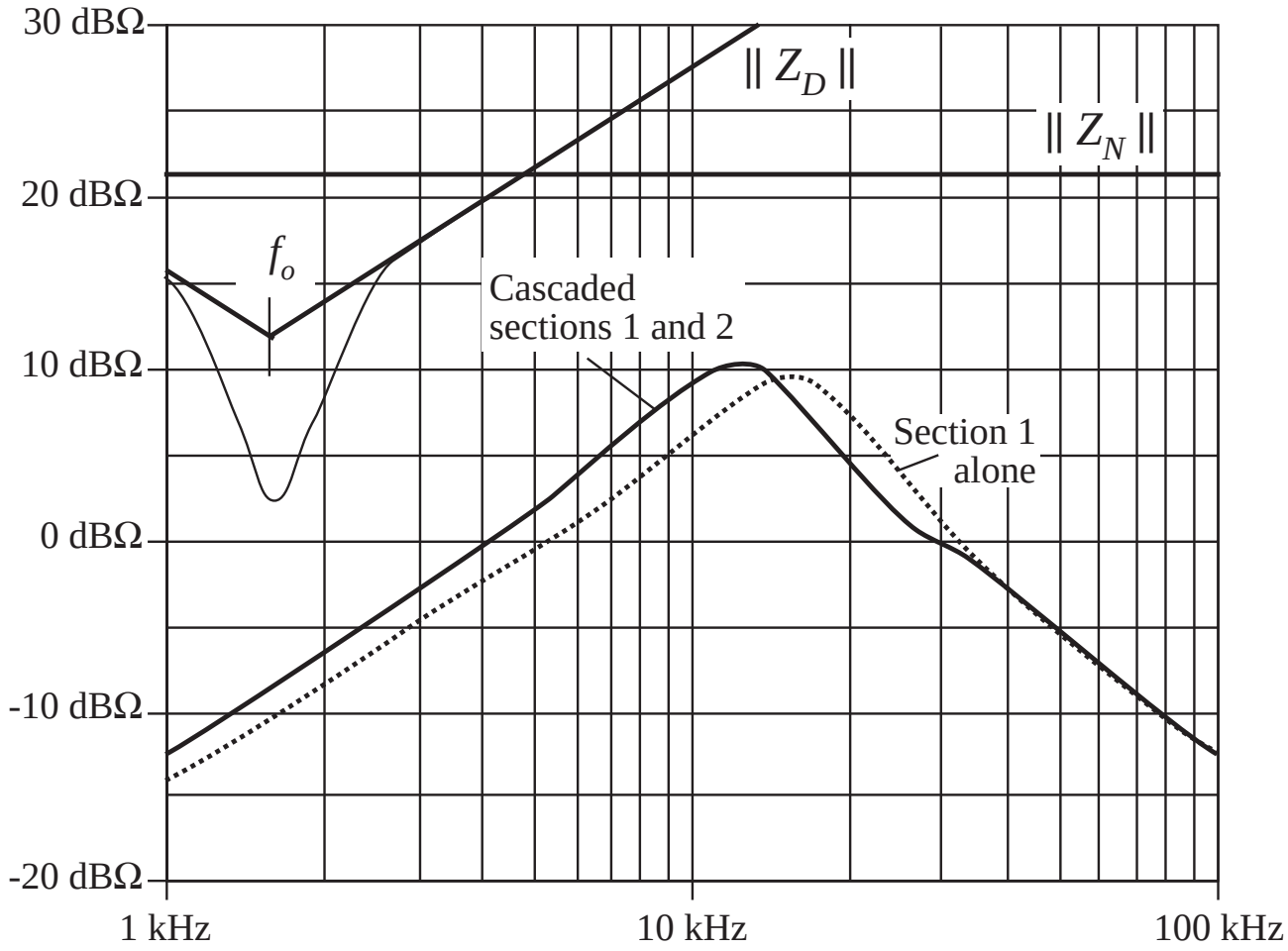
$$Z_a \ll Z_{N1} = Z_{i1}\Big|_{\text{output shorted}} = \left(R_1 + sn_1L_1\right) \| sL_1$$

$$Z_a \ll Z_{D1} = Z_{i1}\Big|_{\text{output open-circuited}} = \frac{1}{sC_1} + \left(R_1 + sn_1L_1\right) \| sL_1$$

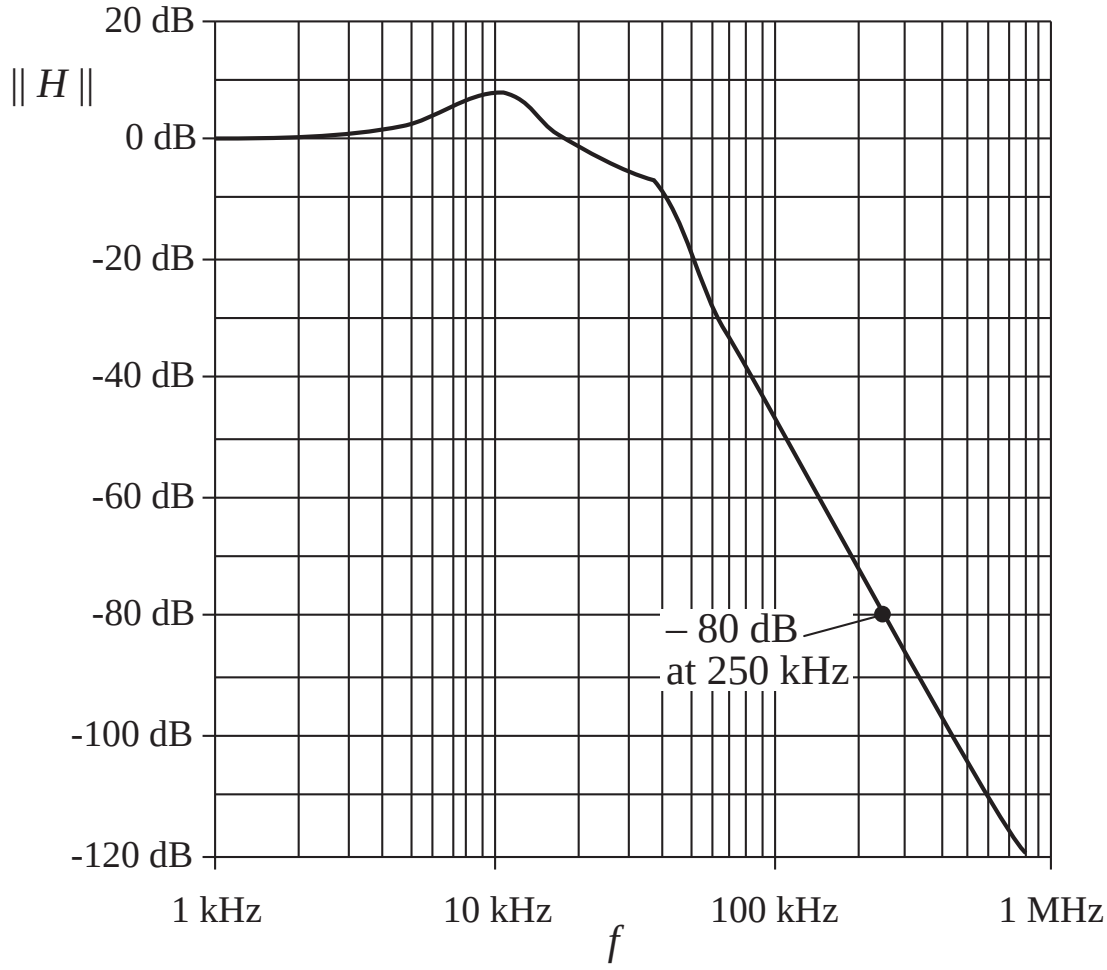
Plots of Z_{N1} and Z_{D1}



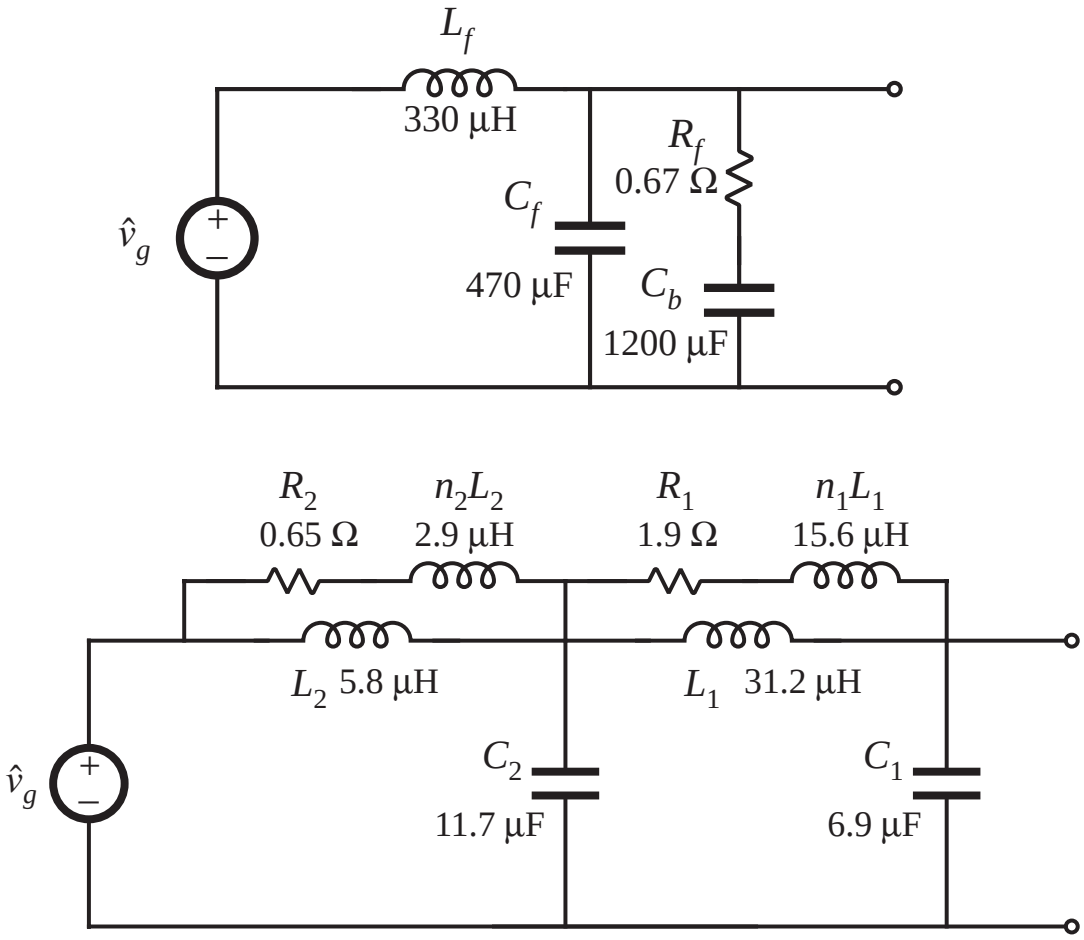
Section 1 output impedance inequalities



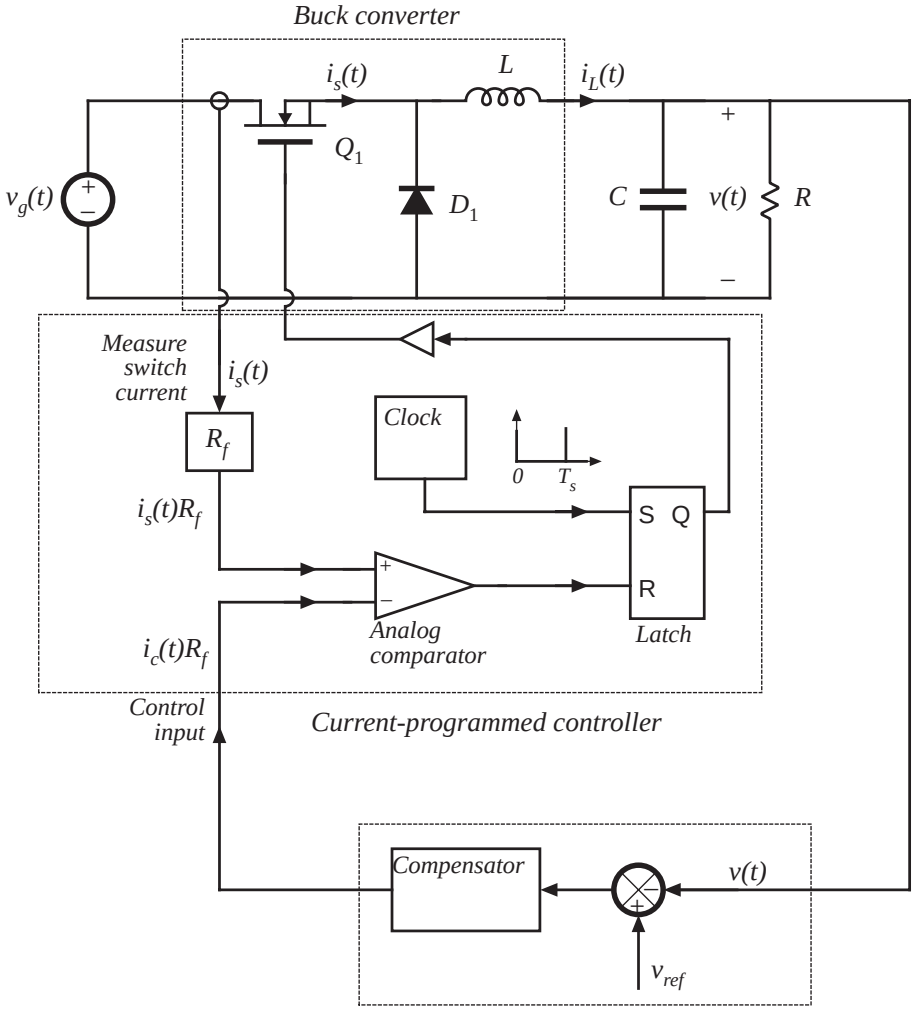
Resulting filter transfer function



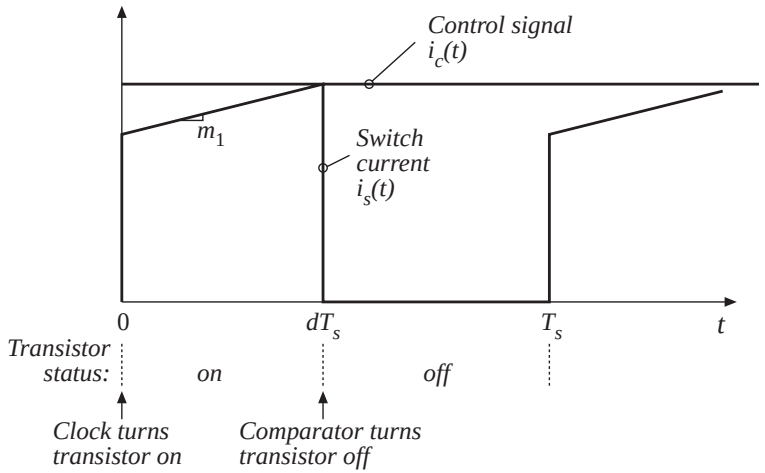
Comparison of single-section and two-section designs



Chapter 11
Current Programmed Control



The peak transistor current replaces the duty cycle as the converter control input.



Current programmed control vs. duty cycle control

Advantages of current programmed control:

- Simpler dynamics —inductor pole is moved to high frequency
- Simple robust output voltage control, with large phase margin, can be obtained without use of compensator lead networks
- It is always necessary to sense the transistor current, to protect against overcurrent failures. We may as well use the information during normal operation, to obtain better control
- Transistor failures due to excessive current can be prevented simply by limiting $i_c(t)$
- Transformer saturation problems in bridge or push-pull converters can be mitigated

A disadvantage: susceptibility to noise

Chapter 11: Outline

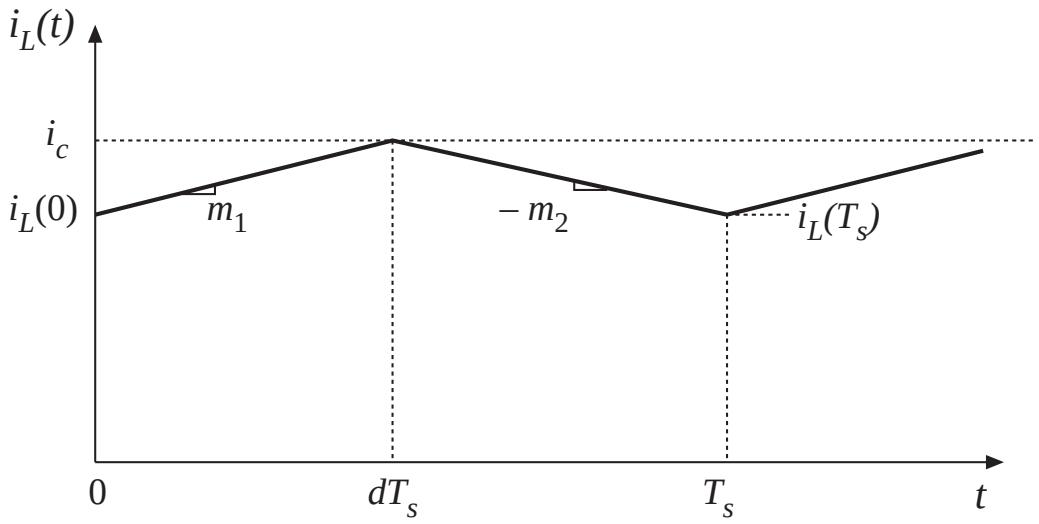
11.1 Oscillation for $D > 0.5$

- The current programmed controller is inherently unstable for $D > 0.5$, regardless of the converter topology
- Controller can be stabilized by addition of an artificial ramp

Objectives of this section:

- Stability analysis
- Describe artificial ramp scheme

Inductor current waveform, CCM



Inductor current slopes m_1 *and* $-m_2$

buck converter

$$m_1 = \frac{v_g - v}{L} \qquad -m_2 = -\frac{v}{L}$$

boost converter

$$m_1 = \frac{v_g}{L} \qquad -m_2 = \frac{v_g - v}{L}$$

buck–boost converter

$$m_1 = \frac{v_g}{L} \qquad -m_2 = \frac{v}{L}$$

Steady-state inductor current waveform, CPM

First interval:

$$i_L(dT_s) = i_c = i_L(0) + m_1 dT_s$$

Solve for d:

$$d = \frac{i_c - i_L(0)}{m_1 T_s}$$

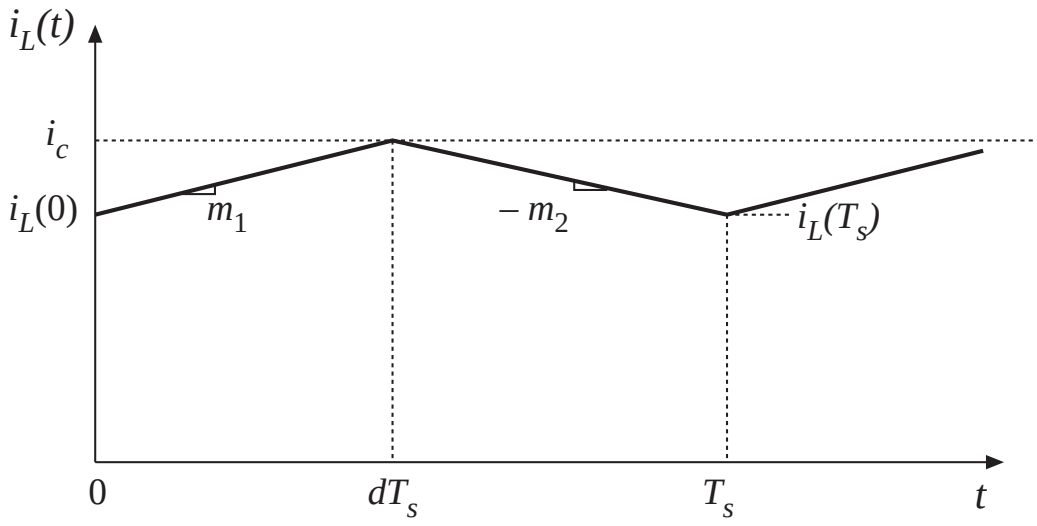
Second interval:

$$i_L(T_s) = i_L(dT_s) - m_2 d' T_s$$
$$= i_L(0) + m_1 dT_s - m_2 d' T_s$$

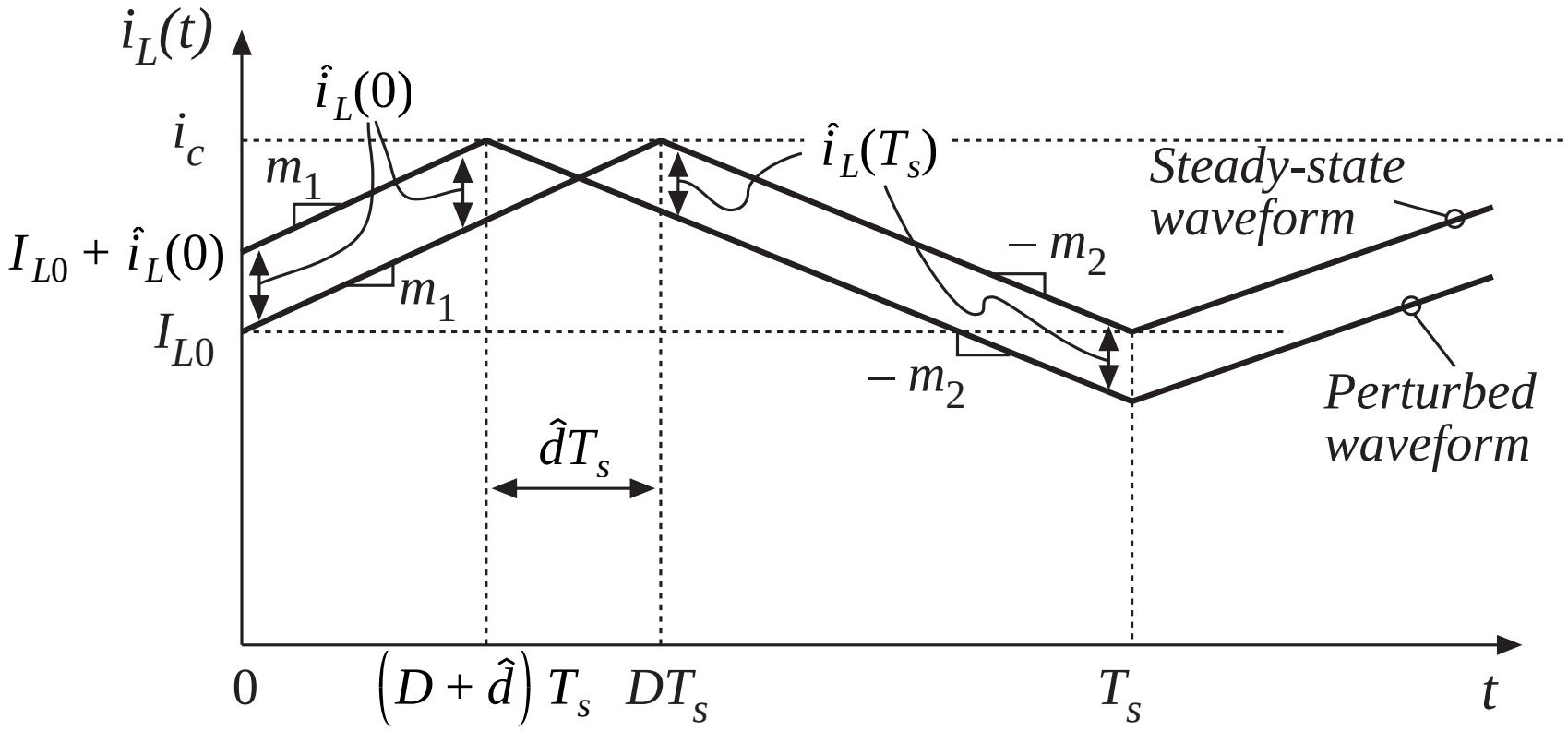
In steady state:

$$0 = M_1 DT_s - M_2 D' T_s$$

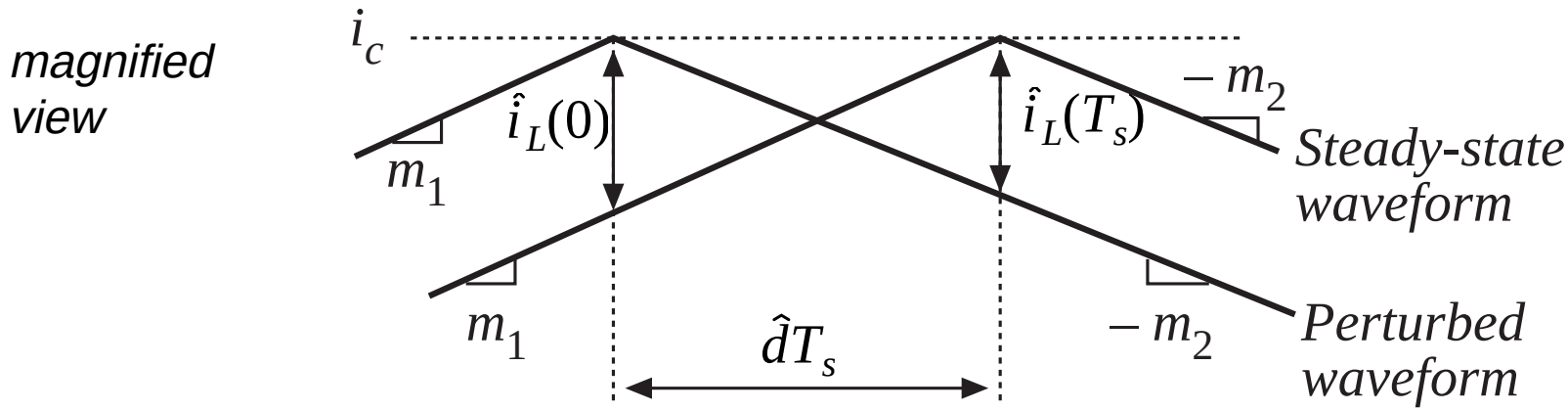
$$\frac{M_2}{M_1} = \frac{D}{D'}$$



Perturbed inductor current waveform



Change in inductor current perturbation over one switching period



$$\hat{i}_L(0) = -m_1 \hat{d} T_s$$

$$\hat{i}_L(T_s) = m_2 \hat{d} T_s$$

$$\hat{i}_L(T_s) = \hat{i}_L(0) \left(-\frac{m_2}{m_1} \right)$$

$$\hat{i}_L(T_s) = \hat{i}_L(0) \left(-\frac{D}{D'} \right)$$

Change in inductor current perturbation over many switching periods

$$\hat{i}_L(T_s) = \hat{i}_L(0)\left(-\frac{D}{D'}\right)$$

$$\hat{i}_L(2T_s) = \hat{i}_L(T_s)\left(-\frac{D}{D'}\right) = \hat{i}_L(0)\left(-\frac{D}{D'}\right)^2$$

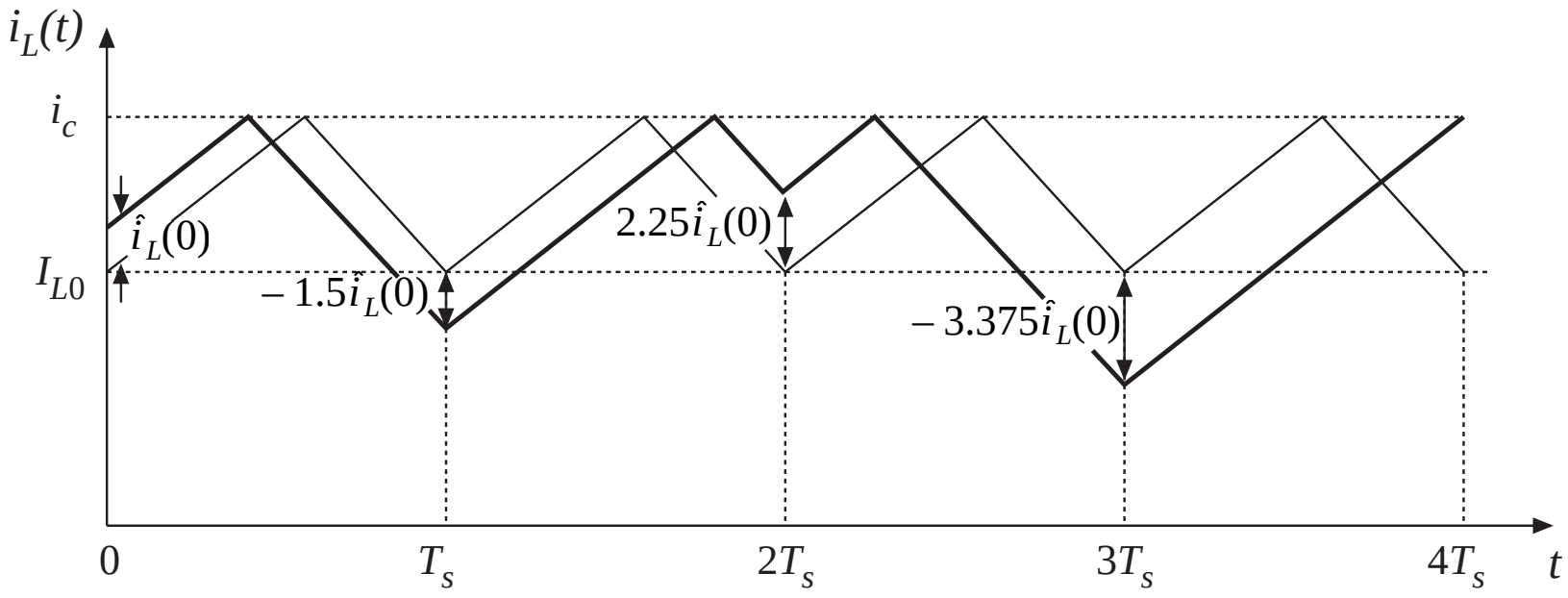
$$\hat{i}_L(nT_s) = \hat{i}_L((n-1)T_s)\left(-\frac{D}{D'}\right) = \hat{i}_L(0)\left(-\frac{D}{D'}\right)^n$$

$$\left|\hat{i}_L(nT_s)\right| \rightarrow \begin{cases} 0 & \text{when } \left|-\frac{D}{D'}\right| < 1 \\ \infty & \text{when } \left|-\frac{D}{D'}\right| > 1 \end{cases}$$

For stability: $D < 0.5$

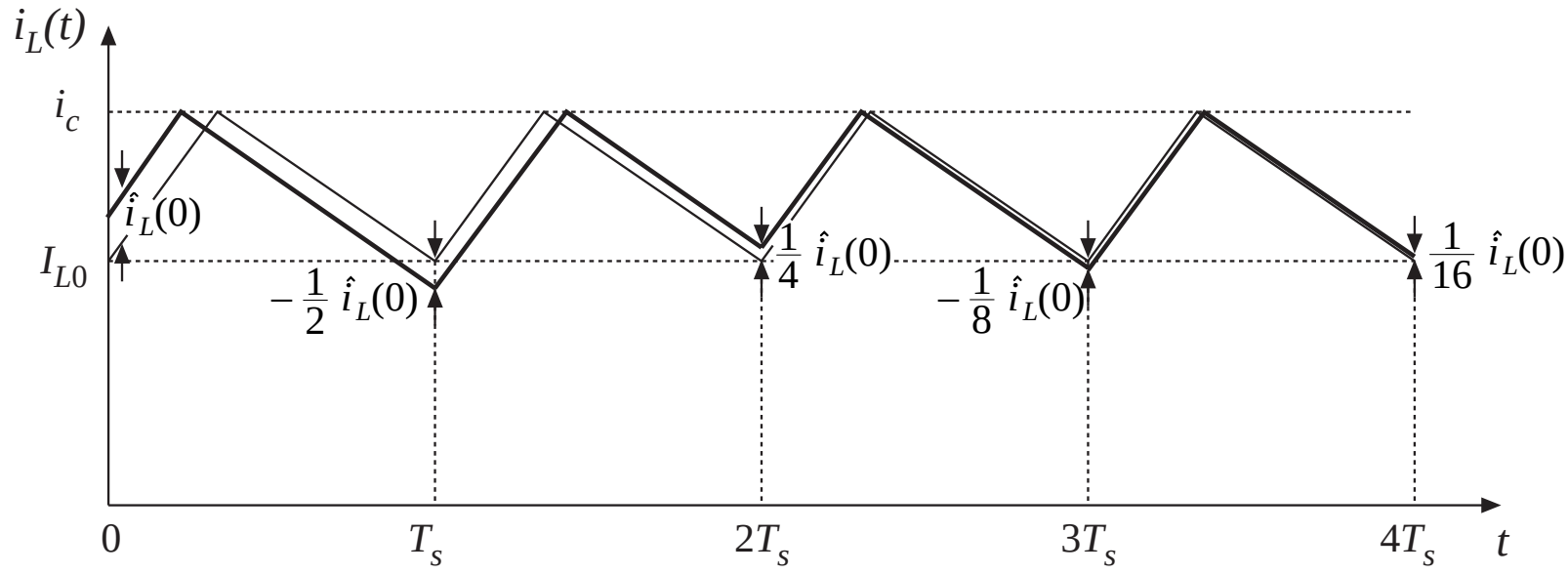
Example: unstable operation for $D = 0.6$

$$\alpha = -\frac{D}{D'} = \left(-\frac{0.6}{0.4}\right) = -1.5$$

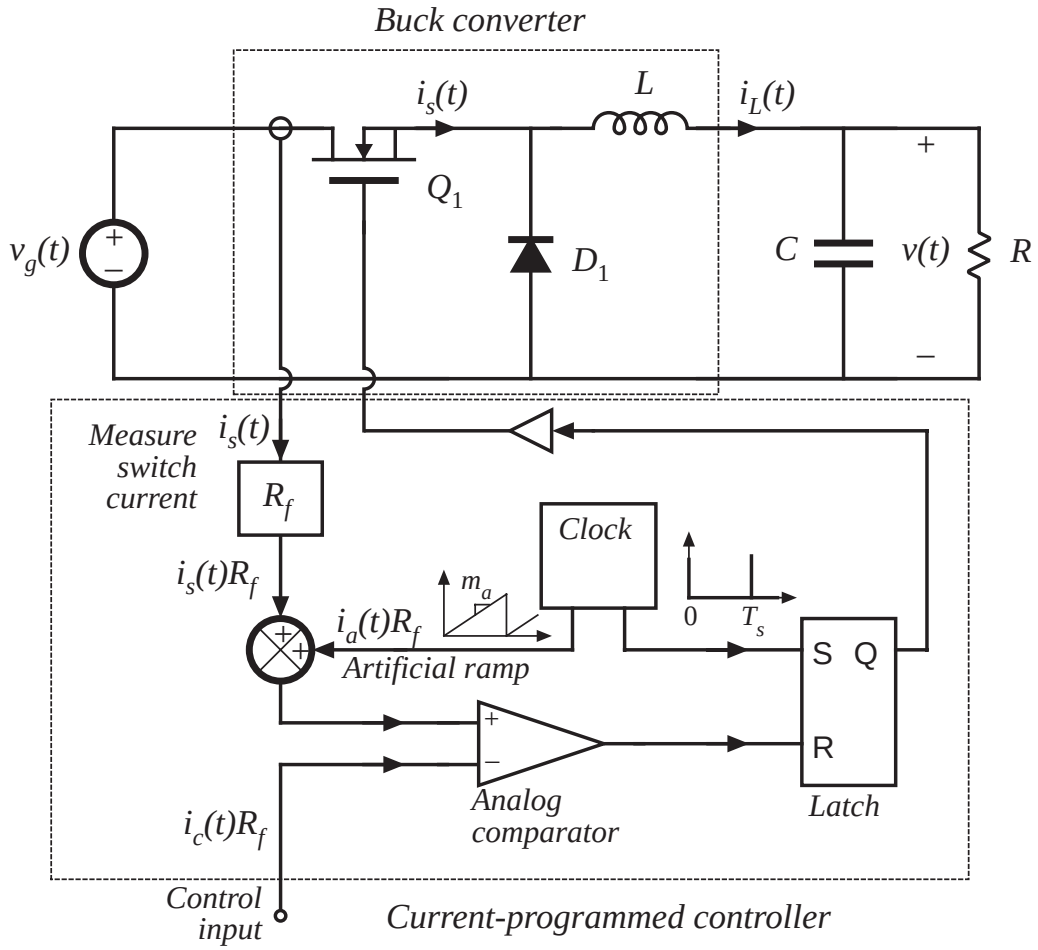


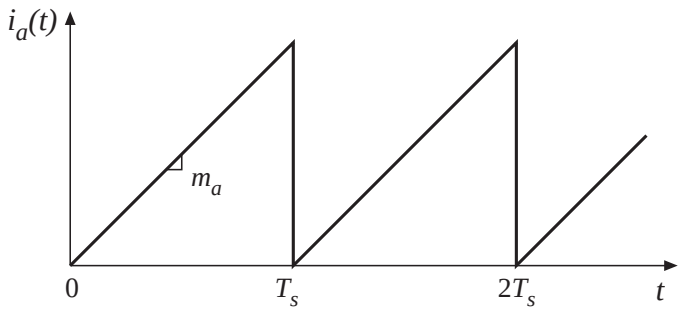
Example: stable operation for $D = 1/3$

$$\alpha = -\frac{D}{D'} = \left(-\frac{1/3}{2/3}\right) = -0.5$$



Stabilization via addition of an artificial ramp to the measured switch current waveform





Now, transistor switches off when

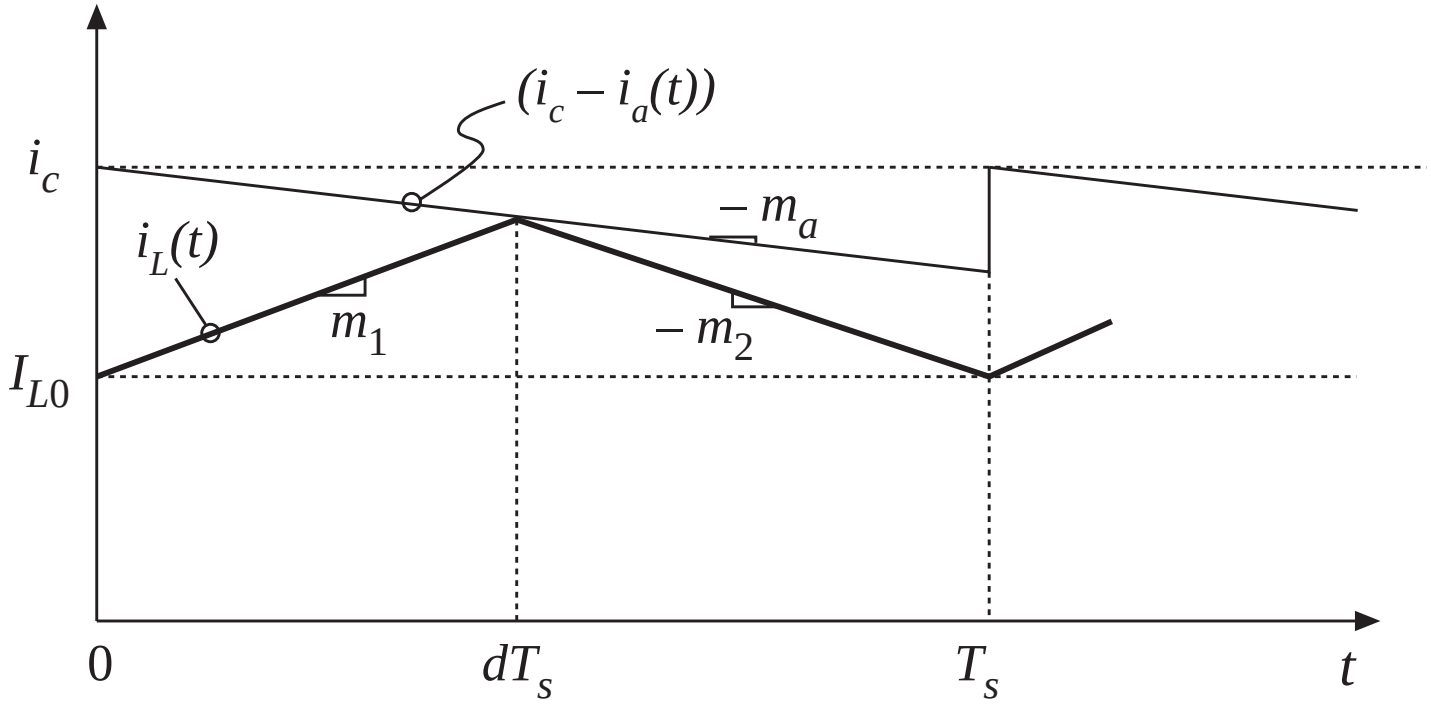
$$i_a(dT_s) + i_L(dT_s) = i_c$$

or,

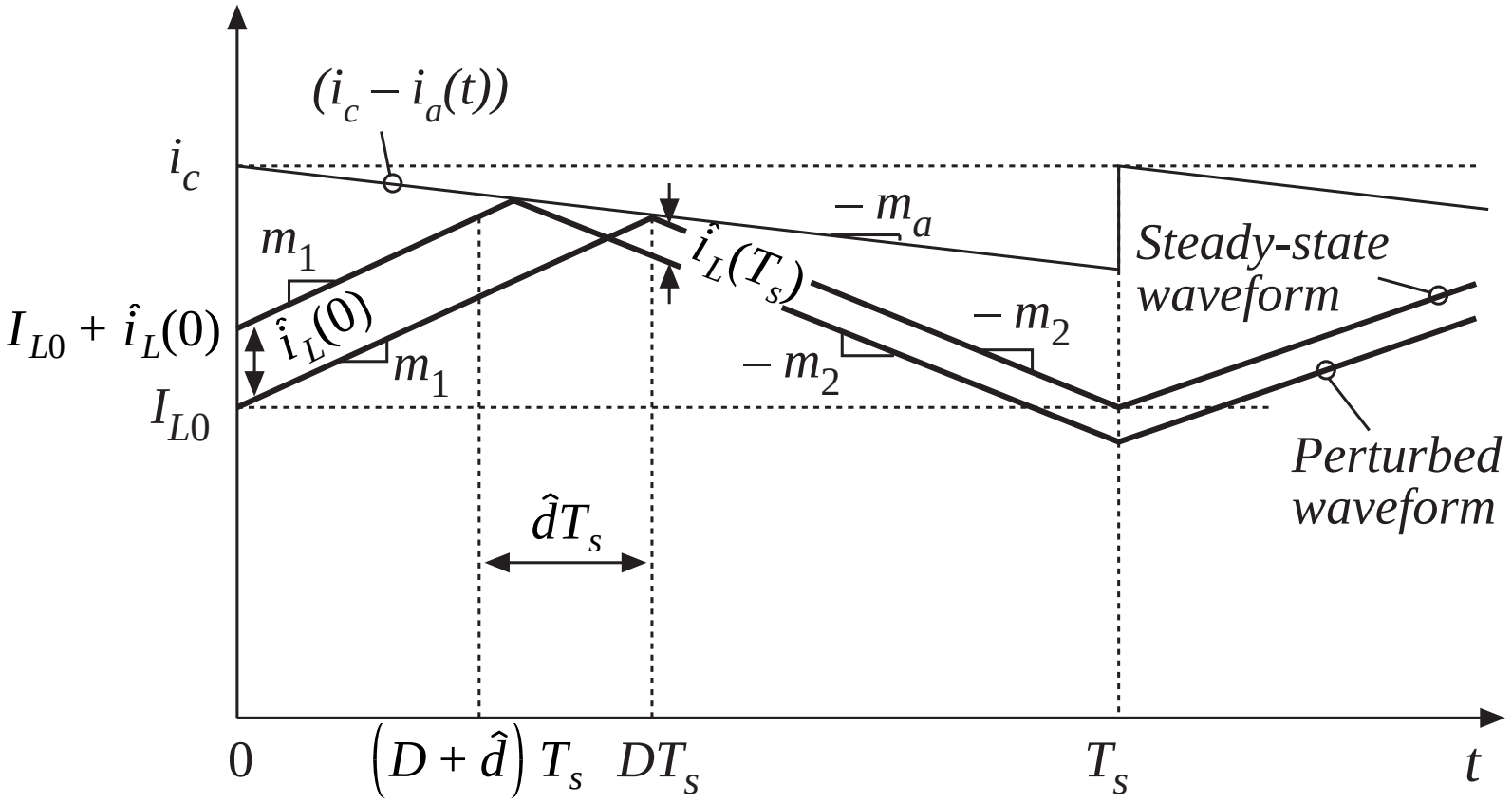
$$i_L(dT_s) = i_c - i_a(dT_s)$$

Steady state waveforms with artificial ramp

$$i_L(dT_s) = i_c - i_a(dT_s)$$



Stability analysis: perturbed waveform



Stability analysis: change in perturbation over complete switching periods

First subinterval:

$$\hat{i}_L(0) = -\hat{d} T_s \left(m_1 + m_a \right)$$

Second subinterval:

$$\hat{i}_L(T_s) = -\hat{d} T_s \left(m_a - m_2 \right)$$

Net change over one switching period:

$$\hat{i}_L(T_s) = \hat{i}_L(0) \left(-\frac{m_2 - m_a}{m_1 + m_a} \right)$$

After n switching periods:

$$\hat{i}_L(nT_s) = \hat{i}_L((n-1)T_s) \left(-\frac{m_2 - m_a}{m_1 + m_a} \right) = \hat{i}_L(0) \left(-\frac{m_2 - m_a}{m_1 + m_a} \right)^n = \hat{i}_L(0)\, \alpha^n$$

Characteristic value:

$$\alpha = -\frac{m_2 - m_a}{m_1 + m_a}$$

$$\left| \hat{i}_L(nT_s) \right| \rightarrow \begin{cases} 0 & \text{when } |\alpha| < 1 \\ \infty & \text{when } |\alpha| > 1 \end{cases}$$

The characteristic value α

$$\alpha = -\frac{1 - \frac{m_a}{m_2}}{\frac{D'}{D} + \frac{m_a}{m_2}}$$

- For stability, require $|\alpha| < 1$
- Buck and buck-boost converters: $m_2 = -v/L$

  So if v is well-regulated, then m_2 is also well-regulated
- A common choice: $m_a = 0.5\, m_2$

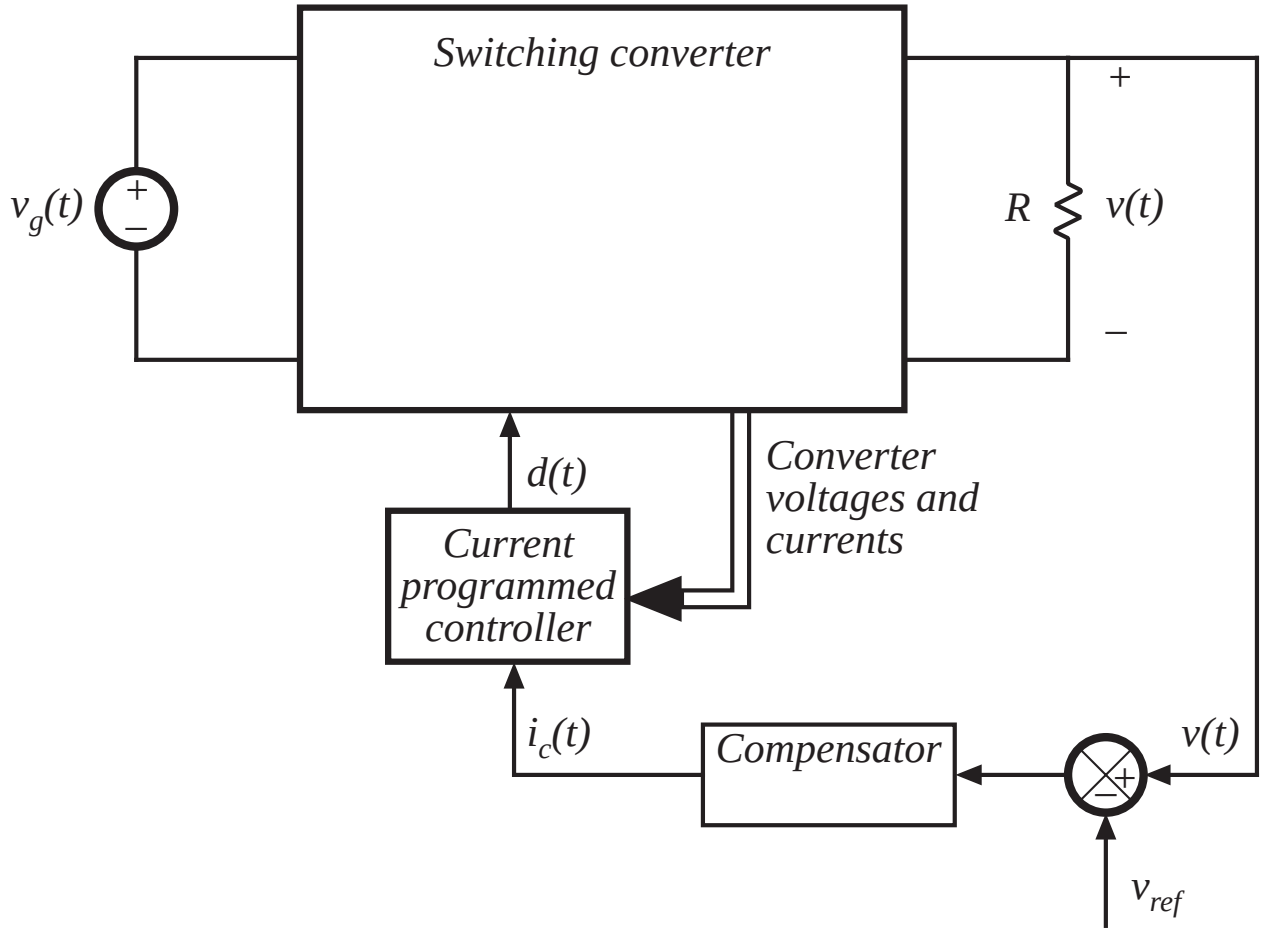
  This leads to $\alpha = -1$ at $D = 1$, and $|\alpha| < 1$ for $0 \le D < 1$.

  The minimum α that leads to stability for all D.
- Another common choice: $m_a = m_2$

  This leads to $\alpha = 0$ for $0 \le D < 1$.

  Deadbeat control, finite settling time

11.2 A Simple First-Order Model



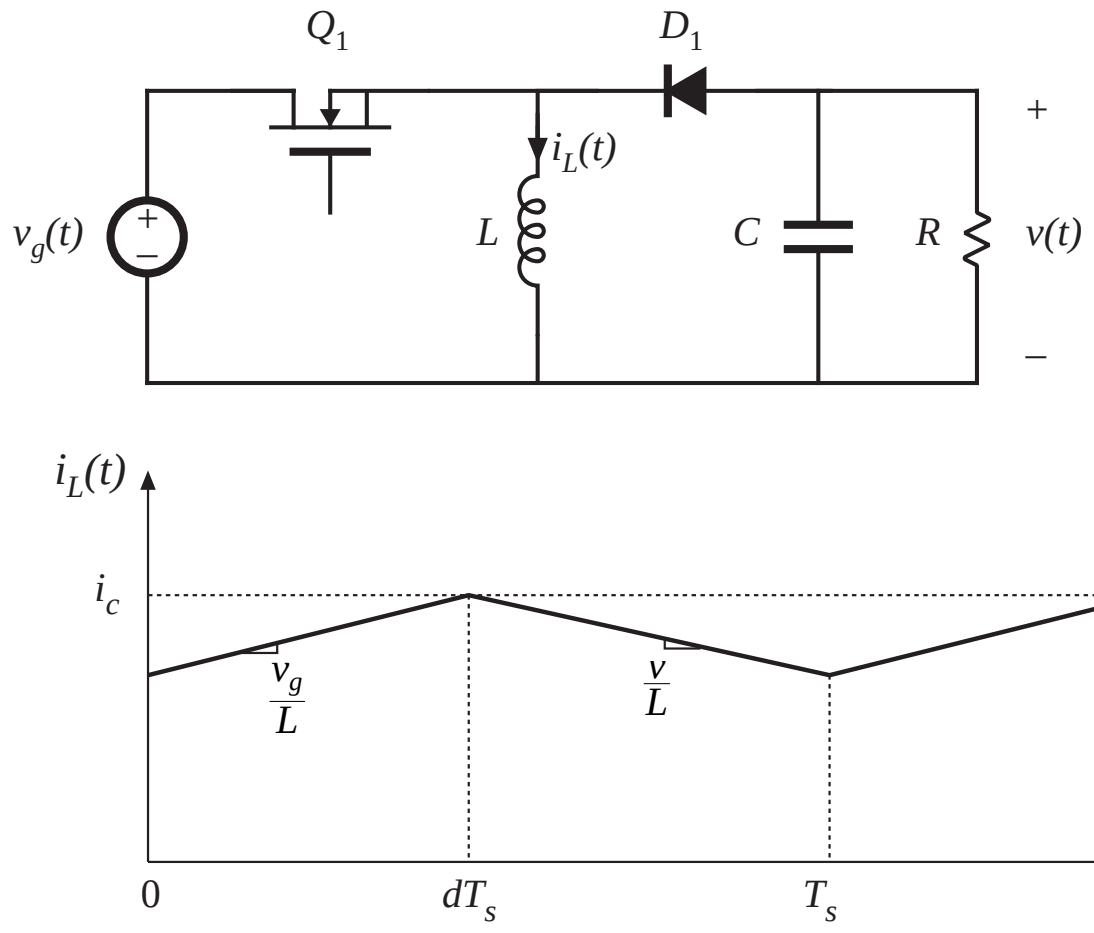
The first-order approximation

$$\left\langle i_L(t) \right\rangle_{T_s} = i_c(t)$$

- Neglects switching ripple and artificial ramp
- Yields physical insight and simple first-order model
- Accurate when converter operates well into CCM (so that switching ripple is small) and when the magnitude of the artificial ramp is not too large
- Resulting small-signal relation:

$$\hat{i}_L(s) \approx \hat{i}_c(s)$$

11.2.1 Simple model via algebraic approach: CCM buck-boost example



Small-signal equations of CCM buck–boost, duty cycle control

$$L \frac{d \hat{i}_L(t)}{dt} = D\hat{v}_g(t) + D'\hat{v}(t) + \left(V_g - V\right)\hat{d}(t)$$

$$C \frac{d \hat{v}(t)}{dt} = - D'\hat{i}_L - \frac{\hat{v}(t)}{R} + I_L \hat{d}(t)$$

$$\hat{i}_g(t) = D\hat{i}_L + I_L \hat{d}(t)$$

Derived in Chapter 7

Transformed equations

Take Laplace transform, letting initial conditions be zero:

$$sL\hat{i}_L(s) = D\hat{v}_g(s) + D'\hat{v}(s) + \left(V_g - V\right)\hat{d}(s)$$

$$sC\hat{v}(s) = -D'\hat{i}_L(s) - \frac{\hat{v}(s)}{R} + I_L\hat{d}(s)$$

$$\hat{i}_g(s) = D\hat{i}_L(s) + I_L\hat{d}(s)$$

The simple approximation

Now let

$$\hat{i}_L(s) \approx \hat{i}_c(s)$$

Eliminate the duty cycle (now an intermediate variable), to express the equations using the new control input i_L. The inductor equation becomes:

$$sL\hat{i}_c(s) \approx D\hat{v}_g(s) + D'\hat{v}(s) + \left(V_g - V\right)\hat{d}(s)$$

Solve for the duty cycle variations:

$$\hat{d}(s) = \frac{sL\hat{i}_c(s) - D\hat{v}_g(s) - D'\hat{v}(s)}{\left(V_g - V\right)}$$

The simple approximation, continued

Substitute this expression to eliminate the duty cycle from the remaining equations:

$$sC\hat{v}(s) = -D'\hat{i}_c(s) - \frac{\hat{v}(s)}{R} + I_L \frac{sL\hat{i}_c(s) - D\hat{v}_g(s) - D'\hat{v}(s)}{\left(V_g - V\right)}$$

$$\hat{i}_g(s) = D\hat{i}_c(s) + I_L \frac{sL\hat{i}_c(s) - D\hat{v}_g(s) - D'\hat{v}(s)}{\left(V_g - V\right)}$$

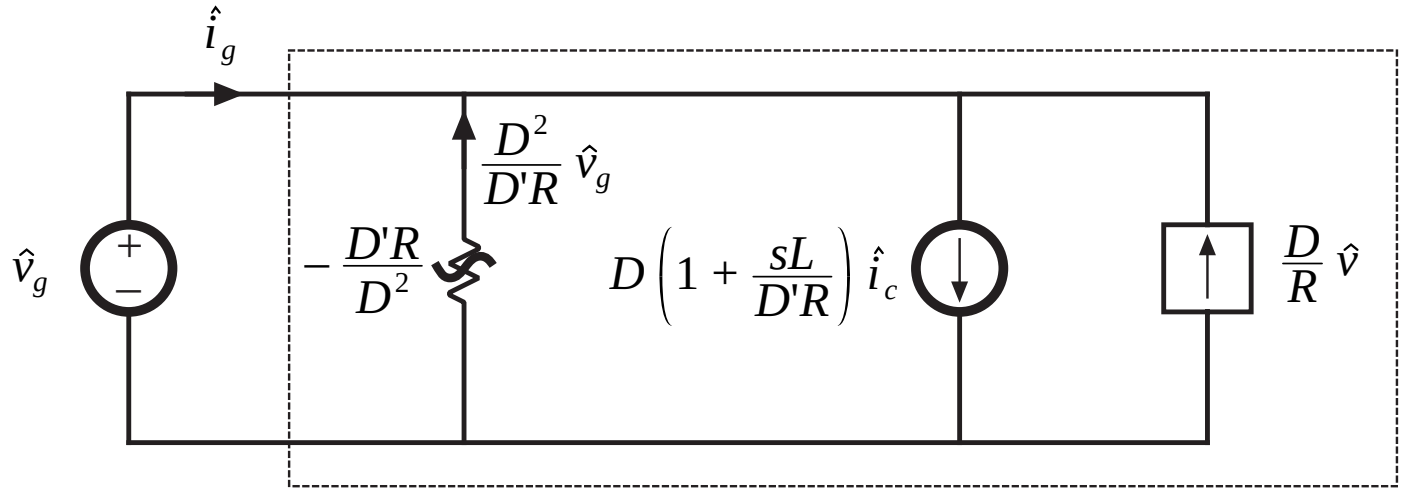
Collect terms, simplify using steady-state relations:

$$sC\hat{v}(s) = \left(\frac{sLD}{D'R} - D'\right)\hat{i}_c(s) - \left(\frac{D}{R} + \frac{1}{R}\right)\hat{v}(s) - \left(\frac{D^2}{D'R}\right)\hat{v}_g(s)$$

$$\hat{i}_g(s) = \left(\frac{sLD}{D'R} + D\right)\hat{i}_c(s) - \left(\frac{D}{R}\right)\hat{v}(s) - \left(\frac{D^2}{D'R}\right)\hat{v}_g(s)$$

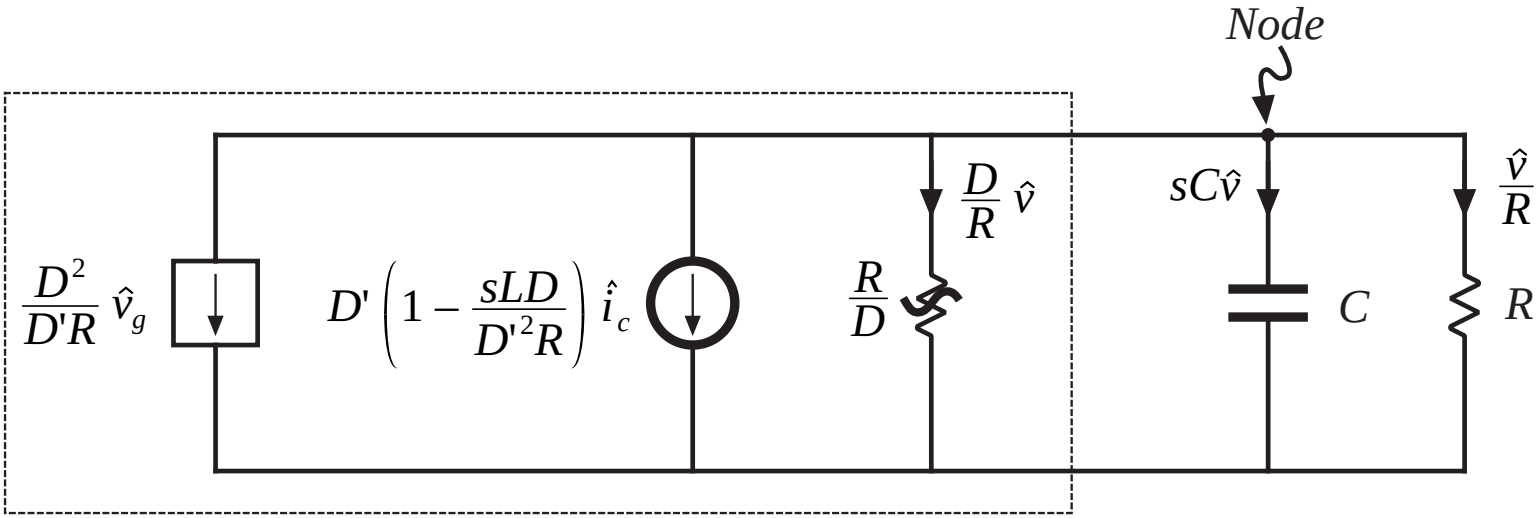
Construct equivalent circuit: input port

$$\hat{i}_g(s) = \left(\frac{sLD}{D'R} + D \right) \hat{i}_c(s) - \left(\frac{D}{R} \right) \hat{v}(s) - \left(\frac{D^2}{D'R} \right) \hat{v}_g(s)$$



Construct equivalent circuit: output port

$$sC\hat{v}(s) = \left(\frac{sLD}{D'R} - D' \right) \hat{i}_c(s) - \left(\frac{D}{R} + \frac{1}{R} \right) \hat{v}(s) - \left(\frac{D^2}{D'R} \right) \hat{v}_g(s)$$



CPM Canonical Model, Simple Approximation

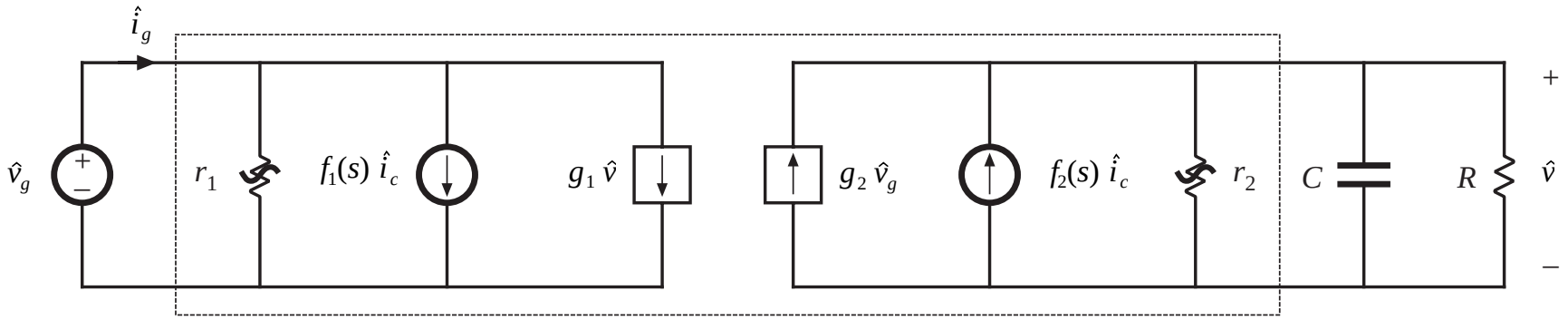
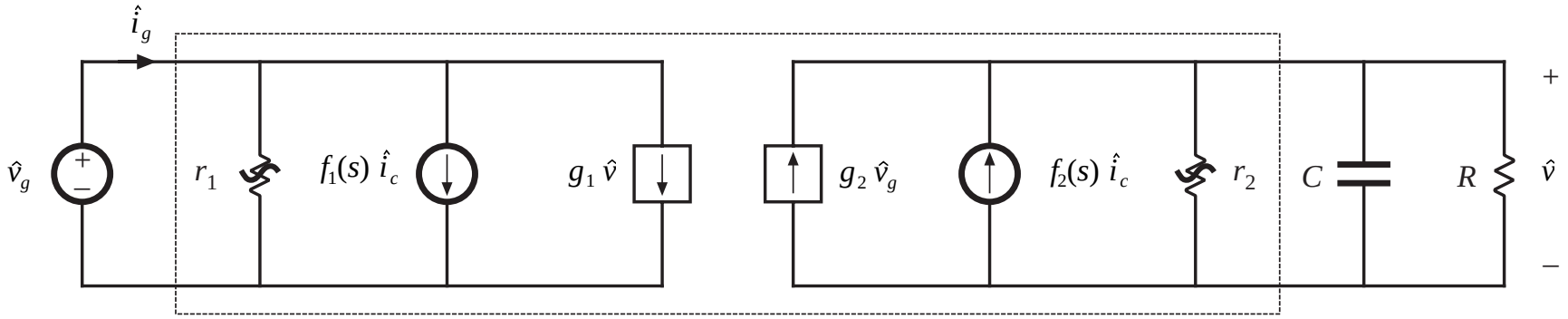


Table of results for basic converters

Table 11.1 Current programmed mode small-signal equivalent circuit parameters, simple model

Converter	g_1	f_1	r_1	g_2	f_2	r_2
Buck	$\frac{D}{R}$	$D\left(1+\frac{sL}{R}\right)$	$-\frac{R}{D^2}$	0	1	∞
Boost	0	1	∞	$\frac{1}{D'R}$	$D'\left(1-\frac{sL}{D'^2R}\right)$	R
Buck-boost	$-\frac{D}{R}$	$D\left(1+\frac{sL}{D'R}\right)$	$-\frac{D'R}{D^2}$	$-\frac{D^2}{D'R}$	$-D'\left(1-\frac{sDL}{D'^2R}\right)$	$\frac{R}{D}$

Transfer functions predicted by simple model



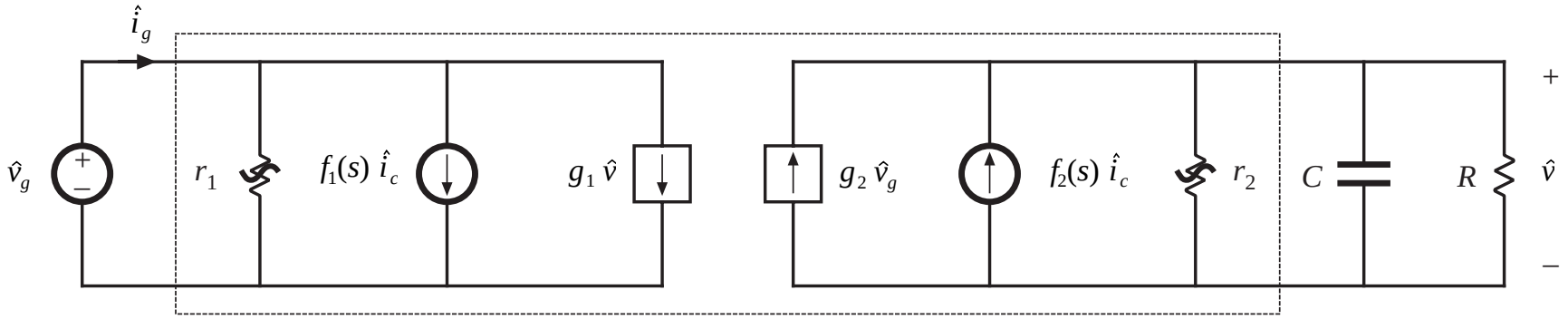
Control-to-output transfer function

$$G_{vc}(s) = \left.\frac{\hat{v}(s)}{\hat{i}_c(s)}\right|_{\hat{v}_g = 0} = f_2 \left(r_2 \parallel R \parallel \frac{1}{sC} \right)$$

Result for buck-boost example

$$G_{vc}(s) = -R \frac{D'}{1+D} \frac{\left(1 - s\frac{DL}{D'^2 R}\right)}{\left(1 + s\frac{RC}{1+D}\right)}$$

Transfer functions predicted by simple model



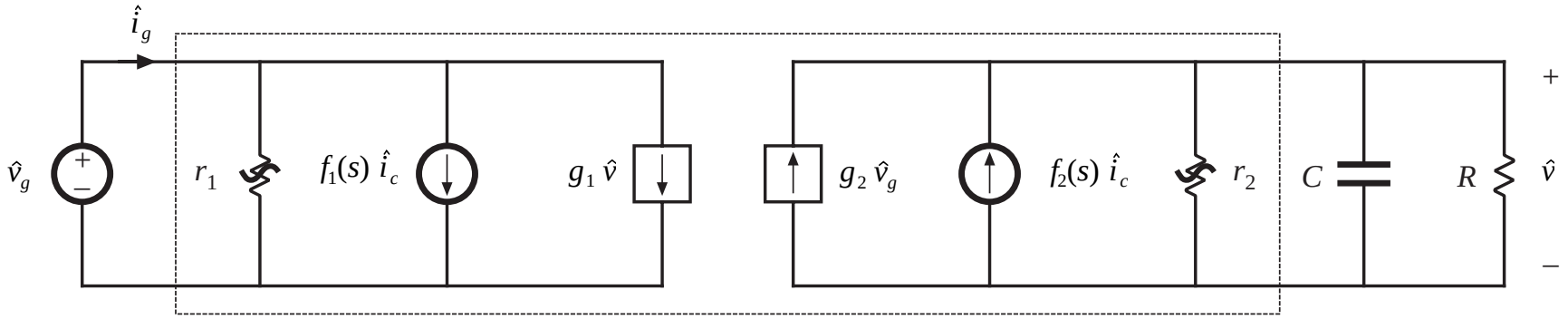
Line-to-output transfer function

$$G_{vg}(s) = \left. \frac{\hat{v}(s)}{\hat{v}_g(s)} \right|_{\hat{i}_c = 0} = g_2 \left(r_2 \parallel R \parallel \frac{1}{sC} \right)$$

Result for buck-boost example

$$G_{vg}(s) = -\frac{D^2}{1 - D^2} \frac{1}{\left(1 + s \frac{RC}{1 + D} \right)}$$

Transfer functions predicted by simple model



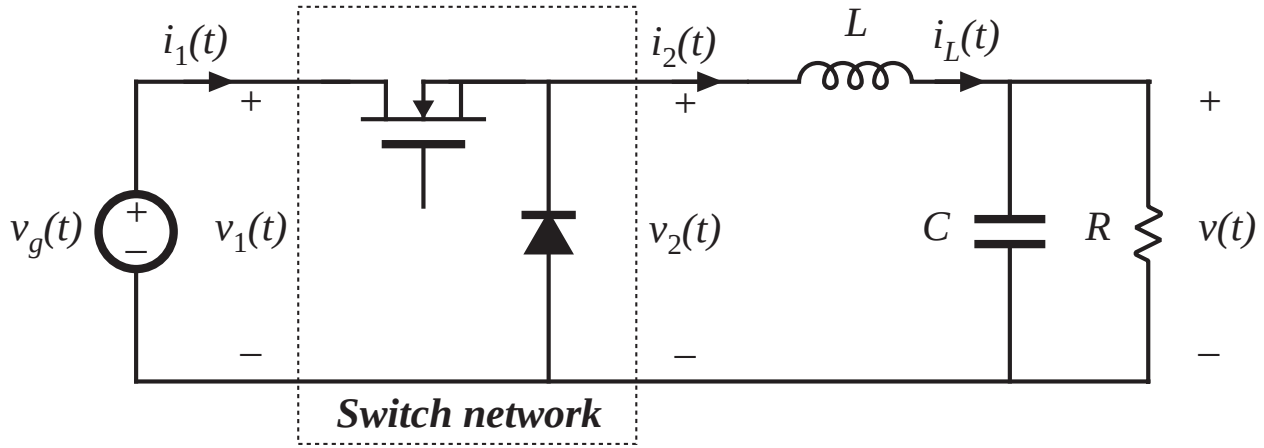
Output impedance

$$Z_{out}(s) = r_2 \parallel R \parallel \frac{1}{sC}$$

Result for buck-boost example

$$Z_{out}(s) = \frac{R}{1+D} \frac{1}{\left(1 + s \frac{RC}{1+D}\right)}$$

11.2.2 Averaged switch modeling
with the simple approximation



Averaged terminal waveforms, CCM:

$$\left\langle v_2(t) \right\rangle_{T_s} = d(t) \left\langle v_1(t) \right\rangle_{T_s}$$

$$\left\langle i_1(t) \right\rangle_{T_s} = d(t) \left\langle i_2(t) \right\rangle_{T_s}$$

The simple approximation:

$$\left\langle i_2(t) \right\rangle_{T_s} \approx \left\langle i_c(t) \right\rangle_{T_s}$$

CPM averaged switch equations

$$\left\langle v_2(t) \right\rangle_{T_s} = d(t) \left\langle v_1(t) \right\rangle_{T_s} \qquad \left\langle i_2(t) \right\rangle_{T_s} \approx \left\langle i_c(t) \right\rangle_{T_s}$$

$$\left\langle i_1(t) \right\rangle_{T_s} = d(t) \left\langle i_2(t) \right\rangle_{T_s}$$

Eliminate duty cycle:

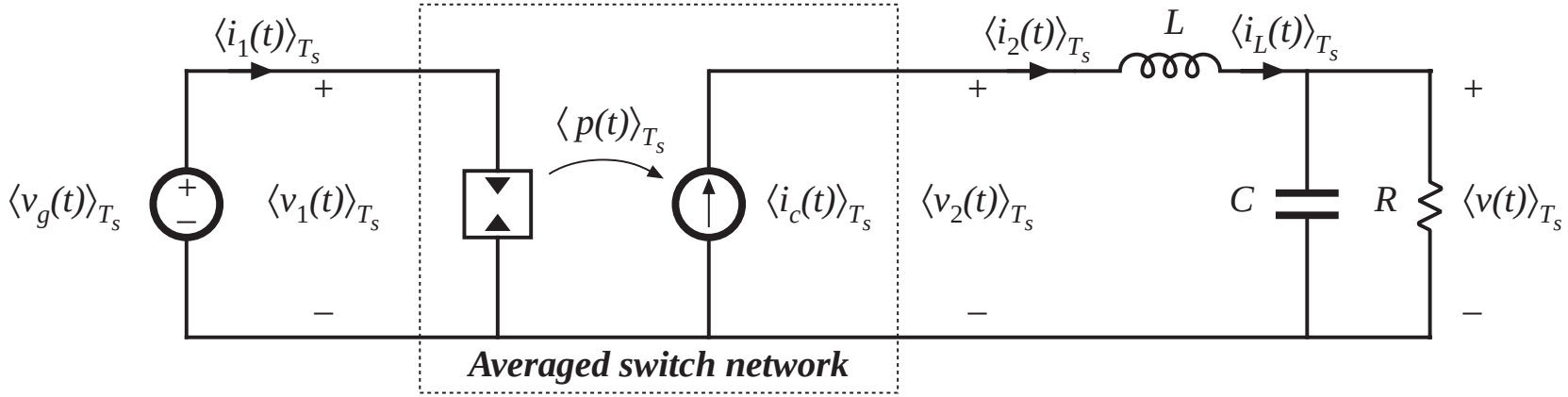
$$\left\langle i_1(t) \right\rangle_{T_s} = d(t) \left\langle i_c(t) \right\rangle_{T_s} = \frac{\left\langle v_2(t) \right\rangle_{T_s}}{\left\langle v_1(t) \right\rangle_{T_s}} \left\langle i_c(t) \right\rangle_{T_s}$$

$$\left\langle i_1(t) \right\rangle_{T_s} \left\langle v_1(t) \right\rangle_{T_s} = \left\langle i_c(t) \right\rangle_{T_s} \left\langle v_2(t) \right\rangle_{T_s} = \left\langle p(t) \right\rangle_{T_s}$$

So:

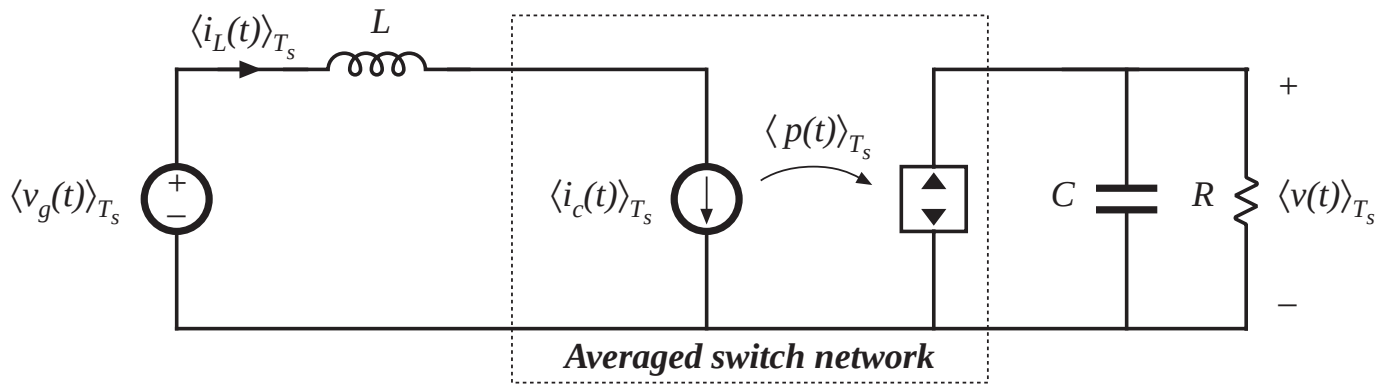
- Output port is a current source
- Input port is a dependent current sink

CPM averaged switch model

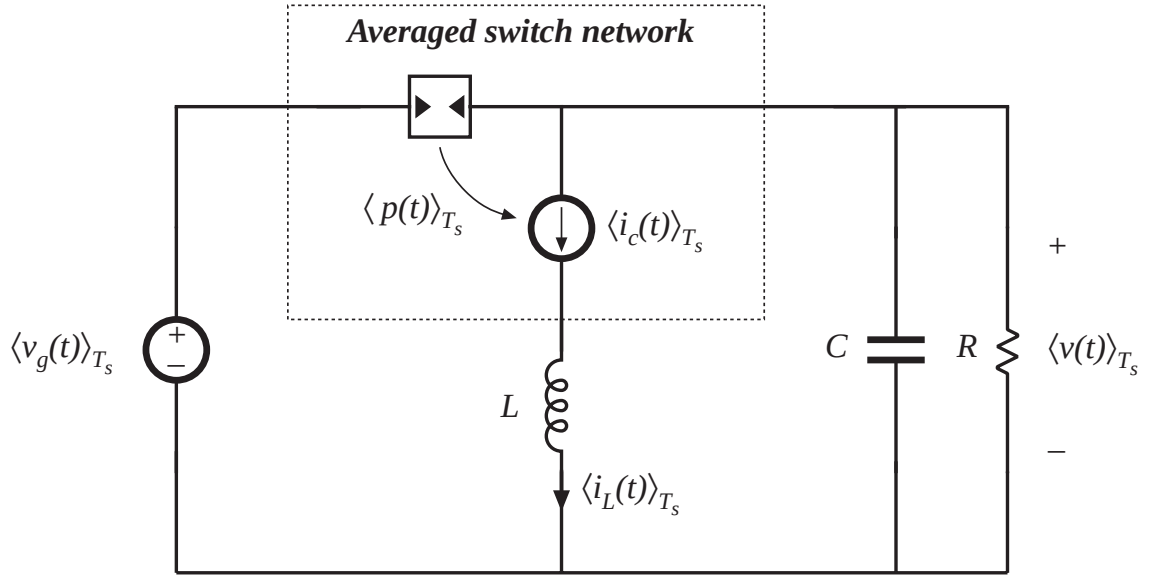


Results for other converters

Boost



Buck-boost



Perturbation and linearization to construct small-signal model

Let

$$\left\langle v_1(t) \right\rangle_{T_s} = V_1 + \hat{v}_1(t)$$
$$\left\langle i_1(t) \right\rangle_{T_s} = I_1 + \hat{i}_1(t)$$
$$\left\langle v_2(t) \right\rangle_{T_s} = V_2 + \hat{v}_2(t)$$
$$\left\langle i_2(t) \right\rangle_{T_s} = I_2 + \hat{i}_2(t)$$
$$\left\langle i_c(t) \right\rangle_{T_s} = I_c + \hat{i}_c(t)$$

Resulting input port equation:

$$\left(V_1 + \hat{v}_1(t)\right)\left(I_1 + \hat{i}_1(t)\right) = \left(I_c + \hat{i}_c(t)\right)\left(V_2 + \hat{v}_2(t)\right)$$

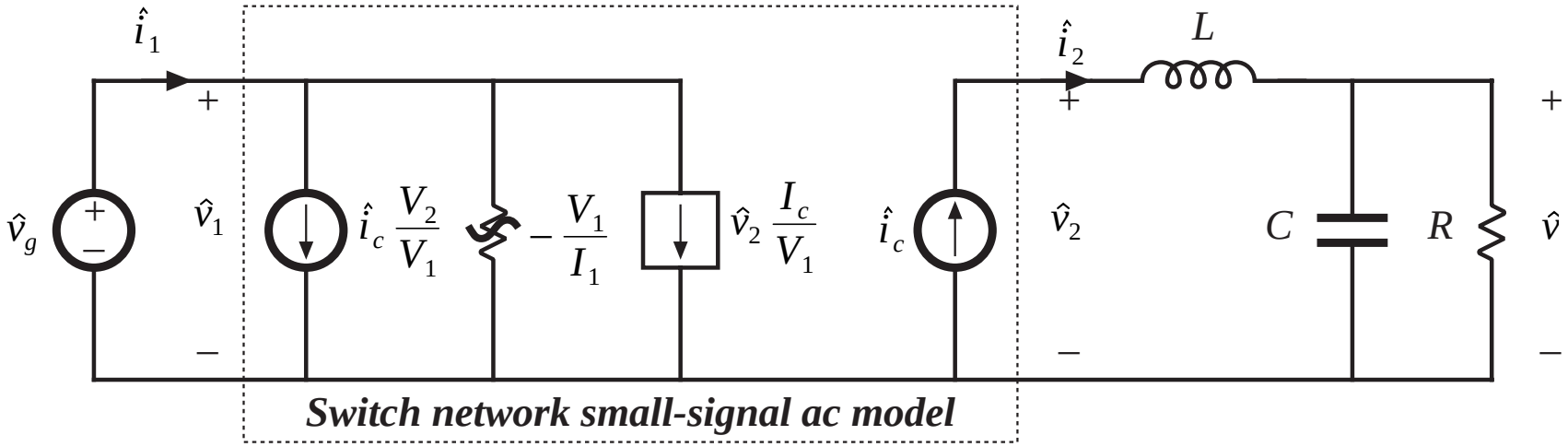
Small-signal result:

$$\hat{i}_1(t) = \hat{i}_c(t)\,\frac{V_2}{V_1} + \hat{v}_2(t)\,\frac{I_c}{V_1} - \hat{v}_1(t)\,\frac{I_1}{V_1}$$

Output port equation:

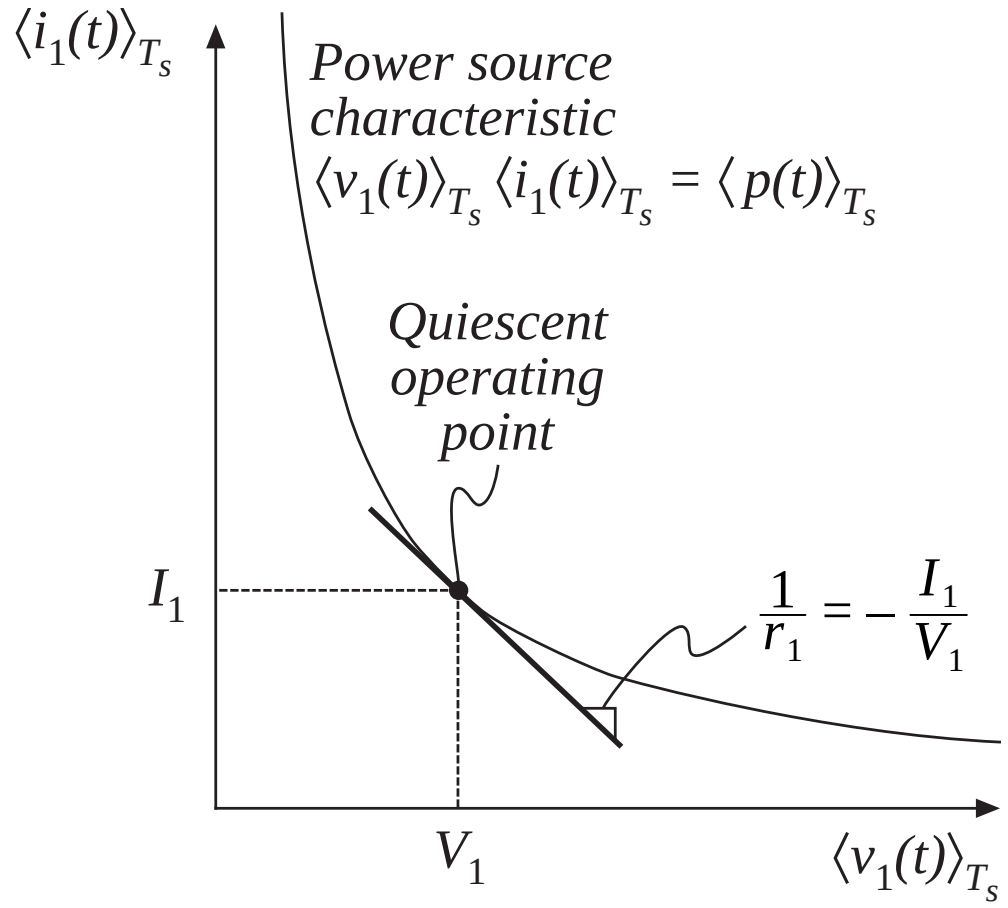
$$\hat{i}_2 = \hat{i}_c$$

Resulting small-signal model
Buck example

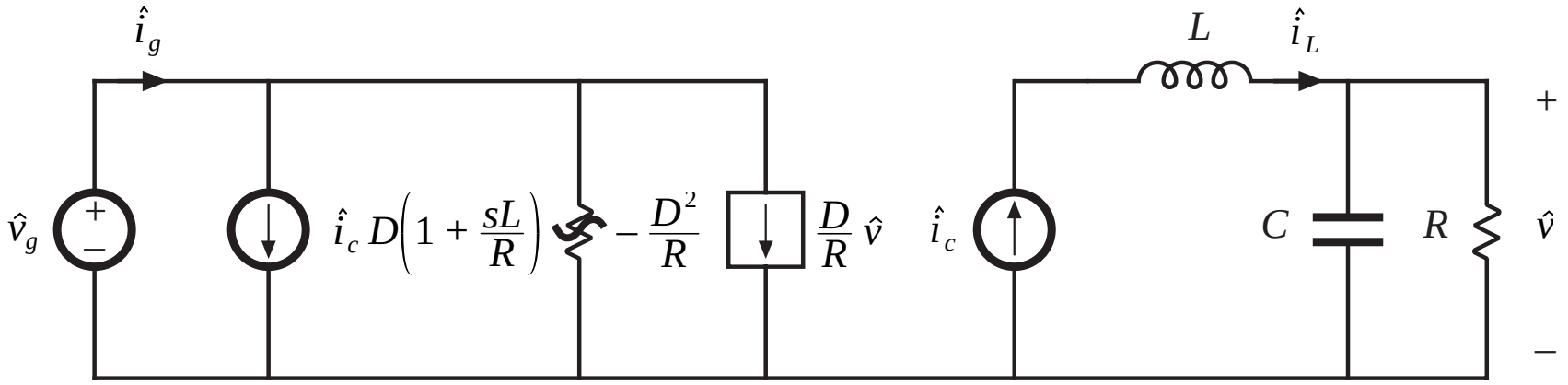


$$\hat{i}_1(t) = \hat{i}_c(t)\,\frac{V_2}{V_1} + \hat{v}_2(t)\,\frac{I_c}{V_1} - \hat{v}_1(t)\,\frac{I_1}{V_1}$$

Origin of input port negative incremental resistance

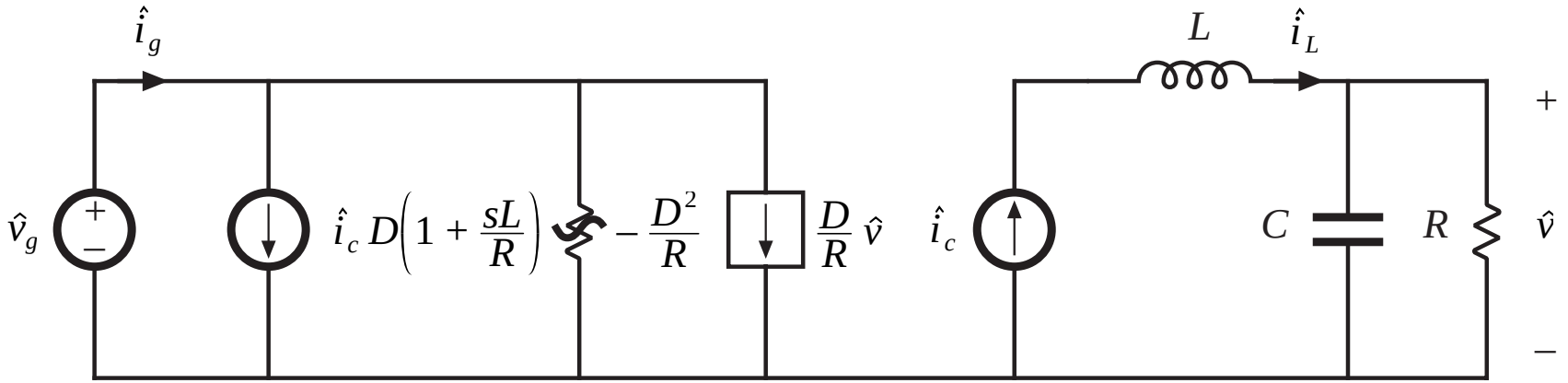


Expressing the equivalent circuit in terms of the converter input and output voltages



$$\hat{i}_1(s) = D\left(1 + s\frac{L}{R}\right)\hat{i}_c(s) + \frac{D}{R}\hat{v}(s) - \frac{D^2}{R}\hat{v}_g(s)$$

Predicted transfer functions of the CPM buck converter



$$G_{vc}(s) = \left.\frac{\hat{v}(s)}{\hat{i}_c(s)}\right|_{\hat{v}_g = 0} = \left(R \parallel \frac{1}{sC}\right)$$

$$G_{vg}(s) = \left.\frac{\hat{v}(s)}{\hat{v}_g(s)}\right|_{\hat{i}_c = 0} = 0$$

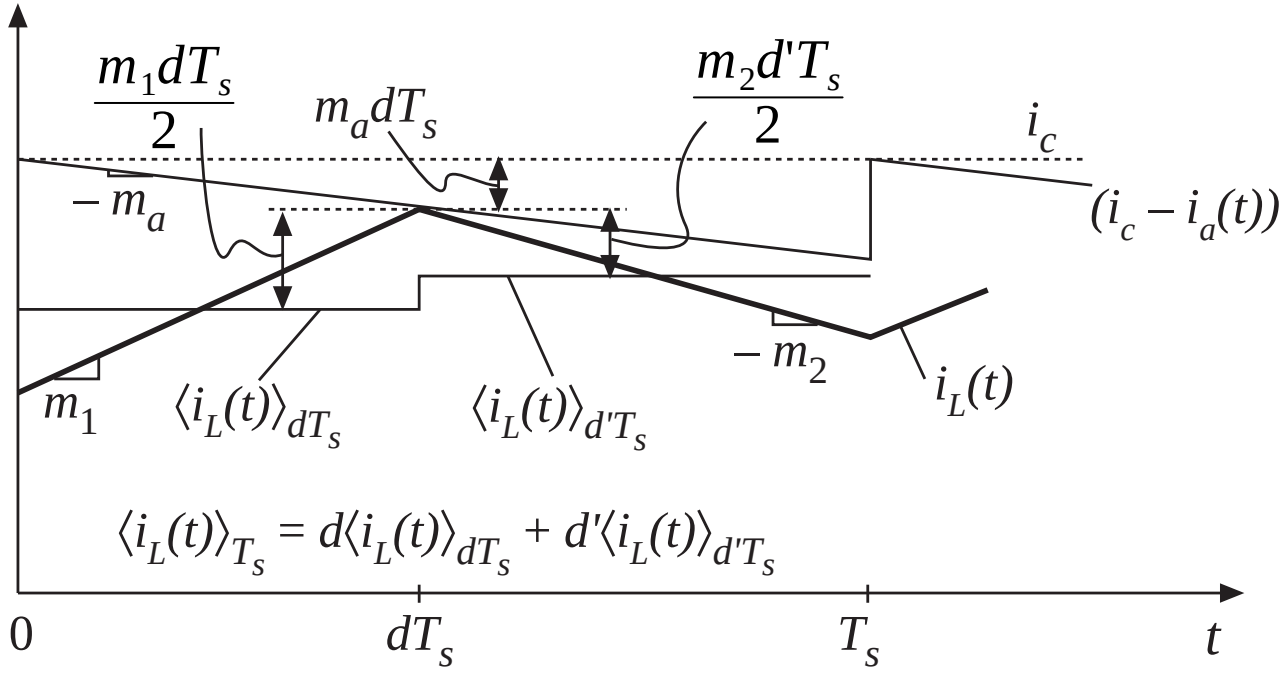
11.3 A More Accurate Model

- The simple models of the previous section yield insight into the low-frequency behavior of CPM converters
- Unfortunately, they do not always predict everything that we need to know:

  Line-to-output transfer function of the buck converter

  Dynamics at frequencies approaching f_s
- More accurate model accounts for nonideal operation of current mode controller built-in feedback loop
- Converter duty-cycle-controlled model, plus block diagram that accurately models equations of current mode controller

11.3.1 Current programmed controller model



$$\left\langle i_L(t)\right\rangle_{T_s} = \left\langle i_c(t)\right\rangle_{T_s} - m_a dT_s - d\,\frac{m_1 dT_s}{2} - d'\,\frac{m_2 d'T_s}{2}$$

$$= \left\langle i_c(t)\right\rangle_{T_s} - m_a dT_s - m_1\,\frac{d^2 T_s}{2} - m_2\,\frac{d'^2 T_s}{2}$$

Perturb

Let

$$\left\langle i_L(t) \right\rangle_{T_s} = I_L + \hat{i}_L(t)$$

$$\left\langle i_c(t) \right\rangle_{T_s} = I_c + \hat{i}_c(t)$$

$$d(t) = D + \hat{d}(t)$$

$$m_1(t) = M_1 + \hat{m}_1(t)$$

$$m_2(t) = M_2 + \hat{m}_2(t)$$

It is assumed that the artificial ramp slope does not vary.

Note that it is necessary to perturb the slopes, since these depend on the applied inductor voltage. For basic converters,

buck converter

$$\hat{m}_1 = \frac{\hat{v}_g - \hat{v}}{L} \qquad \hat{m}_2 = \frac{\hat{v}}{L}$$

boost converter

$$\hat{m}_1 = \frac{\hat{v}_g}{L} \qquad \hat{m}_2 = \frac{\hat{v} - \hat{v}_g}{L}$$

buck-boost converter

$$\hat{m}_1 = \frac{\hat{v}_g}{L} \qquad \hat{m}_2 = -\frac{\hat{v}}{L}$$

Linearize

$$\left(I_L + \hat{i}_L(t)\right) = \left(I_c + \hat{i}_c(t)\right) - M_a T_s \left(D + \hat{d}(t)\right) - \left(M_1 + \hat{m}_1(t)\right)\left(D + \hat{d}(t)\right)^2 \frac{T_s}{2}$$
$$- \left(M_2 + \hat{m}_2(t)\right)\left(D' - \hat{d}(t)\right)^2 \frac{T_s}{2}$$

The first-order ac terms are

$$\hat{i}_L(t) = \hat{i}_c(t) - \left(M_a T_s + D M_1 T_s - D' M_2 T_s\right) \hat{d}(t) - \frac{D^2 T_s}{2} \hat{m}_1(t) - \frac{D'^2 T_s}{2} \hat{m}_2(t)$$

Simplify using dc relationships:

$$\hat{i}_L(t) = \hat{i}_c(t) - M_a T_s \hat{d}(t) - \frac{D^2 T_s}{2} \hat{m}_1(t) - \frac{D'^2 T_s}{2} \hat{m}_2(t)$$

Solve for duty cycle variations:

$$\hat{d}(t) = \frac{1}{M_a T_s} \left[\hat{i}_c(t) - \hat{i}_L(t) - \frac{D^2 T_s}{2} \hat{m}_1(t) - \frac{D'^2 T_s}{2} \hat{m}_2(t) \right]$$

Equation of the current programmed controller

The expression for the duty cycle is of the general form

$$\hat{d}(t) = F_m \left[\hat{i}_c(t) - \hat{i}_L(t) - F_g \hat{v}_g(t) - F_v \hat{v}(t) \right]$$

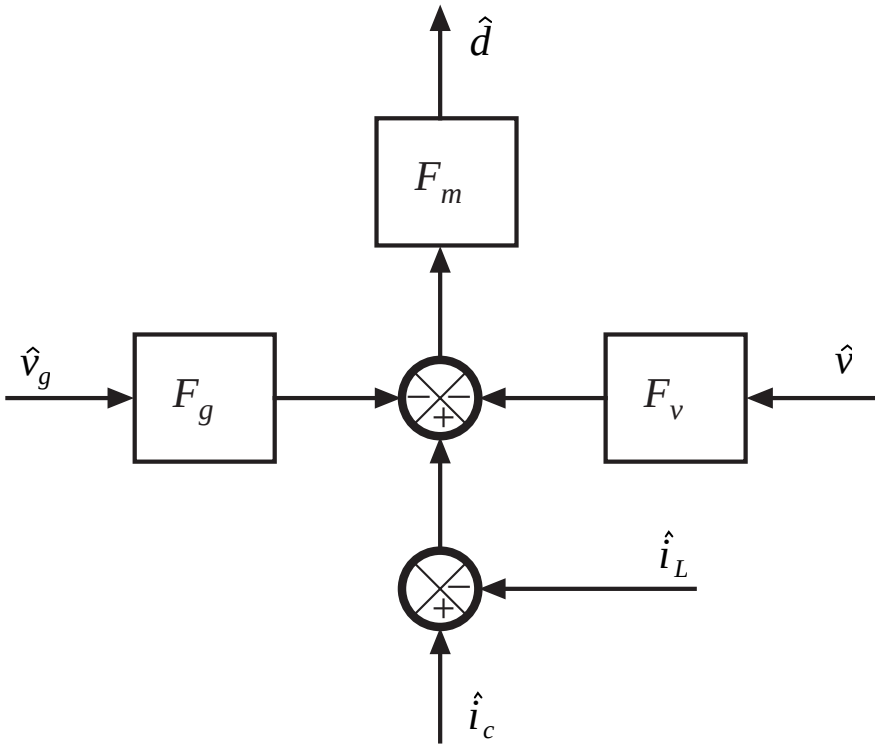
$$F_m = 1/M_a T_s$$

Table 11.2. Current programmed controller gains for basic converters

Converter	F_g	F_v
Buck	$\frac{D^2 T_s}{2L}$	$\frac{\left(1-2D\right) T_s}{2L}$
Boost	$\frac{\left(2D-1\right) T_s}{2L}$	$\frac{D'^2 T_s}{2L}$
Buck-boost	$\frac{D^2 T_s}{2L}$	$-\frac{D'^2 T_s}{2L}$

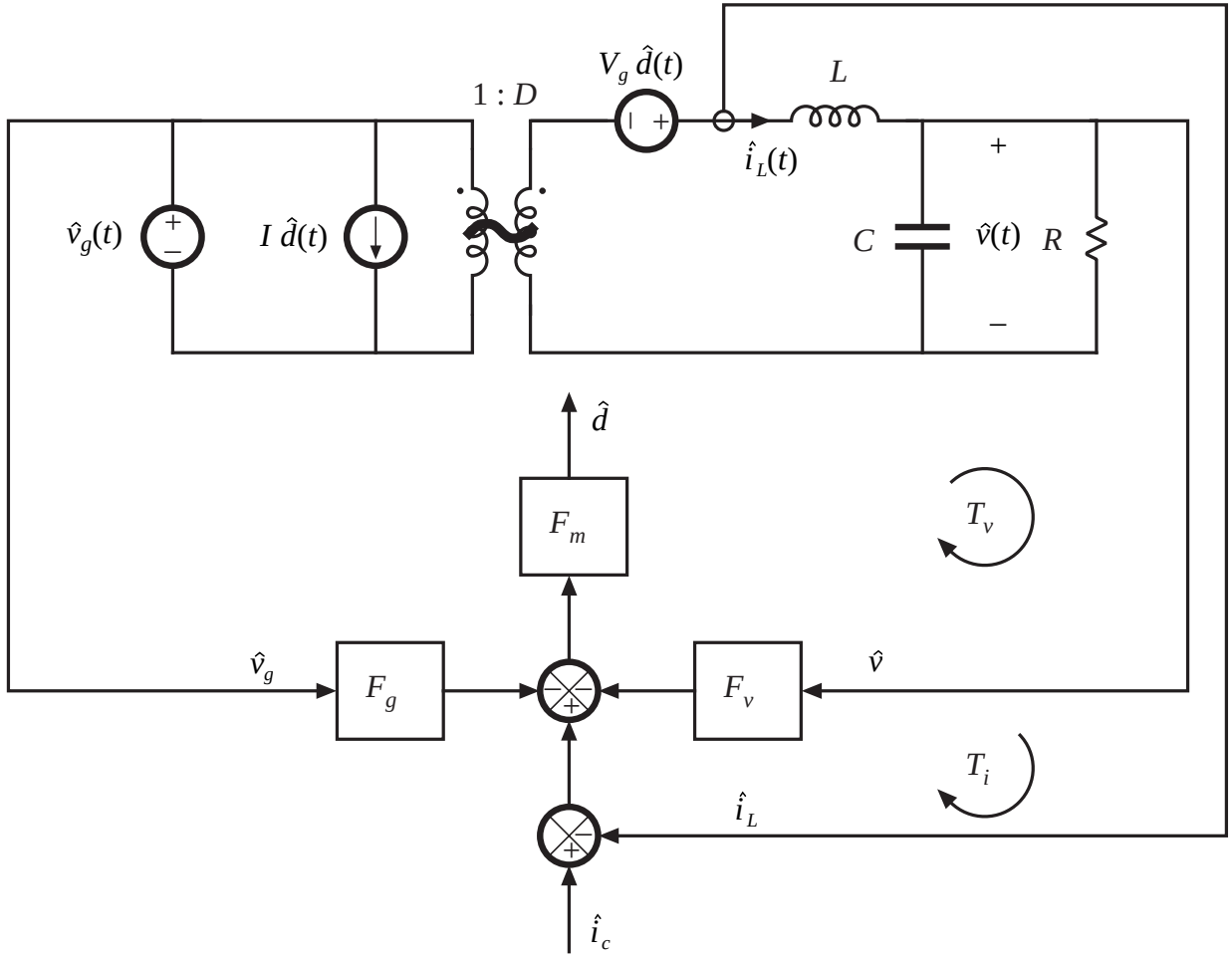
Block diagram of the current programmed controller

$$\hat{d}(t) = F_m \left[\hat{i}_c(t) - \hat{i}_L(t) - F_g \hat{v}_g(t) - F_v \hat{v}(t) \right]$$

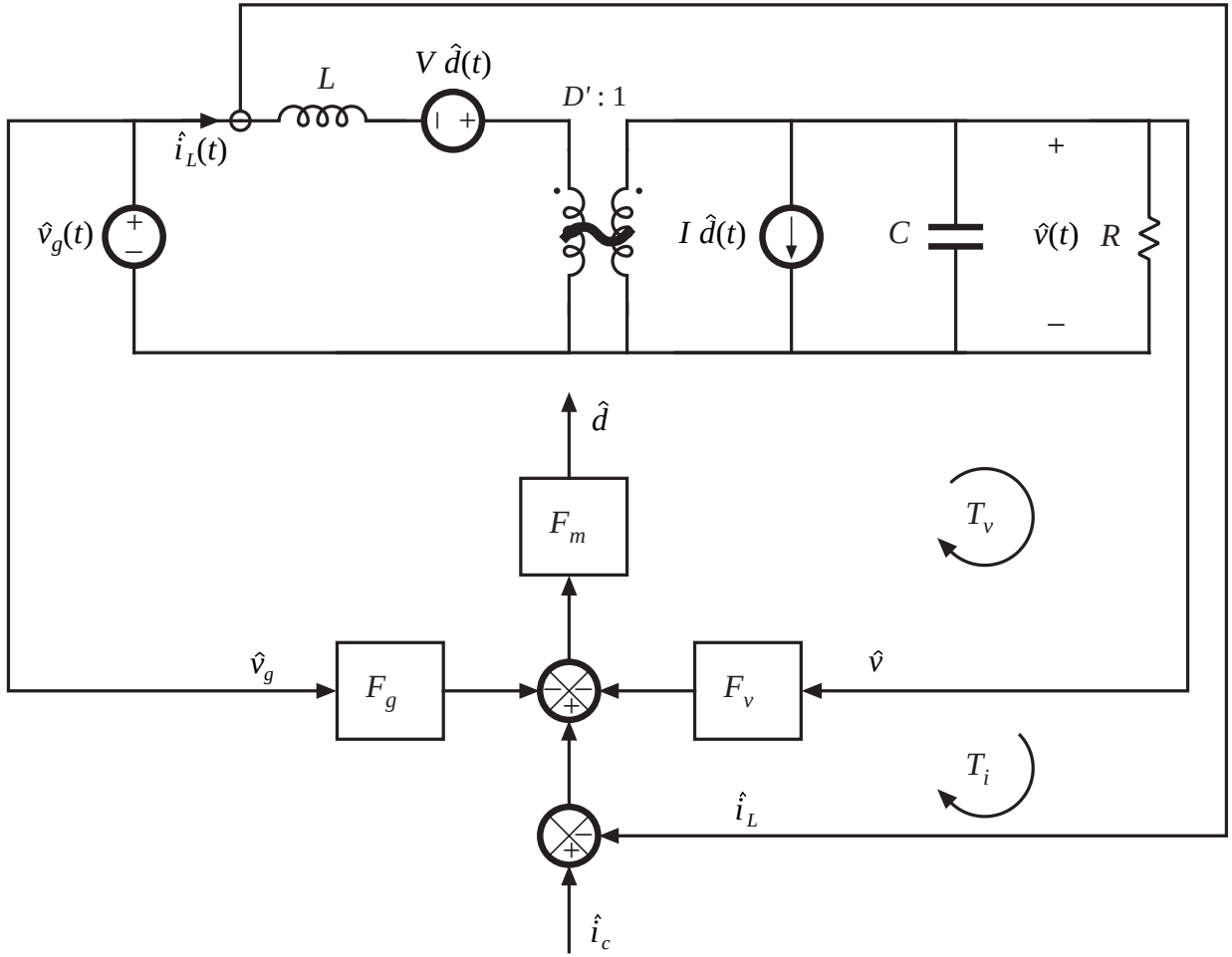


- Describes the duty cycle chosen by the CPM controller
- Append this block diagram to the duty cycle controlled converter model, to obtain a complete CPM system model

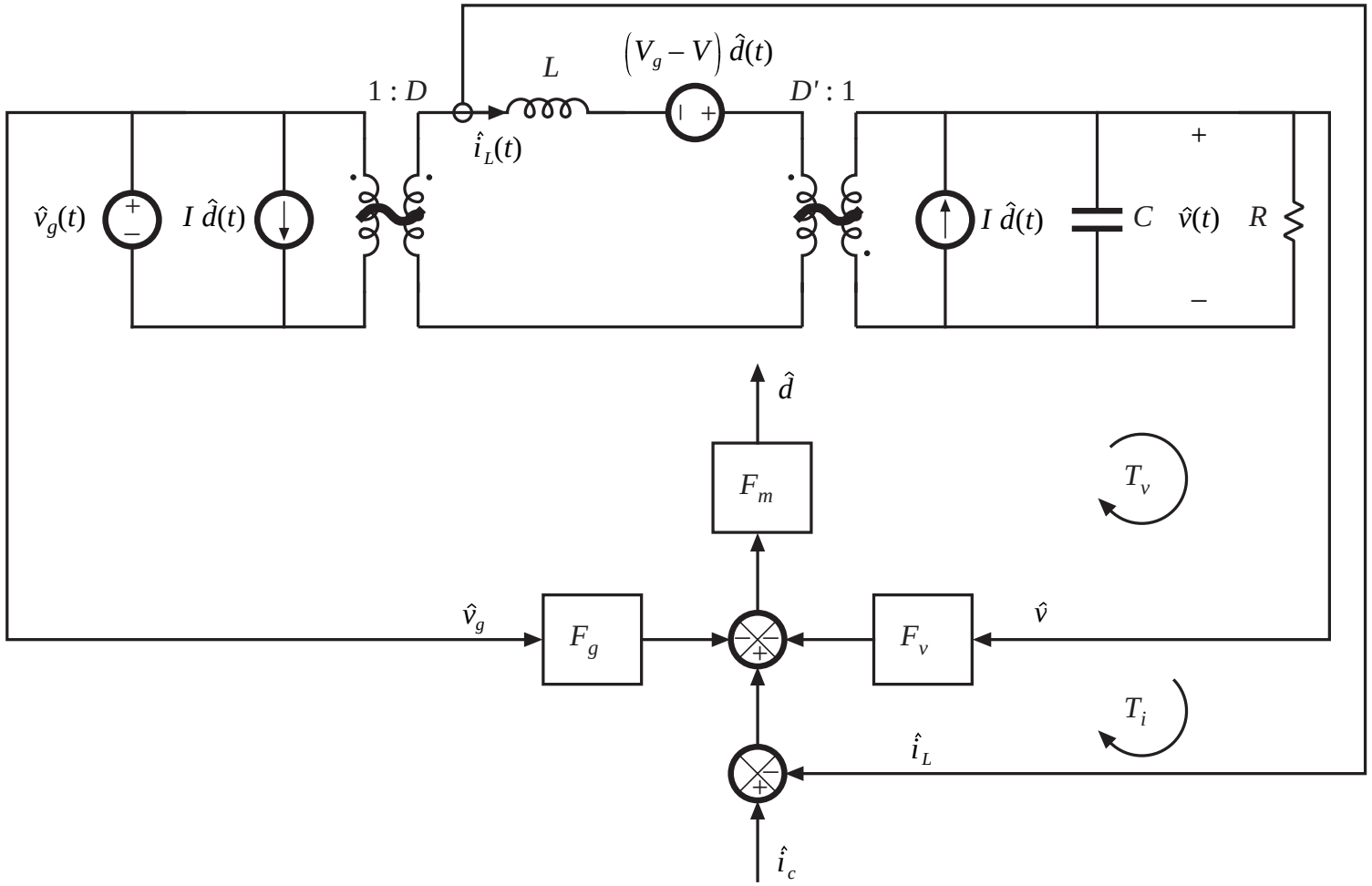
CPM buck converter model



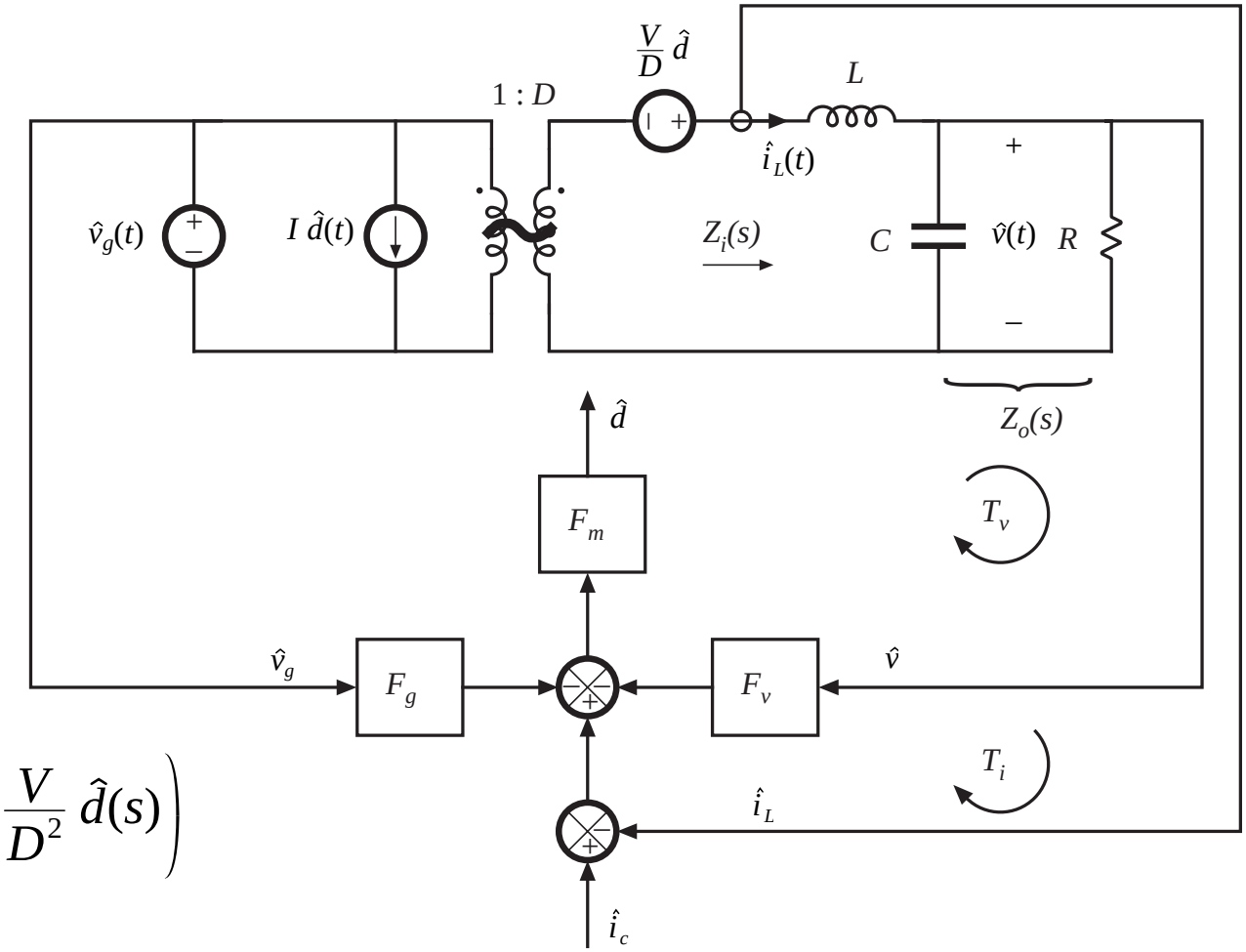
CPM boost converter model



CPM buck-boost converter model



11.3.2 Example: analysis of CPM buck converter



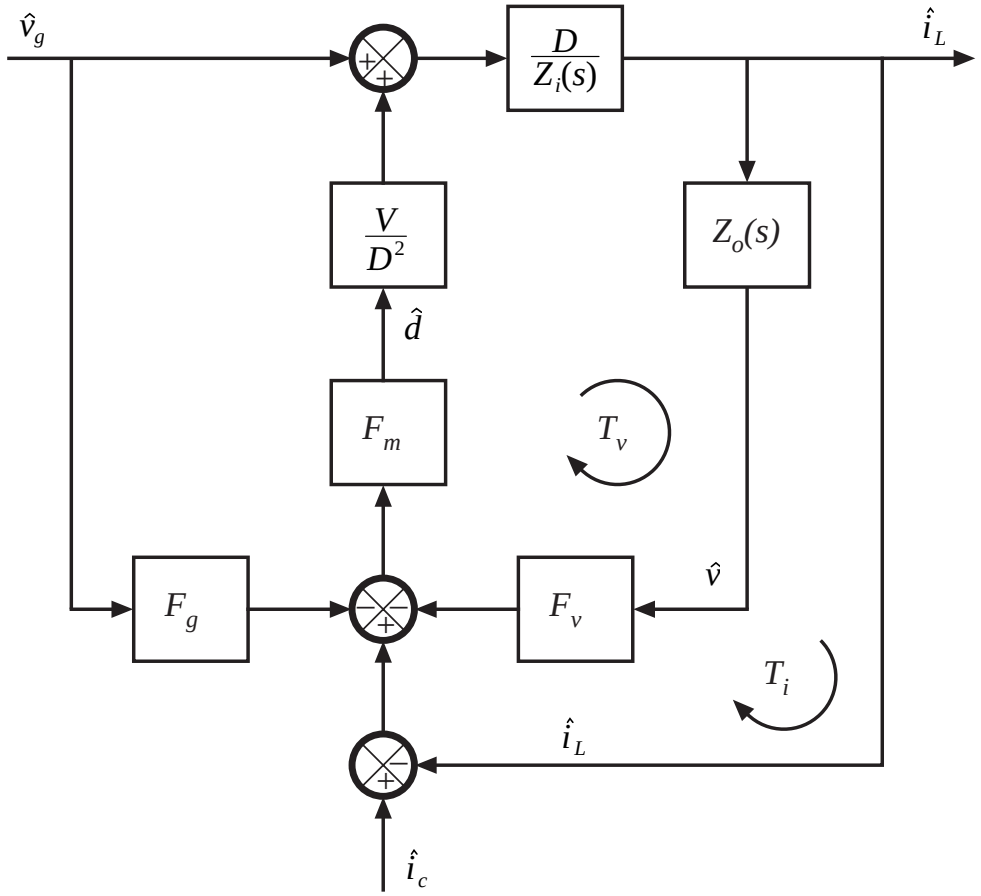
$$Z_o = R \parallel \frac{1}{sC}$$

$$Z_i = sL + \left(R \parallel \frac{1}{sC} \right)$$

$$\hat{i}_L(s) = \frac{D}{Z_i(s)} \left(\hat{v}_g(s) + \frac{V}{D^2}\,\hat{d}(s) \right)$$

$$\hat{v}(s) = \hat{i}_L(s)\, Z_o(s)$$

Block diagram of entire CPM buck converter



Voltage loop gain:

$$T_v(s) = F_m \frac{V}{D^2} \frac{D}{Z_i(s)} Z_o(s) F_v$$

Current loop gain:

$$T_i(s) = \frac{1}{Z_o(s) F_v} \frac{T_v(s)}{1 + T_v(s)}$$

$$T_i(s) = \frac{F_m \frac{V}{D^2} \frac{D}{Z_i(s)}}{1 + F_m \frac{V}{D^2} \frac{D}{Z_i(s)} Z_o(s) F_v}$$

Transfer function from $\hat{i}_c$ to $\hat{i}_L$:

$$\frac{\hat{i}_L(s)}{\hat{i}_c(s)} = \frac{T_i(s)}{1 + T_i(s)}$$

Discussion: Transfer function from $\hat{i}_c$ to $\hat{i}_L$

- When the loop gain Ti(s) is large in magnitude, then $\hat{i}_L$ is approximately equal to $\hat{i}_c$. The results then coincide with the simple approximation.

$$\frac{\hat{i}_L(s)}{\hat{i}_c(s)} = \frac{T_i(s)}{1 + T_i(s)}$$

- The control-to-output transfer function can be written as

$$G_{vc}(s) = \frac{\hat{v}(s)}{\hat{i}_c(s)} = Z_o(s) \frac{T_i(s)}{1 + T_i(s)}$$

which is the simple approximation result, multiplied by the factor $T_i/(1 + T_i)$.

Loop gain $T_i(s)$

Result for the buck converter:

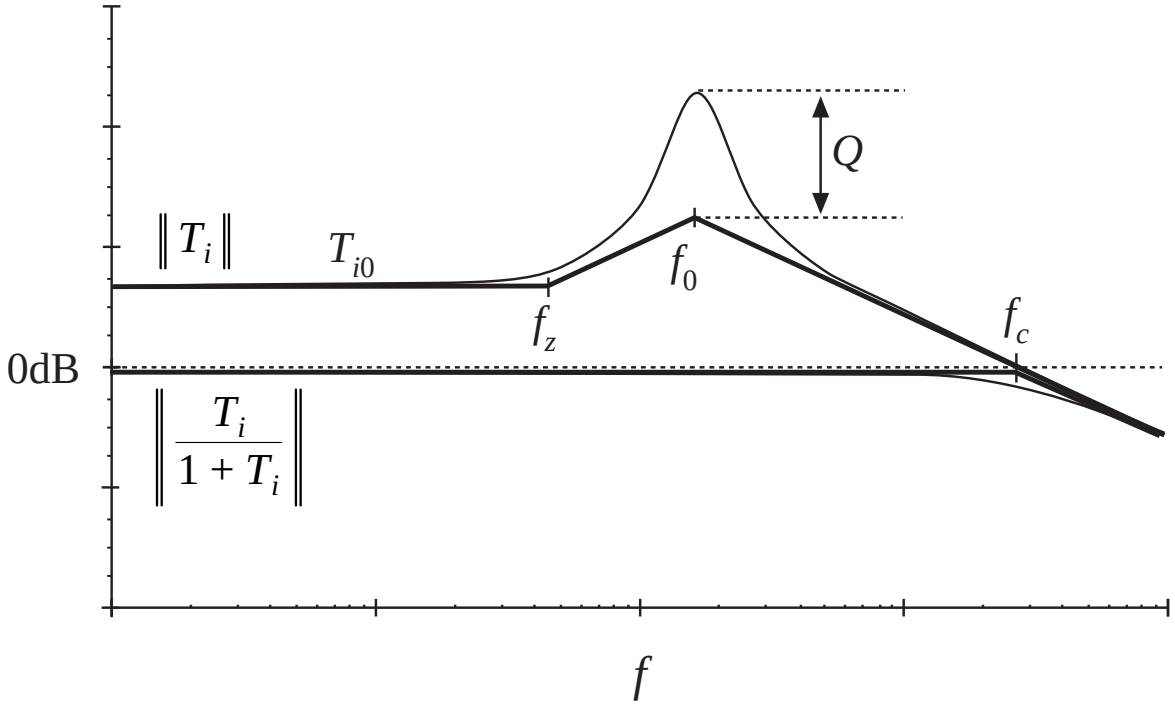
$$T_i(s) = \left(K \frac{1-\alpha}{1+\alpha} \right) \frac{\left(1 + sRC\right)}{1 + s\left(\frac{L}{R} \frac{2DM_a}{M_2} \frac{1-\alpha}{1+\alpha} \right) + s^2 \left(LC \frac{2DM_a}{M_2} \frac{1-\alpha}{1+\alpha} \right)}$$

Characteristic value $\alpha = -\dfrac{1 - \dfrac{m_a}{m_2}}{\dfrac{D'}{D} + \dfrac{m_a}{m_2}}$ Controller stable for $|\alpha| < 1$

$K = 2L/RT_s$

CCM for $K > D'$

Loop gain



$$T_i(s) = T_{i0} \frac{\left(1 + \frac{s}{\omega_z}\right)}{1 + \frac{s}{Q\omega_0} + \left(\frac{s}{\omega_0}\right)^2}$$

$$T_{i0} = K \frac{1 - \alpha}{1 + \alpha}$$

$$\omega_z = \frac{1}{RC}$$

$$\omega_0 = \frac{1}{\sqrt{LC \frac{2DM_a}{M_2} \frac{1 - \alpha}{1 + \alpha}}}$$

$$Q = R \sqrt{\frac{C}{L}} \sqrt{\frac{M_2}{2DM_a} \frac{1 + \alpha}{1 - \alpha}}$$

Crossover frequency f_c

High frequency asymptote of T_i is

$$T_i(s) \approx T_{i0} \frac{\left(\frac{s}{\omega_z}\right)}{\left(\frac{s}{\omega_0}\right)^2} = T_{i0} \frac{\omega_0^2}{s\omega_z}$$

Equate magnitude to one at crossover frequency:

$$\left\| T_i(j2\pi f_c) \right\| \approx T_{i0} \frac{f_0^2}{2\pi f_c f_z} = 1$$

Solve for crossover frequency:

$$f_c = \frac{M_2}{M_a} \frac{f_s}{2\pi D}$$

Construction of transfer functions

$$\frac{\hat{i}_L(s)}{\hat{i}_c(s)} = \frac{T_i(s)}{1 + T_i(s)} \approx \frac{1}{\left(1 + \frac{s}{\omega_c}\right)}$$

$$G_{vc}(s) = Z_o(s) \frac{T_i(s)}{1 + T_i(s)} \approx R \frac{1}{\left(1 + sRC\right)\left(1 + \frac{s}{\omega_c}\right)}$$

—the result of the simple first-order model, with an added pole at the loop crossover frequency

Exact analysis

$$G_{vc}(s) = R\left(\frac{T_{i0}}{1+T_{i0}}\right)\frac{1}{1+s\left(\frac{T_{i0}}{1+T_{i0}}\frac{1}{\omega_z}+\frac{1}{\left(1+T_{i0}\right)Q\omega_0}\right)+\frac{1}{1+T_{i0}}\left(\frac{s}{\omega_0}\right)^2}$$

for $|T_{i0}| >> 1$,

$$G_{vc}(s) \approx R\frac{1}{1+\frac{s}{\omega_z}+\frac{s^2}{T_{i0}\,\omega_0^2}}$$

Low Q approximation:

$$G_{vc}(s) \approx R\frac{1}{\left(1+\frac{s}{\omega_z}\right)\left(1+\frac{s\omega_z}{T_{i0}\omega_0^2}\right)}$$

which agrees with the previous slide

Line-to-output transfer function

Solution of complete block diagram leads to

$$\hat{v}(s) = \hat{i}_c(s)\, Z_o(s)\, \frac{T_i(s)}{1 + T_i(s)} + \hat{v}_g(s)\, \frac{G_{g0}(s)}{1 + T_i(s)}$$

with

$$G_{g0}(s) = Z_o(s)\, \frac{D}{Z_i(s)}\, \frac{\left(1 - \frac{V}{D^2} F_m F_g\right)}{\left(1 + \frac{V}{D^2} F_m F_v Z_o(s)\, \frac{D}{Z_i(s)}\right)}$$

Line-to-output transfer function

$$G_{vg}(s) = \left. \frac{\hat{v}(s)}{\hat{v}_g(s)} \right|_{\hat{i}_c(s) = 0} = \frac{G_{g0}(s)}{1 + T_i(s)}$$

$$G_{vg}(s) = \frac{\left(\frac{1}{1 + T_{i0}} \right) \frac{(1 - \alpha)}{(1 + \alpha)} 2D^2 \left(\frac{M_a}{M_2} - \frac{1}{2} \right)}{1 + s \left(\frac{T_{i0}}{1 + T_{i0}} \frac{1}{\omega_z} + \frac{1}{\left(1 + T_{i0}\right) Q \omega_0} \right) + \frac{1}{1 + T_{i0}} \left(\frac{s}{\omega_0} \right)^2}$$

Poles are identical to control-to-output transfer function, and can be factored the same way:

$$G_{vg}(s) \approx \frac{G_{vg}(0)}{\left(1 + \frac{s}{\omega_z} \right) \left(1 + \frac{s}{\omega_c} \right)}$$

Line-to-output transfer function: dc gain

$$G_{vg}(0) \approx \frac{2D^2}{K}\left(\frac{M_a}{M_2} - \frac{1}{2}\right)$$ for large T_{i0}

For any T_{i0} , the dc gain goes to zero when $M_a/M_2 = 0.5$

Effective feedforward of input voltage variations in CPM controller then effectively cancels out the v_g variations in the direct forward path of the converter.

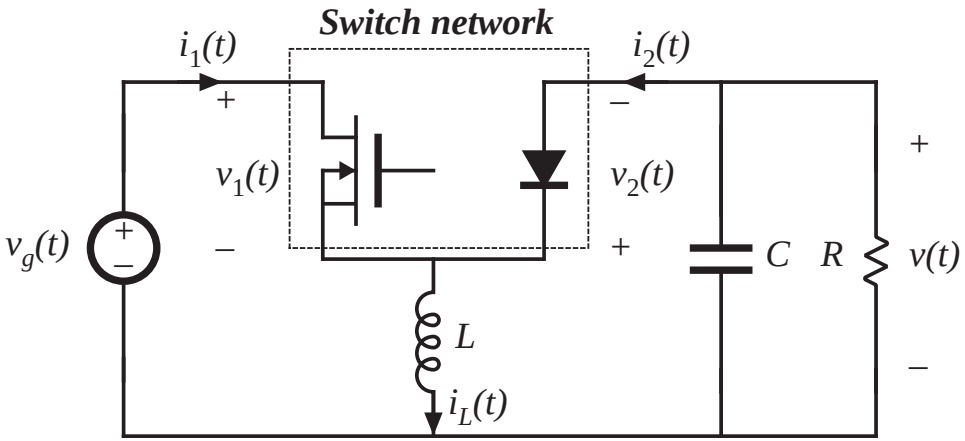
11.4 Discontinuous conduction mode

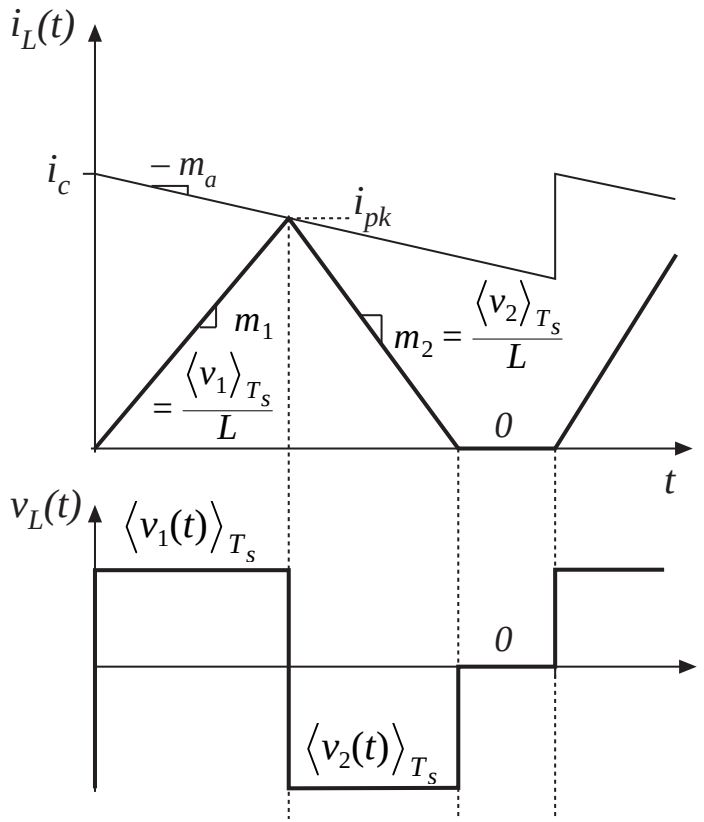
- Again, use averaged switch modeling approach
- Result: simply replace

  Transistor by power sink

  Diode by power source
- Inductor dynamics appear at high frequency, near to or greater than the switching frequency
- Small-signal transfer functions contain a single low frequency pole
- DCM CPM boost and buck-boost are stable without artificial ramp
- DCM CPM buck without artificial ramp is stable for $D < 2/3$. A small artificial ramp $m_a \geq 0.086 m_2$ leads to stability for all D.

DCM CPM buck-boost example





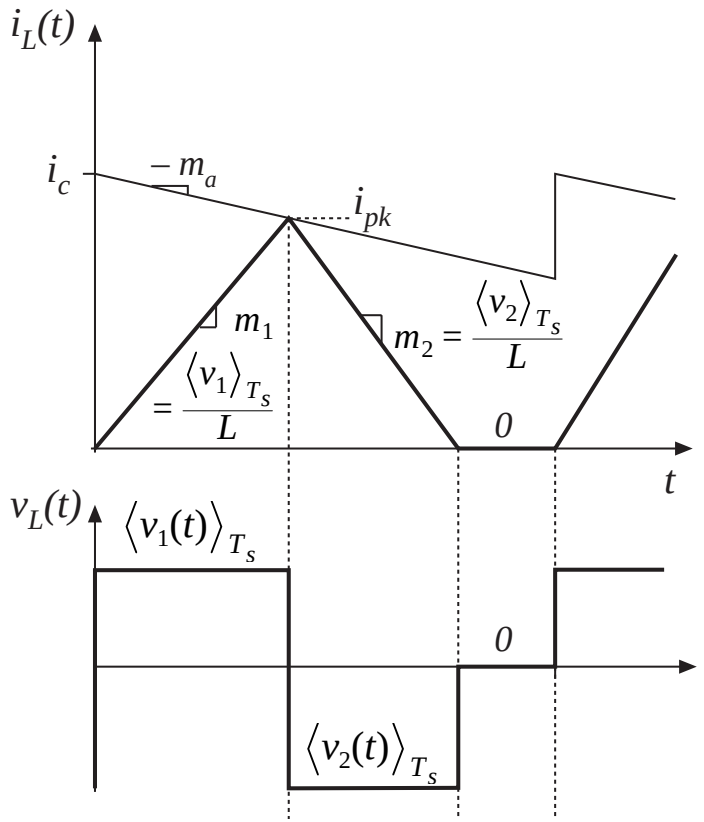
Analysis

$$i_{pk} = m_1 d_1 T_s$$

$$m_1 = \frac{\left\langle v_1(t) \right\rangle_{T_s}}{L}$$

$$\begin{aligned} i_c &= i_{pk} + m_a d_1 T_s \\ &= \left(m_1 + m_a \right) d_1 T_s \end{aligned}$$

$$d_1(t) = \frac{i_c(t)}{\left(m_1 + m_a \right) T_s}$$



Averaged switch input port equation

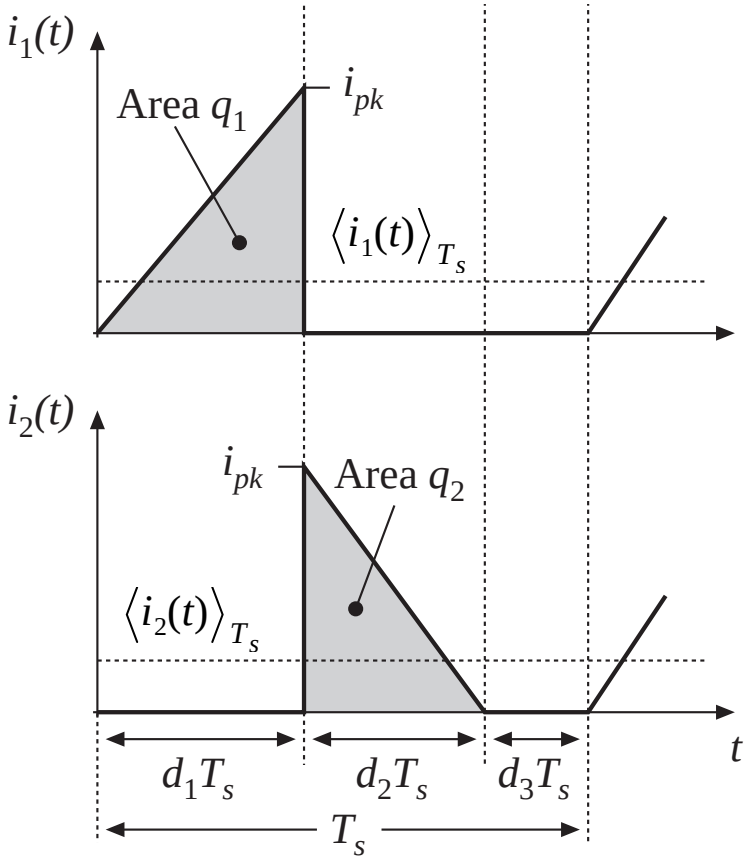
$$\left\langle i_1(t) \right\rangle_{T_s} = \frac{1}{T_s} \int_t^{t+T_s} i_1(\tau) \mathrm{d}\tau = \frac{q_1}{T_s}$$

$$\left\langle i_1(t) \right\rangle_{T_s} = \frac{1}{2} i_{pk}(t) d_1(t)$$

$$\left\langle i_1(t) \right\rangle_{T_s} = \frac{1}{2} m_1 d_1^2(t) T_s$$

$$\left\langle i_1(t) \right\rangle_{T_s} = \frac{\frac{1}{2} L i_c^2 f_s}{\left\langle v_1(t) \right\rangle_{T_s} \left(1 + \frac{m_a}{m_1} \right)^2}$$

$$\left\langle i_1(t) \right\rangle_{T_s} \left\langle v_1(t) \right\rangle_{T_s} = \frac{\frac{1}{2} L i_c^2 f_s}{\left(1 + \frac{m_a}{m_1} \right)^2} = \left\langle p(t) \right\rangle_{T_s}$$



Discussion: switch network input port

- Averaged transistor waveforms obey a power sink characteristic
- During first subinterval, energy is transferred from input voltage source, through transistor, to inductor, equal to

$$W = \frac{1}{2} L i_{pk}^2$$

This energy transfer process accounts for power flow equal to

$$\left\langle p(t) \right\rangle_{T_s} = W f_s = \frac{1}{2} L i_{pk}^2 f_s$$

which is equal to the power sink expression of the previous slide.

Averaged switch output port equation

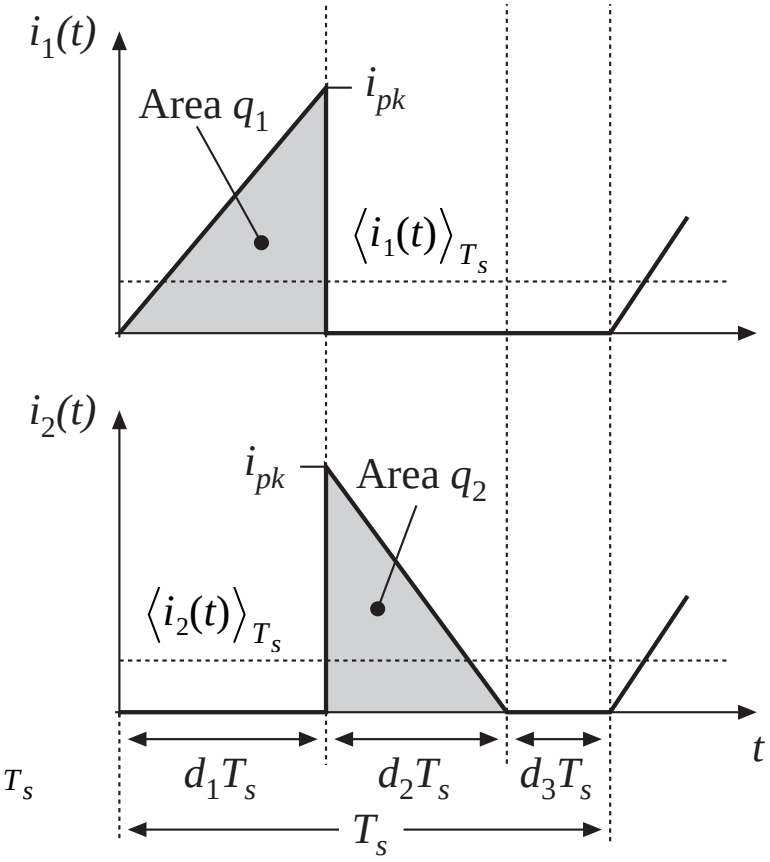
$$\left\langle i_2(t)\right\rangle_{T_s} = \frac{1}{T_s}\int_t^{t+T_s} i_2(\tau)\,\mathrm{d}\tau = \frac{q_2}{T_s}$$

$$q_2 = \tfrac{1}{2}\, i_{pk} d_2 T_s$$

$$d_2(t) = d_1(t)\,\frac{\left\langle v_1(t)\right\rangle_{T_s}}{\left\langle v_2(t)\right\rangle_{T_s}}$$

$$\left\langle i_2(t)\right\rangle_{T_s} = \frac{\left\langle p(t)\right\rangle_{T_s}}{\left\langle v_2(t)\right\rangle_{T_s}}$$

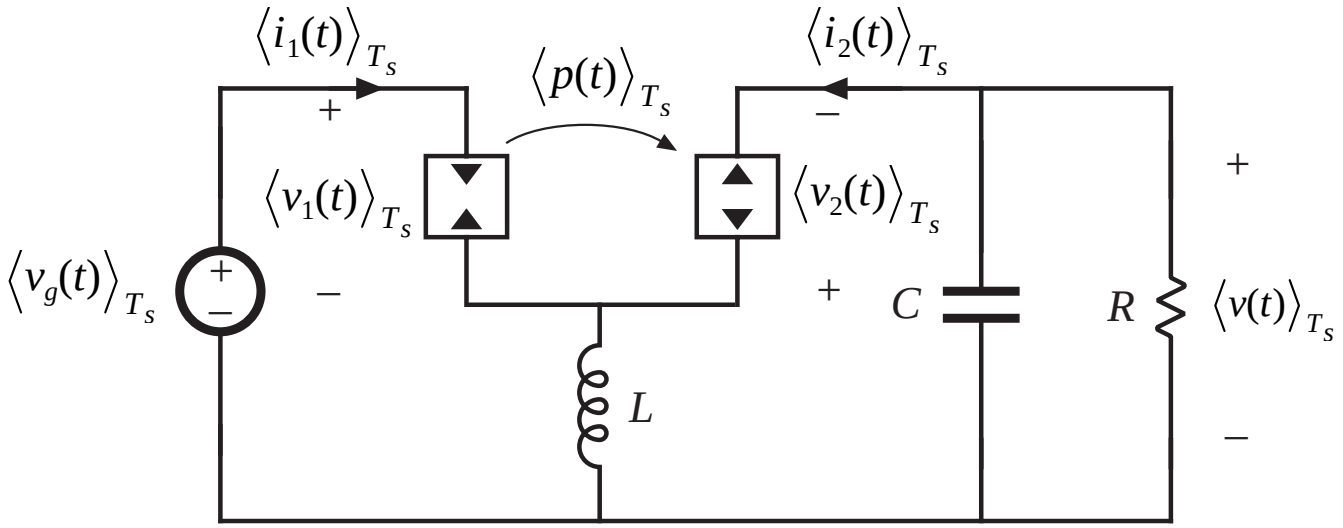
$$\left\langle i_2(t)\right\rangle_{T_s}\left\langle v_2(t)\right\rangle_{T_s} = \frac{\frac{1}{2} L i_c^2(t) f_s}{\left(1+\frac{m_a}{m_1}\right)^2} = \left\langle p(t)\right\rangle_{T_s}$$



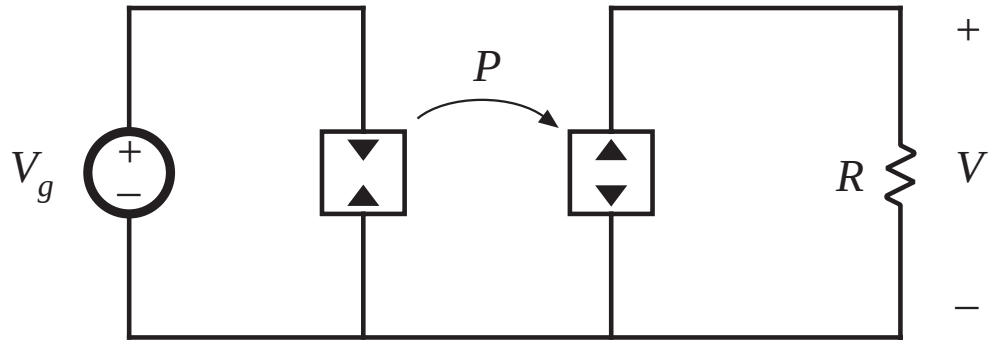
Discussion: switch network output port

- Averaged diode waveforms obey a power sink characteristic
- During second subinterval, all stored energy in inductor is transferred, through diode, to load
- Hence, in averaged model, diode becomes a power source, having value equal to the power consumed by the transistor power sink element

Averaged equivalent circuit



Steady state model: DCM CPM buck-boost



Solution

$$\frac{V^2}{R} = P$$

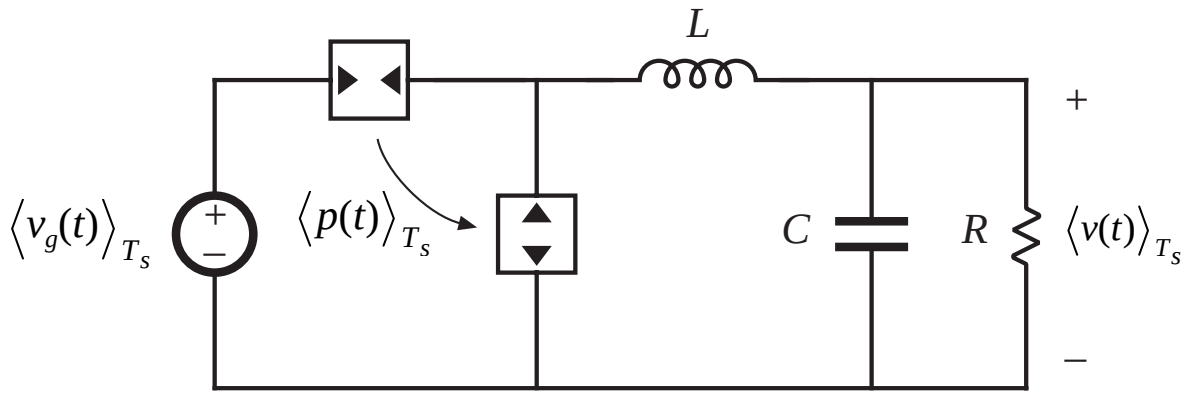
$$P = \frac{\frac{1}{2} L I_c^2(t) f_s}{\left(1 + \frac{M_a}{M_1}\right)^2}$$

$$V = \sqrt{PR} = I_c \sqrt{\frac{RL f_s}{2\left(1 + \frac{M_a}{M_1}\right)^2}}$$

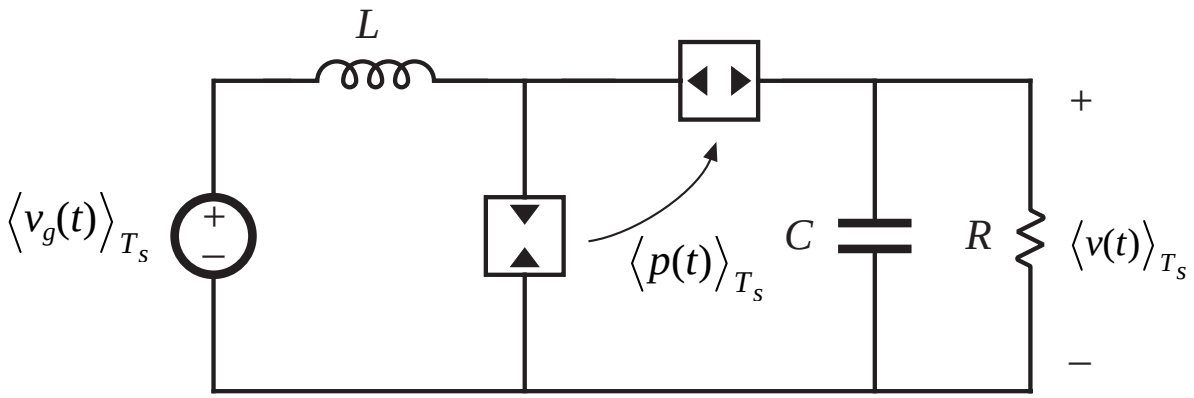
for a resistive load

Models of buck and boost

Buck



Boost



Summary of steady-state DCM CPM characteristics

Table 11.3. Steady-state DCM CPM characteristics of basic converters

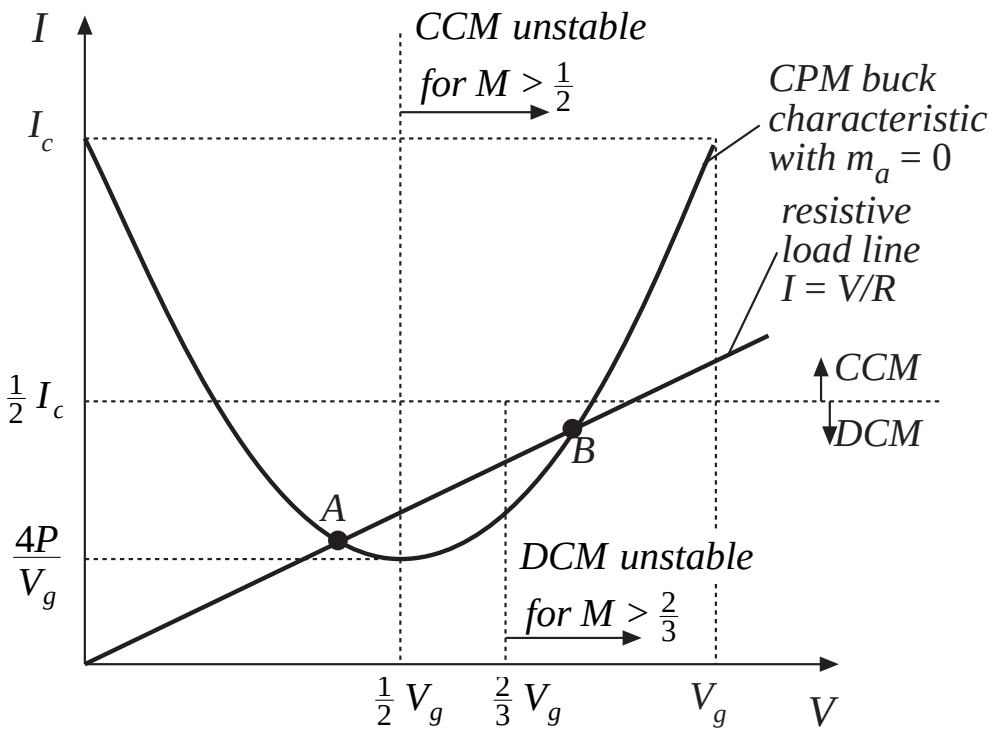
Converter	M	I_{crit}	Stability range when $m_a = 0$
Buck	$\frac{P_{load} - P}{P_{load}}$	$\frac{1}{2}\left(I_c - M\, m_a\, T_$	$0 \le M < \frac{2}{3}$
Boost	$\frac{P_{load}}{P_{load} - P}$	$\frac{\left(I_c - \frac{M-1}{M}\, m_a\, T_s\right)}{2\, M}$	$0 \le D \le 1$
Buck-boost	Depends on load characteristic: $P_{load} = P$	$\frac{\left(I_c - \frac{M}{M-1}\, m_a\, T_s\right)}{2\left(M-1\right)}$	$0 \le D \le 1$

$$\left|I\right| > \left|I_{crit}\right| \quad \text{for CCM}$$

$$\left|I\right| < \left|I_{crit}\right| \quad \text{for DCM}$$

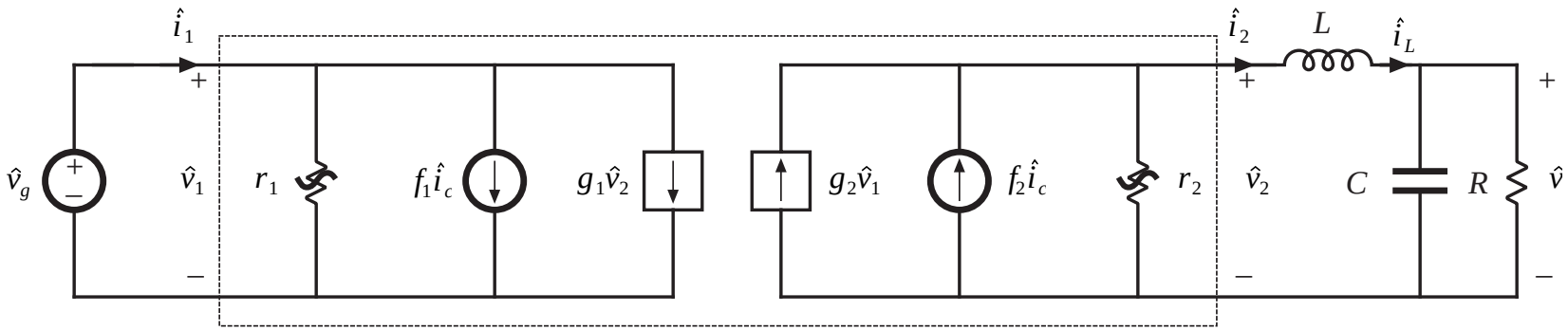
Buck converter: output characteristic with $m_a = 0$

$$I = \frac{P}{V_g - V} + \frac{P}{V} = \frac{P}{V\left(1 - \frac{V_g}{V}\right)}$$

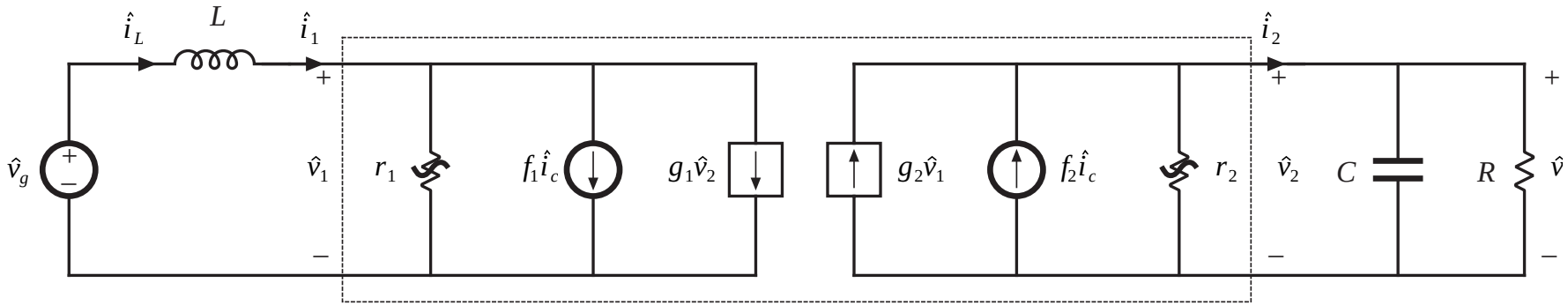


- with a resistive load, there can be two operating points
- the operating point having $V > 0.67 V_g$ can be shown to be unstable

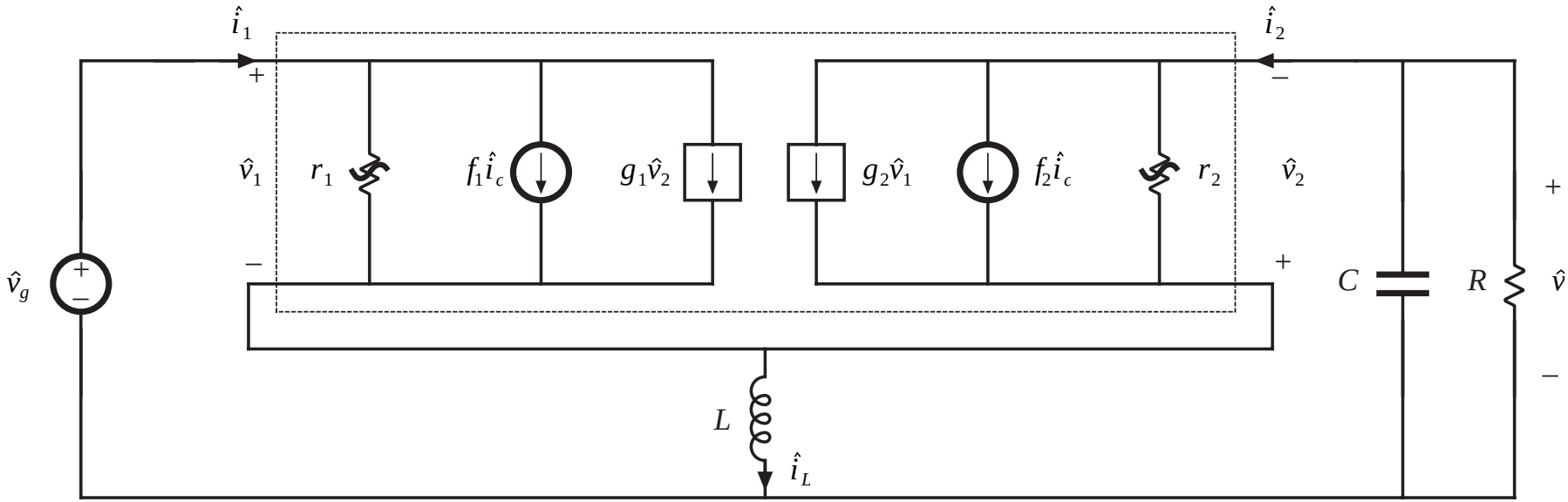
Linearized small-signal models: Buck



Linearized small-signal models: Boost



Linearized small-signal models: Buck-boost



DCM CPM small-signal parameters: input port

Table 11.4. Current programmed DCM small-signal equivalent circuit parameters: input port

Converter	g_1	f_1	r_1
Buck	$\frac{1}{R}\left(\frac{M^2}{1-M}\right)\frac{\left(1-\frac{m_a}{m_1}\right)}{\left(1+\frac{m_a}{m_1}\right)}$	$2\frac{I_1}{I_c}$	$-R\left(\frac{1-M}{M^2}\right)\frac{\left(1+\frac{m_a}{m_1}\right)}{\left(1-\frac{m_a}{m_1}\right)}$
Boost	$-\frac{1}{R}\left(\frac{M}{M-1}\right)$	$2\frac{I}{I_c}$	$\frac{R}{M^2\left(\frac{2-M}{M-1}+\frac{2\frac{m_a}{m_1}}{1+\frac{m_a}{m_1}}\right)}$
Buck-boost	0	$2\frac{I_1}{I_c}$	$\frac{-R}{M^2}\frac{\left(1+\frac{m_a}{m_1}\right)}{\left(1-\frac{m_a}{m_1}\right)}$

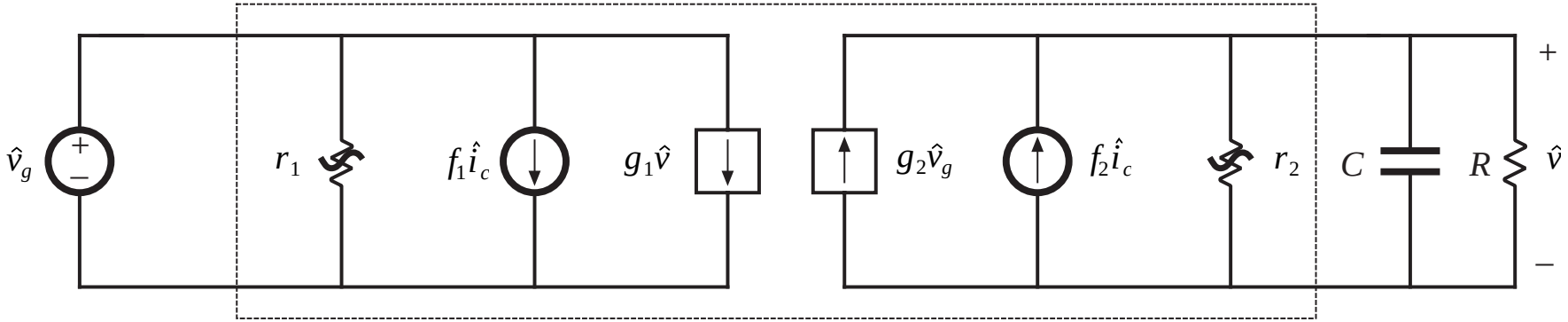
DCM CPM small-signal parameters: output port

Table 11.5. Current programmed DCM small-signal equivalent circuit parameters: output port

Converter	g_2	f_2	r_2
Buck	$\frac{1}{R}\left(\frac{M}{1-M}\right)\frac{\left(\frac{m_a}{m_1}\left(2-M\right)-M\right.}{\left(1+\frac{m_a}{m_1}\right)}$	$2\frac{I}{I_c}$	$R\frac{\left(1-M\right)\left(1+\frac{m_a}{m_1}\right.}{\left(1-2M+\frac{m_a}{m_1}\right)}$
Boost	$\frac{1}{R}\left(\frac{M}{M-1}\right)$	$2\frac{I_2}{I_c}$	$R\left(\frac{M-1}{M}\right)$
Buck-boost	$\frac{2M}{R}\frac{\left(\frac{m_a}{m_1}\right)}{\left(1+\frac{m_a}{m_1}\right)}$	$2\frac{I_2}{I_c}$	R

Simplified DCM CPM model, with $L = 0$

Buck, boost, buck-boost all become



$$G_{vc}(s) = \left.\frac{\hat{v}}{\hat{i}_c}\right|_{\hat{v}_g = 0} = \frac{G_{c0}}{1 + \frac{s}{\omega_p}}$$

$$G_{vg}(s) = \left.\frac{\hat{v}}{\hat{v}_g}\right|_{\hat{i}_c = 0} = \frac{G_{g0}}{1 + \frac{s}{\omega_p}}$$

$$G_{c0} = f_2 \left(R \parallel r_2 \right)$$

$$\omega_p = \frac{1}{\left(R \parallel r_2 \right) C}$$

$$G_{g0} = g_2 \left(R \parallel r_2 \right)$$

Buck ω_p

Plug in parameters:

$$\omega_p = \frac{1}{RC} \frac{\left(2 - 3M\right)\left(1 - M\right) + \frac{m_a}{m_2} M\left(2 - M\right)}{\left(1 - M\right)\left(1 - M + M \frac{m_a}{m_2}\right)}$$

- For $m_a = 0$, numerator is negative when $M > 2/3$.
- ω_p then constitutes a RHP pole. Converter is unstable.
- Addition of small artificial ramp stabilizes system.
- $m_a > 0.086$ leads to stability for all $M \leq 1$.
- Output voltage feedback can also stabilize system, without an artificial ramp

11.5 Summary of key points

1. In current-programmed control, the peak switch current $i_s(t)$ follows the control input $i_c(t)$. This widely used control scheme has the advantage of a simpler control-to-output transfer function. The line-to-output transfer functions of current-programmed buck converters are also reduced.

2. The basic current-programmed controller is unstable when $D > 0.5$, regardless of the converter topology. The controller can be stabilized by addition of an artificial ramp having slope ma. When $m_a \geq 0.5\, m_2$, then the controller is stable for all duty cycle.

3. The behavior of current-programmed converters can be modeled in a simple and intuitive manner by the first-order approximation $\langle\, i_L(t)\, \rangle_{T_s} \approx i_c(t)$. The averaged terminal waveforms of the switch network can then be modeled simply by a current source of value i_c , in conjunction with a power sink or power source element. Perturbation and linearization of these elements leads to the small-signal model. Alternatively, the small-signal converter equations derived in Chapter 7 can be adapted to cover the current programmed mode, using the simple approximation $i_L(t) \approx i_c(t)$.

Summary of key points

4. The simple model predicts that one pole is eliminated from the converter line-to-output and control-to-output transfer functions. Current programming does not alter the transfer function zeroes. The dc gains become load-dependent.

5. The more accurate model of Section 11.3 correctly accounts for the difference between the average inductor current $\langle i_L(t) \rangle_{T_S}$ and the control input $i_c(t)$. This model predicts the nonzero line-to-output transfer function $G_{vg}(s)$ of the buck converter. The current-programmed controller behavior is modeled by a block diagram, which is appended to the small-signal converter models derived in Chapter 7. Analysis of the resulting multiloop feedback system then leads to the relevant transfer functions.

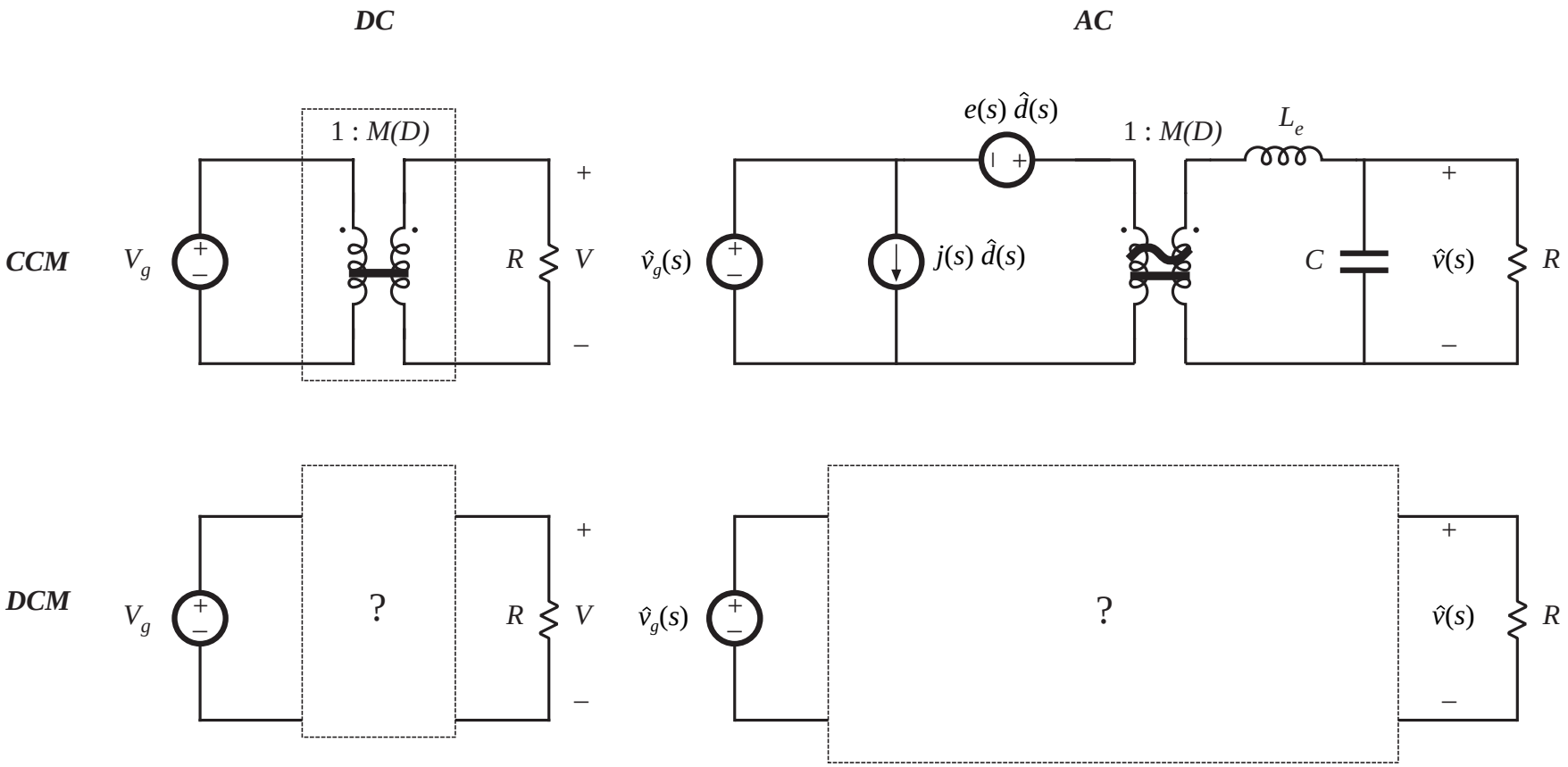
6. The more accurate model predicts that the inductor pole occurs at the crossover frequency fc of the effective current feedback loop gain $T_i(s)$. The frequency f_c typically occurs in the vicinity of the converter switching frequency f_s . The more accurate model also predicts that the line-to-output transfer function $G_{vg}(s)$ of the buck converter is nulled when $m_a = 0.5\ m_2$.

Summary of key points

7. Current programmed converters operating in the discontinuous conduction mode are modeled in Section 11.4. The averaged transistor waveforms can be modeled by a power sink, while the averaged diode waveforms are modeled by a power source. The power is controlled by $i_c(t)$. Perturbation and linearization of these averaged models, as usual, leads to small-signal equivalent circuits.

Chapter 11
AC and DC Equivalent Circuit Modeling of the Discontinuous Conduction Mode

We are missing ac and dc equivalent circuit models for the discontinuous conduction mode



Change in characteristics at the CCM/DCM boundary

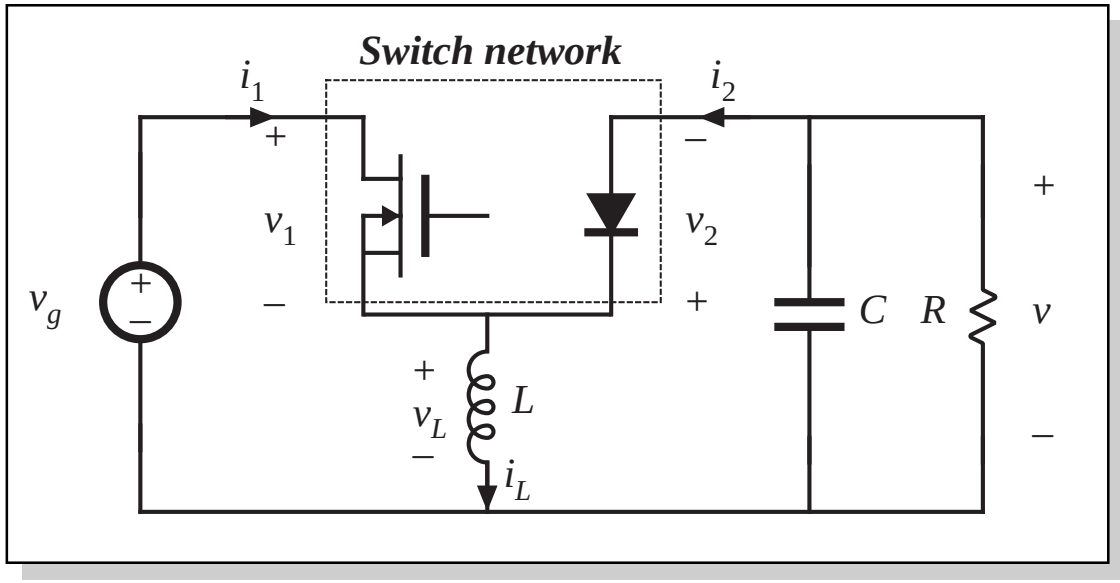
- Steady-state output voltage becomes strongly load-dependent
- Simpler dynamics: one pole and the RHP zero are moved to very high frequency, and can normally be ignored
- Traditionally, boost and buck-boost converters are designed to operate in DCM at full load
- All converters may operate in DCM at light load

So we need equivalent circuits that model the steady-state and small-signal ac models of converters operating in DCM

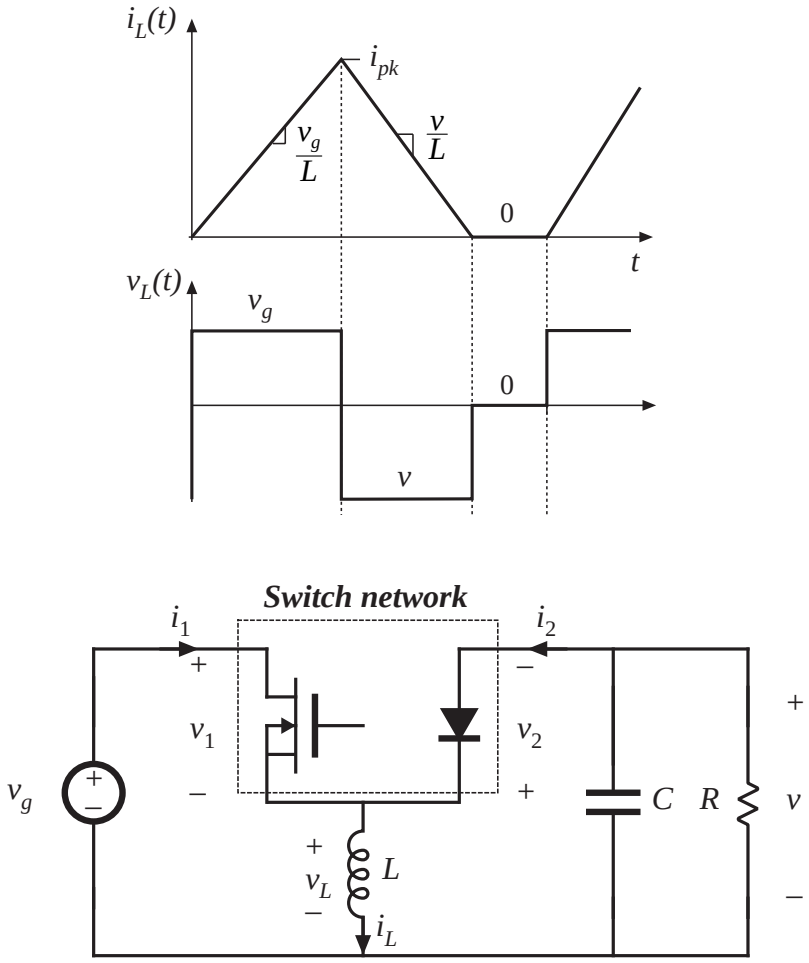
The averaged switch approach will be employed

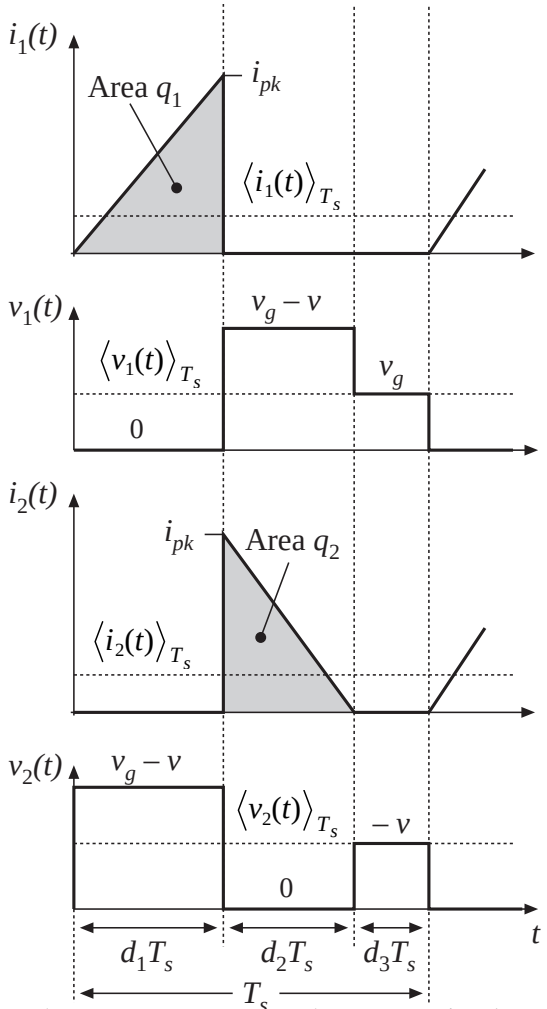
11.1 Derivation of DCM averaged switch model: buck-boost example

- Define switch terminal quantities v_1, i_1, v_2, i_2, as shown
- Let us find the averaged quantities $\langle v_1 \rangle$, $\langle i_1 \rangle$, $\langle v_2 \rangle$, $\langle i_2 \rangle$, for operation in DCM, and determine the relations between them



DCM waveforms





Basic DCM equations: i_{pk}, v_L, and d_2 (Approximate method)

Peak inductor current:

$$i_{pk} = \frac{v_g}{L} d_1 T_s$$

Average inductor voltage:

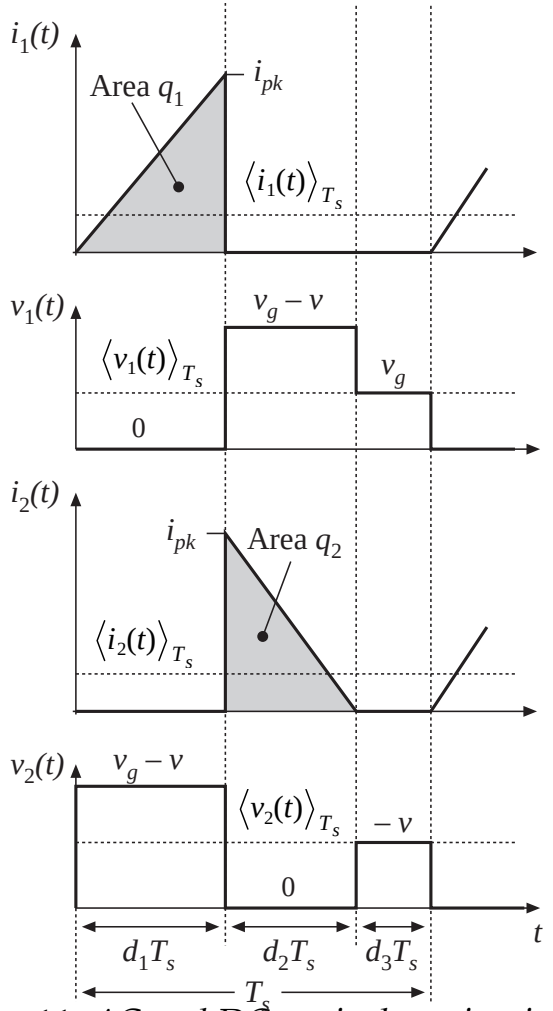
$$\left\langle v_L(t) \right\rangle_{T_s} = d_1 \left\langle v_g(t) \right\rangle_{T_s} + d_2 \left\langle v(t) \right\rangle_{T_s} + d_3 \cdot 0$$

In DCM, the diode switches off when the inductor current reaches zero. Hence, $i(0) = i(T_s) = 0$, and the average inductor voltage is zero. This is true even during transients.

$$\left\langle v_L(t) \right\rangle_{T_s} = d_1(t) \left\langle v_g(t) \right\rangle_{T_s} + d_2(t) \left\langle v(t) \right\rangle_{T_s} = 0$$

Solve for d_2:

$$d_2(t) = - d_1(t) \frac{\left\langle v_g(t) \right\rangle_{T_s}}{\left\langle v(t) \right\rangle_{T_s}}$$



Average switch network terminal voltages

Average the $v_1(t)$ waveform:

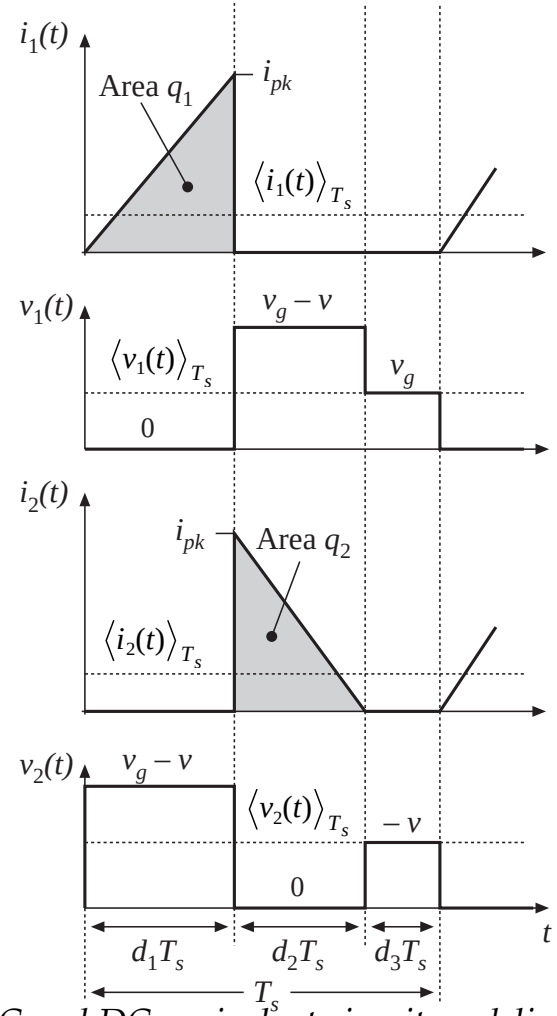
$$\left\langle v_1(t) \right\rangle_{T_s} = d_1(t) \cdot 0 + d_2(t) \left(\left\langle v_g(t) \right\rangle_{T_s} - \left\langle v(t) \right\rangle_{T_s} \right) + d_3(t) \left\langle v_g(t) \right\rangle_{T_s}$$

Eliminate d_2 and d_3:

$$\left\langle v_1(t) \right\rangle_{T_s} = \left\langle v_g(t) \right\rangle_{T_s}$$

Similar analysis for $v_2(t)$ waveform leads to

$$\begin{aligned} \left\langle v_2(t) \right\rangle_{T_s} &= d_1(t) \left(\left\langle v_g(t) \right\rangle_{T_s} - \left\langle v(t) \right\rangle_{T_s} \right) + d_2(t) \cdot 0 + d_3(t) \left(- \left\langle v(t) \right\rangle_{T_s} \right) \\ &= - \left\langle v(t) \right\rangle_{T_s} \end{aligned}$$



Average switch network terminal currents

Average the $i_1(t)$ waveform:

$$\left\langle i_1(t) \right\rangle_{T_s} = \frac{1}{T_s} \int_t^{t+T_s} i_1(t)\,dt = \frac{q_1}{T_s}$$

The integral q_1 is the area under the $i_1(t)$ waveform during first subinterval. Use triangle area formula:

$$q_1 = \int_t^{t+T_s} i_1(t)\,dt = \frac{1}{2}\left(d_1 T_s\right)\left(i_{pk}\right)$$

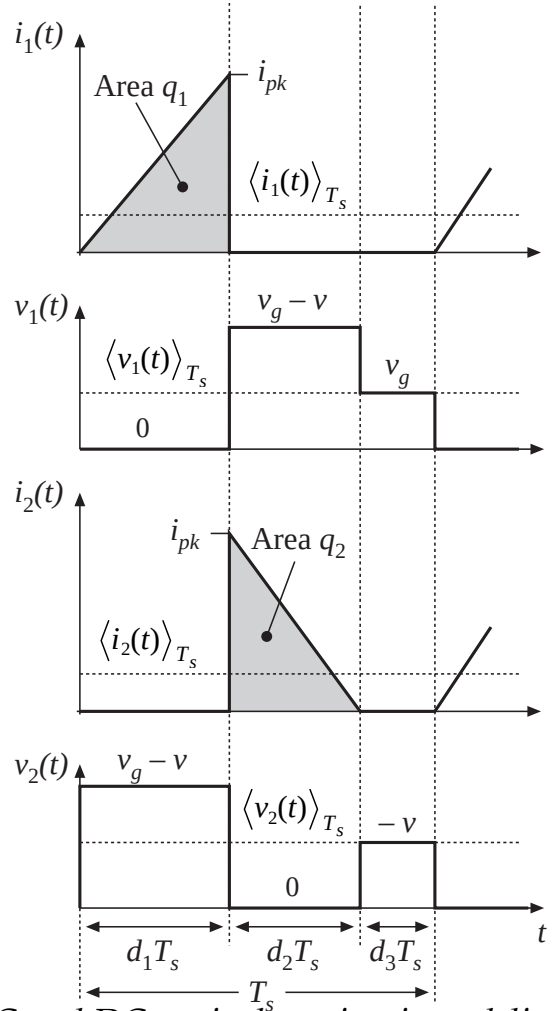
Eliminate i_{pk}:

$$\left\langle i_1(t) \right\rangle_{T_s} = \frac{d_1^2(t)\,T_s}{2L} \left\langle v_1(t) \right\rangle_{T_s}$$

Note $\langle i_1(t) \rangle_{Ts}$ is not equal to $d\,\langle i_L(t) \rangle_{Ts}$!

Similar analysis for $i_2(t)$ waveform leads to

$$\left\langle i_2(t) \right\rangle_{T_s} = \frac{d_1^2(t)\,T_s}{2L} \frac{\left\langle v_1(t) \right\rangle_{T_s}^2}{\left\langle v_2(t) \right\rangle_{T_s}}$$

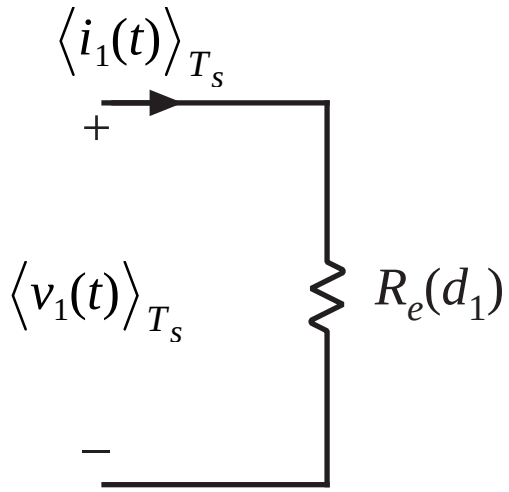


Input port: Averaged equivalent circuit

$$\left\langle i_1(t) \right\rangle_{T_s} = \frac{d_1^2(t)\, T_s}{2L} \left\langle v_1(t) \right\rangle_{T_s}$$

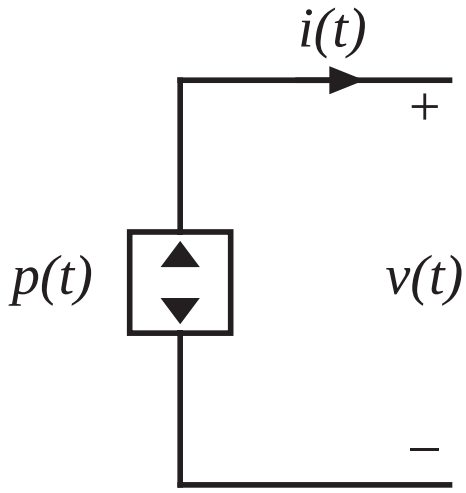
$$\left\langle i_1(t) \right\rangle_{T_s} = \frac{\left\langle v_1(t) \right\rangle_{T_s}}{R_e(d_1)}$$

$$R_e(d_1) = \frac{2L}{d_1^2\, T_s}$$



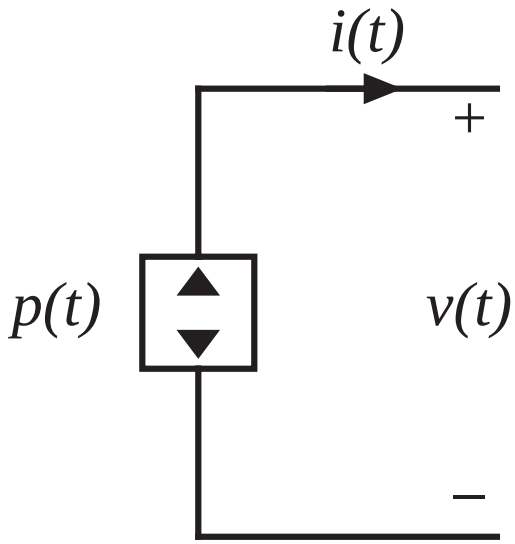
Output port: Averaged equivalent circuit

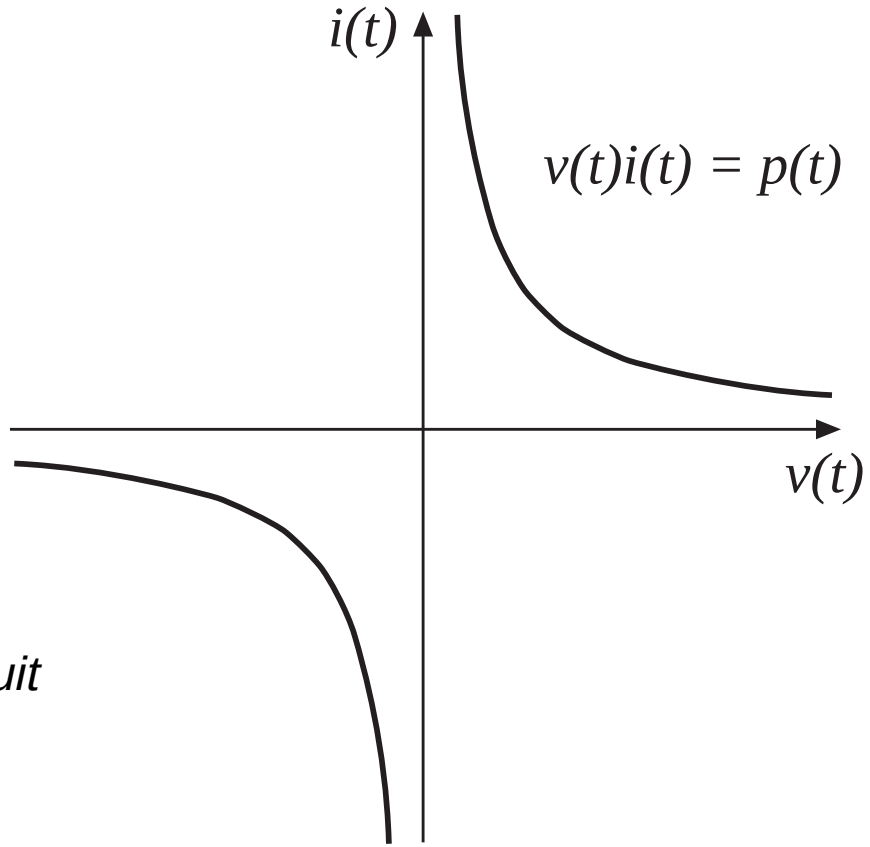
$$\left\langle i_2(t) \right\rangle_{T_s} = \frac{d_1^2(t)\, T_s}{2L} \frac{\left\langle v_1(t) \right\rangle_{T_s}^2}{\left\langle v_2(t) \right\rangle_{T_s}}$$



$$\left\langle i_2(t) \right\rangle_{T_s} \left\langle v_2(t) \right\rangle_{T_s} = \frac{\left\langle v_1(t) \right\rangle_{T_s}^2}{R_e(d_1)} = \left\langle p(t) \right\rangle_{T_s}$$

The dependent power source





- *Must avoid open- and short-circuit connections of power sources*
- *Power sink: negative* $p(t)$

How the power source arises in lossless two-port networks

In a lossless two-port network without internal energy storage: instantaneous input power is equal to instantaneous output power

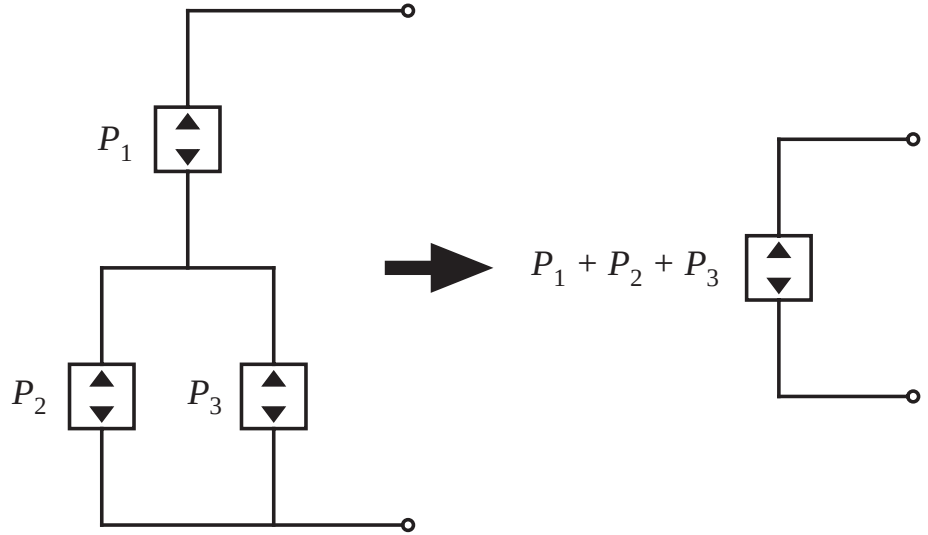
In all but a small number of special cases, the instantaneous power throughput is dependent on the applied external source and load

If the instantaneous power depends only on the external elements connected to one port, then the power is not dependent on the characteristics of the elements connected to the other port. The other port becomes a source of power, equal to the power flowing through the first port

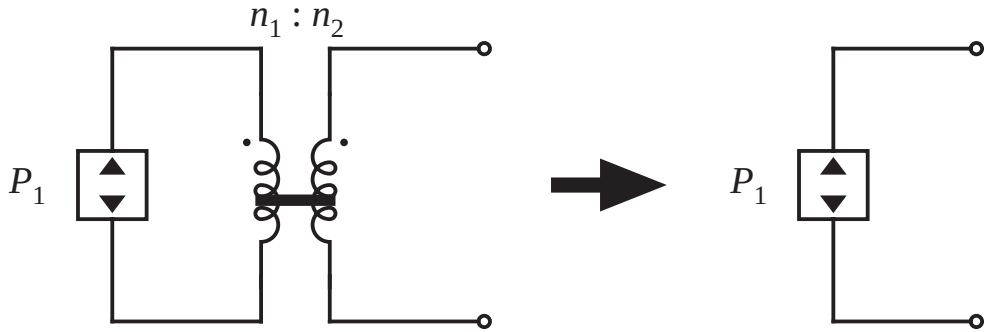
A power source (or power sink) element is obtained

Properties of power sources

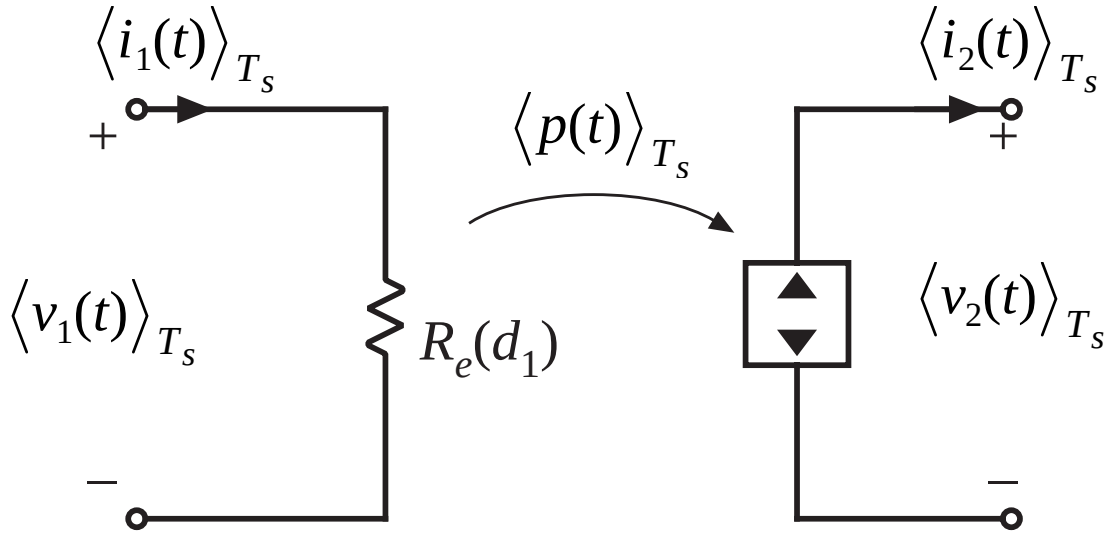
Series and parallel connection of power sources



Reflection of power source through a transformer



The loss-free resistor (LFR)

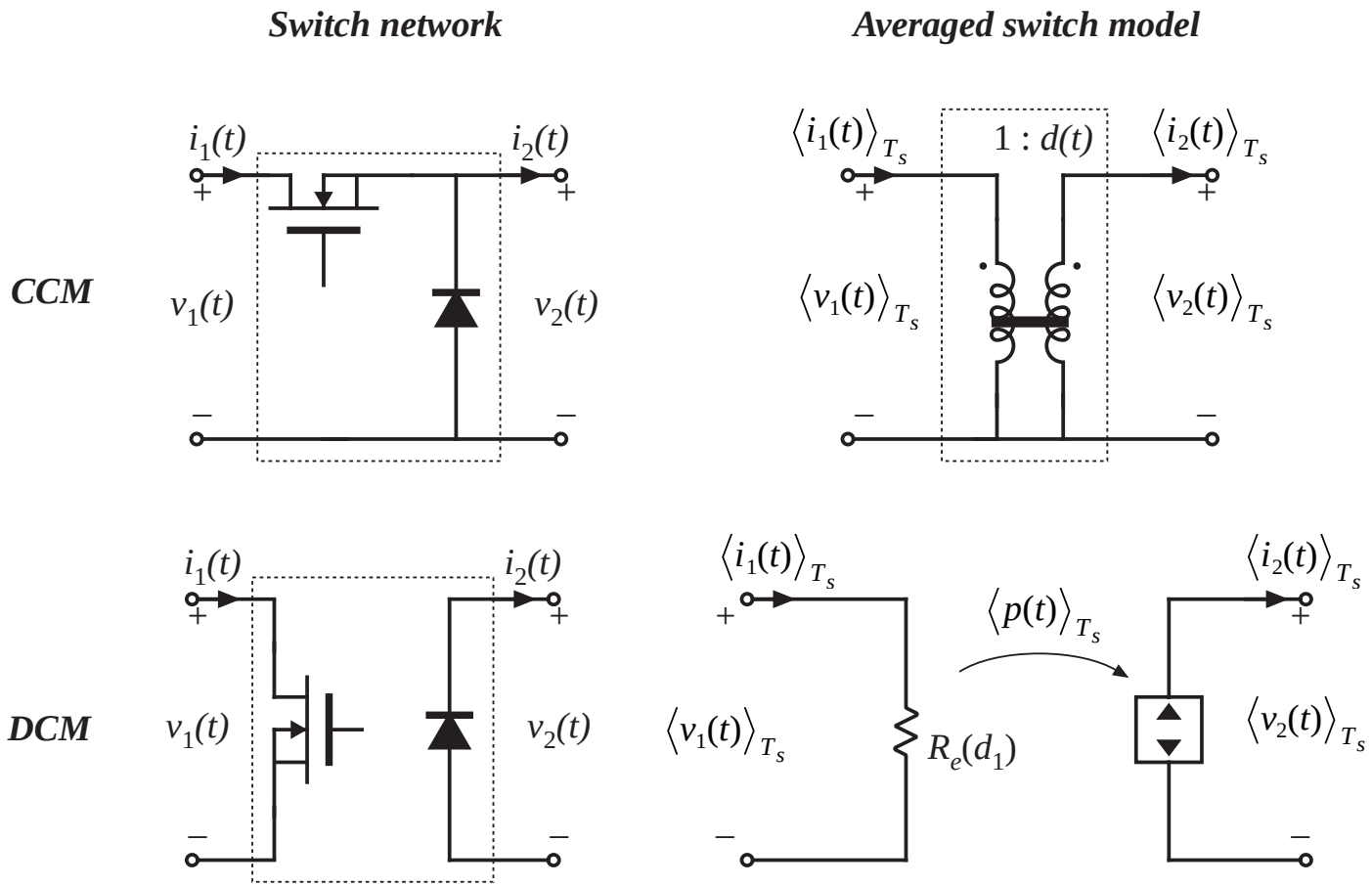


A two-port lossless network

Input port obeys Ohm's Law

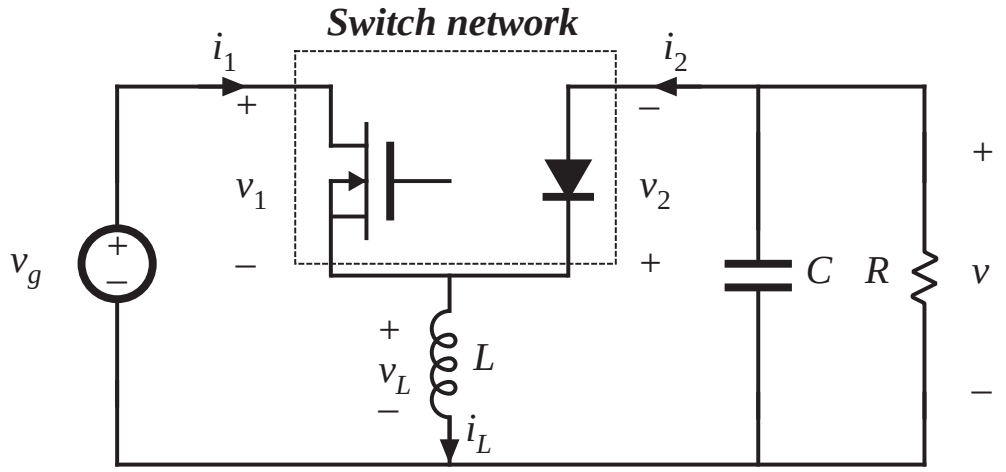
Power entering input port is transferred to output port

Averaged modeling of CCM and DCM switch networks

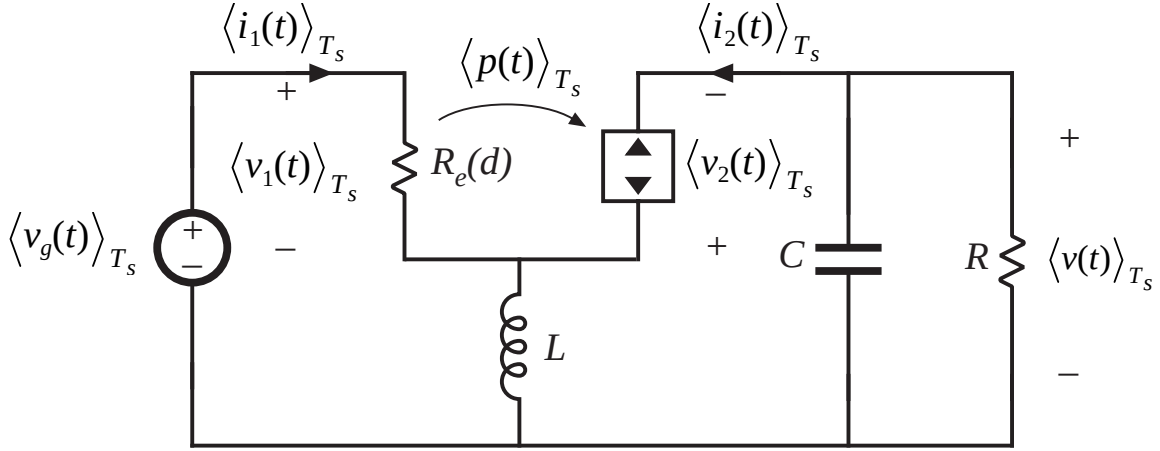


Averaged switch model: buck-boost example

Original circuit



Averaged model

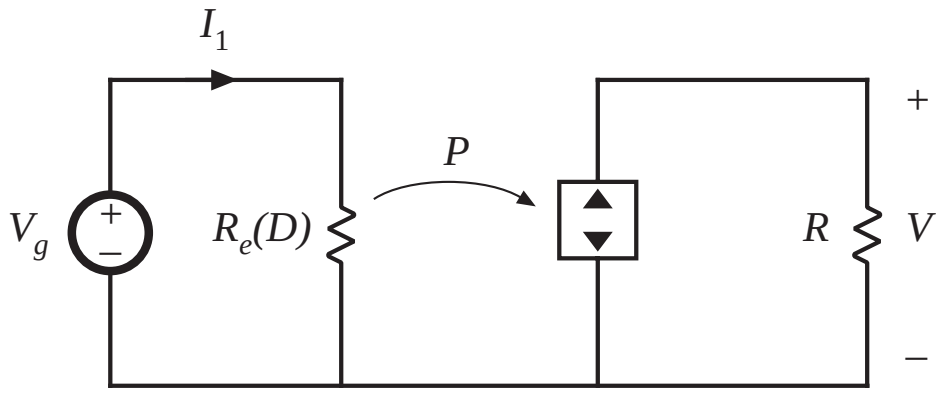


Solution of averaged model: steady state

Let

$L \rightarrow$ short circuit

$C \rightarrow$ open circuit



Converter input power:

$$P = \frac{V_g^2}{R_e}$$

Converter output power:

$$P = \frac{V^2}{R}$$

Equate and solve:

$$P = \frac{V_g^2}{R_e} = \frac{V^2}{R}$$

$$\frac{V}{V_g} = \pm \sqrt{\frac{R}{R_e}}$$

Steady-state LFR solution

$$\frac{V}{V_g} = \pm \sqrt{\frac{R}{R_e}}$$

is a general result, for any system that can be modeled as an LFR.

For the buck-boost converter, we have

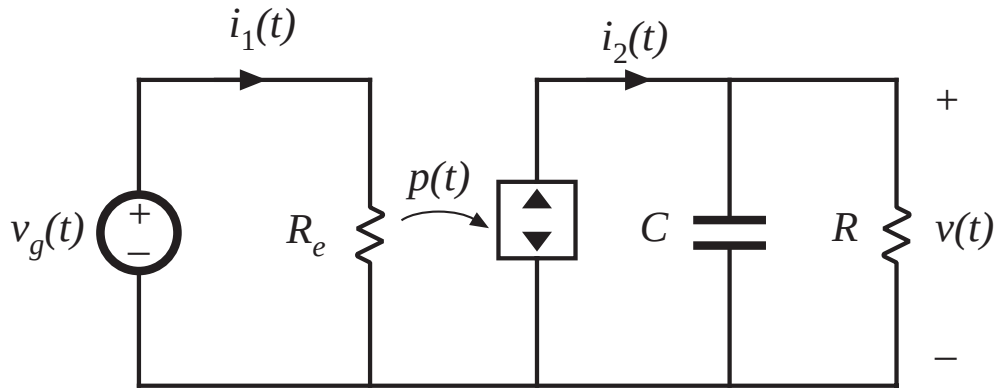
$$R_e(D) = \frac{2L}{D^2 T_s}$$

Eliminate R_e:

$$\frac{V}{V_g} = -\sqrt{\frac{D^2 T_s R}{2L}} = -\frac{D}{\sqrt{K}}$$

which agrees with the previous steady-state solution of Chapter 5.

Steady-state LFR solution with ac terminal waveforms



Converter average input power:

$$P_{av} = \frac{V_{g,rms}^2}{R_e}$$

Converter average output power:

$$P_{av} = \frac{V_{rms}^2}{R}$$

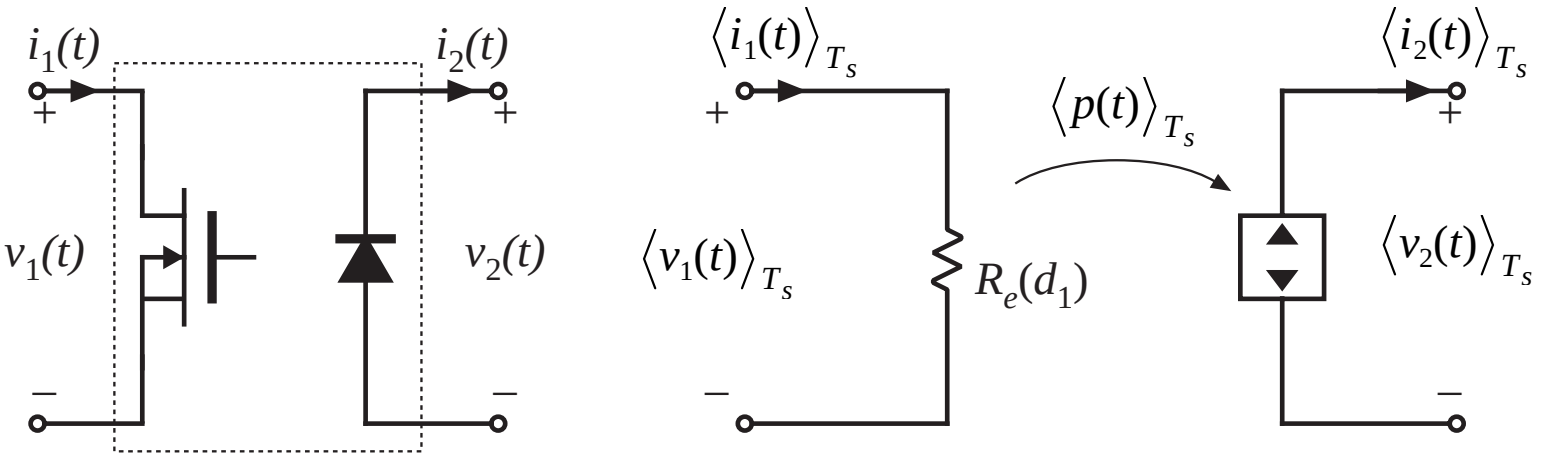
Note that no average power flows into capacitor

Equate and solve:

$$\frac{V_{rms}}{V_{g,rms}} = \sqrt{\frac{R}{R_e}}$$

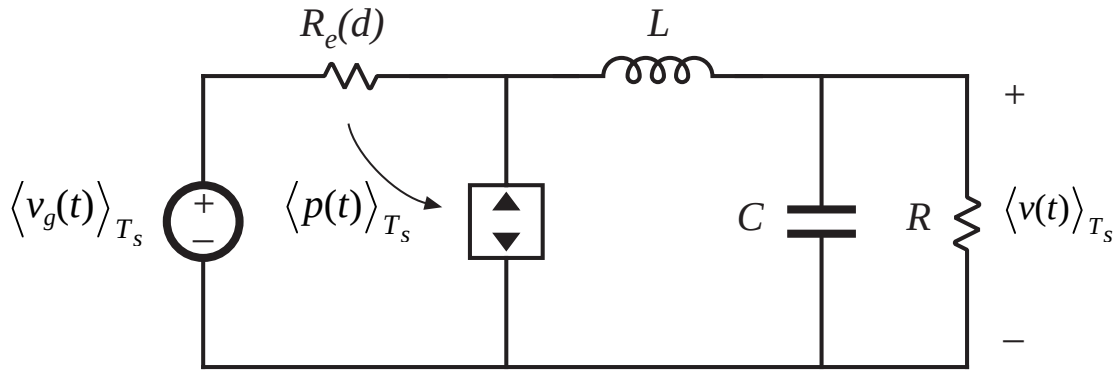
Averaged models of other DCM converters

- Determine averaged terminal waveforms of switch network
- In each case, averaged transistor waveforms obey Ohm's law, while averaged diode waveforms behave as dependent power source
- Can simply replace transistor and diode with the averaged model as follows:



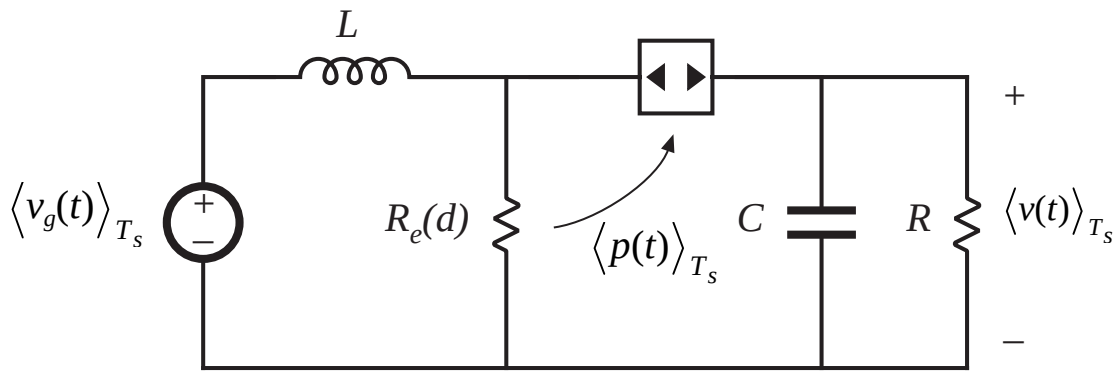
DCM buck, boost

Buck



$$R_e = \frac{2L}{d^2 T_s}$$

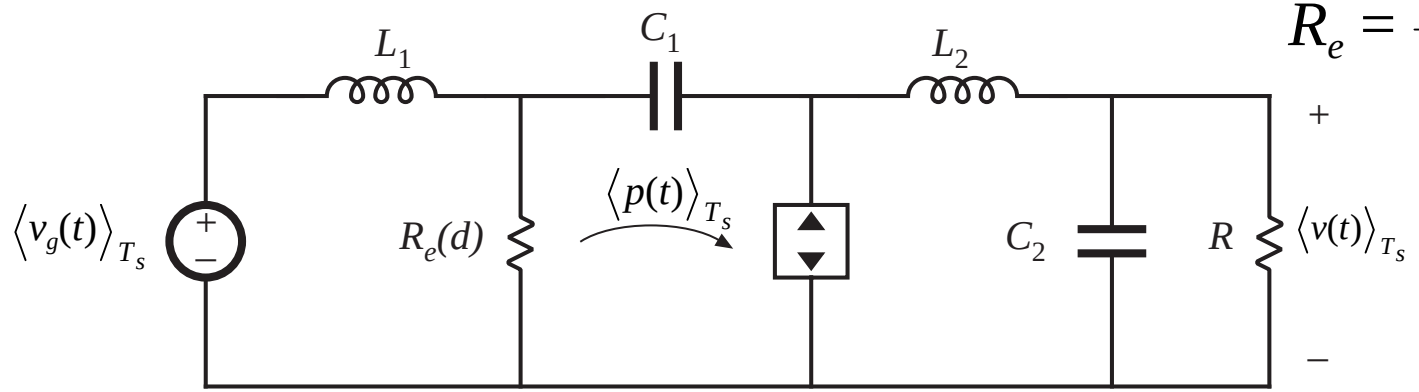
Boost



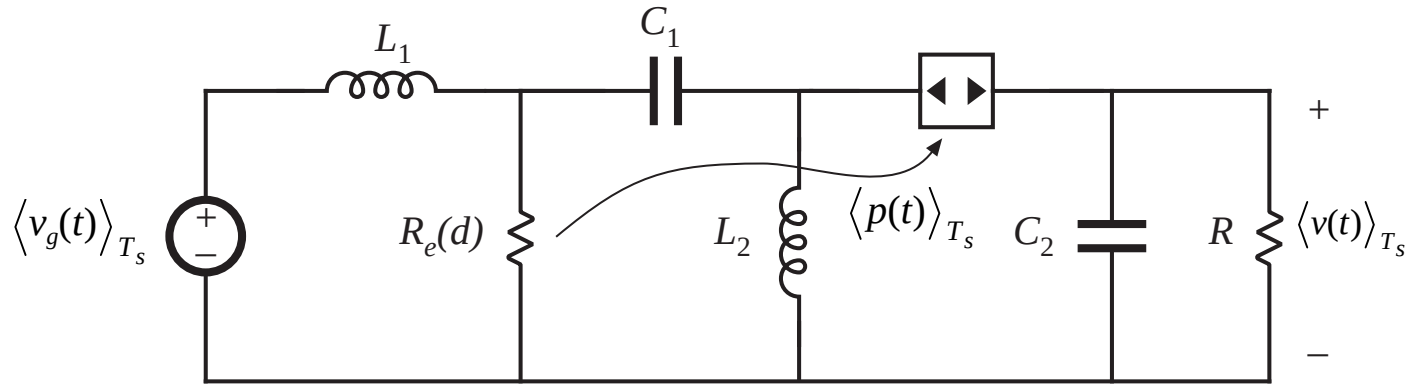
DCM Cuk, SEPIC

$$R_e = \frac{2\left(L_1 \| L_2\right)}{d^2 T_s}$$

Cuk



SEPIC

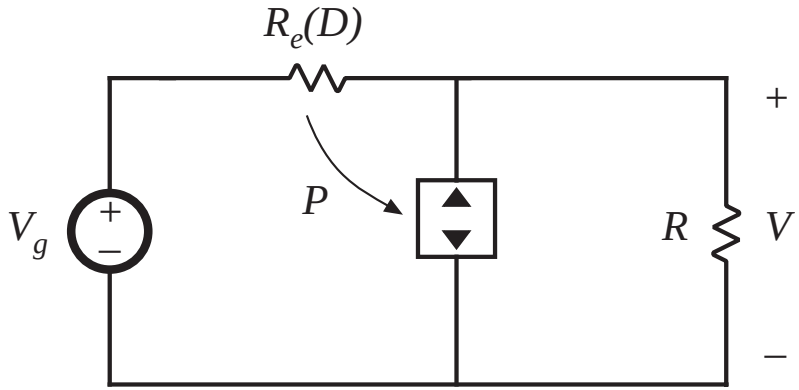


Steady-state solution: DCM buck, boost

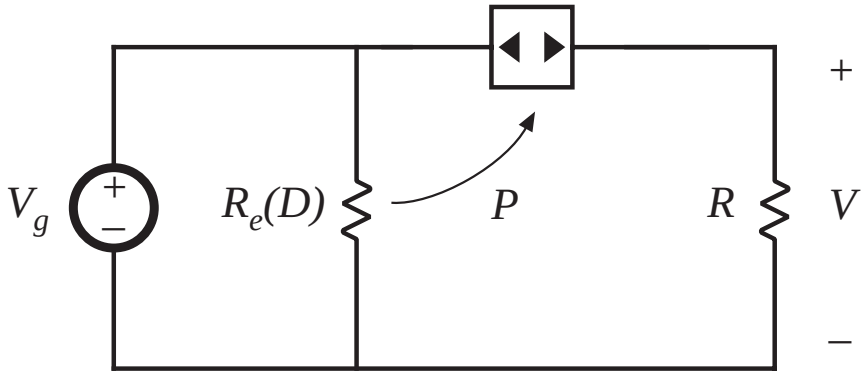
Let $L \rightarrow$ short circuit

$C \rightarrow$ open circuit

Buck



Boost



Steady-state solution of DCM/LFR models

Table 11.1. CCM and DCM conversion ratios of basic converters

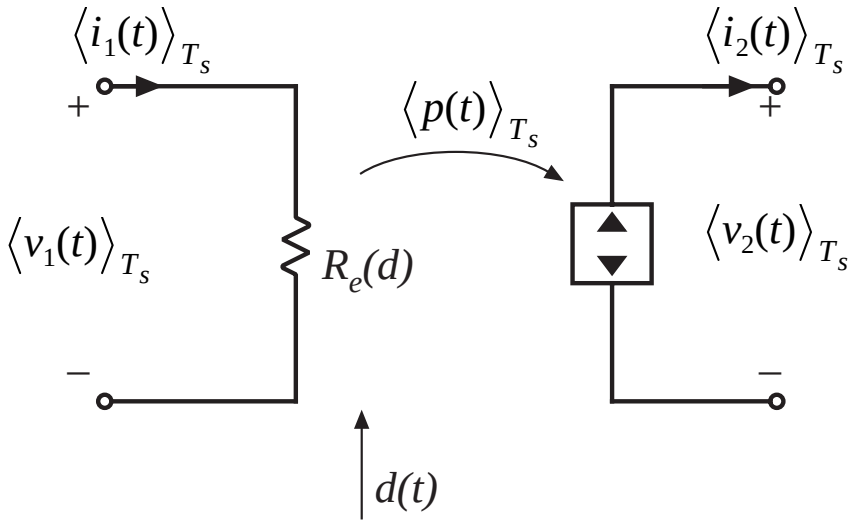
Converter	M, CCM	M, DCM
Buck	D	$\frac{2}{1+\sqrt{1+4R_e/R}}$
Boost	$\frac{1}{1-D}$	$\frac{1+\sqrt{1+4R/R_e}}{2}$
Buck-boost, Cuk	$\frac{-D}{1-D}$	$-\sqrt{\frac{R}{R_e}}$
SEPIC	$\frac{D}{1-D}$	$\sqrt{\frac{R}{R_e}}$

$I > I_{crit}$ for CCM
$I < I_{crit}$ for DCM

$$I_{crit} = \frac{1-D}{D} \frac{V_g}{R_e(D)}$$

11.2 Small-signal ac modeling of the DCM switch network

Large-signal averaged model



$$\langle i_1(t)\rangle_{T_s} = \frac{d_1^2(t)\,T_s}{2L}\langle v_1(t)\rangle_{T_s}$$

$$\langle i_2(t)\rangle_{T_s} = \frac{d_1^2(t)\,T_s}{2L}\frac{\langle v_1(t)\rangle_{T_s}^2}{\langle v_2(t)\rangle_{T_s}}$$

Perturb and linearize: let

$$d(t) = D + \hat{d}(t)$$

$$\langle v_1(t)\rangle_{T_s} = V_1 + \hat{v}_1(t)$$

$$\langle i_1(t)\rangle_{T_s} = I_1 + \hat{i}_1(t)$$

$$\langle v_2(t)\rangle_{T_s} = V_2 + \hat{v}_2(t)$$

$$\langle i_2(t)\rangle_{T_s} = I_2 + \hat{i}_2(t)$$

$$\hat{i}_1 = \frac{\hat{v}_1}{r_1} + j_1\hat{d} + g_1\hat{v}_2$$

$$\hat{i}_2 = -\frac{\hat{v}_2}{r_2} + j_2\hat{d} + g_2\hat{v}_1$$

Linearization via Taylor series

Given the nonlinear equation

$$\left\langle i_1(t) \right\rangle_{T_s} = \frac{\left\langle v_1(t) \right\rangle_{T_s}}{R_e(d(t))} = f_1\left(\left\langle v_1(t) \right\rangle_{T_s}, \left\langle v_2(t) \right\rangle_{T_s}, d(t) \right)$$

Expand in three-dimensional Taylor series about the quiescent operating point:

$$I_1 + \hat{i}_1(t) = f_1\left(V_1, V_2, D\right) + \hat{v}_1(t) \left. \frac{d f_1\left(v_1, V_2, D\right)}{d v_1} \right|_{v_1 = V_1}$$

(for simple notation, drop angle brackets)

$$+ \hat{v}_2(t) \left. \frac{d f_1\left(V_1, v_2, D\right)}{d v_2} \right|_{v_2 = V_2} + \hat{d}(t) \left. \frac{d f_1\left(V_1, V_2, d\right)}{d d} \right|_{d = D}$$

+ higher–order nonlinear terms

Equate dc and first-order ac terms

AC

$$\hat{i}_1(t) = \hat{v}_1(t)\,\frac{1}{r_1} + \hat{v}_2(t)\,g_1 + \hat{d}(t)\,j_1$$

$$\frac{1}{r_1} = \left.\frac{d\,f_1\left(v_1, V_2, D\right)}{dv_1}\right|_{v_1 = V_1} = \frac{1}{R_e(D)}$$

$$g_1 = \left.\frac{d\,f_1\left(V_1, v_2, D\right)}{dv_2}\right|_{v_2 = V_2} = 0$$

$$j_1 = \left.\frac{d\,f_1\left(V_1, V_2, d\right)}{dd}\right|_{d = D} = -\frac{V_1}{R_e^2(D)}\left.\frac{dR_e(d)}{dd}\right|_{d = D}$$

$$= \frac{2V_1}{DR_e(D)}$$

DC

$$I_1 = f_1\left(V_1, V_2, D\right) = \frac{V_1}{R_e(D)}$$

Output port
same approach

$$\left\langle i_2(t)\right\rangle_{T_s} = \frac{\left\langle v_1(t)\right\rangle_{T_s}^2}{R_e(d(t))\left\langle v_2(t)\right\rangle_{T_s}} = f_2\left(\left\langle v_1(t)\right\rangle_{T_s}, \left\langle v_2(t)\right\rangle_{T_s}, d(t)\right)$$

$$I_2 = f_2\left(V_1, V_2, D\right) = \frac{V_1^2}{R_e(D)\, V_2}$$

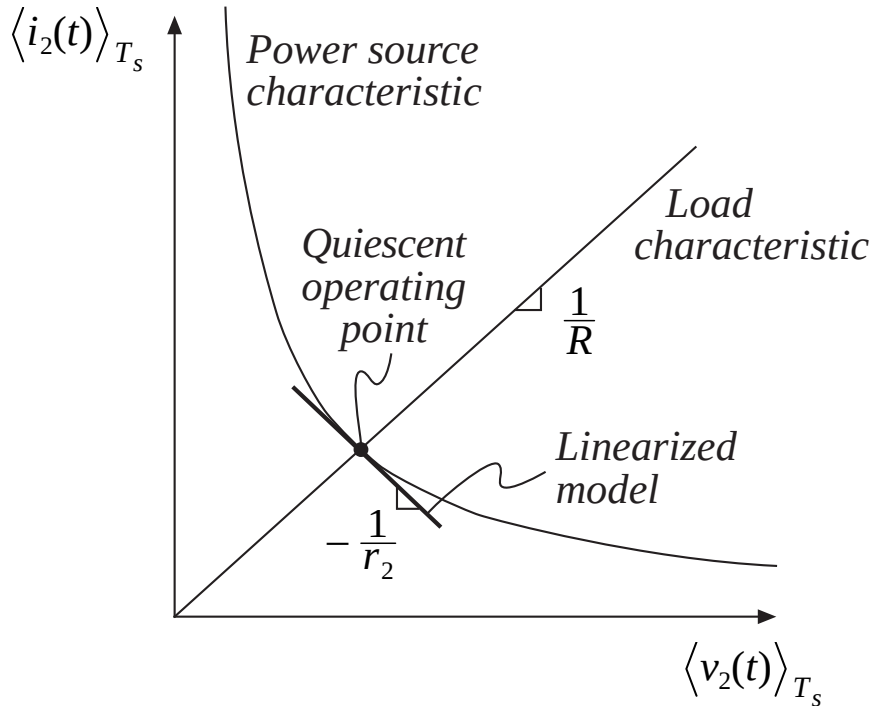
DC terms

$$\hat{i}_2(t) = \hat{v}_2(t)\left(-\frac{1}{r_2}\right) + \hat{v}_1(t) g_2 + \hat{d}(t) j_2$$

Small-signal ac linearization

Output resistance parameter r_2

$$\frac{1}{r_2} = - \left. \frac{d f_2\left(V_1, v_2, D\right)}{d v_2} \right|_{v_2 = V_2} = \frac{1}{R} = \frac{1}{M^2 R_e(D)}$$



Small-signal DCM switch model parameters

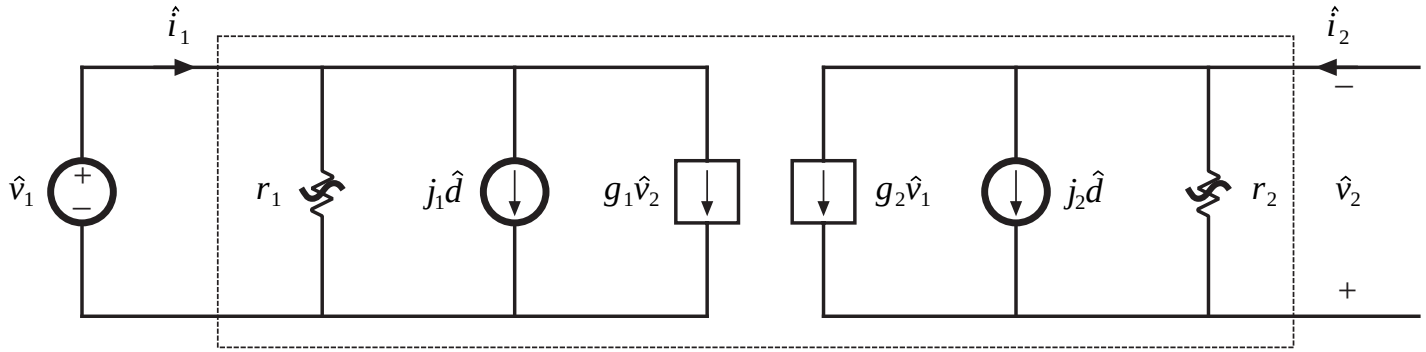
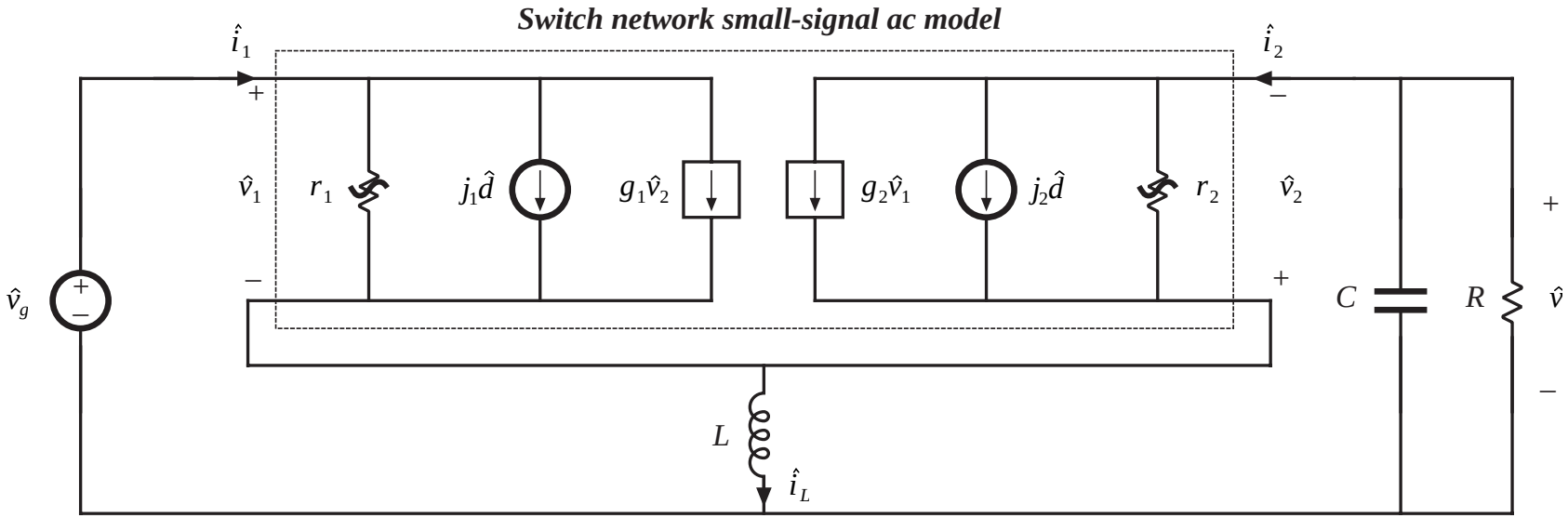


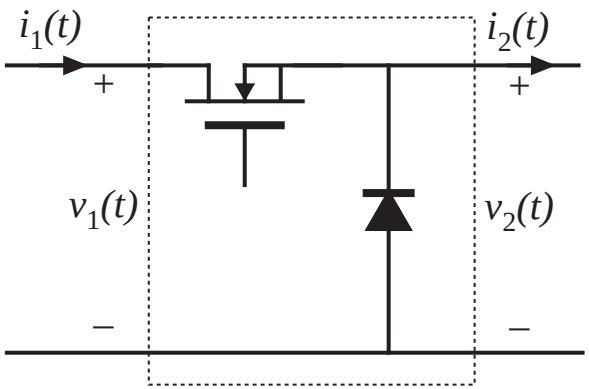
Table 11.2. Small-signal DCM switch model parameters

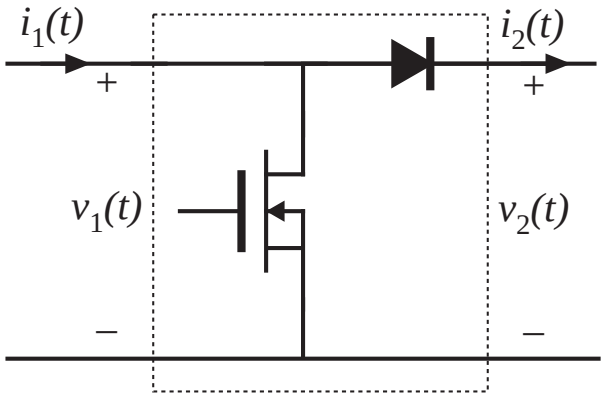
Switch type	g_1	j_1	r_1	g_2	j_2	r_2
Buck, Fig. 11.16(a)	$\frac{1}{R_e}$	$\frac{2(1-M)V_1}{DR_e}$	R_e	$\frac{2-M}{MR_e}$	$\frac{2(1-M)V_1}{DMR_e}$	M^2R_e
Boost, Fig. 11.16(b)	$\frac{1}{(M-1)^2 R_e}$	$\frac{2MV_1}{D(M-1)R_e}$	$\frac{(M-1)^2}{M} R_e$	$\frac{2M-1}{(M-1)^2 R_e}$	$\frac{2V_1}{D(M-1)R_e}$	$(M-1)^2R_e$
Gen two-switch Fig. 11.7(a)	0	$\frac{2V_1}{DR_e}$	R_e	$\frac{2M}{R_e}$	$\frac{2V_1}{DMR_e}$	M^2R_e

Small-signal ac model, DCM buck-boost example

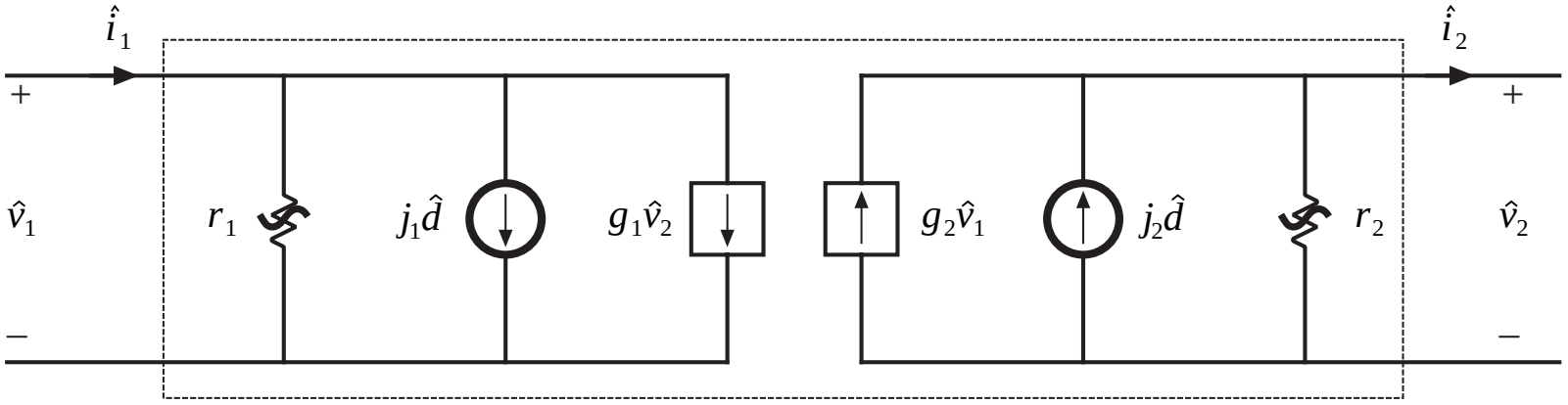


A more convenient way to model the buck and boost small-signal DCM switch networks

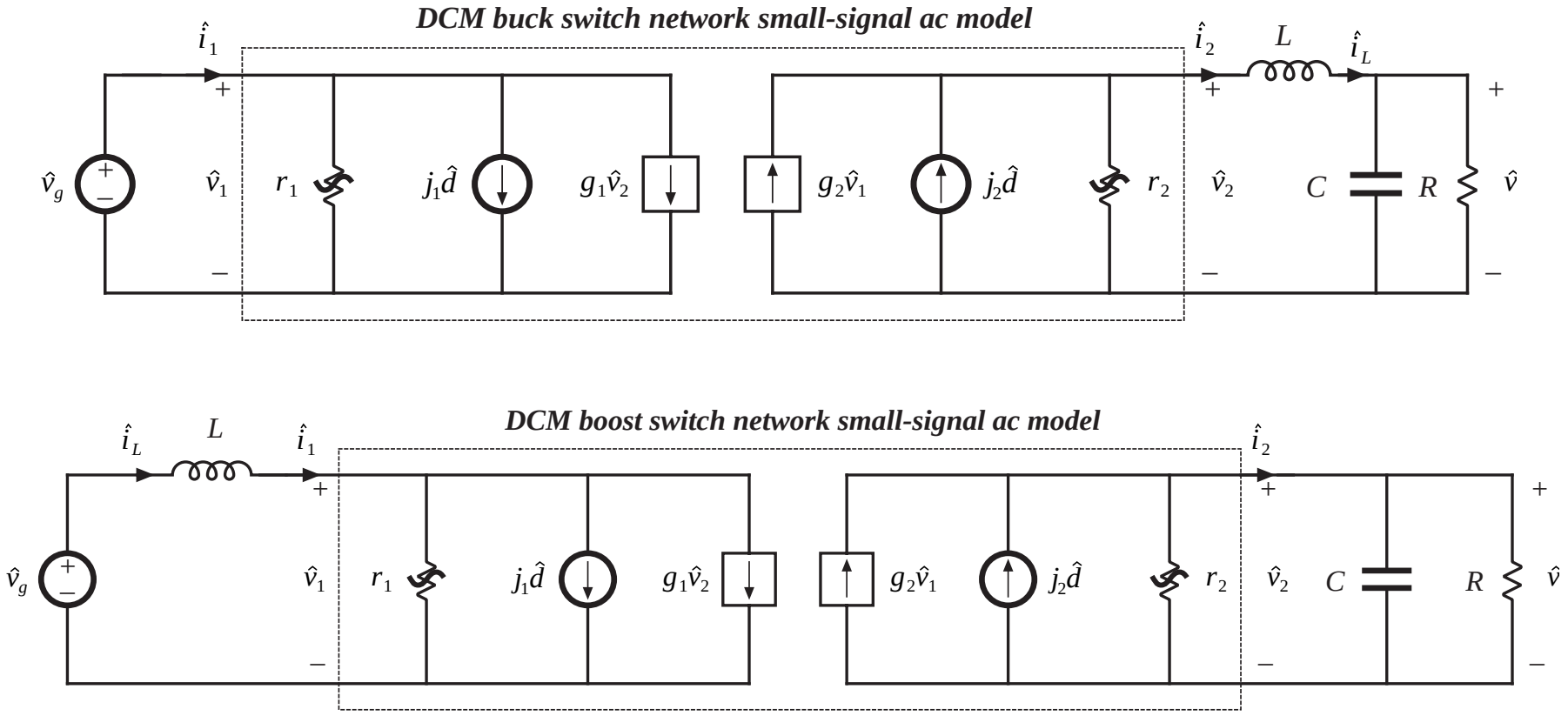




In any event, a small-signal two-port model is used, of the form



Small-signal ac models of the DCM buck and boost converters (more convenient forms)



DCM small-signal transfer functions

- When expressed in terms of R, L, C, and M (not D), the small-signal transfer functions are the same in DCM as in CCM
- Hence, DCM boost and buck-boost converters exhibit two poles and one RHP zero in control-to-output transfer functions
- ***But***, value of L is small in DCM. Hence

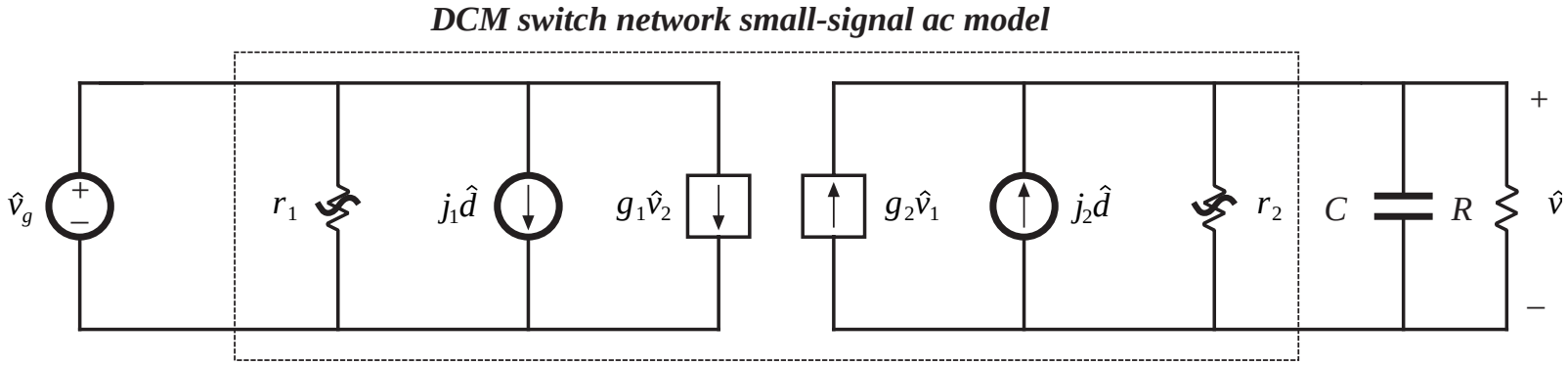
  RHP zero appears at high frequency, usually greater than switching frequency

  Pole due to inductor dynamics appears at high frequency, near to or greater than switching frequency

  So DCM buck, boost, and buck-boost converters exhibit essentially a single-pole response
- A simple approximation: let $L \rightarrow 0$

The simple approximation $L \rightarrow 0$

Buck, boost, and buck-boost converter models all reduce to



Transfer functions

control-to-output

$$G_{vd}(s) = \left.\frac{\hat{v}}{\hat{d}}\right|_{\hat{v}_g = 0} = \frac{G_{d0}}{1 + \frac{s}{\omega_p}}$$

with

$$G_{d0} = j_2 \left(R \parallel r_2\right)$$

$$\omega_p = \frac{1}{\left(R \parallel r_2\right) C}$$

line-to-output

$$G_{vg}(s) = \left.\frac{\hat{v}}{\hat{v}_g}\right|_{\hat{d} = 0} = \frac{G_{g0}}{1 + \frac{s}{\omega_p}}$$

$$G_{g0} = g_2 \left(R \parallel r_2\right) = M$$

Transfer function salient features

Table 11.3. Salient features of DCM converter small-signal transfer functions

Converter	G_{d0}	G_{g0}	ω_p
Buck	$\frac{2V}{D}\,\frac{1-M}{2-M}$	M	$\frac{2-M}{(1-M)RC}$
Boost	$\frac{2V}{D}\,\frac{M-1}{2M-1}$	M	$\frac{2M-1}{(M-1)RC}$
Buck-boost	$\frac{V}{D}$	M	$\frac{2}{RC}$

DCM boost example

$R = 12\ \Omega$

$L = 5\ \mu\text{H}$

$C = 470\ \mu\text{F}$

$f_s = 100\ \text{kHz}$

The output voltage is regulated to be $V = 36$ V. It is desired to determine $G_{vd}(s)$ at the operating point where the load current is $I = 3$ A and the dc input voltage is $V_g = 24$ V.

Evaluate simple model parameters

$$P = I\left(V - V_g\right) = \left(3\text{ A}\right)\left(36\text{ V} - 24\text{ V}\right) = 36\text{ W}$$

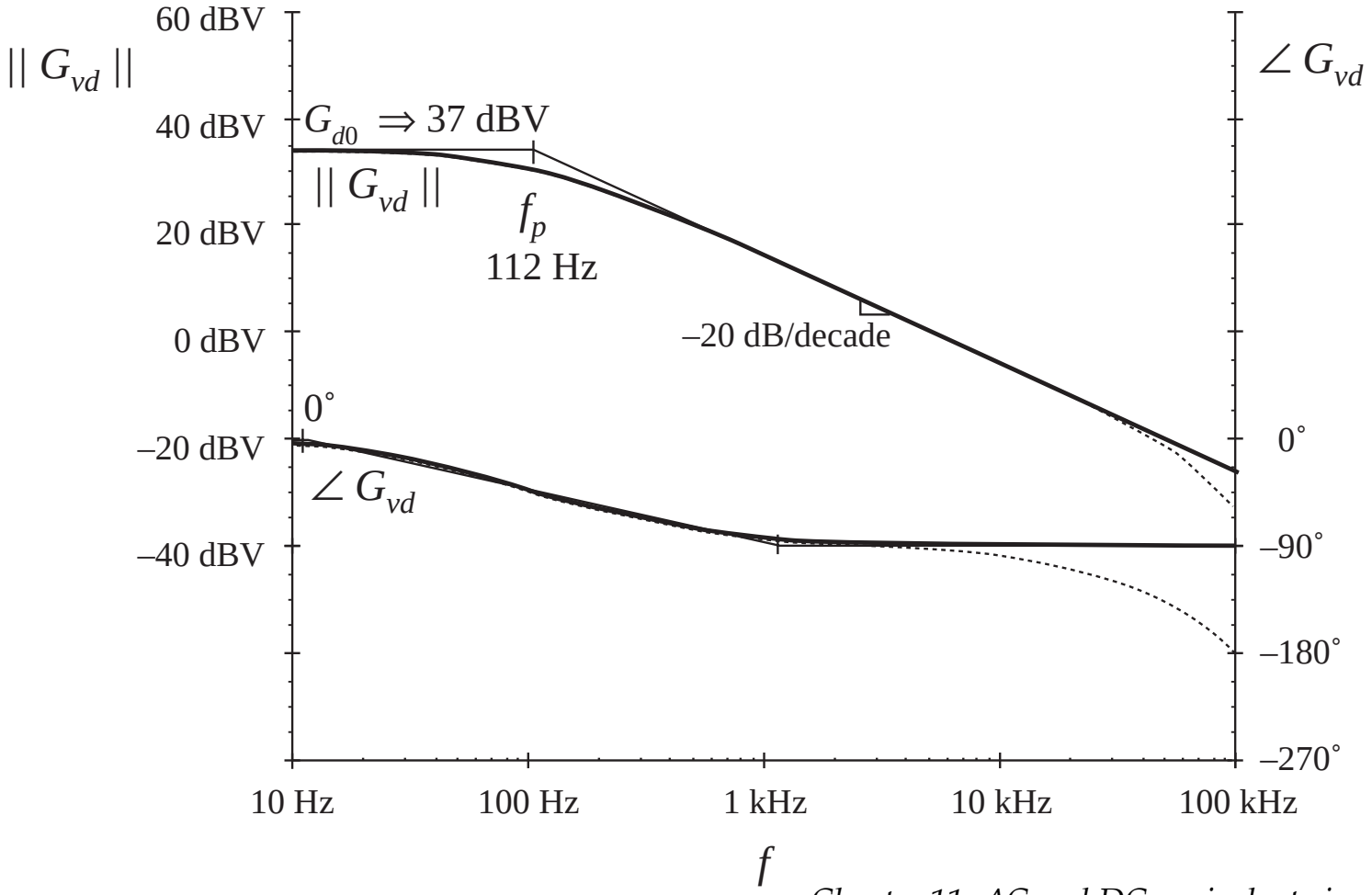
$$R_e = \frac{V_g^2}{P} = \frac{(24\text{ V})^2}{36\text{ W}} = 16\ \Omega$$

$$D = \sqrt{\frac{2L}{R_e T_s}} = \sqrt{\frac{2(5\ \mu\text{H})}{(16\ \Omega)(10\ \mu\text{s})}} = 0.25$$

$$G_{d0} = \frac{2V}{D}\,\frac{M-1}{2M-1} = \frac{2(36\text{ V})}{(0.25)}\,\frac{\left(\frac{(36\text{ V})}{(24\text{ V})} - 1\right)}{\left(2\,\frac{(36\text{ V})}{(24\text{ V})} - 1\right)} = 72\text{ V} \Rightarrow 37\text{ dBV}$$

$$f_p = \frac{\omega_p}{2\pi} = \frac{2M-1}{2\pi\,(M-1)RC} = \frac{\left(2\,\frac{(36\text{ V})}{(24\text{ V})} - 1\right)}{2\pi\left(\frac{(36\text{ V})}{(24\text{ V})} - 1\right)(12\ \Omega)(470\ \mu\text{F})} = 112\text{ Hz}$$

Control-to-output transfer function, boost example



11.4 Summary of Key Points

1. In the discontinuous conduction mode, the average transistor voltage and current are proportional, and hence obey Ohm's law. An averaged equivalent circuit can be obtained by replacing the transistor with an effective resistor $R_e(d)$. The average diode voltage and current obey a power source characteristic, with power equal to the power effectively dissipated by R_e. In the averaged equivalent circuit, the diode is replaced with a dependent power source.
2. The two-port lossless network consisting of an effective resistor and power source, which results from averaging the transistor and diode waveforms of DCM converters, is called a loss-free resistor. This network models the basic power-processing functions of DCM converters, much in the same way that the ideal dc transformer models the basic functions of CCM converters.
3. The large-signal averaged model can be solved under equilibrium conditions to determine the quiescent values of the converter currents and voltages. Average power arguments can often be used.

Key points

4. A small-signal ac model for the DCM switch network can be derived by perturbing and linearizing the loss-free resistor network. The result has the form of a two-port *y*-parameter model. The model describes the small-signal variations in the transistor and diode currents, as functions of variations in the duty cycle and in the transistor and diode ac voltage variations. This model is most convenient for ac analysis of the buck-boost converter.
5. To simplify the ac analysis of the DCM buck and boost converters, it is convenient to define two other forms of the small-signal switch model, corresponding to the switch networks of Figs. 10.16(a) and 10.16(b). These models are also *y*-parameter two-port models, but have different parameter values.

Key points

6. Since the inductor value is small when the converter operates in the discontinuous conduction mode, the inductor dynamics of the DCM buck, boost, and buck-boost converters occur at high frequency, above or just below the switching frequency. Hence, in most cases the inductor dynamics can be ignored. In the small-signal ac model, the inductance L is set to zero, and the remaining model is solved relatively easily for the low-frequency converter dynamics. The DCM buck, boost, and buck-boost converters exhibit transfer functions containing a single low-frequency dominant pole.
7. It is also possible to adapt the CCM models developed in Chapter 7 to treat converters with switches that operate in DCM, as well as other switches discussed in later chapters. The switch conversion ratio μ is a generalization of the duty cycle d of CCM switch networks; this quantity can be substituted in place of d in any CCM model. The result is a model that is valid for DCM operation. Hence, existing CCM models can be adapted directly.

Key points

8. The conversion ratio μ of DCM switch networks is a function of the applied voltage and current. As a result, the switch network contains effective feedback. So the small-signal model of a DCM converter can be expressed as the CCM converter model, plus effective feedback representing the behavior of the DCM switch network. Two effects of this feedback are increase of the converter output impedance via current feedback, and decrease of the Q-factor of the transfer function poles. The pole arising from the inductor dynamics occurs at the crossover frequency of the effective current feedback loop.

Part III. Magnetics

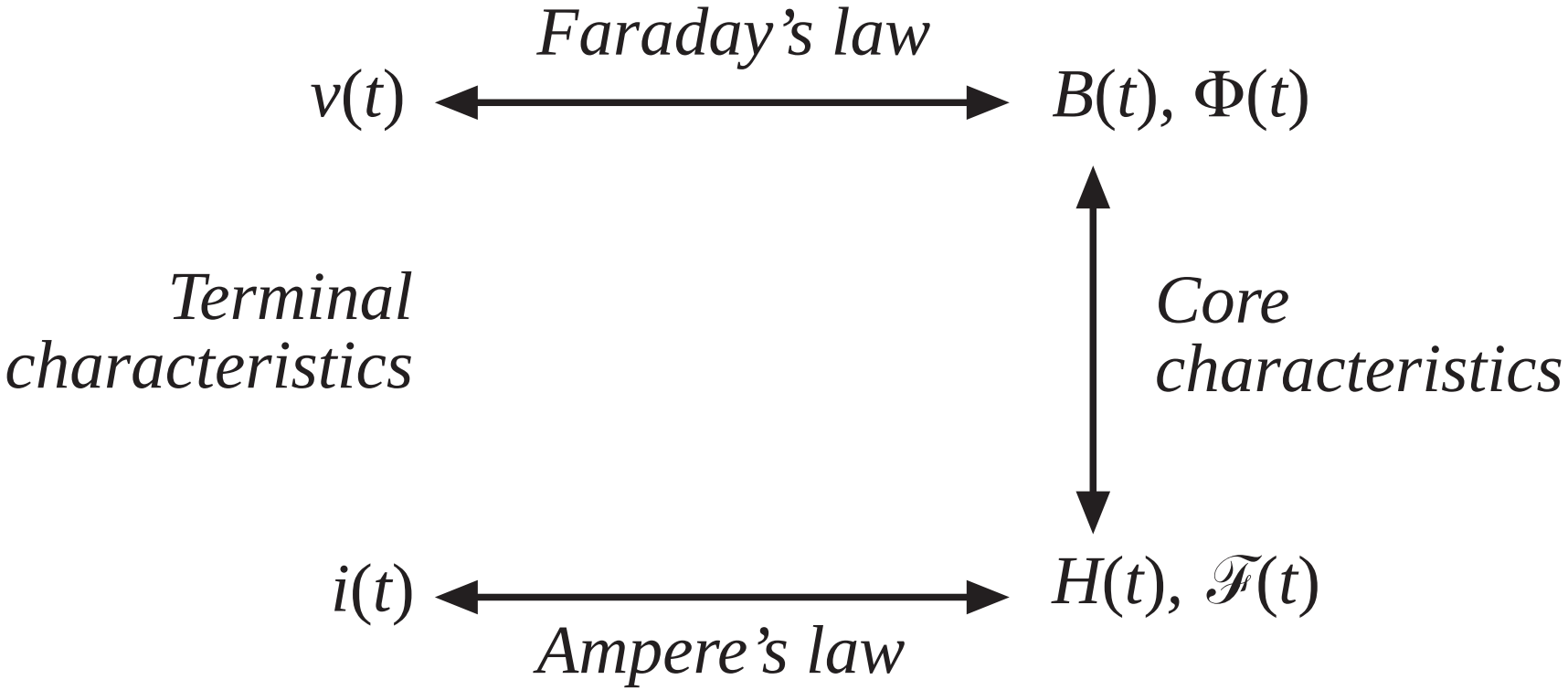
13 Basic Magnetics Theory
14 Inductor Design
15 Transformer Design

Chapter 13 Basic Magnetics Theory

Chapter 13 Basic Magnetics Theory

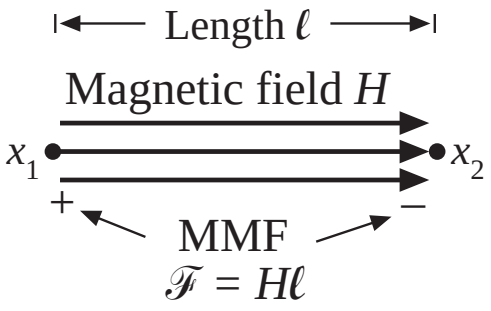
13.1 Review of Basic Magnetics

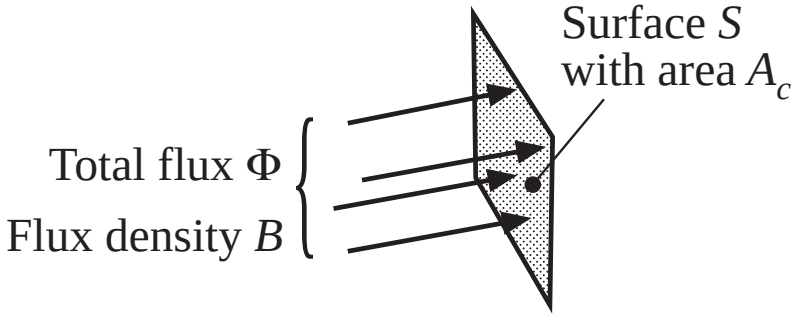
13.1.1 Basic relationships



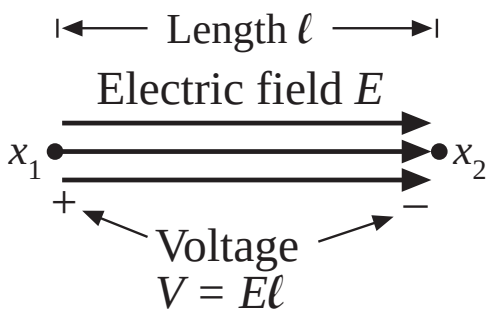
Basic quantities

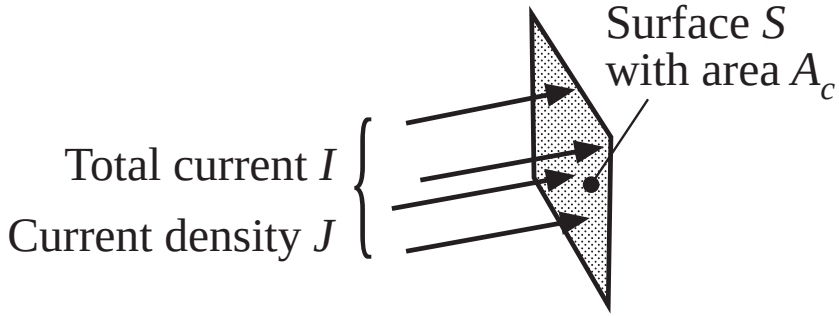
Magnetic quantities





Electrical quantities



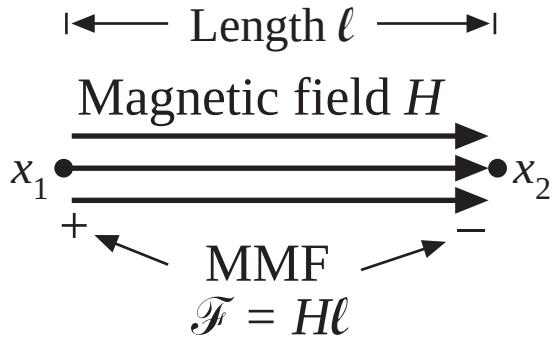


Magnetic field $\boldsymbol{H}$ and magnetomotive force $\mathscr{F}$

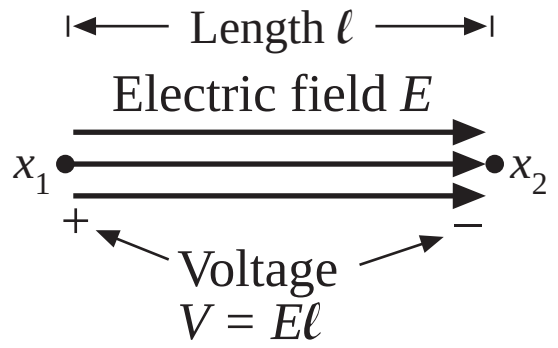
Magnetomotive force (MMF) $\mathscr{F}$ between points x_1 and x_2 is related to the magnetic field $\boldsymbol{H}$ according to

$$\mathscr{F} = \int_{x_1}^{x_2} \boldsymbol{H} \cdot d\boldsymbol{\ell}$$

Example: uniform magnetic field of magnitude H



Analogous to electric field of strength E, which induces voltage (EMF) V:

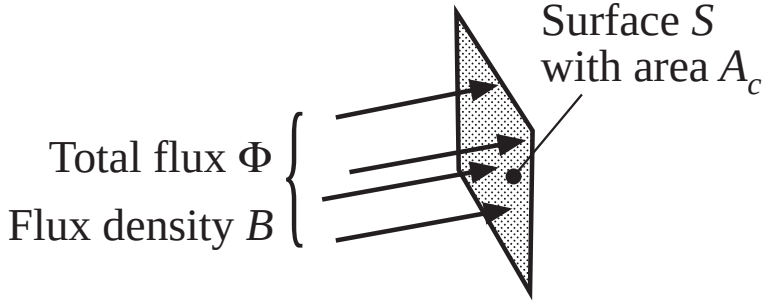


Flux density $\boldsymbol{B}$ and total flux Φ

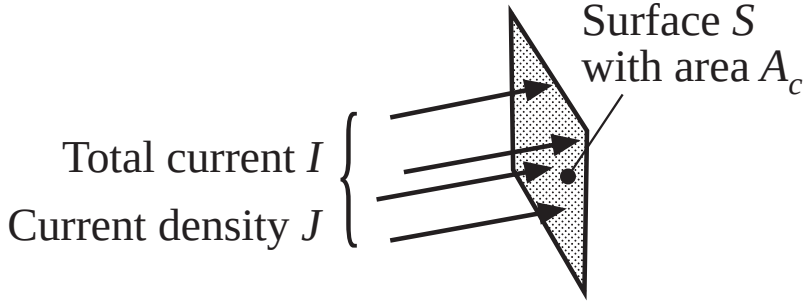
The total magnetic flux Φ passing through a surface of area A_c is related to the flux density $\boldsymbol{B}$ according to

$$\Phi = \int_{\text{surface } S} \boldsymbol{B} \cdot d\boldsymbol{A}$$

Example: uniform flux density of magnitude B



Analogous to electrical conductor current density of magnitude J, which leads to total conductor current I:



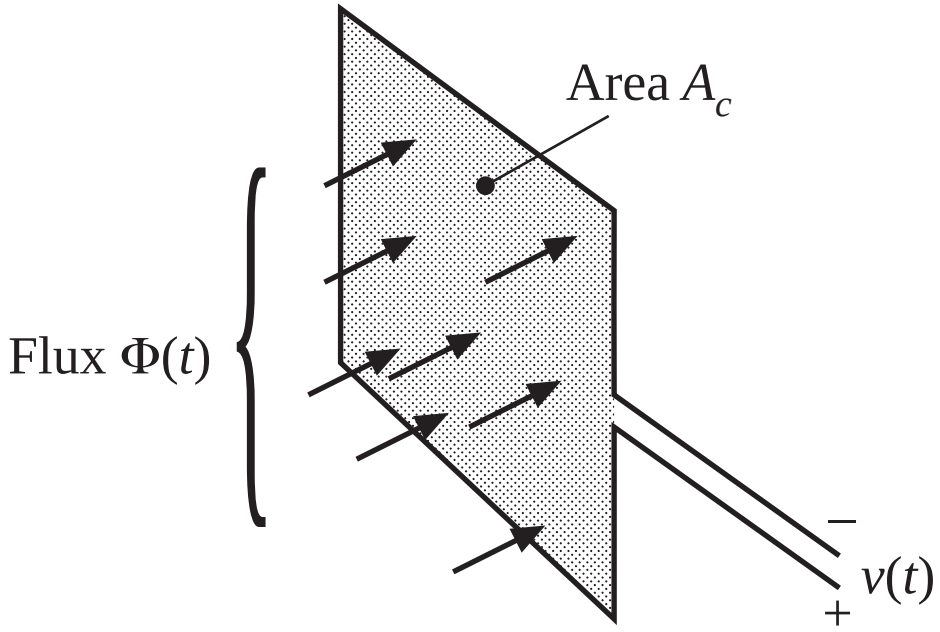
Faraday's law

Voltage $v(t)$ is induced in a loop of wire by change in the total flux $\Phi(t)$ passing through the interior of the loop, according to

$$v(t) = \frac{d\Phi(t)}{dt}$$

For uniform flux distribution, $\Phi(t) = B(t)A_c$ and hence

$$v(t) = A_c \frac{dB(t)}{dt}$$

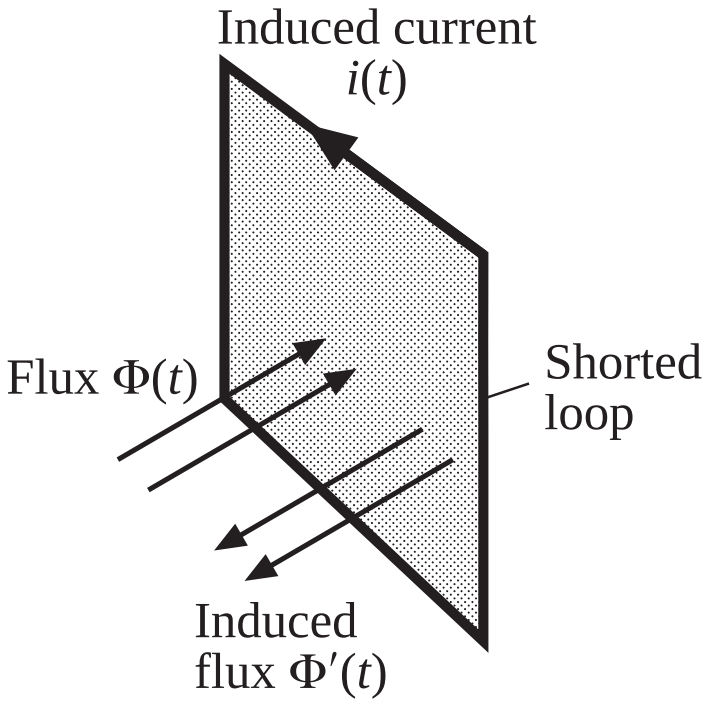


Lenz's law

The voltage $v(t)$ induced by the changing flux $\Phi(t)$ is of the polarity that tends to drive a current through the loop to counteract the flux change.

Example: a shorted loop of wire

- Changing flux $\Phi(t)$ induces a voltage $v(t)$ around the loop
- This voltage, divided by the impedance of the loop conductor, leads to current $i(t)$
- This current induces a flux $\Phi'(t)$, which tends to oppose changes in $\Phi(t)$



Ampere's law

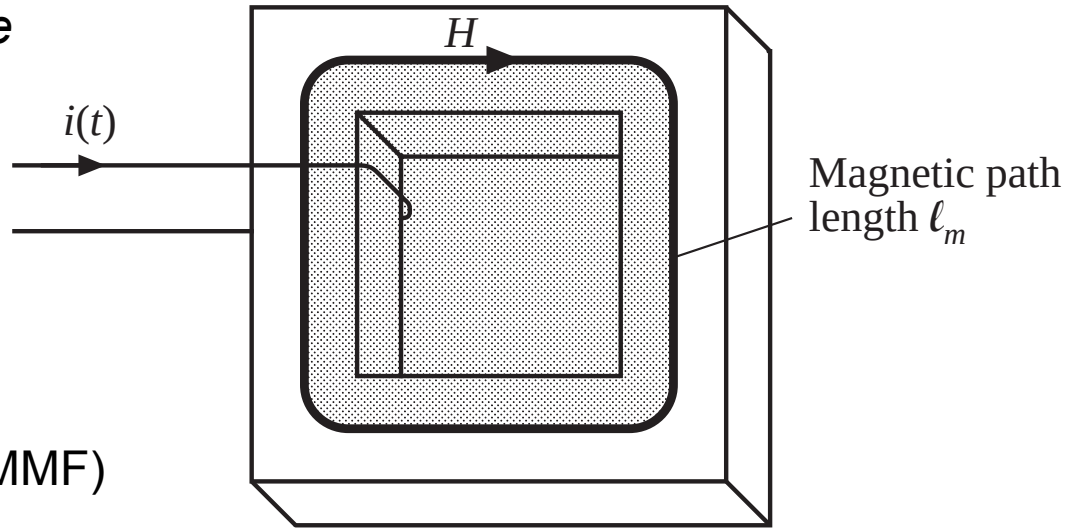
The net MMF around a closed path is equal to the total current passing through the interior of the path:

$$\oint_{\text{closed path}} \boldsymbol{H} \cdot d\boldsymbol{\ell} = \text{total current passing through interior of path}$$

Example: magnetic core. Wire carrying current $i(t)$ passes through core window.

- Illustrated path follows magnetic flux lines around interior of core
- For uniform magnetic field strength $H(t)$, the integral (MMF) is $H(t)\ell_m$. So

$$\mathcal{F}(t) = H(t)\ell_m = i(t)$$



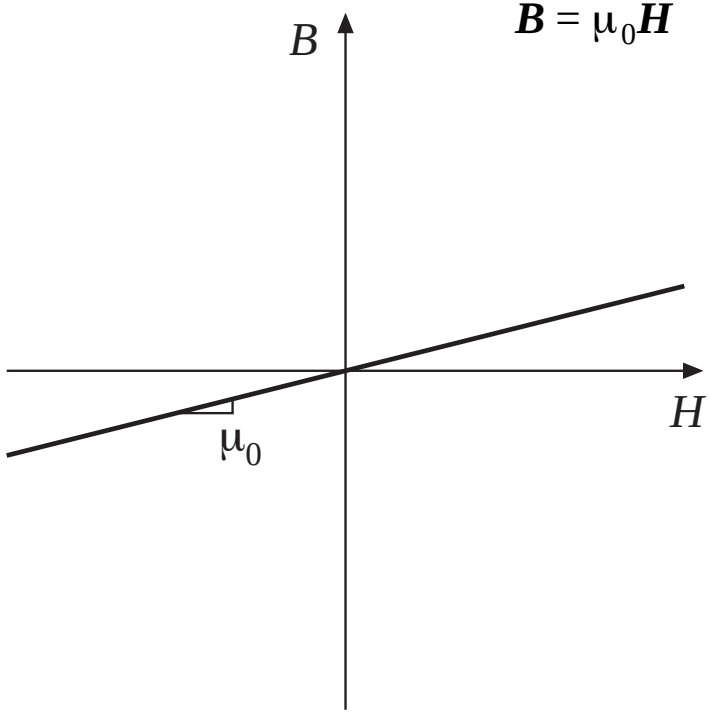
Ampere's law: discussion

- Relates magnetic field strength $H(t)$ to winding current $i(t)$
- We can view winding currents as sources of MMF
- Previous example: total MMF around core, $\mathscr{F}(t) = H(t)\ell_m$, is equal to the winding current MMF $i(t)$
- The total MMF around a closed loop, accounting for winding current MMF's, is zero

Core material characteristics: the relation between $\boldsymbol{B}$ and $\boldsymbol{H}$

Free space

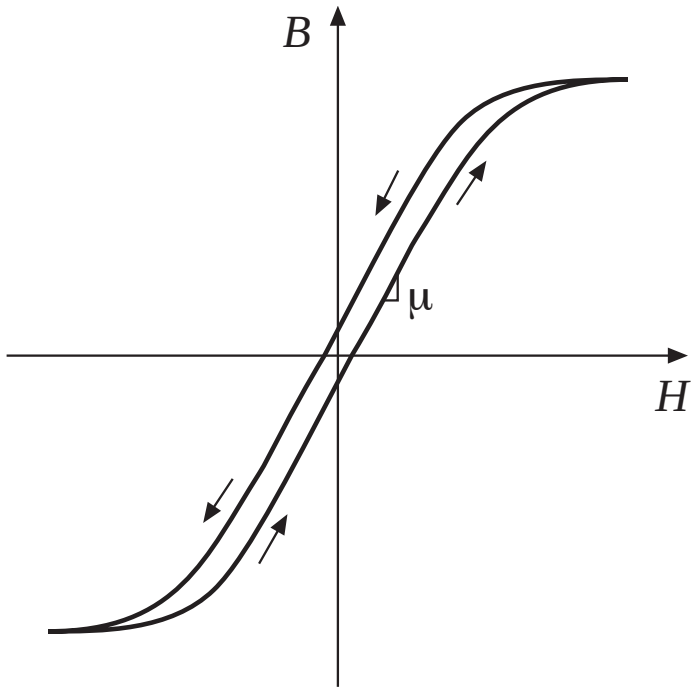
$\boldsymbol{B} = \mu_0 \boldsymbol{H}$



μ_0 = permeability of free space

= $4\pi \cdot 10^{-7}$ Henries per meter

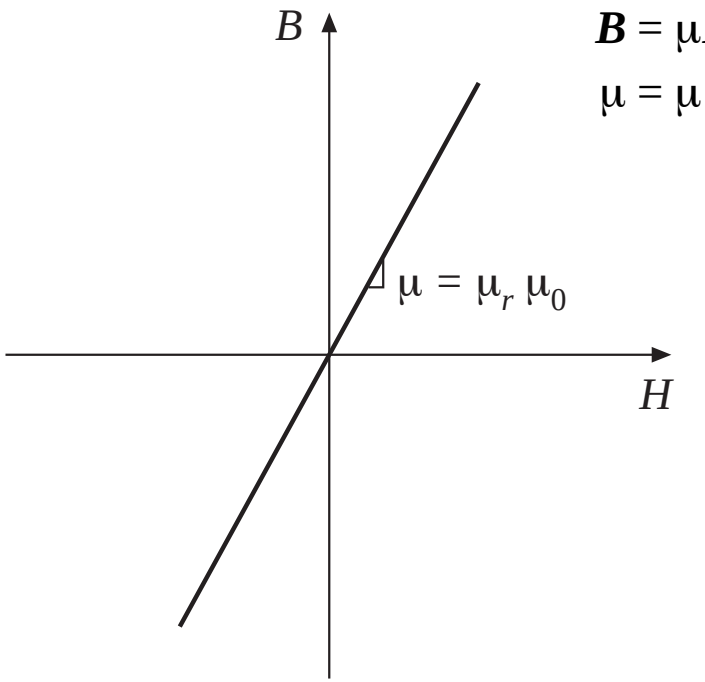
A magnetic core material



Highly nonlinear, with hysteresis and saturation

Piecewise-linear modeling of core material characteristics

No hysteresis or saturation

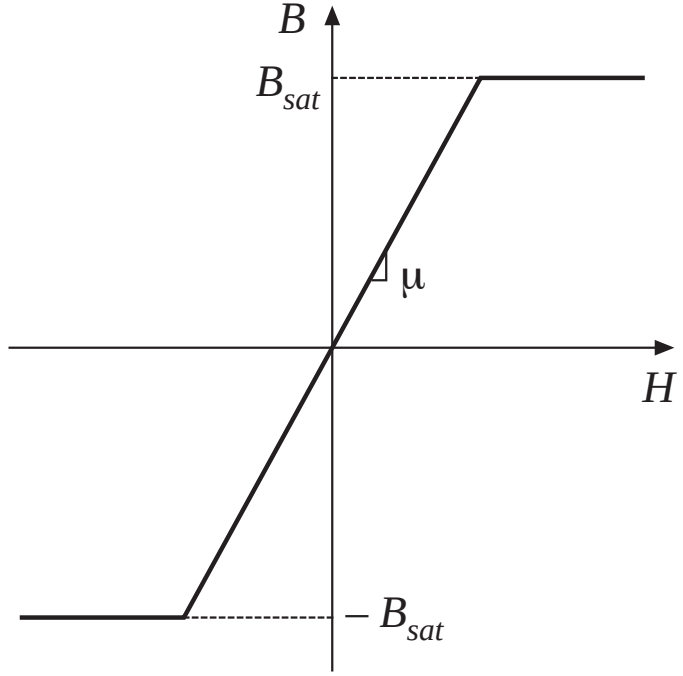


$\boldsymbol{B} = \mu \boldsymbol{H}$

$\mu = \mu_r \mu_0$

Typical $\mu_r = 10^3$ to 10^5

Saturation, no hysteresis



Typical B_{sat} = 0.3 to 0.5T, ferrite
0.5 to 1T, powdered iron
1 to 2T, iron laminations

Units

Table 12.1. Units for magnetic quantities

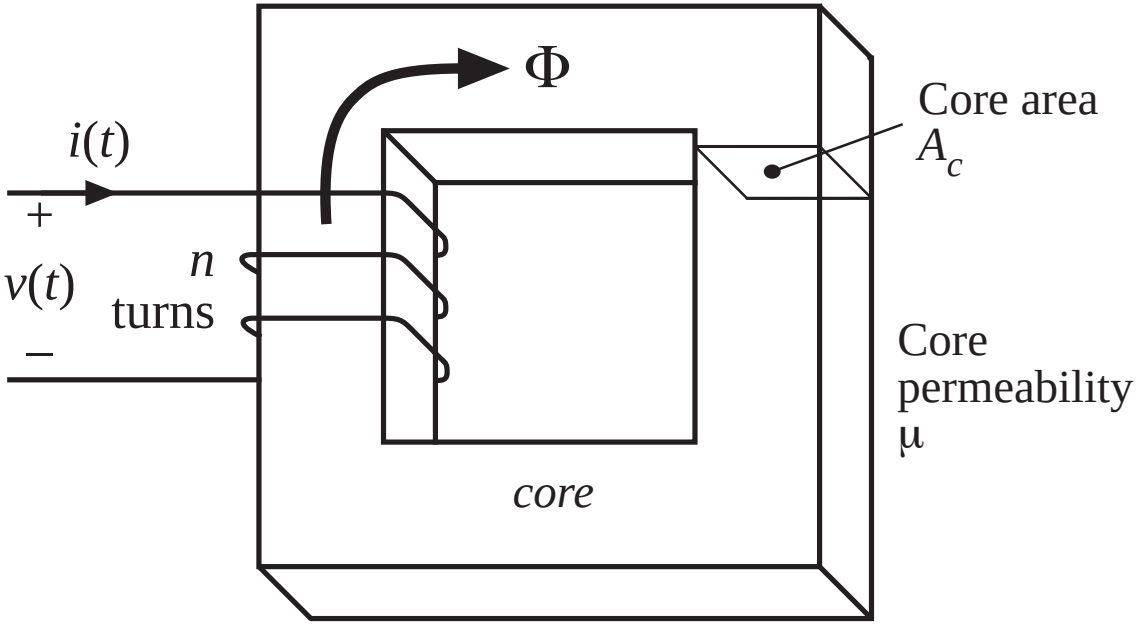
quantity	*MKS*	*unrationalized cgs*	*conversions*
core material equation	$B = \mu_0 \mu_r H$	$B = \mu_r H$	
B	Tesla	Gauss	$1\text{T} = 10^4\text{G}$
H	Ampere / meter	Oersted	$1\text{A/m} = 4\pi \cdot 10^{-3}$ Oe
Φ	Weber	Maxwell	$1\text{Wb} = 10^8$ Mx $1\text{T} = 1\text{Wb} / \text{m}^2$

Example: a simple inductor

Faraday's law:

For each turn of wire, we can write

$$v_{turn}(t) = \frac{d\Phi(t)}{dt}$$



Total winding voltage is

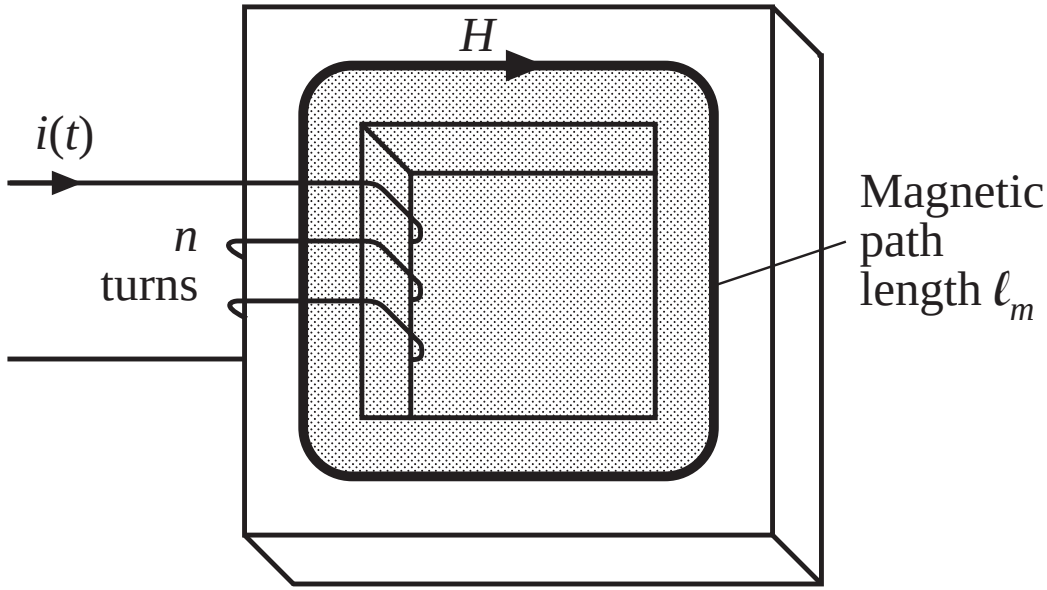
$$v(t) = nv_{turn}(t) = n\frac{d\Phi(t)}{dt}$$

Express in terms of the average flux density $B(t) = \mathscr{F}(t)/A_c$

$$v(t) = nA_c\frac{dB(t)}{dt}$$

Inductor example: Ampere's law

Choose a closed path which follows the average magnetic field line around the interior of the core. Length of this path is called the *mean magnetic path length* ℓ_m.



For uniform field strength $H(t)$, the core MMF around the path is $H\,\ell_m$.

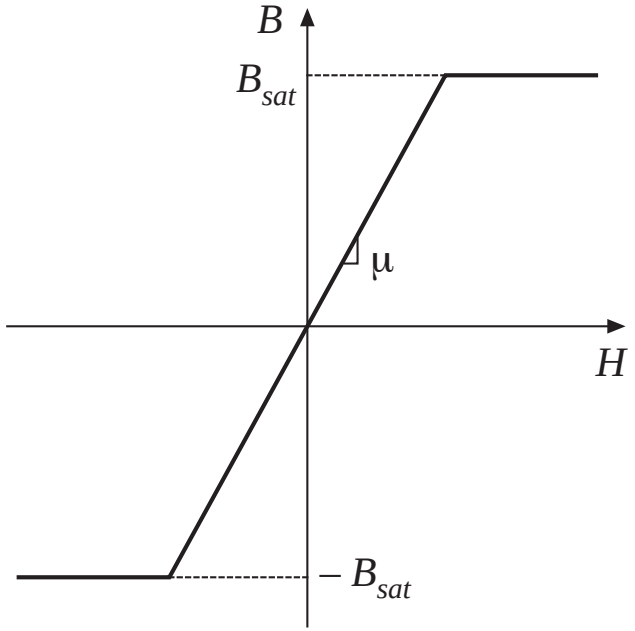
Winding contains n turns of wire, each carrying current $i(t)$. The net current passing through the path interior (i.e., through the core window) is $ni(t)$.

From Ampere's law, we have

$$H(t)\,\ell_m = n\,i(t)$$

Inductor example: core material model

$$B = \begin{cases} B_{sat} & \text{for } H \geq B_{sat}/\mu \\ \mu H & \text{for } |H| < B_{sat}/\mu \\ -B_{sat} & \text{for } H \leq -B_{sat}/\mu \end{cases}$$



Find winding current at onset of saturation: substitute $i = I_{sat}$ and $H = B_{sat}/\mu$ into equation previously derived via Ampere's law. Result is

$$I_{sat} = \frac{B_{sat}\ell_m}{\mu n}$$

Electrical terminal characteristics

We have:

$$v(t) = nA_c \frac{dB(t)}{dt} \qquad H(t)\,\ell_m = n\,i(t) \qquad B = \begin{cases} B_{sat} & \text{for } H \geq B_{sat}/\mu \\ \mu H & \text{for } |H| < B_{sat}/\mu \\ -B_{sat} & \text{for } H \leq -B_{sat}/\mu \end{cases}$$

Eliminate B and H, and solve for relation between v and i. For $|\,i\,| < I_{sat}$,

$$v(t) = \mu n A_c \frac{dH(t)}{dt} \longrightarrow v(t) = \frac{\mu n^2 A_c}{\ell_m} \frac{di(t)}{dt}$$

which is of the form

$$v(t) = L \frac{di(t)}{dt} \qquad \text{with} \qquad L = \frac{\mu n^2 A_c}{\ell_m}$$

—an inductor

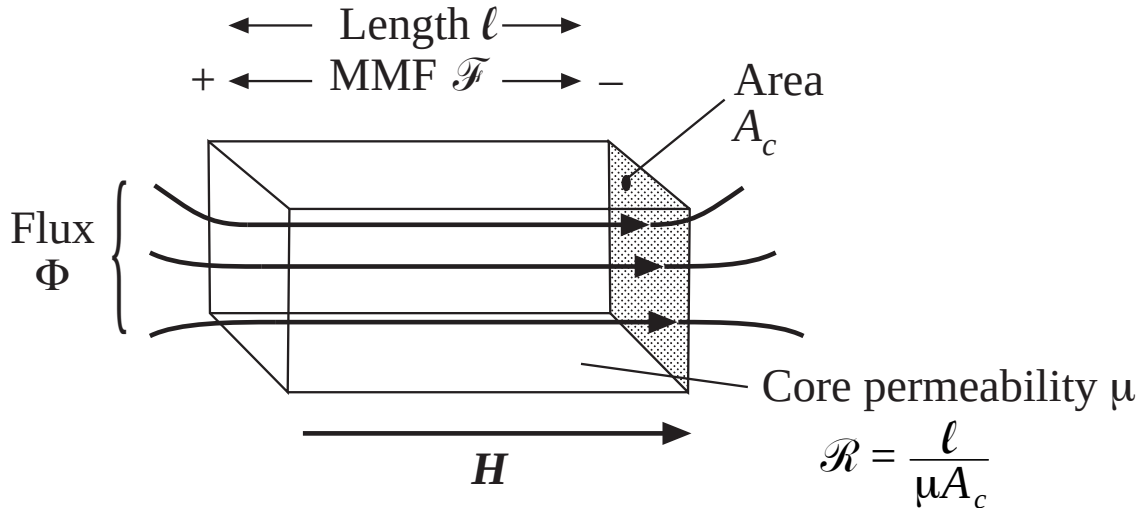
For $|\,i\,| > I_{sat}$ the flux density is constant and equal to B_{sat}. Faraday's law then predicts

$$v(t) = nA_c \frac{dB_{sat}}{dt} = 0$$

—saturation leads to short circuit

13.1.2 Magnetic circuits

Uniform flux and magnetic field inside a rectangular element:



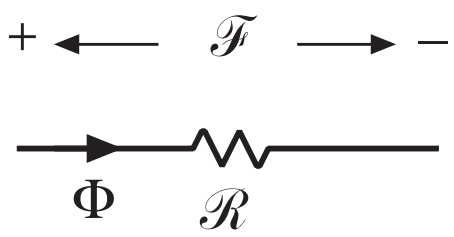
MMF between ends of element is

$$\mathscr{F} = H\ell$$

Since $H = B / \mu$ and $B = \Phi / A_c$, we can express $\mathscr{F}$ as

$$\mathscr{F} = \Phi\mathscr{R} \qquad \text{with} \qquad \mathscr{R} = \frac{\ell}{\mu A_c}$$

A corresponding model:



$\mathscr{R}$ = reluctance of element

Magnetic circuits: magnetic structures composed of multiple windings and heterogeneous elements

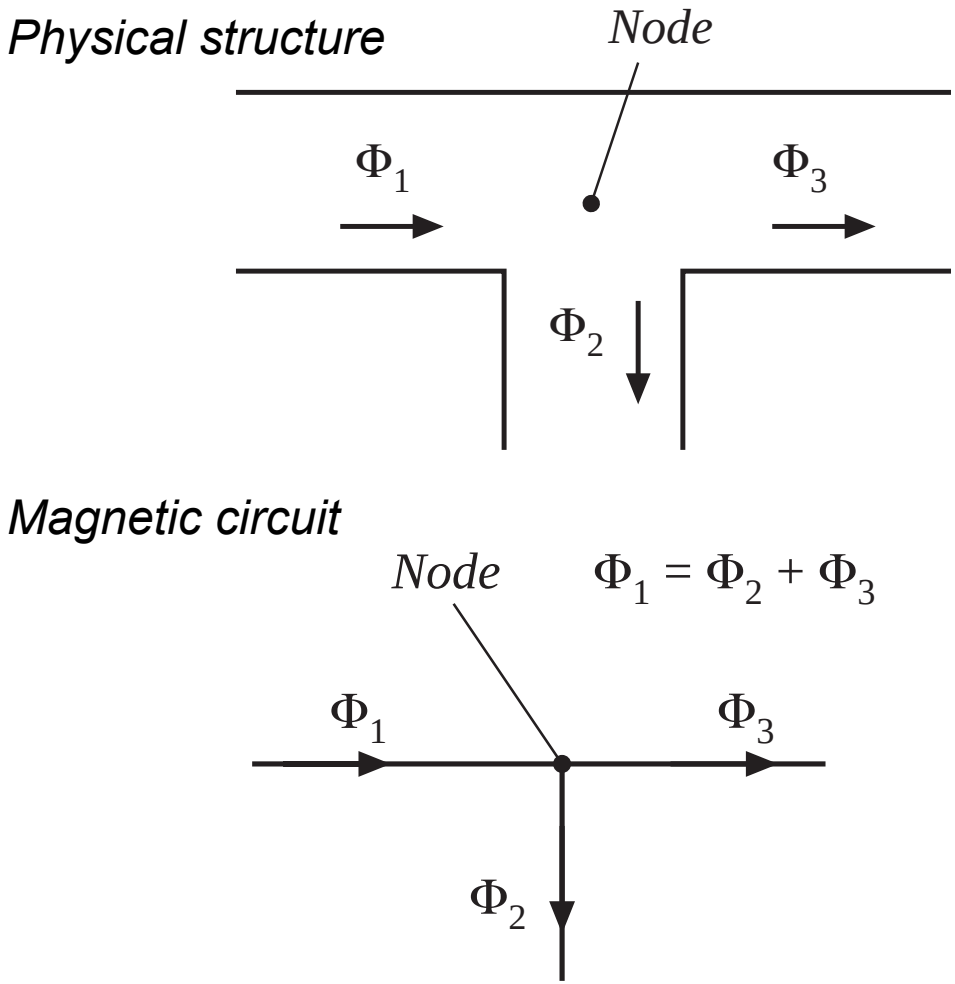
- Represent each element with reluctance
- Windings are sources of MMF
- MMF → voltage, flux → current
- Solve magnetic circuit using Kirchoff's laws, etc.

Magnetic analog of Kirchoff's current law

Divergence of $\boldsymbol{B} = 0$

Flux lines are continuous and cannot end

Total flux entering a node must be zero



Magnetic analog of Kirchoff's voltage law

Follows from Ampere's law:

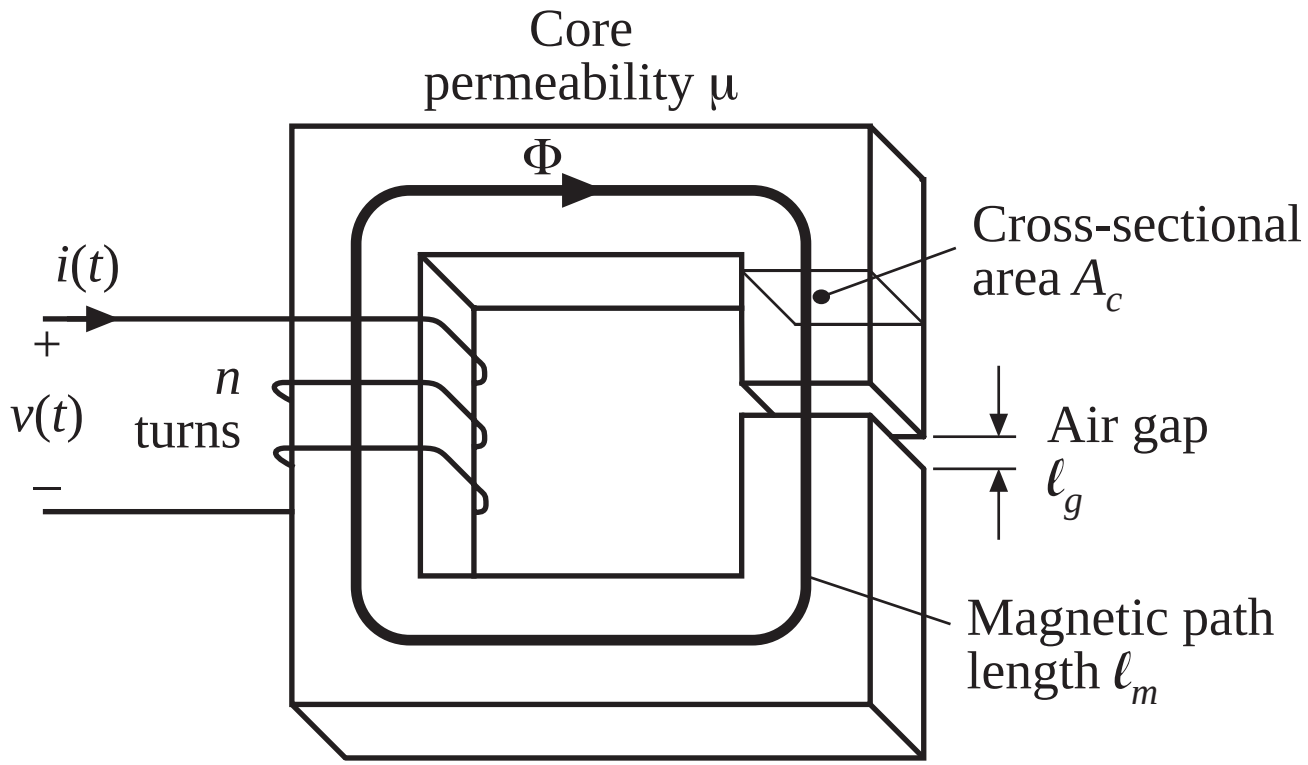
$$\oint_{closed\ path} \boldsymbol{H} \cdot d\boldsymbol{\ell} = \text{total current passing through interior of path}$$

Left-hand side: sum of MMF's across the reluctances around the closed path

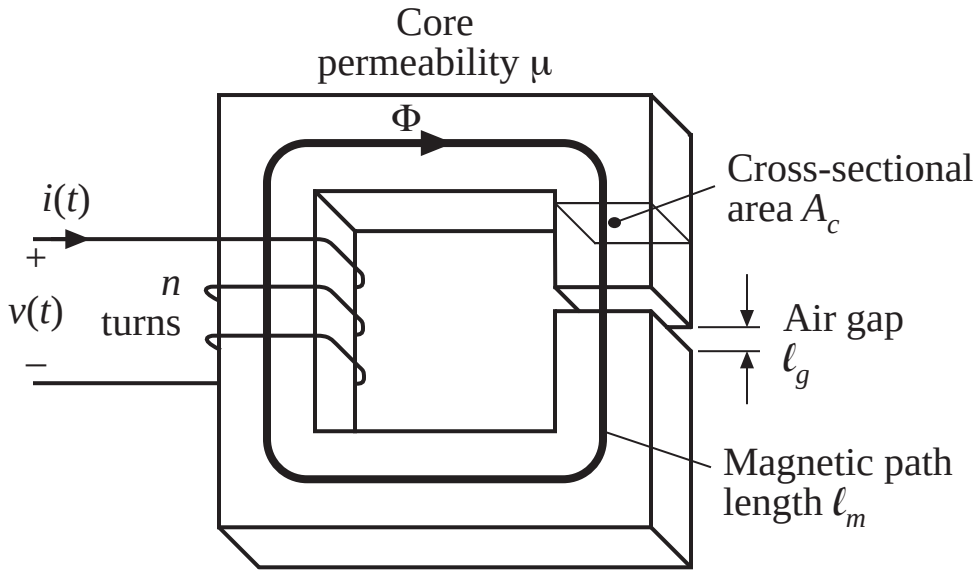
Right-hand side: currents in windings are sources of MMF's. An n-turn winding carrying current $i(t)$ is modeled as an MMF (voltage) source, of value $ni(t)$.

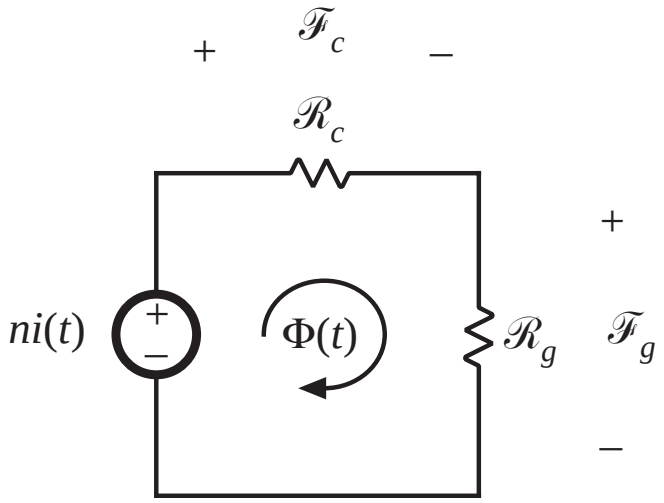
Total MMF's around the closed path add up to zero.

Example: inductor with air gap



Magnetic circuit model





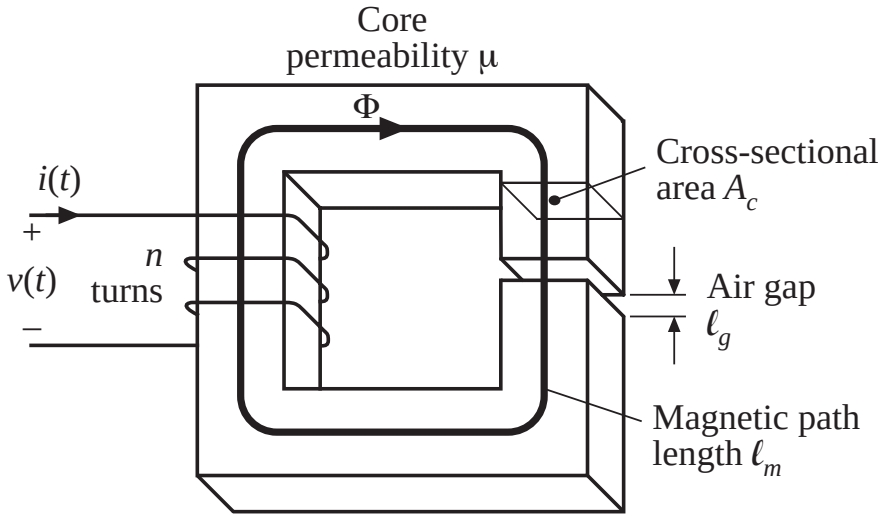
$$\mathscr{F}_c + \mathscr{F}_g = ni$$

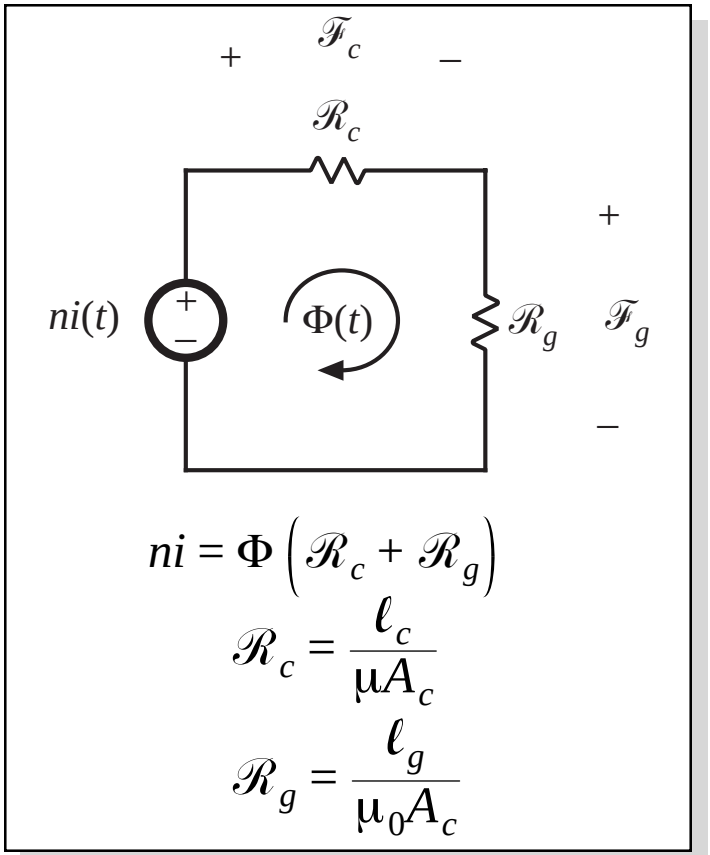
$$ni = \Phi\left(\mathscr{R}_c + \mathscr{R}_g\right)$$

$$\mathscr{R}_c = \frac{\ell_c}{\mu A_c}$$

$$\mathscr{R}_g = \frac{\ell_g}{\mu_0 A_c}$$

Solution of model





Faraday's law: $$v(t) = n \frac{d\Phi(t)}{dt}$$

Substitute for Φ: $$v(t) = \frac{n^2}{\mathscr{R}_c + \mathscr{R}_g} \frac{di(t)}{dt}$$

Hence inductance is

$$L = \frac{n^2}{\mathscr{R}_c + \mathscr{R}_g}$$

$$ni = \Phi \left(\mathscr{R}_c + \mathscr{R}_g \right)$$

$$\mathscr{R}_c = \frac{\ell_c}{\mu A_c}$$

$$\mathscr{R}_g = \frac{\ell_g}{\mu_0 A_c}$$

Effect of air gap

$$ni = \Phi \left(\mathscr{R}_c + \mathscr{R}_g \right)$$

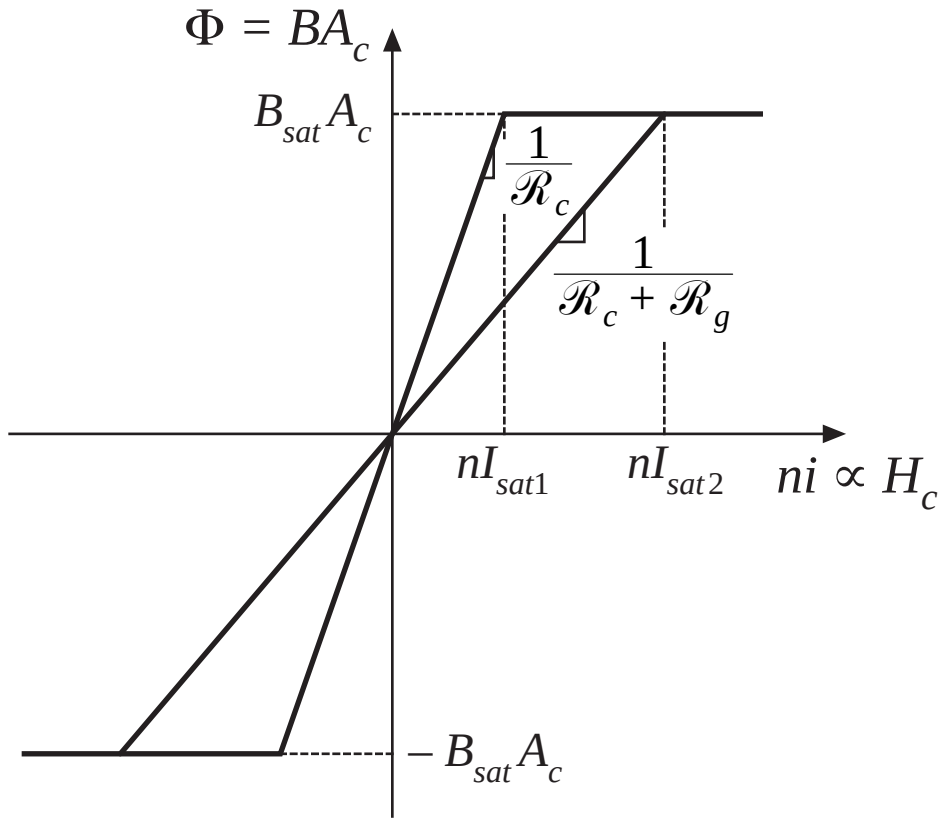
$$L = \frac{n^2}{\mathscr{R}_c + \mathscr{R}_g}$$

$$\Phi_{sat} = B_{sat} A_c$$

$$I_{sat} = \frac{B_{sat} A_c}{n} \left(\mathscr{R}_c + \mathscr{R}_g \right)$$

Effect of air gap:

- decrease inductance
- increase saturation current
- inductance is less dependent on core permeability



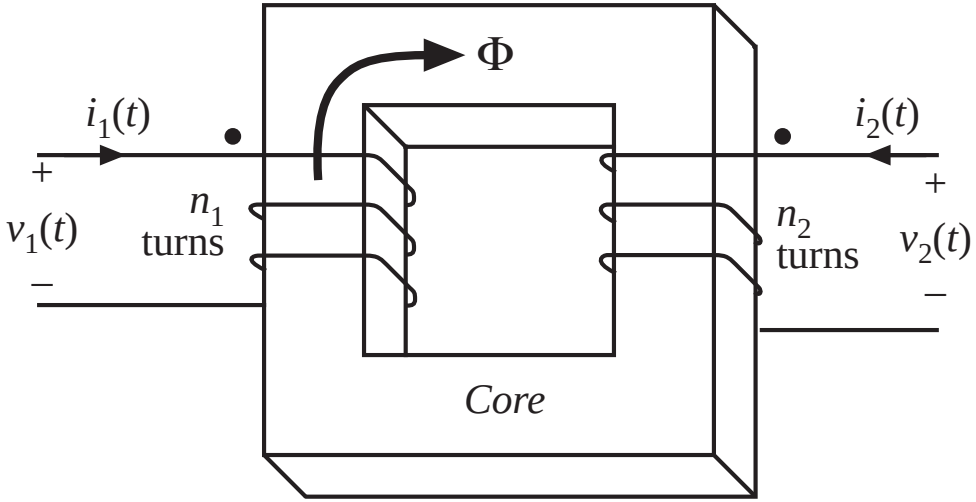
13.2 Transformer modeling

Two windings, no air gap:

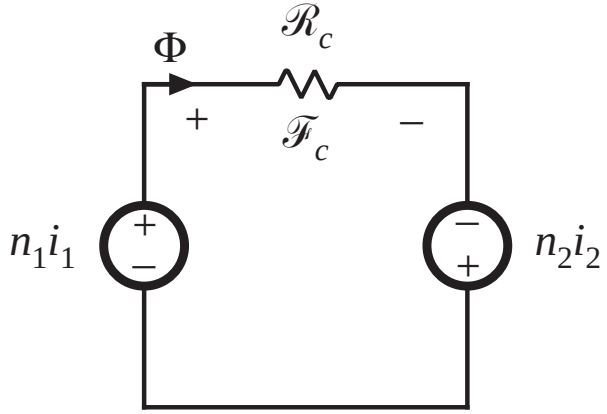
$$\mathscr{R} = \frac{\ell_m}{\mu A_c}$$

$$\mathscr{F}_c = n_1 i_1 + n_2 i_2$$

$$\Phi \mathscr{R} = n_1 i_1 + n_2 i_2$$



Magnetic circuit model:



13.2.1 The ideal transformer

In the ideal transformer, the core reluctance $\mathscr{R}$ approaches zero.

MMF $\mathscr{F}_c = \Phi\,\mathscr{R}$ also approaches zero. We then obtain

$$0 = n_1 i_1 + n_2 i_2$$

Also, by Faraday's law,

$$v_1 = n_1 \frac{d\Phi}{dt}$$

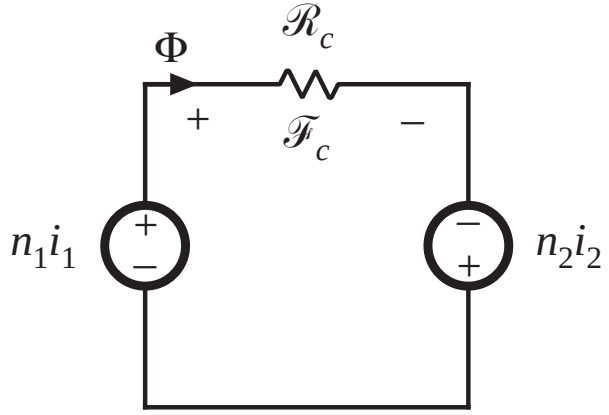
$$v_2 = n_2 \frac{d\Phi}{dt}$$

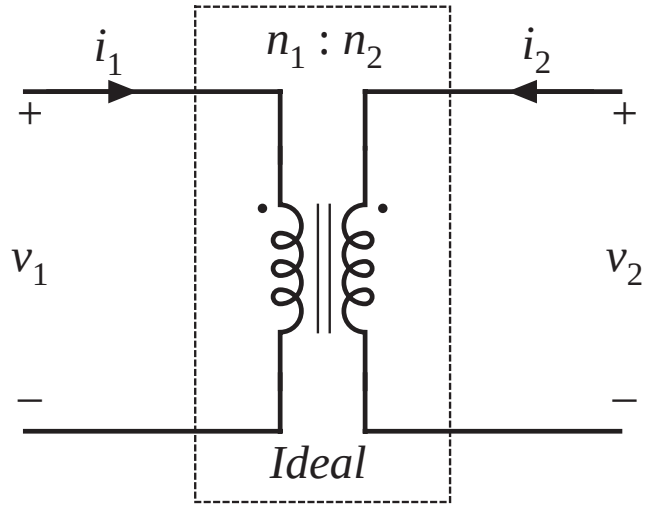
Eliminate Φ :

$$\frac{d\Phi}{dt} = \frac{v_1}{n_1} = \frac{v_2}{n_2}$$

Ideal transformer equations:

$$\frac{v_1}{n_1} = \frac{v_2}{n_2} \quad \text{and} \quad n_1 i_1 + n_2 i_2 = 0$$

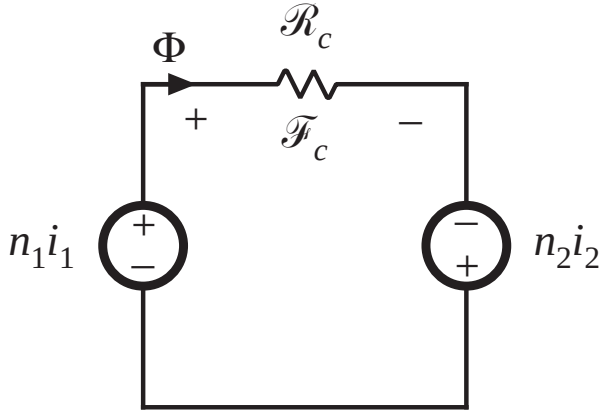




13.2.2 The magnetizing inductance

For nonzero core reluctance, we obtain

$$\Phi\mathscr{R} = n_1 i_1 + n_2 i_2 \quad \text{with} \quad v_1 = n_1 \frac{d\Phi}{dt}$$



Eliminate Φ:

$$v_1 = \frac{n_1^2}{\mathscr{R}} \frac{d}{dt}\left[i_1 + \frac{n_2}{n_1} i_2 \right]$$

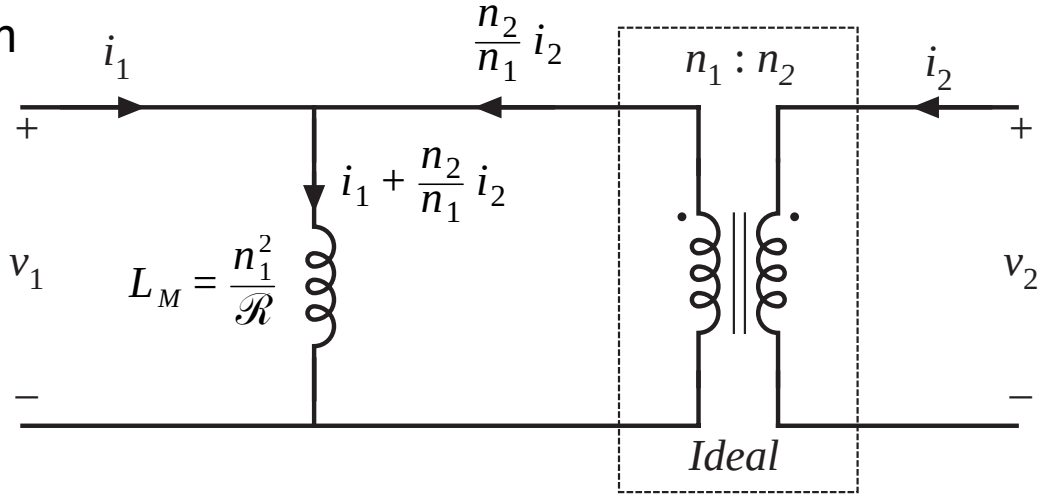
This equation is of the form

$$v_1 = L_M \frac{di_M}{dt}$$

with

$$L_M = \frac{n_1^2}{\mathscr{R}}$$

$$i_M = i_1 + \frac{n_2}{n_1} i_2$$



Magnetizing inductance: discussion

- Models magnetization of core material
- A real, physical inductor, that exhibits saturation and hysteresis
- If the secondary winding is disconnected:

  we are left with the primary winding on the core

  primary winding then behaves as an inductor

  the resulting inductor is the magnetizing inductance, referred to the primary winding
- Magnetizing current causes the ratio of winding currents to differ from the turns ratio

Transformer saturation

- Saturation occurs when core flux density $B(t)$ exceeds saturation flux density B_{sat}.
- When core saturates, the magnetizing current becomes large, the impedance of the magnetizing inductance becomes small, and the windings are effectively shorted out.
- Large winding currents $i_1(t)$ and $i_2(t)$ ***do not*** necessarily lead to saturation. If

  $$0 = n_1 i_1 + n_2 i_2$$

  then the magnetizing current is zero, and there is no net magnetization of the core.
- Saturation is caused by excessive applied volt-seconds

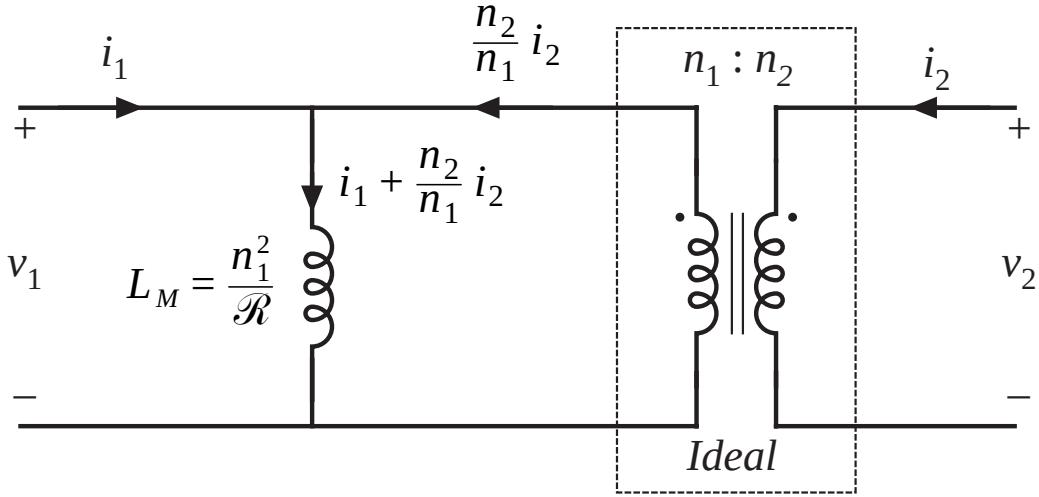
Saturation vs. applied volt-seconds

Magnetizing current depends on the integral of the applied winding voltage:

$$i_M(t) = \frac{1}{L_M} \int v_1(t)\,dt$$

Flux density is proportional:

$$B(t) = \frac{1}{n_1 A_c} \int v_1(t)\,dt$$

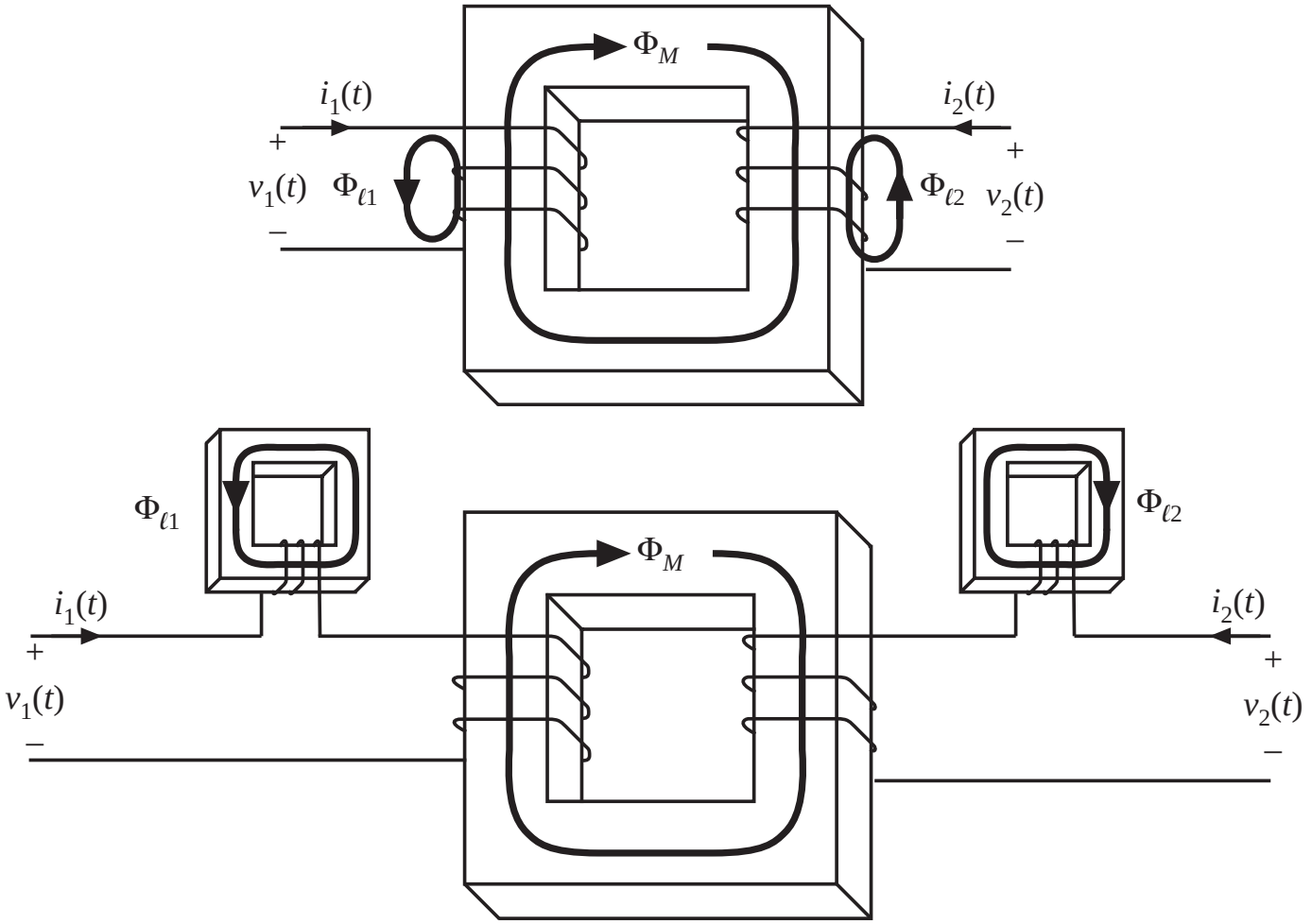


Flux density becomes large, and core saturates, when the applied volt-seconds λ_1 are too large, where

$$\lambda_1 = \int_{t_1}^{t_2} v_1(t)\,dt$$

limits of integration chosen to coincide with positive portion of applied voltage waveform

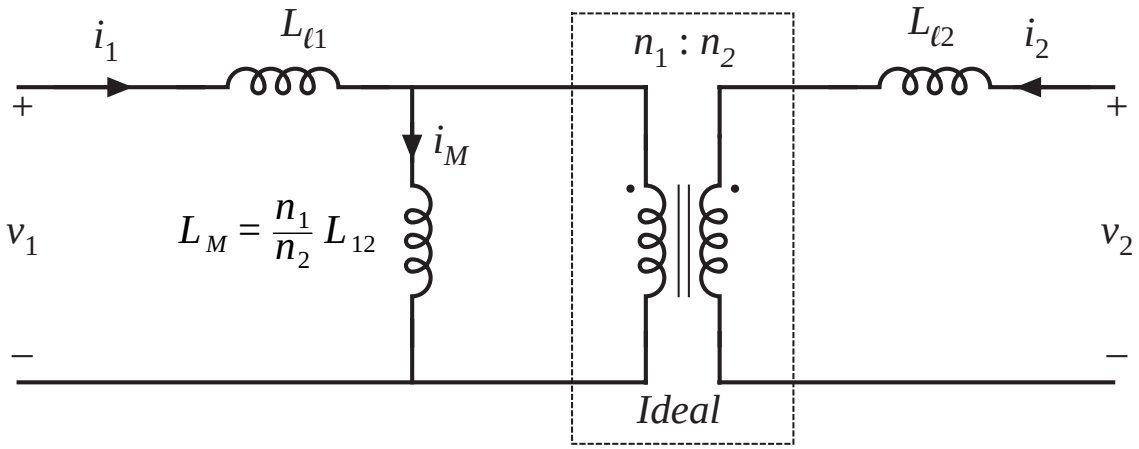
13.2.3 Leakage inductances



Transformer model, including leakage inductance

Terminal equations can be written in the form

$$\begin{bmatrix} v_1(t) \\ v_2(t) \end{bmatrix} = \begin{bmatrix} L_{11} & L_{12} \\ L_{12} & L_{22} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_1(t) \\ i_2(t) \end{bmatrix}$$



mutual inductance:

$$L_{12} = \frac{n_1 n_2}{\mathcal{R}} = \frac{n_2}{n_1} L_M$$

primary and secondary self-inductances:

$$L_{11} = L_{\ell 1} + \frac{n_1}{n_2} L_{12}$$

$$L_{22} = L_{\ell 2} + \frac{n_2}{n_1} L_{12}$$

effective turns ratio $n_e = \sqrt{\frac{L_{22}}{L_{11}}}$

coupling coefficient $k = \frac{L_{12}}{\sqrt{L_{11} L_{22}}}$

13.3 Loss mechanisms in magnetic devices

Low-frequency losses:

- Dc copper loss
- Core loss: hysteresis loss

High-frequency losses: the skin effect

- Core loss: classical eddy current losses
- Eddy current losses in ferrite cores

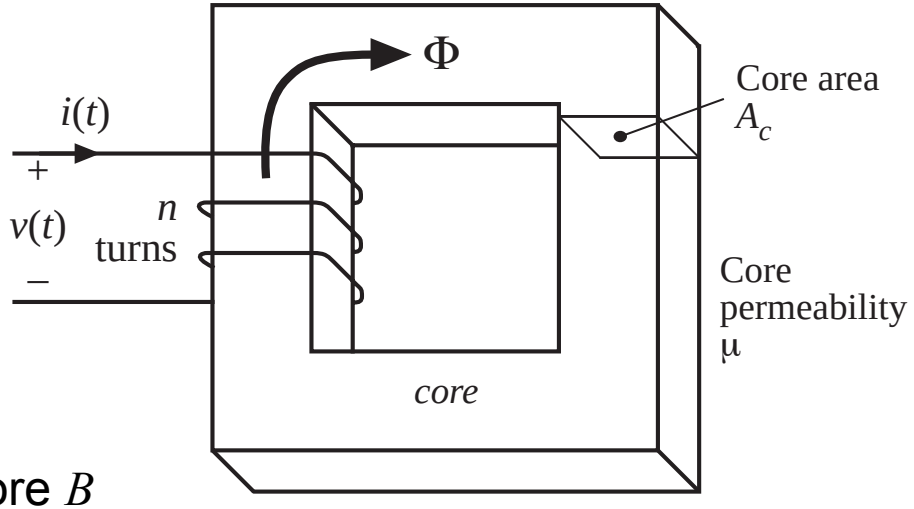
High frequency copper loss: the proximity effect

- Proximity effect: high frequency limit
- MMF diagrams, losses in a layer, and losses in basic multilayer windings
- Effect of PWM waveform harmonics

13.3.1 Core loss

Energy per cycle W flowing into n-turn winding of an inductor, excited by periodic waveforms of frequency f:

$$W = \int_{\text{one cycle}} v(t) i(t) \, dt$$



Relate winding voltage and current to core B and H via Faraday's law and Ampere's law:

$$v(t) = nA_c \frac{dB(t)}{dt} \qquad H(t)\ell_m = ni(t)$$

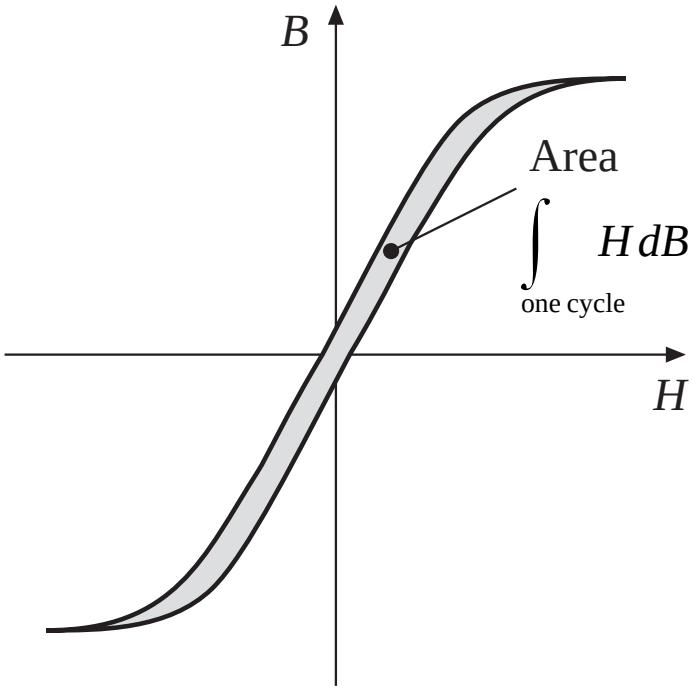
Substitute into integral:

$$W = \int_{\text{one cycle}} \left(nA_c \frac{dB(t)}{dt} \right) \left(\frac{H(t)\ell_m}{n} \right) dt$$

$$= \left(A_c \ell_m \right) \int_{\text{one cycle}} H \, dB$$

Core loss: Hysteresis loss

$$W = \left(A_c \ell_m\right) \int_{\text{one cycle}} H\, dB$$



The term $A_c \ell_m$ is the volume of the core, while the integral is the area of the B–H loop.

(energy lost per cycle) = (core volume) (area of B–H loop)

$$P_H = \left(f\right)\left(A_c \ell_m\right) \int_{\text{one cycle}} H\, dB$$

Hysteresis loss is directly proportional to applied frequency

Modeling hysteresis loss

- Hysteresis loss varies directly with applied frequency
- Dependence on maximum flux density: how does area of B–H loop depend on maximum flux density (and on applied waveforms)? Empirical equation (Steinmetz equation):

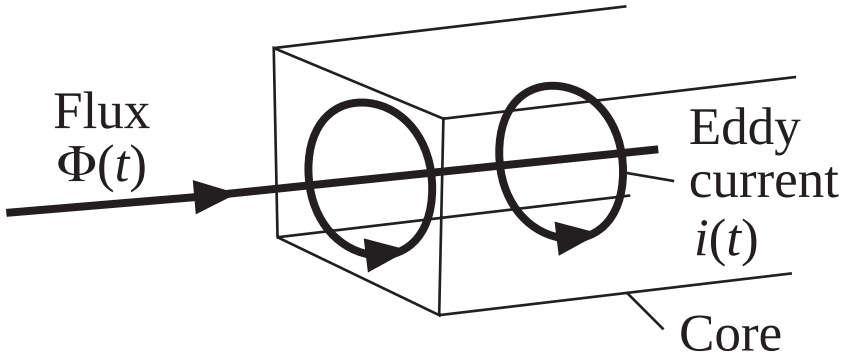
$$P_H = K_H f B_{\max}^{\alpha} (\textit{core volume})$$

The parameters K_H and α are determined experimentally.

Dependence of P_H on B_{max} is predicted by the theory of magnetic domains.

Core loss: eddy current loss

Magnetic core materials are reasonably good conductors of electric current. Hence, according to Lenz's law, magnetic fields within the core induce currents ("eddy currents") to flow within the core. The eddy currents flow such that they tend to generate a flux which opposes changes in the core flux $\Phi(t)$. The eddy currents tend to prevent flux from penetrating the core.



Eddy current loss $i^2(t)R$

Modeling eddy current loss

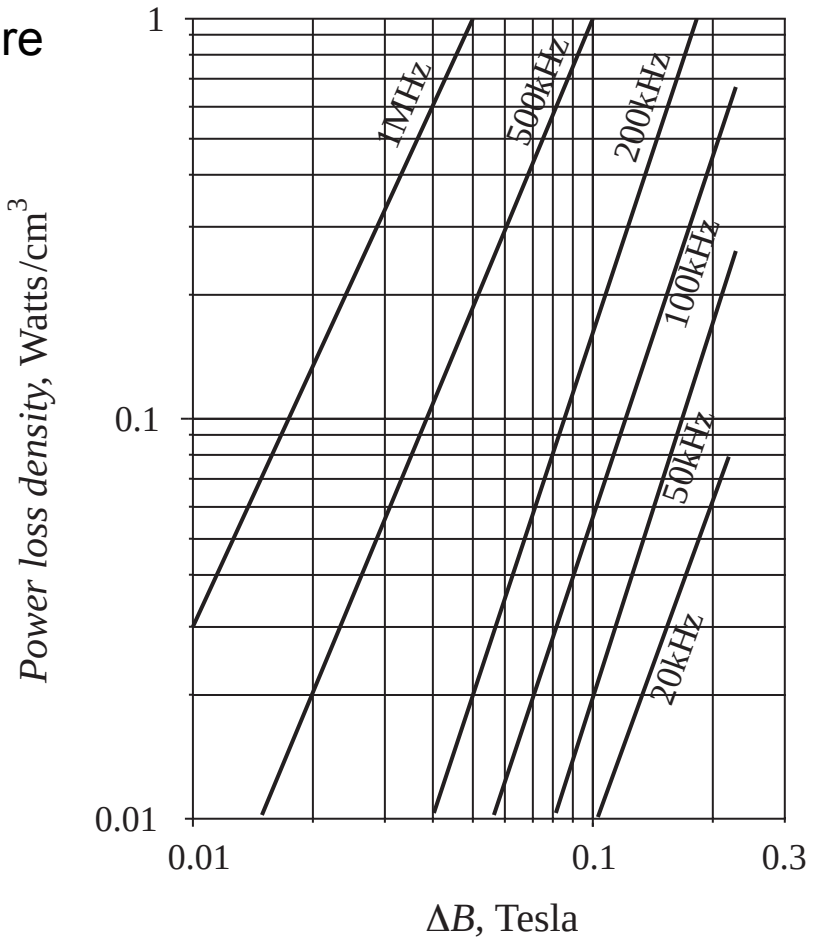
- Ac flux $\Phi(t)$ induces voltage $v(t)$ in core, according to Faraday's law. Induced voltage is proportional to derivative of $\Phi(t)$. In consequence, magnitude of induced voltage is directly proportional to excitation frequency f.
- If core material impedance Z is purely resistive and independent of frequency, $Z = R$, then eddy current magnitude is proportional to voltage: $i(t) = v(t)/R$. Hence magnitude of $i(t)$ is directly proportional to excitation frequency f.
- Eddy current power loss $i^2(t)R$ then varies with square of excitation frequency f.
- Classical Steinmetz equation for eddy current loss:

$$P_E = K_E f^2 B_{\max}^2 (\textit{core volume})$$

- Ferrite core material impedance is capacitive. This causes eddy current power loss to increase as f^4.

Total core loss: manufacturer's data

Ferrite core material



Empirical equation, at a fixed frequency:

$$P_{fe} = K_{fe} (\Delta B)^{\beta} A_c \ell_m$$

Core materials

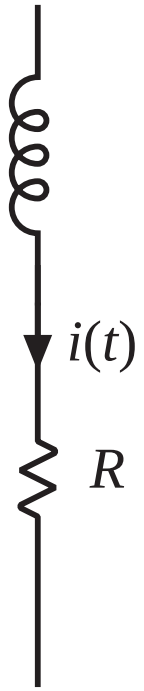
Core type	B_{sat}	Relative core loss	Applications
Laminations iron, silicon steel	1.5 - 2.0 T	high	50-60 Hz transformers, inductors
Powdered cores powdered iron, molypermalloy	0.6 - 0.8 T	medium	1 kHz transformers, 100 kHz filter inductors
Ferrite Manganese-zinc, Nickel-zinc	0.25 - 0.5 T	low	20 kHz - 1 MHz transformers, ac inductors

13.3.2 Low-frequency copper loss

DC resistance of wire

$$R = \rho \frac{\ell_b}{A_w}$$

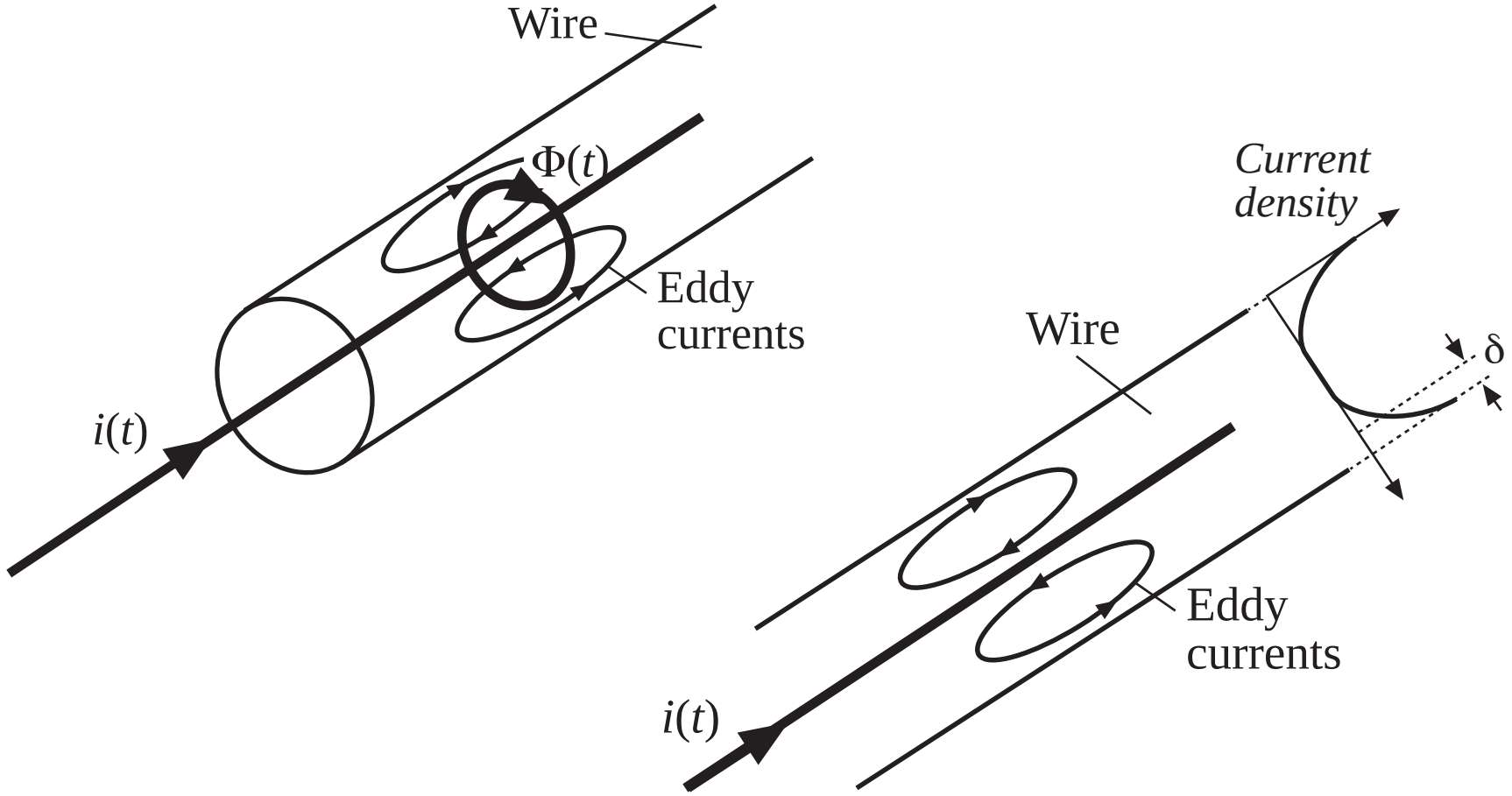
where A_w is the wire bare cross-sectional area, and ℓ_b is the length of the wire. The resistivity ρ is equal to $1.724 \cdot 10^{-6}\ \Omega\ \text{cm}$ for soft-annealed copper at room temperature. This resistivity increases to $2.3 \cdot 10^{-6}\ \Omega\ \text{cm}$ at 100°C.



The wire resistance leads to a power loss of

$$P_{cu} = I_{rms}^2 R$$

13.4 Eddy currents in winding conductors
13.4.1 Intro to the skin and proximity effects



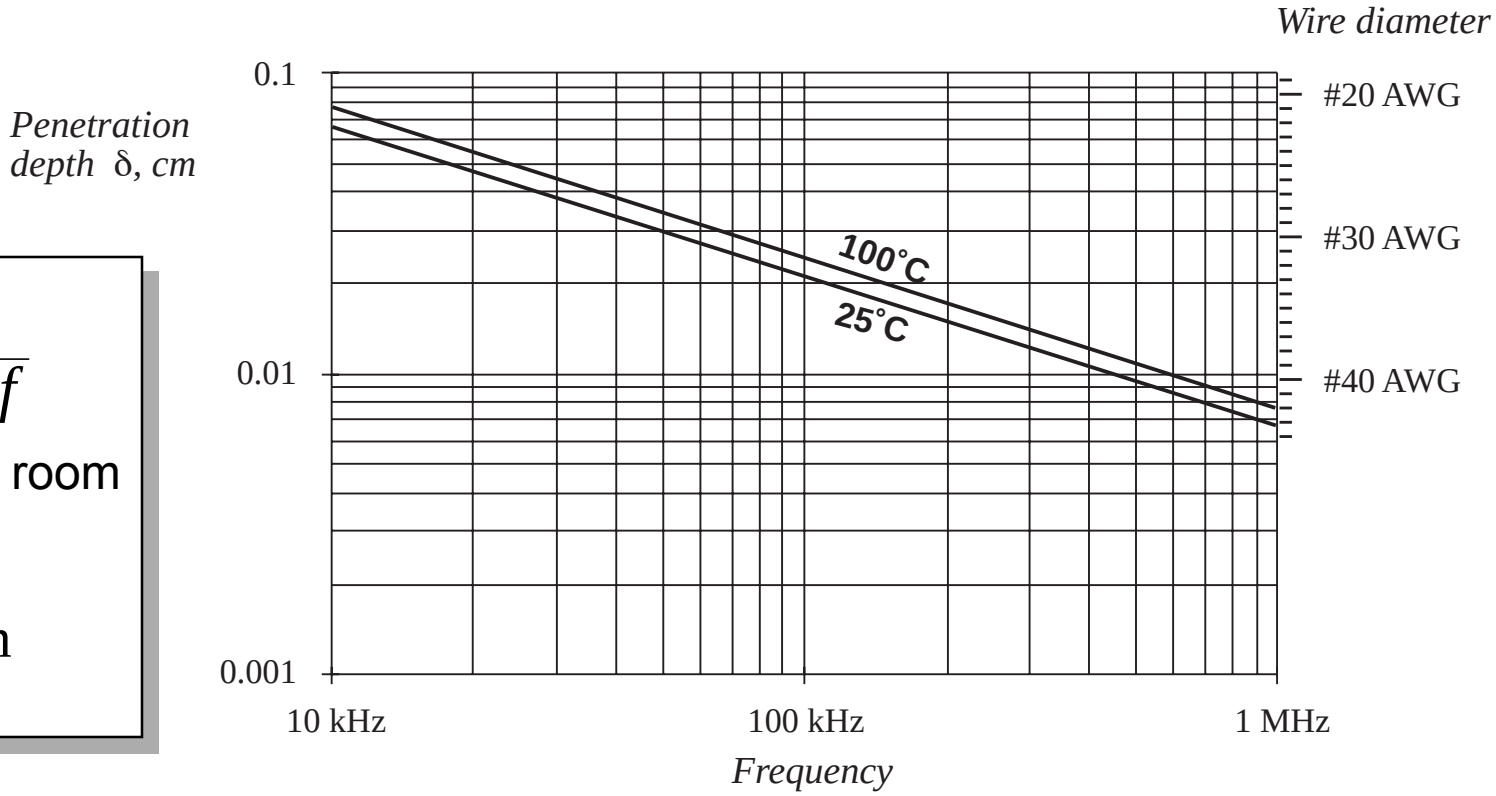
Penetration depth δ

For sinusoidal currents: current density is an exponentially decaying function of distance into the conductor, with characteristic length δ known as the *penetration depth* or *skin depth*.

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}}$$

For copper at room temperature:

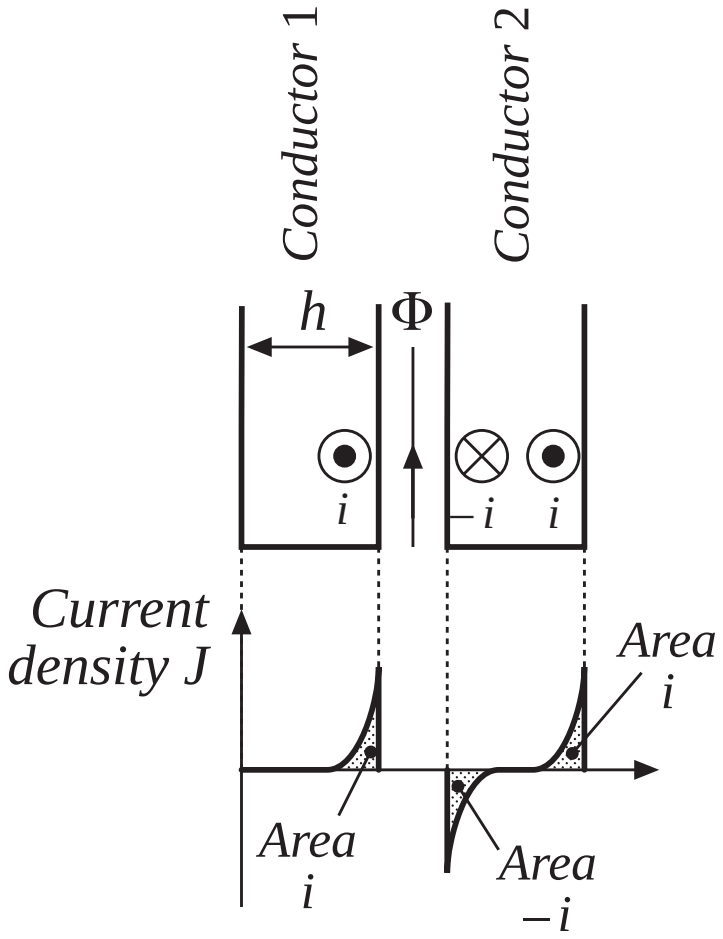
$$\delta = \frac{7.5}{\sqrt{f}} \text{ cm}$$



The proximity effect

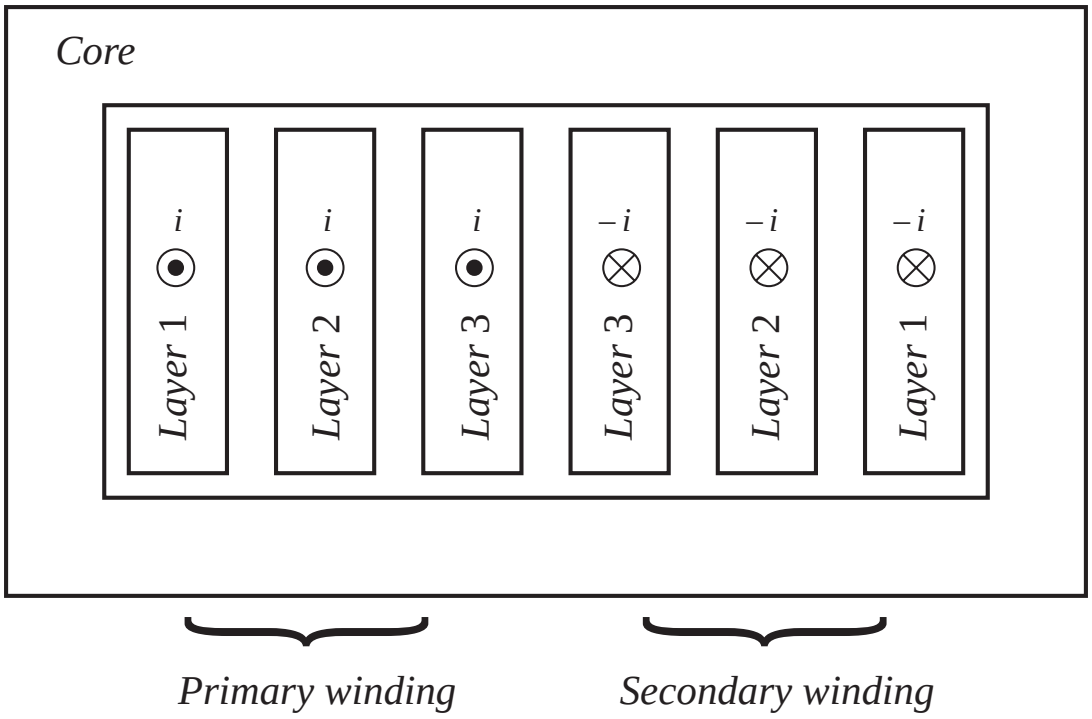
Ac current in a conductor induces eddy currents in adjacent conductors by a process called the *proximity effect*. This causes significant power loss in the windings of high-frequency transformers and ac inductors.

A multi-layer foil winding, with $h \gg \delta$. Each layer carries net current $i(t)$.



Example: a two-winding transformer

Cross-sectional view of two-winding transformer example. Primary turns are wound in three layers. For this example, let's assume that each layer is one turn of a flat foil conductor. The secondary is a similar three-layer winding. Each layer carries net current $i(t)$. Portions of the windings that lie outside of the core window are not illustrated. Each layer has thickness $h \gg \delta$.



Distribution of currents on surfaces of conductors: two-winding example

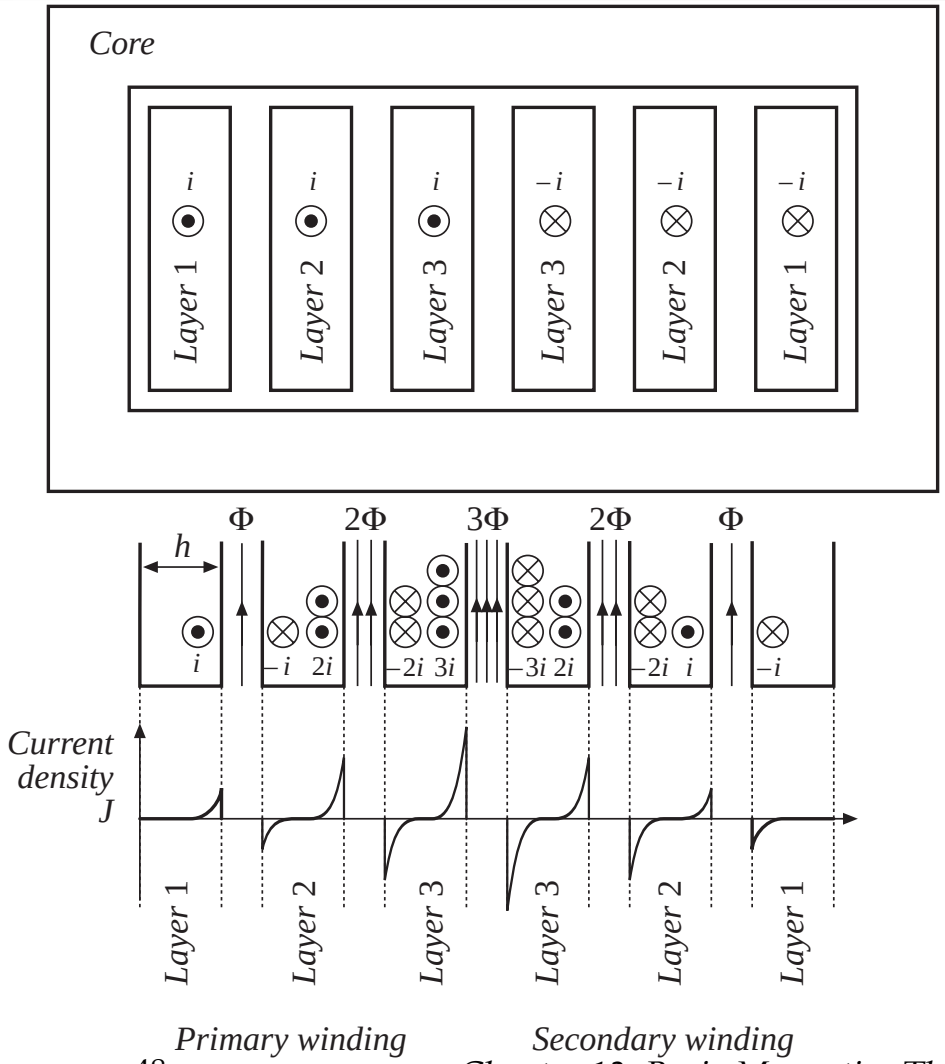
Skin effect causes currents to concentrate on surfaces of conductors

Surface current induces equal and opposite current on adjacent conductor

This induced current returns on opposite side of conductor

Net conductor current is equal to $i(t)$ for each layer, since layers are connected in series

Circulating currents within layers increase with the numbers of layers



Estimating proximity loss: high-frequency limit

The current $i(t)$ having rms value I is confined to thickness d on the surface of layer 1. Hence the effective "ac" resistance of layer 1 is:

$$R_{ac} = \frac{h}{\delta} R_{dc}$$

This induces copper loss P_1 in layer 1:

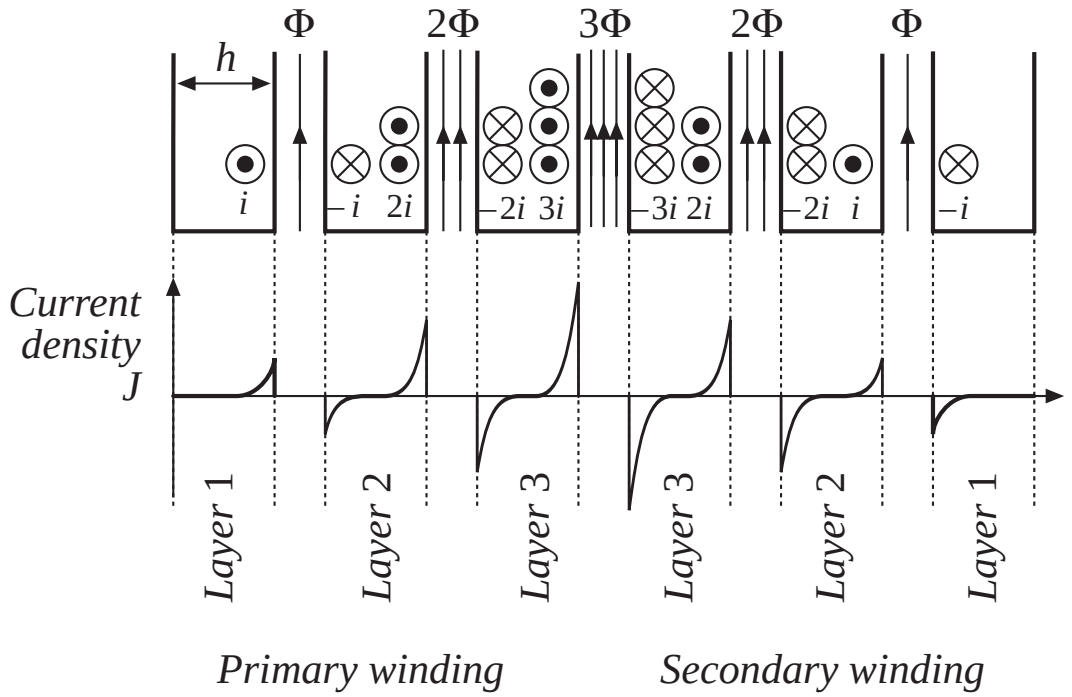
$$P_1 = I^2 R_{ac}$$

Power loss P_2 in layer 2 is:

$$P_2 = P_1 + 4P_1 = 5P_1$$

Power loss P_3 in layer 3 is:

$$P_3 = \left(2^2 + 3^2\right) P_1 = 13P_1$$



Power loss P_m in layer m is:

$$P_m = I^2 \left[\left(m-1\right)^2 + m^2 \right] \left(\frac{h}{\delta} R_{dc} \right)$$

Total loss in M-layer winding: high-frequency limit

Add up losses in each layer:

$$P = I^2\left(\frac{h}{\delta} R_{dc}\right) \sum_{m=1}^{M} \left[\left(m-1\right)^2 + m^2\right]$$

$$= I^2\left(\frac{h}{\delta} R_{dc}\right) \frac{M}{3}\left(2M^2 + 1\right)$$

Compare with dc copper loss:

If foil thickness were $H = \delta$, then at dc each layer would produce copper loss P_1. The copper loss of the M-layer winding would be

$$P_{dc} = I^2 M R_{dc}$$

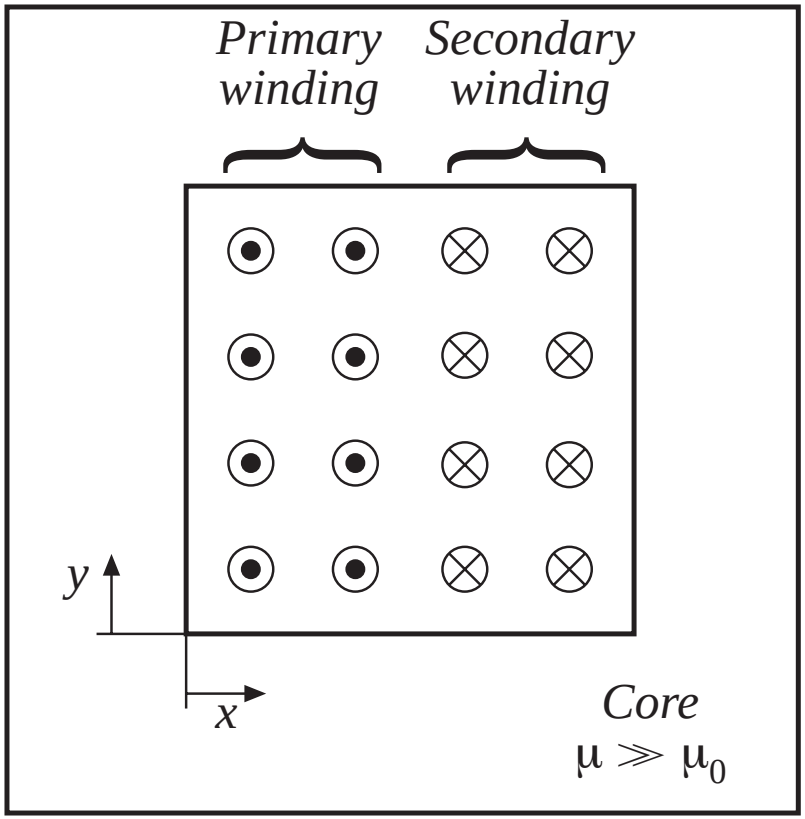
So the proximity effect increases the copper loss by a factor of

$$F_R = \frac{P}{P_{dc}} = \frac{1}{3}\left(\frac{h}{\delta}\right)\left(2M^2 + 1\right)$$

13.4.2 Leakage flux in windings

A simple two-winding transformer example: core and winding geometry

Each turn carries net current $i(t)$ in direction shown

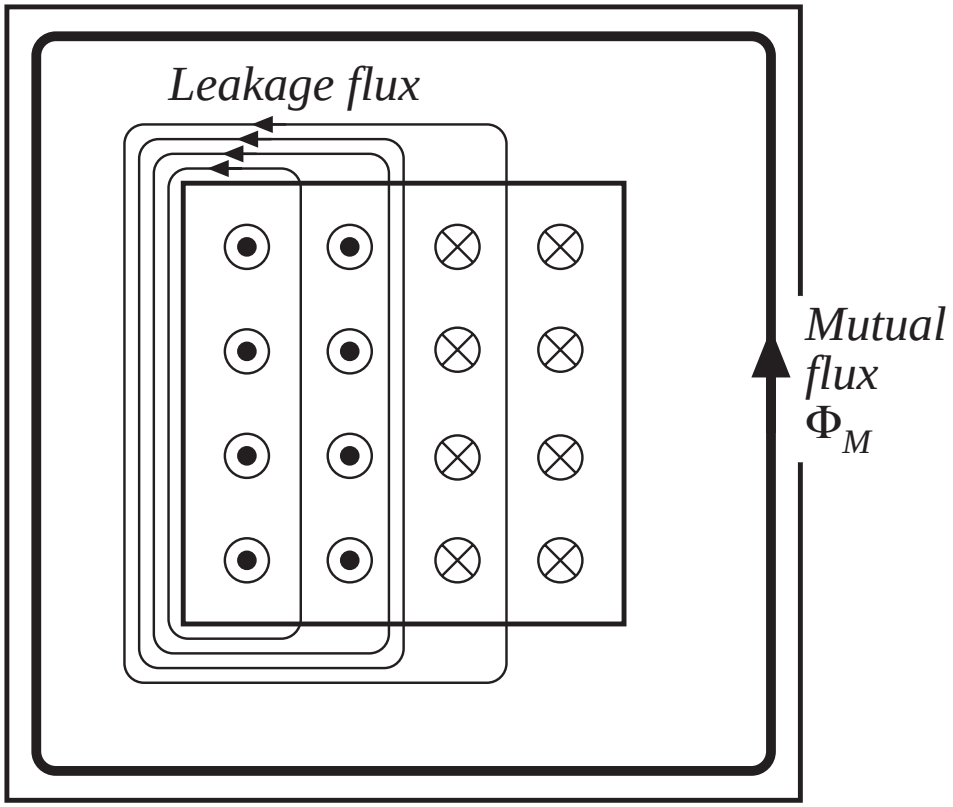


Flux distribution

Mutual flux Φ_M is large and is mostly confined to the core

Leakage flux is present, which does not completely link both windings

Because of symmetry of winding geometry, leakage flux runs approximately vertically through the windings

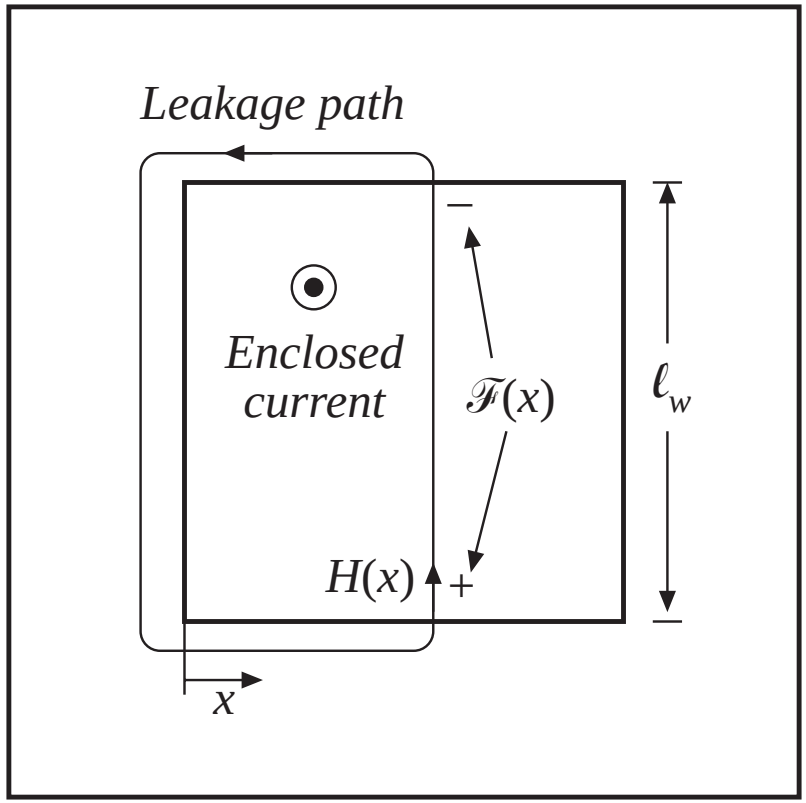


Analysis of leakage flux using Ampere's law

Ampere's law, for the closed path taken by the leakage flux line illustrated:

$$\textit{Enclosed current} = \mathscr{F}(x) = H(x)\ell_w$$

(note that MMF around core is small compared to MMF through the air inside the winding, because of high permeability of core)



Ampere's law for the transformer example

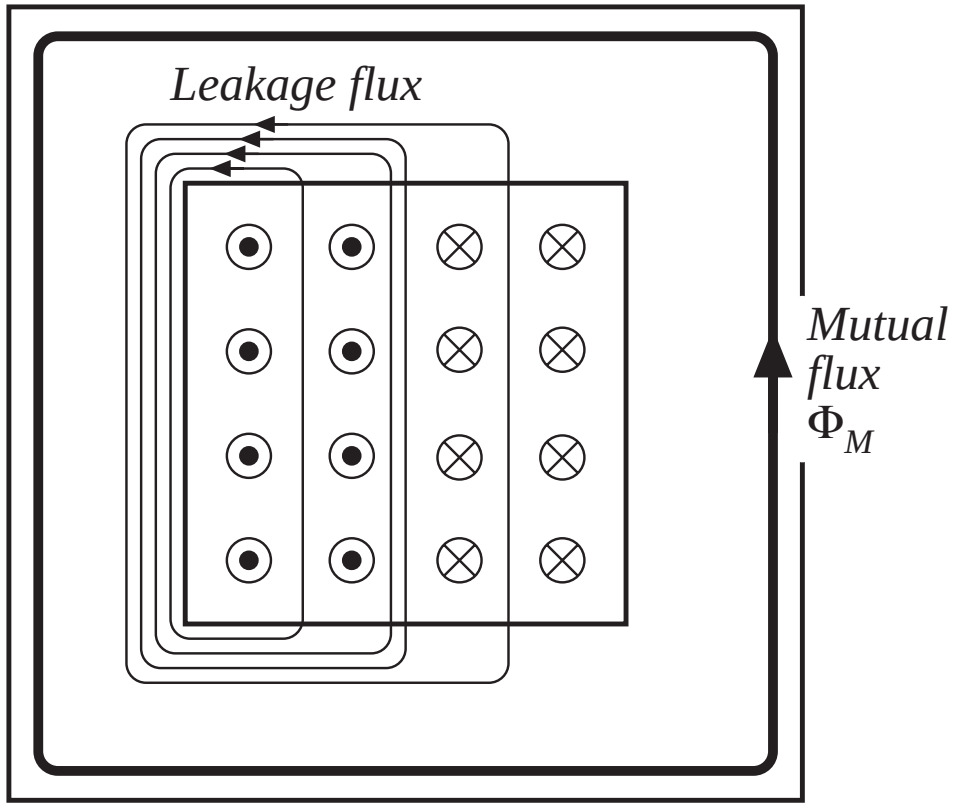
For the innermost leakage path, enclosing the first layer of the primary:

This path encloses four turns, so the total enclosed current is $4i(t)$.

For the next leakage path, enclosing both layers of the primary:

This path encloses eight turns, so the total enclosed current is $8i(t)$.

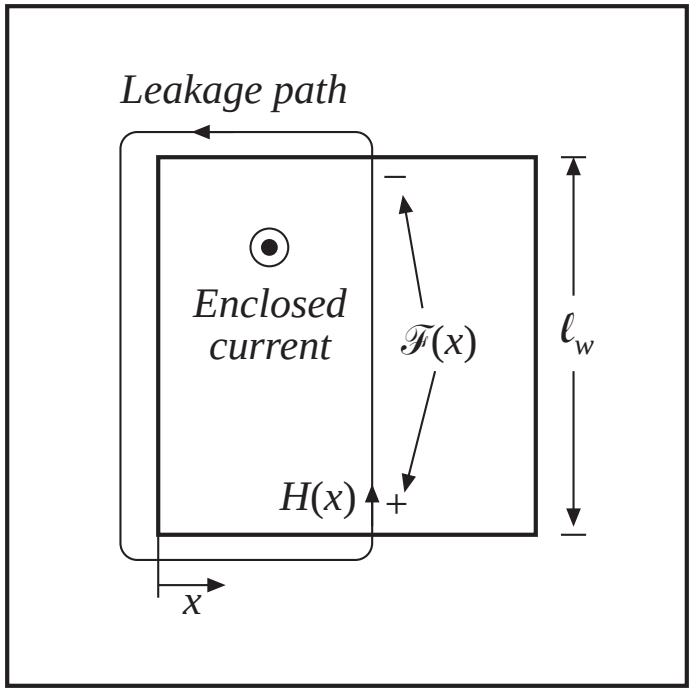
The next leakage path encloses the primary plus four turns of the secondary. The total enclosed current is $8i(t) - 4i(t) = 4i(t)$.

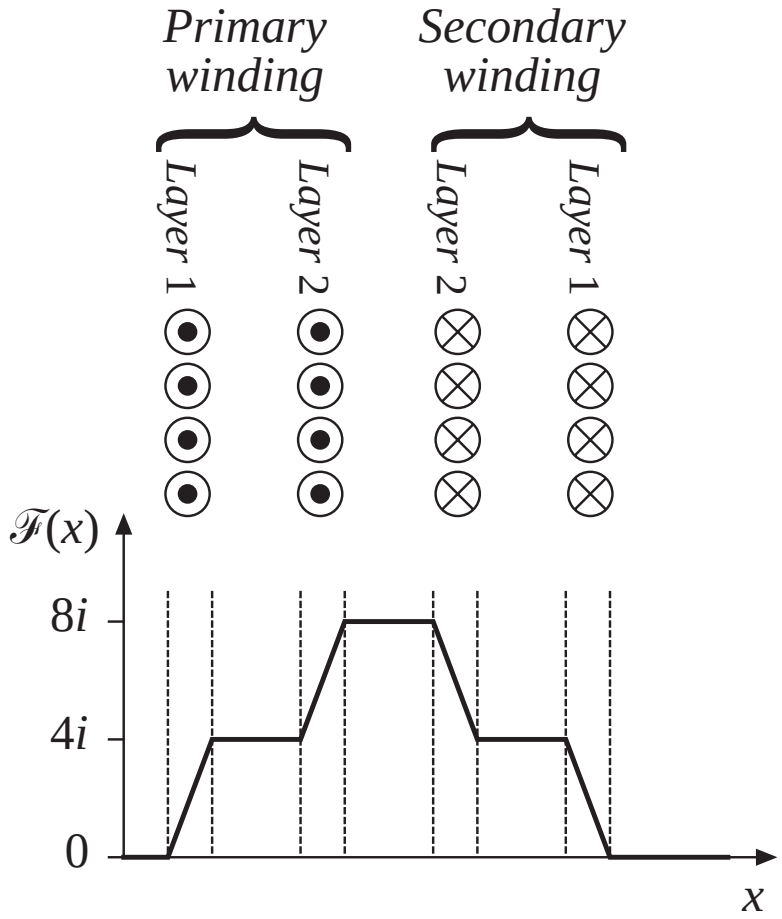


MMF diagram, transformer example

MMF $\mathcal{F}(x)$ across the core window, as a function of position x

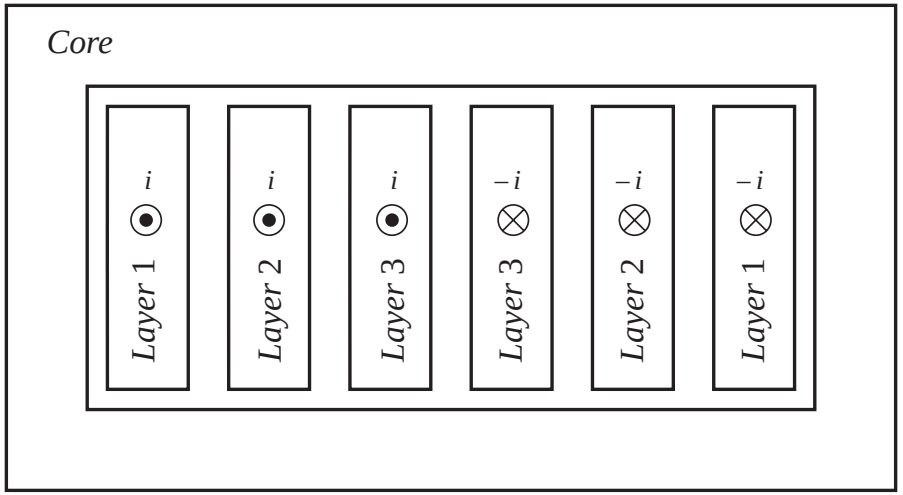
$$\textit{Enclosed current} = \mathcal{F}(x) = H(x)\ell_w$$





Two-winding transformer example

Winding layout



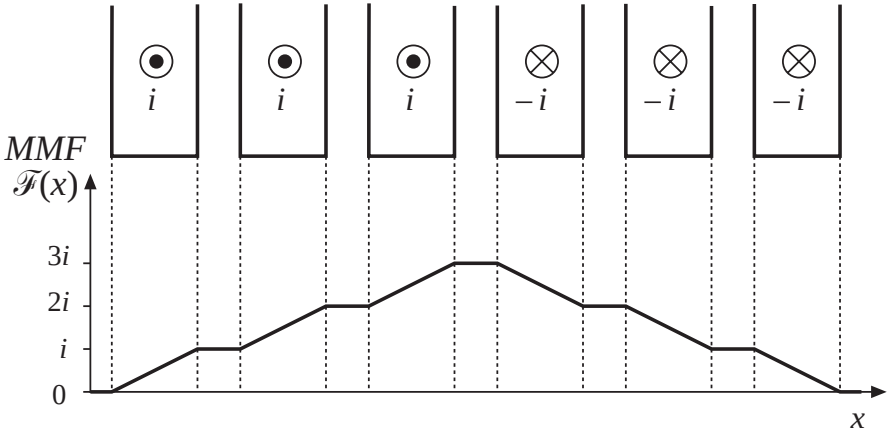
MMF diagram

Use Ampere's law around a closed path taken by a leakage flux line:

$$\left(m_p - m_s\right) i = \mathscr{F}(x)$$

m_p = number of primary layers enclosed by path

m_s = number of secondary layers enclosed by path



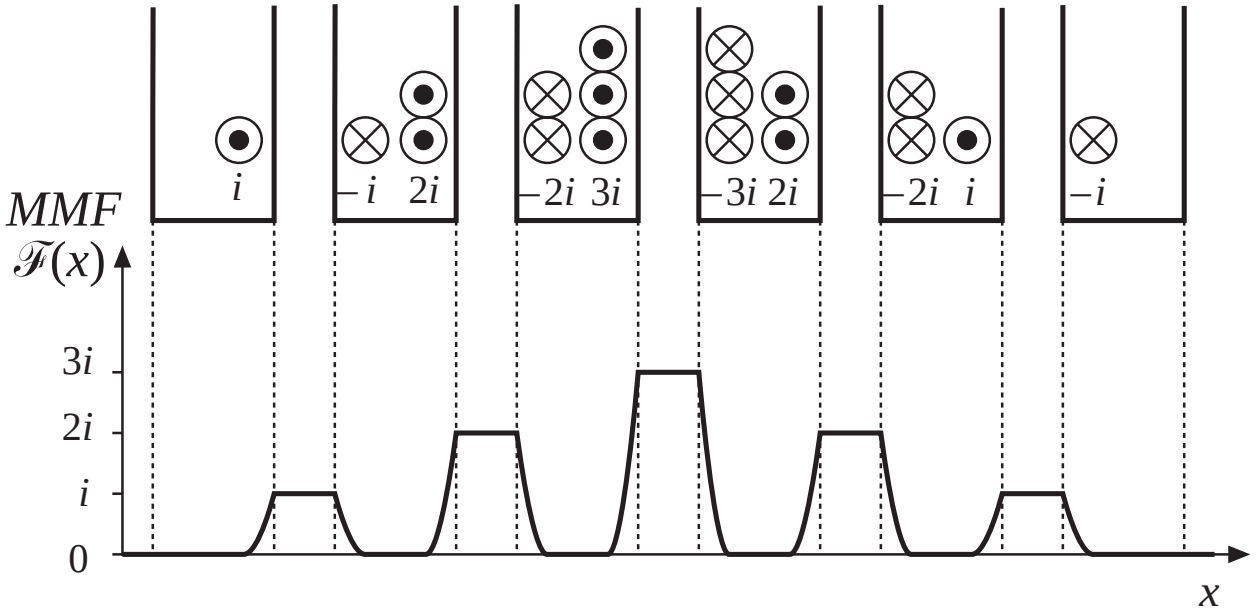
Two-winding transformer example
with proximity effect

Flux does not penetrate conductors

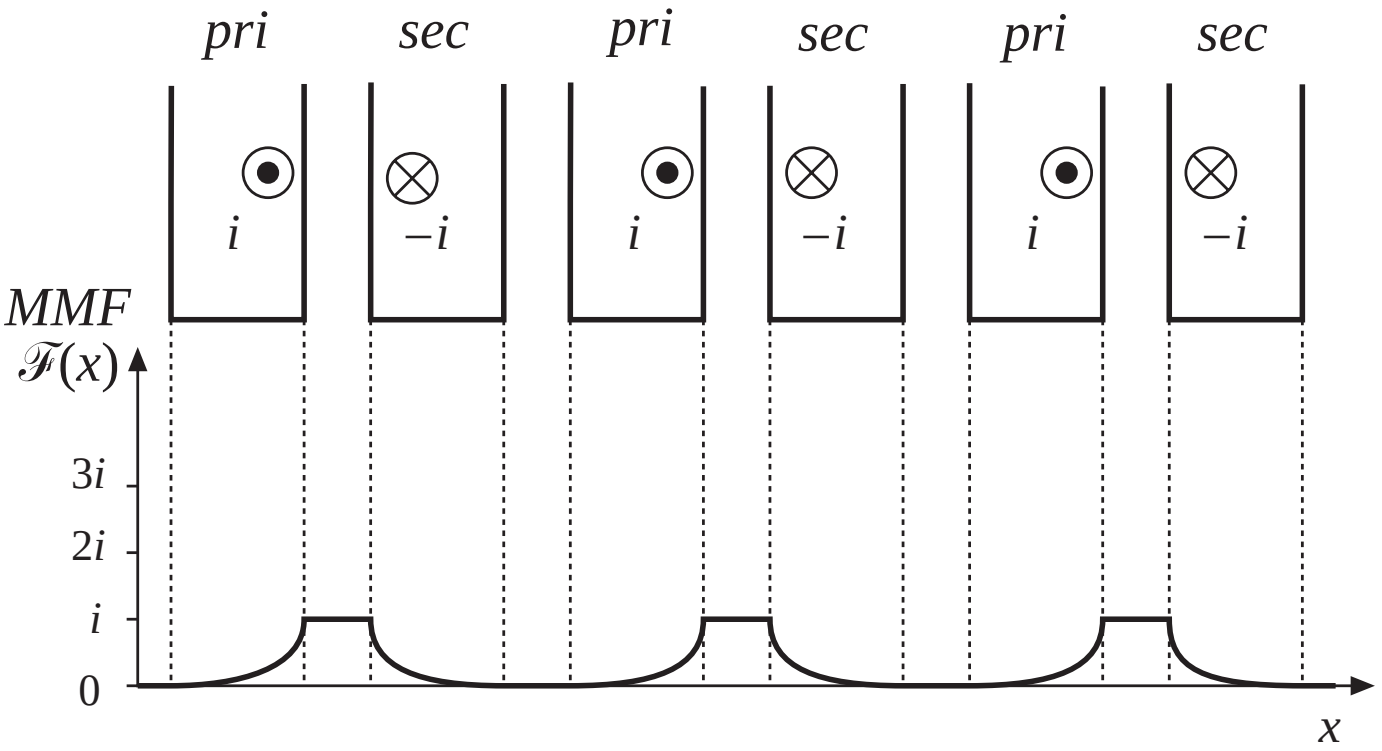
Surface currents cause net current enclosed by leakage path to be zero when path runs down interior of a conductor

Magnetic field strength $H(x)$ within the winding is given by

$$H(x) = \frac{\mathscr{F}(x)}{\ell_w}$$



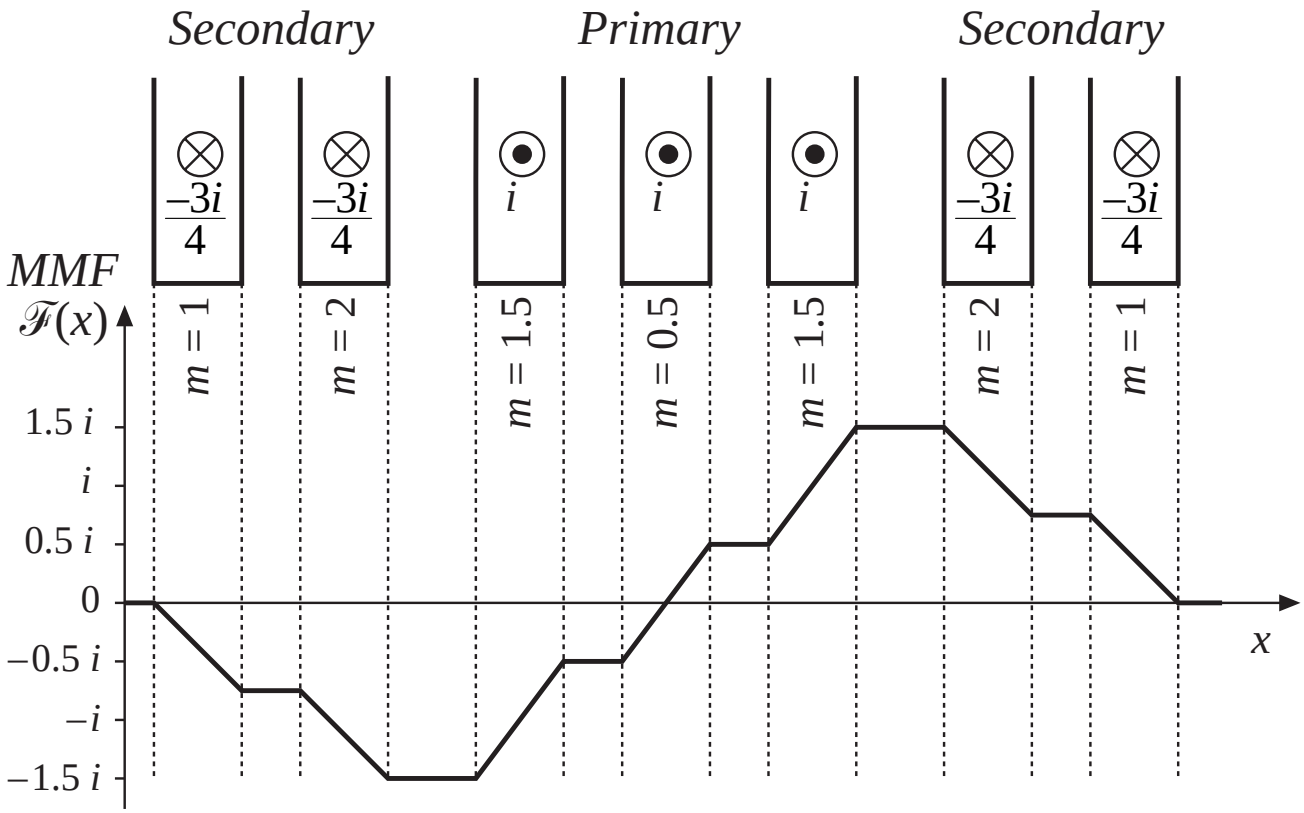
Interleaving the windings: MMF diagram



Greatly reduces the peak MMF, leakage flux, and proximity losses

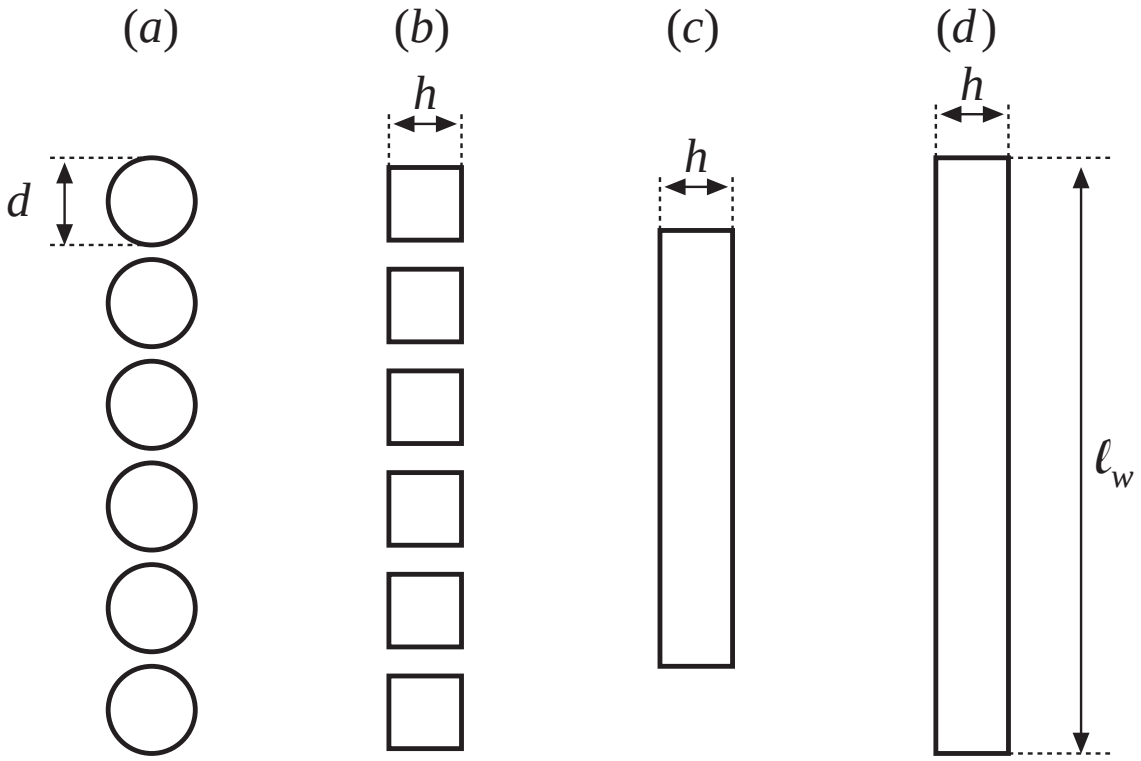
A partially-interleaved transformer

For this example, there are three primary layers and four secondary layers. The MMF diagram contains fractional values.



13.4.3 Foil windings and layers

Approximating a layer of round conductors as an effective single foil conductor:



Square conductors (b) have same cross-sectional area as round conductors (a) if

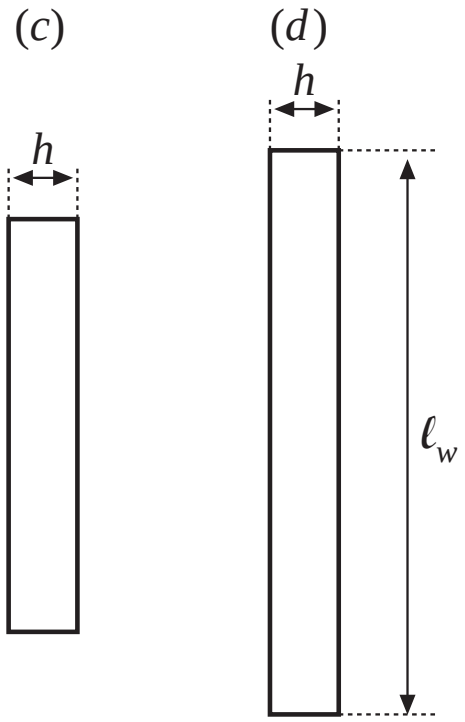
$$h = \sqrt{\frac{\pi}{4}}\, d$$

Eliminate space between square conductors: push together into a single foil turn (c)

(d) Stretch foil so its width is ℓ_w. The adjust conductivity so its dc resistance is unchanged

Winding porosity η

Stretching the conductor increases its area. Compensate by increasing the effective resistivity ρ, to maintain the same dc resistance. Define *winding porosity* η as the ratio of cross-sectional areas. If layer of width ℓ_w contains n_ℓ turns of round wire having diameter d, then the porosity is



$$\eta = \sqrt{\frac{\pi}{4}}\, d\, \frac{n_\ell}{\ell_w}$$

Typical η for full-width round conductors is $\eta = 0.8$. The increased effective resistivity increases the effective skin depth:

$$\delta' = \frac{\delta}{\sqrt{\eta}}$$

Define $\varphi = h/d$. The effective value for a layer of round conductors is

$$\varphi = \frac{h}{\delta'} = \sqrt{\eta}\, \sqrt{\frac{\pi}{4}}\, \frac{d}{\delta}$$

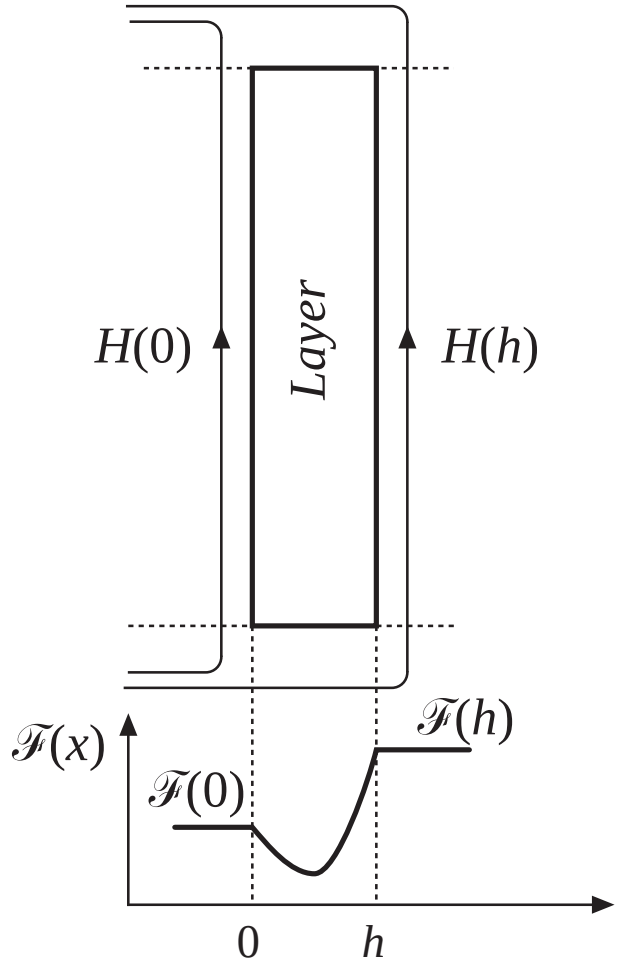
13.4.4 Power loss in a layer

Approximate computation of copper loss in one layer

Assume uniform magnetic fields at surfaces of layer, of strengths $H(0)$ and $H(h)$. Assume that these fields are parallel to layer surface (i.e., neglect fringing and assume field normal component is zero).

The magnetic fields $H(0)$ and $H(h)$ are driven by the MMFs $\mathscr{F}(0)$ and $\mathscr{F}(h)$.

Sinusoidal waveforms are assumed, and rms values are used. It is assumed that $H(0)$ and $H(h)$ are in phase.



Solution for layer copper loss P

Solve Maxwell's equations to find current density distribution within layer. Then integrate to find total copper loss P in layer. Result is

$$P = R_{dc} \frac{\varphi}{n_\ell^2} \left[\left(\mathscr{F}^2(h) + \mathscr{F}^2(0) \right) G_1(\varphi) - 4\, \mathscr{F}(h) \mathscr{F}(0) G_2(\varphi) \right]$$

where

$$R_{dc} = \rho \frac{\ell_b}{A_w} = \rho \frac{(MLT) n_l^3}{\eta \ell_w^2}$$

$$G_1(\varphi) = \frac{\sinh(2\varphi) + \sin(2\varphi)}{\cosh(2\varphi) - \cos(2\varphi)}$$

$$G_2(\varphi) = \frac{\sinh(\varphi)\cos(\varphi) + \cosh(\varphi)\sin(\varphi)}{\cosh(2\varphi) - \cos(2\varphi)}$$

$$\varphi = \frac{h}{\delta'} = \sqrt{\eta} \sqrt{\frac{\pi}{4}} \frac{d}{\delta} \qquad \eta = \sqrt{\frac{\pi}{4}}\, d \frac{n_\ell}{\ell_w}$$

n_l = number of turns in layer,
R_{dc} = dc resistance of layer,
(MLT) = mean-length-per-turn, or circumference, of layer.

Winding carrying current I, with n_l turns per layer

If winding carries current of rms magnitude I, then

$$\mathscr{F}(h) - \mathscr{F}(0) = n_\ell I$$

Express $\mathscr{F}(h)$ in terms of the winding current I, as

$$\mathscr{F}(h) = m n_\ell I$$

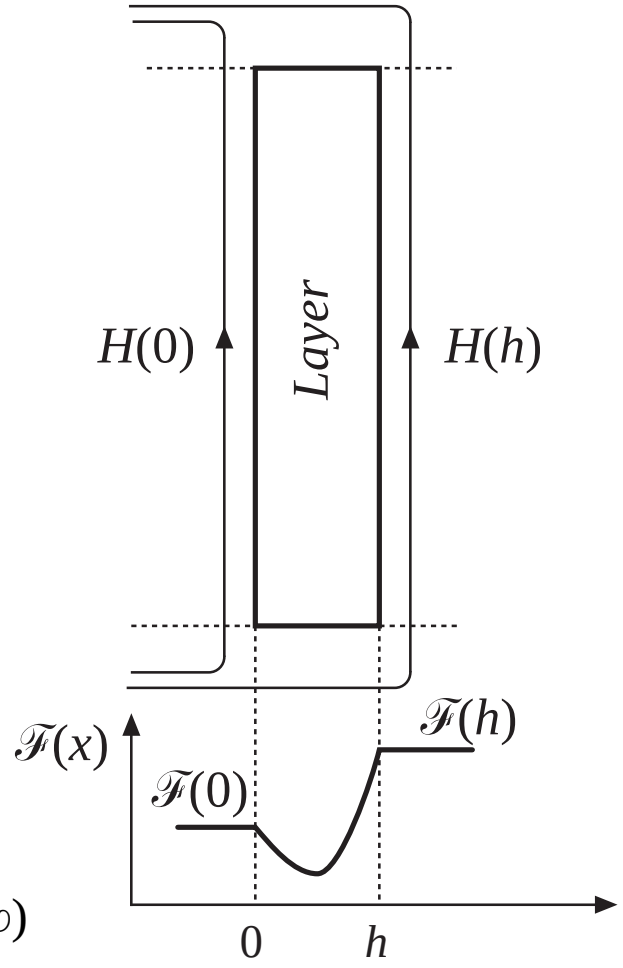
The quantity m is the ratio of the MMF $\mathscr{F}(h)$ to the layer ampere-turns $n_\ell I$. Then,

$$\frac{\mathscr{F}(0)}{\mathscr{F}(h)} = \frac{m-1}{m}$$

Power dissipated in the layer can now be written

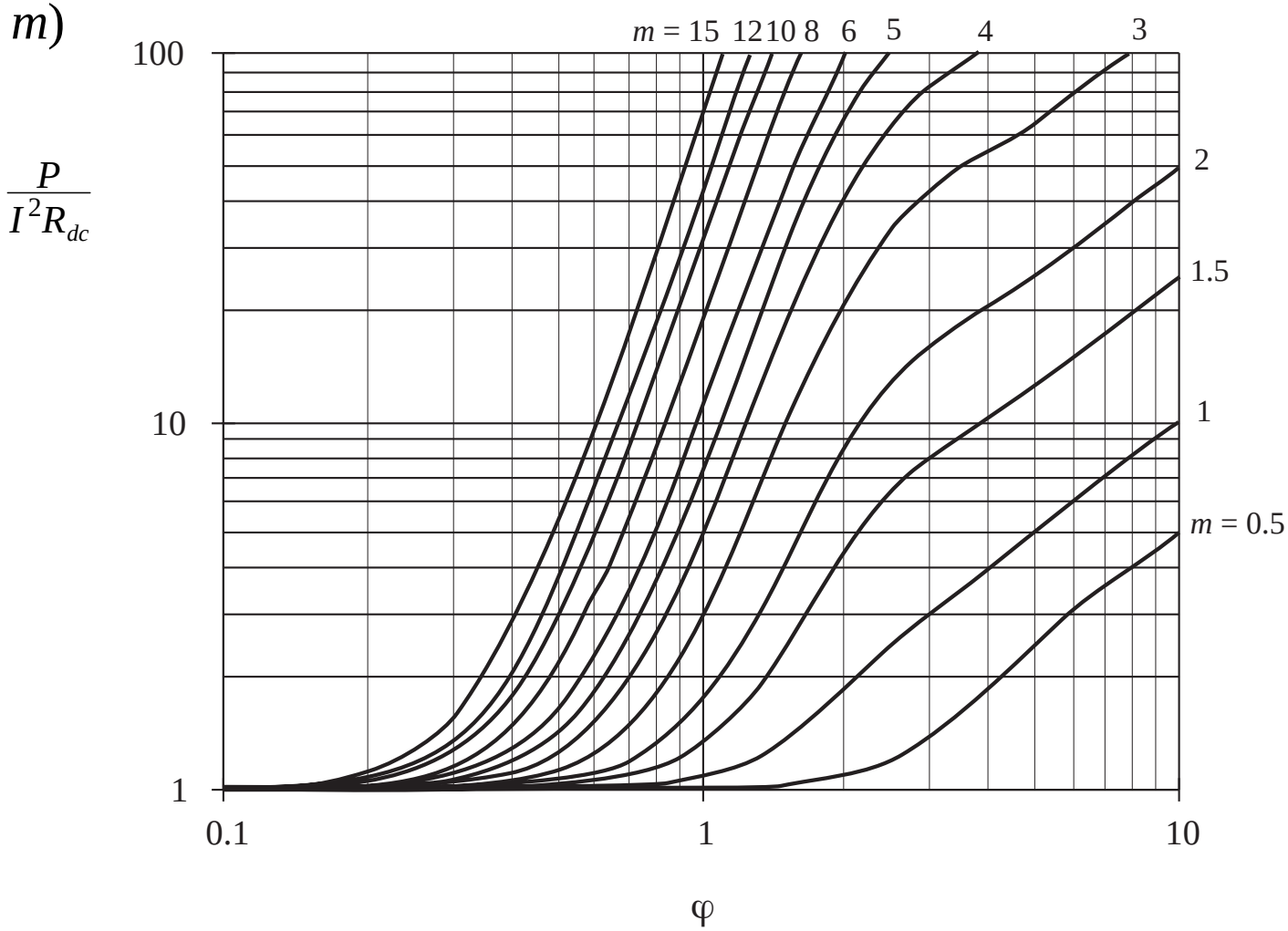
$$P = I^2 R_{dc} \varphi Q'(\varphi, m)$$

$$Q'(\varphi, m) = \left(2m^2 - 2m + 1\right) G_1(\varphi) - 4m\left(m-1\right) G_2(\varphi)$$



Increased copper loss in layer

$$P = I^2 R_{dc} \varphi Q'(\varphi, m)$$

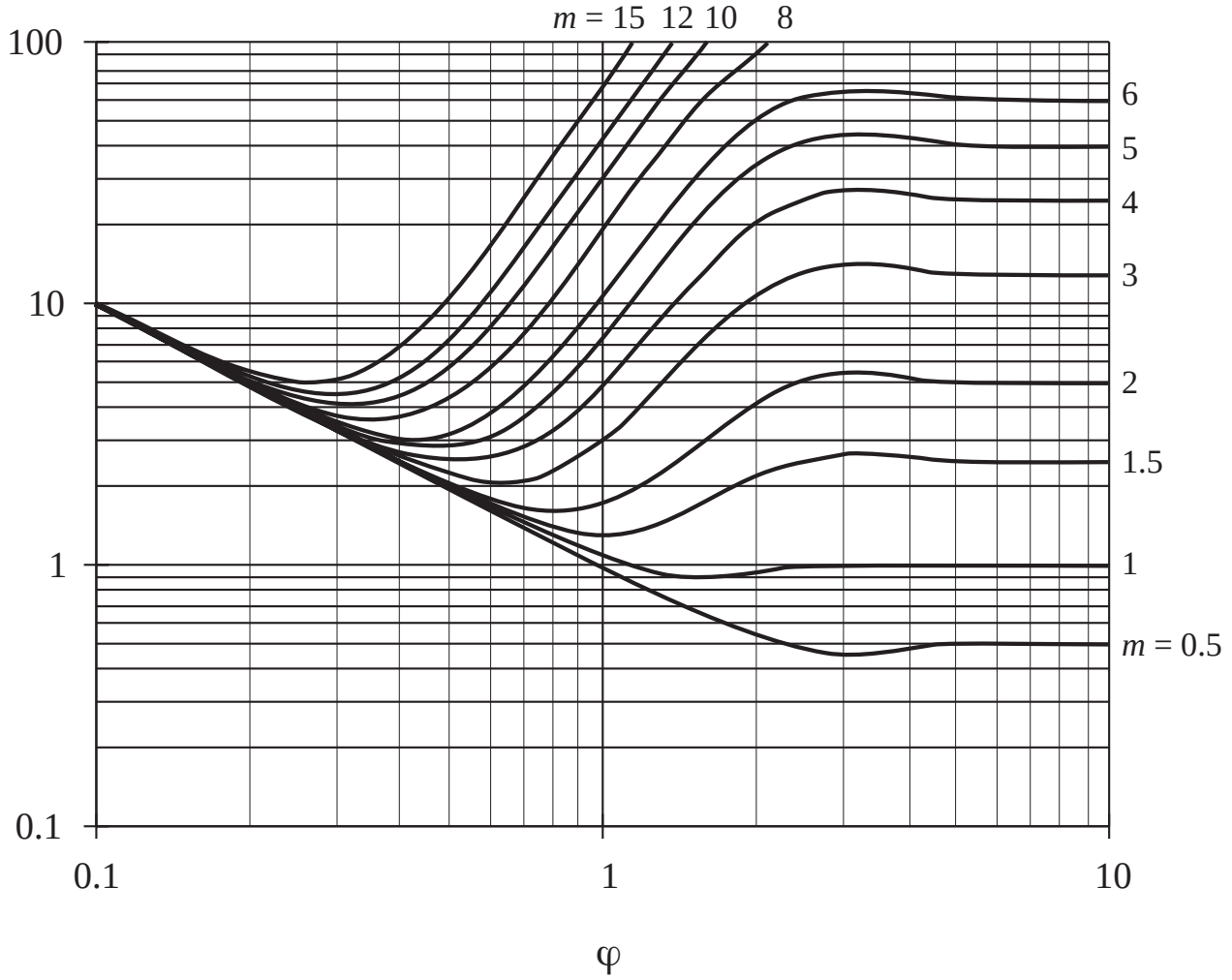


Layer copper loss vs. layer thickness

$$\frac{P}{P_{dc}\big|_{\varphi = 1}} = Q'(\varphi, m)$$

$$\frac{P}{P_{dc}\big|_{\varphi = 1}}$$

Relative to copper loss when $h = \delta$



13.4.5 Example: Power loss in a transformer winding

Two winding transformer

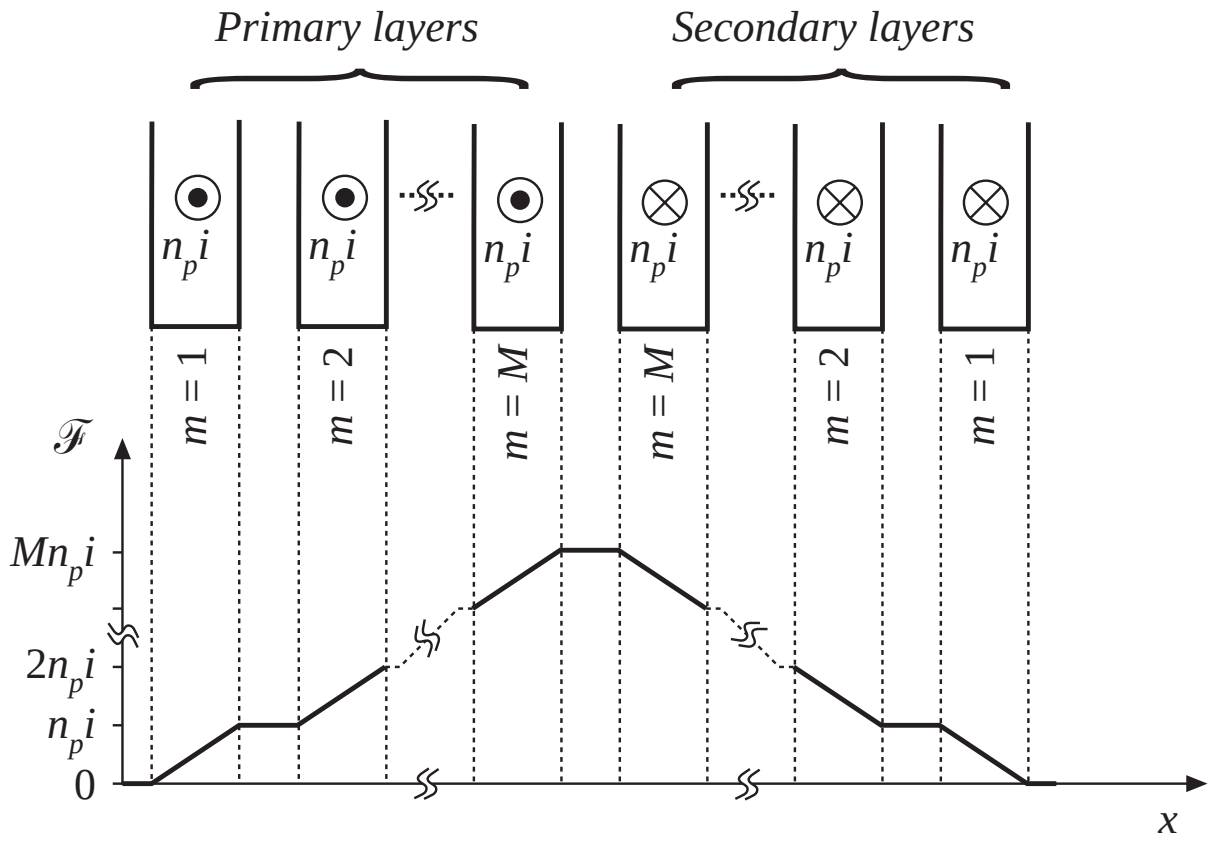
Each winding consists of M layers

Proximity effect increases copper loss in layer m by the factor

$$\varphi Q'(\varphi, m)$$

Sum losses over all primary layers:

$$F_R = \frac{P_{pri}}{P_{pri,dc}} = \frac{1}{M} \sum_{m=1}^{M} \varphi Q'(\varphi, m)$$

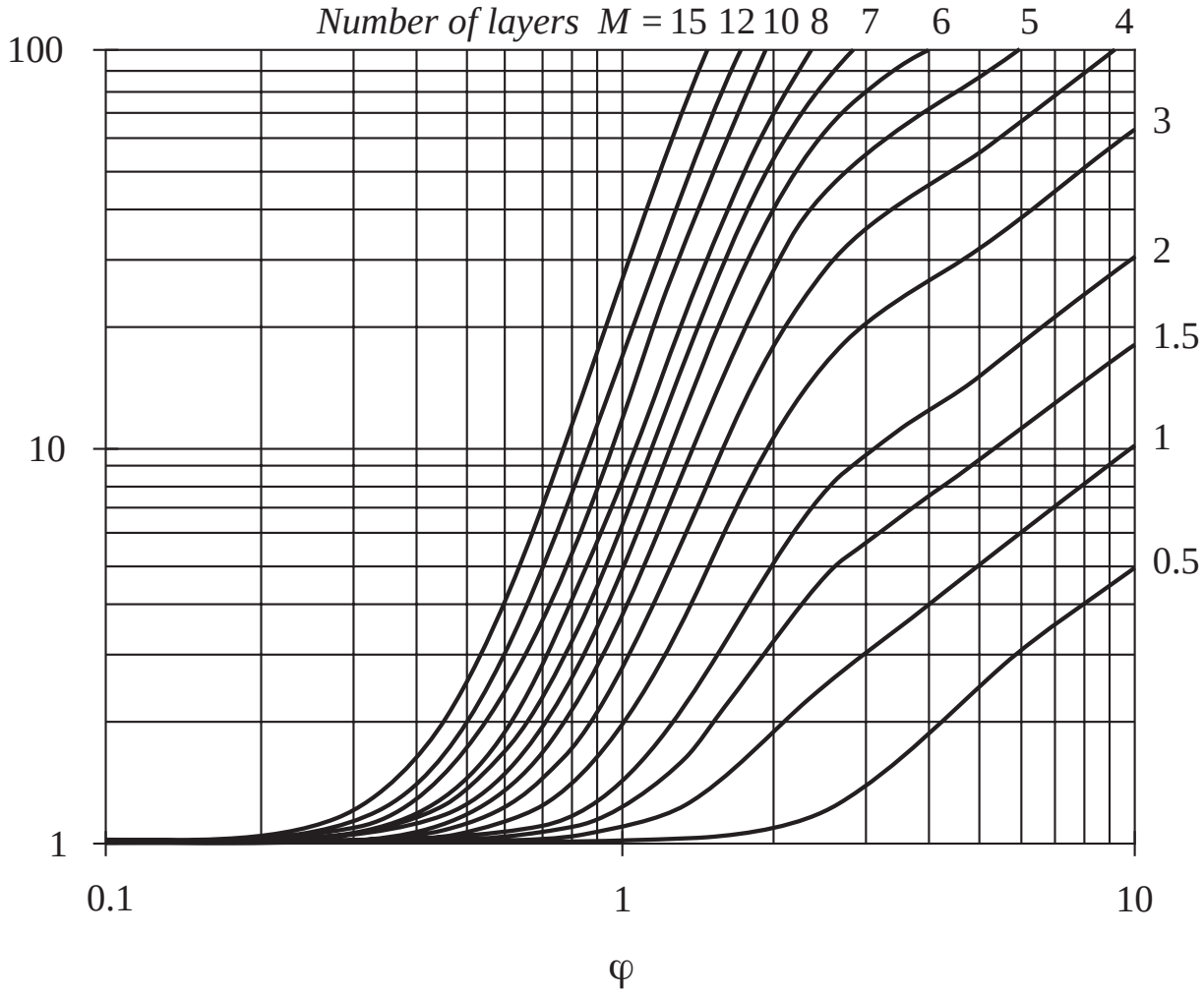


Increased total winding loss

Express summation in closed form:

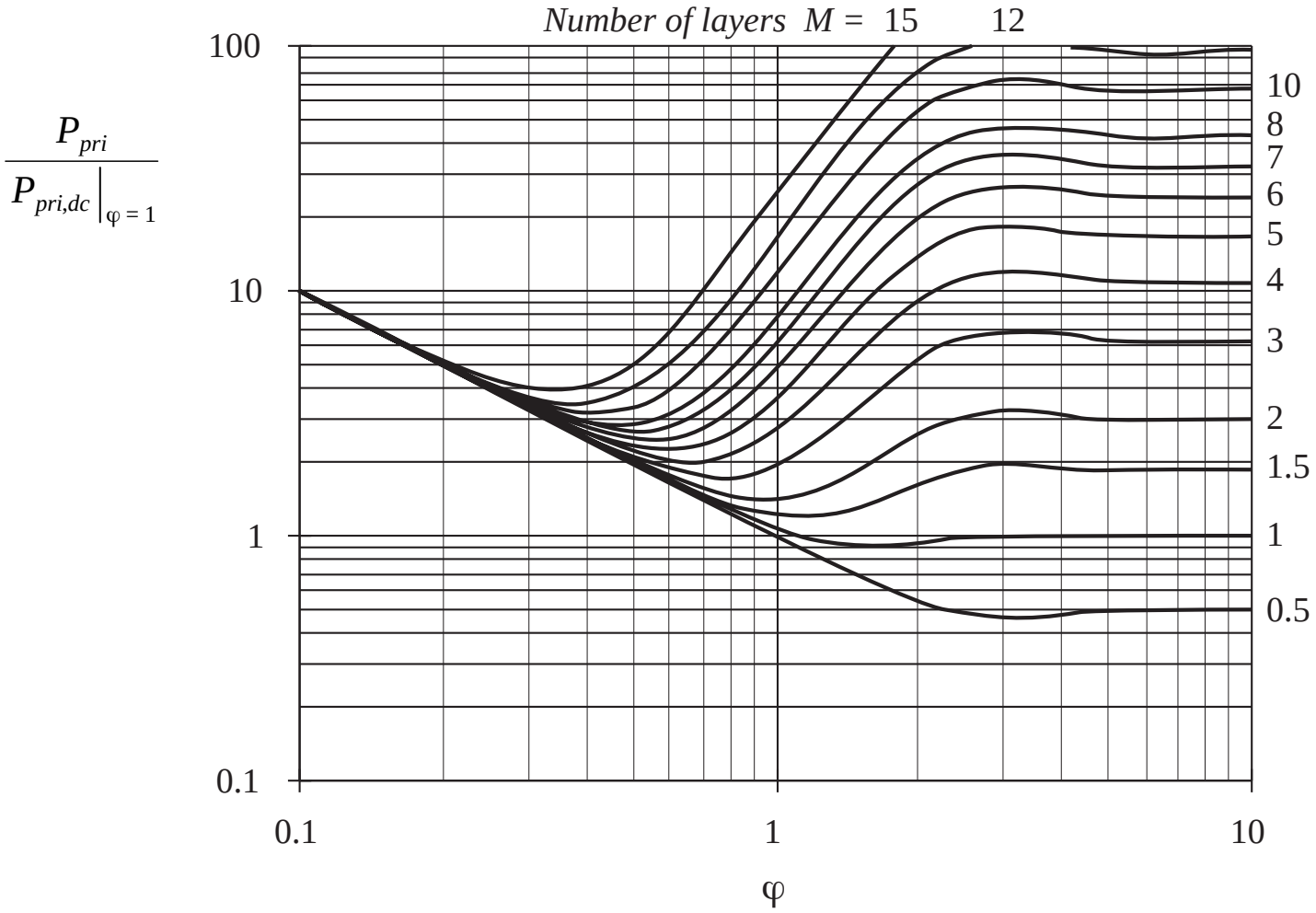
$$F_R = \varphi \left| G_1(\varphi) + \frac{2}{3}\left(M^2 - 1\right)\left(G_1(\varphi) - 2G_2(\varphi)\right) \right|$$

$$F_R = \frac{P_{pri}}{P_{pri,dc}}$$



Total winding loss

$$\frac{P_{pri}}{P_{pri,dc}\Big|_{\varphi = 1}} = G_1(\varphi) + \frac{2}{3}\left(M^2 - 1\right)\left(G_1(\varphi) - 2G_2(\varphi)\right)$$

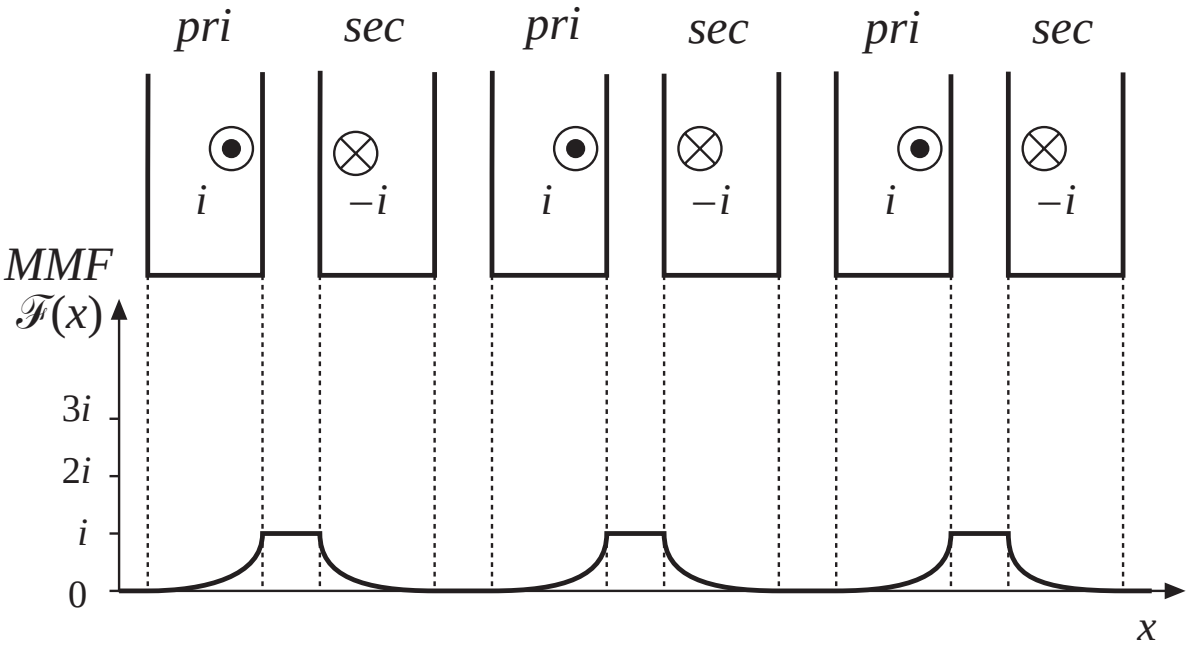


13.4.6 Interleaving the windings

Same transformer example, but with primary and secondary layers alternated

Each layer operates with $\mathcal{F} = 0$ on one side, and $\mathcal{F} = i$ on the other side

Proximity loss of entire winding follows $M = 1$ curve

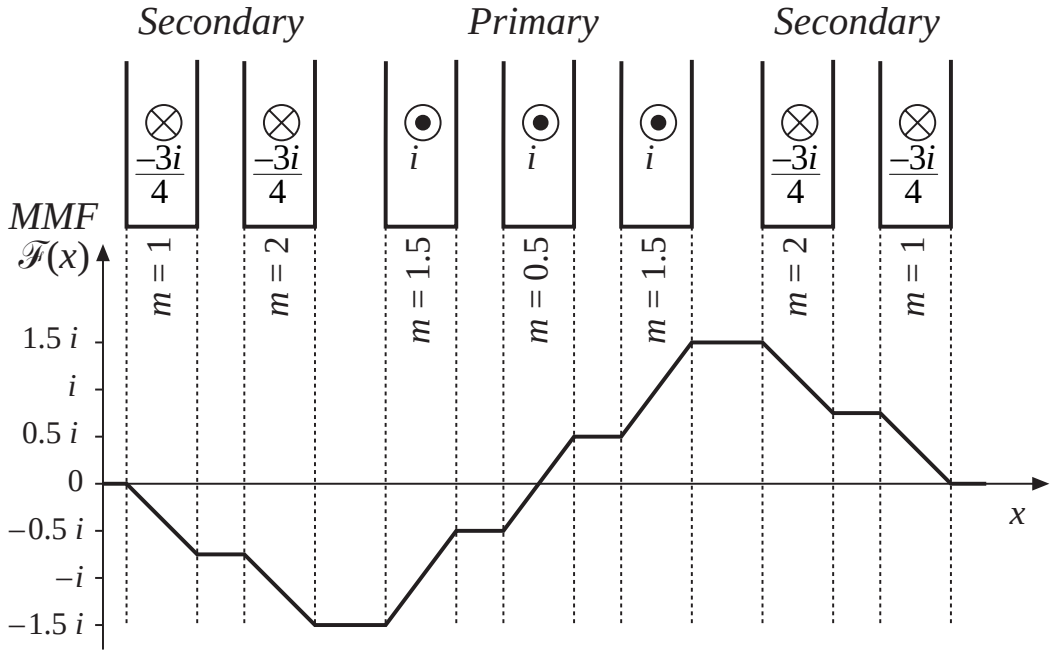


For M = 1: minimum loss occurs with $\varphi = \pi/2$, although copper loss is nearly constant for any $\varphi \geq 1$, and is approximately equal to the dc copper loss obtained when $\varphi = 1$.

Partial interleaving

Partially-interleaved example with 3 primary and 4 secondary layers

Each primary layer carries current i while each secondary layer carries $0.75i$. Total winding currents add to zero. Peak MMF occurs in space between windings, but has value $1.5i$.



We can apply the previous solution for the copper loss in each layer, and add the results to find the total winding losses. To determine the value of m to use for a given layer, evaluate

$$m = \frac{\mathcal{F}(h)}{\mathcal{F}(h) - \mathcal{F}(0)}$$

Determination of m

Leftmost secondary layer:

$$m = \frac{\mathscr{F}(h)}{\mathscr{F}(h) - \mathscr{F}(0)} = \frac{-0.75i}{-0.75i - 0} = 1$$

Next secondary layer:

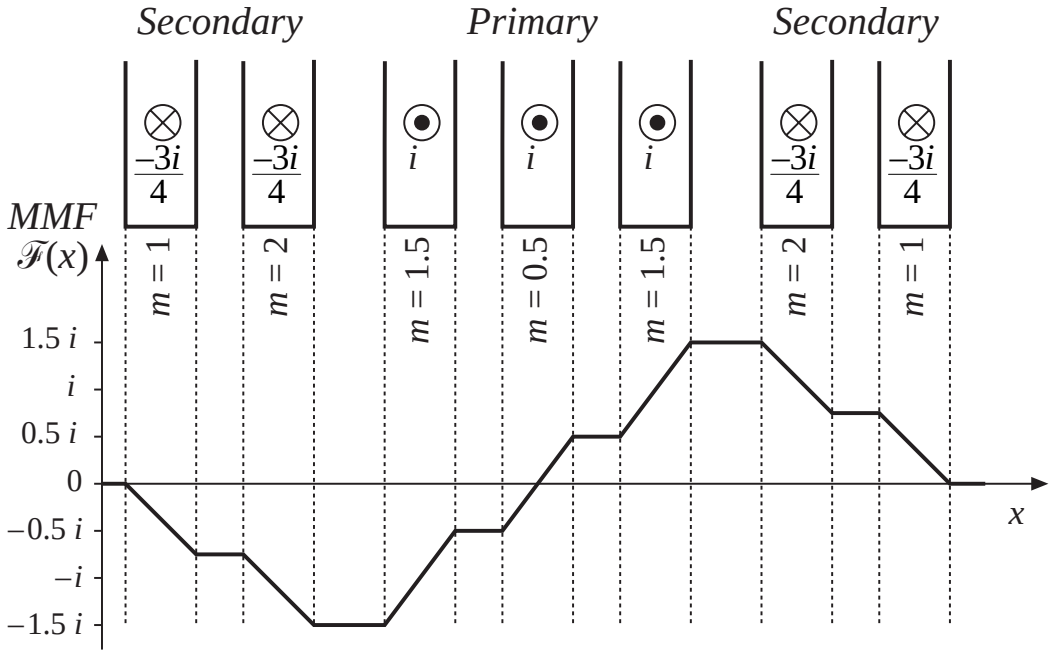
$$m = \frac{\mathscr{F}(h)}{\mathscr{F}(h) - \mathscr{F}(0)} = \frac{-1.5i}{-1.5i - (-0.75i)} = 2$$

Next layer (primary):

$$m = \frac{\mathscr{F}(0)}{\mathscr{F}(0) - \mathscr{F}(h)} = \frac{-1.5i}{-1.5i - (-0.5i)} = 1.5$$

Center layer (primary):

$$m = \frac{\mathscr{F}(h)}{\mathscr{F}(h) - \mathscr{F}(0)} = \frac{0.5i}{0.5i - (-0.5i)} = 0.5$$



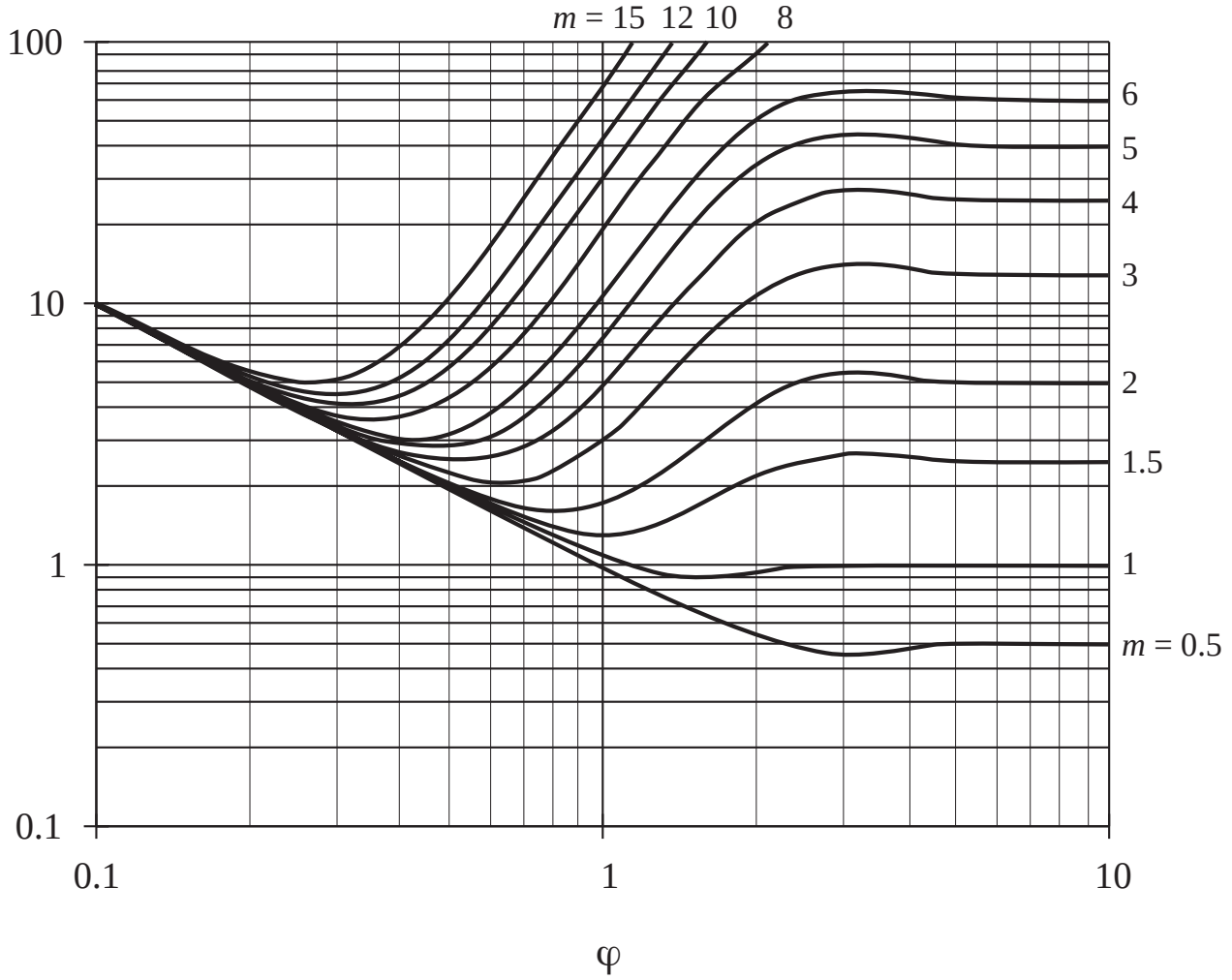
Use the plot for layer loss (repeated on next slide) to find loss for each layer, according to its value of m. Add results to find total loss.

Layer copper loss vs. layer thickness

$$\frac{P}{P_{dc}\big|_{\varphi = 1}} = Q'(\varphi, m)$$

$$\frac{P}{P_{dc}\big|_{\varphi = 1}}$$

Relative to copper loss when $h = \delta$



Discussion: design of winding geometry to minimize proximity loss

- Interleaving windings can significantly reduce the proximity loss when the winding currents are in phase, such as in the transformers of buck-derived converters or other converters
- In some converters (such as flyback or SEPIC) the winding currents are out of phase. Interleaving then does little to reduce the peak MMF and proximity loss. See *Vandelac and Ziogas* [10].
- For sinusoidal winding currents, there is an optimal conductor thickness near $\varphi = 1$ that minimizes copper loss.
- Minimize the number of layers. Use a core geometry that maximizes the width ℓ_w of windings.
- Minimize the amount of copper in vicinity of high MMF portions of the windings

Litz wire

- A way to increase conductor area while maintaining low proximity losses
- Many strands of small-gauge wire are bundled together and are externally connected in parallel
- Strands are twisted, or transposed, so that each strand passes equally through each position on inside and outside of bundle. This prevents circulation of currents between strands.
- Strand diameter should be sufficiently smaller than skin depth
- The Litz wire bundle itself is composed of multiple layers
- Advantage: when properly sized, can significantly reduce proximity loss
- Disadvantage: increased cost and decreased amount of copper within core window

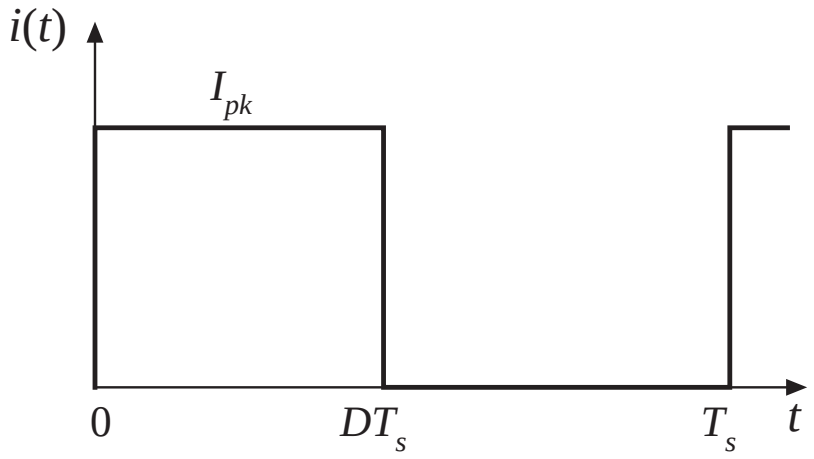
13.4.7 PWM waveform harmonics

Fourier series:

$$i(t) = I_0 + \sum_{j=1}^{\infty} \sqrt{2}\, I_j \cos(j\omega t)$$

with

$$I_j = \frac{\sqrt{2}\, I_{pk}}{j\pi} \sin(j\pi D) \qquad I_0 = DI_{pk}$$



Copper loss:

Dc $P_{dc} = I_0^2 R_{dc}$

Ac $$P_j = I_j^2 R_{dc} \sqrt{j}\, \varphi_1 \left[G_1(\sqrt{j}\, \varphi_1) + \frac{2}{3} \left(M^2 - 1 \right) \left(G_1(\sqrt{j}\, \varphi_1) - 2G_2(\sqrt{j}\, \varphi_1) \right) \right]$$

Total, relative to value predicted by low-frequency analysis:

$$\frac{P_{cu}}{DI_{pk}^2 R_{dc}} = D + \frac{2\varphi_1}{D\pi^2} \sum_{j=1}^{\infty} \frac{\sin^2(j\pi D)}{j\sqrt{j}} \left[G_1(\sqrt{j}\, \varphi_1) + \frac{2}{3} \left(M^2 - 1 \right) \left(G_1(\sqrt{j}\, \varphi_1) - 2G_2(\sqrt{j}\, \varphi_1) \right) \right]$$

Harmonic loss factor F_H

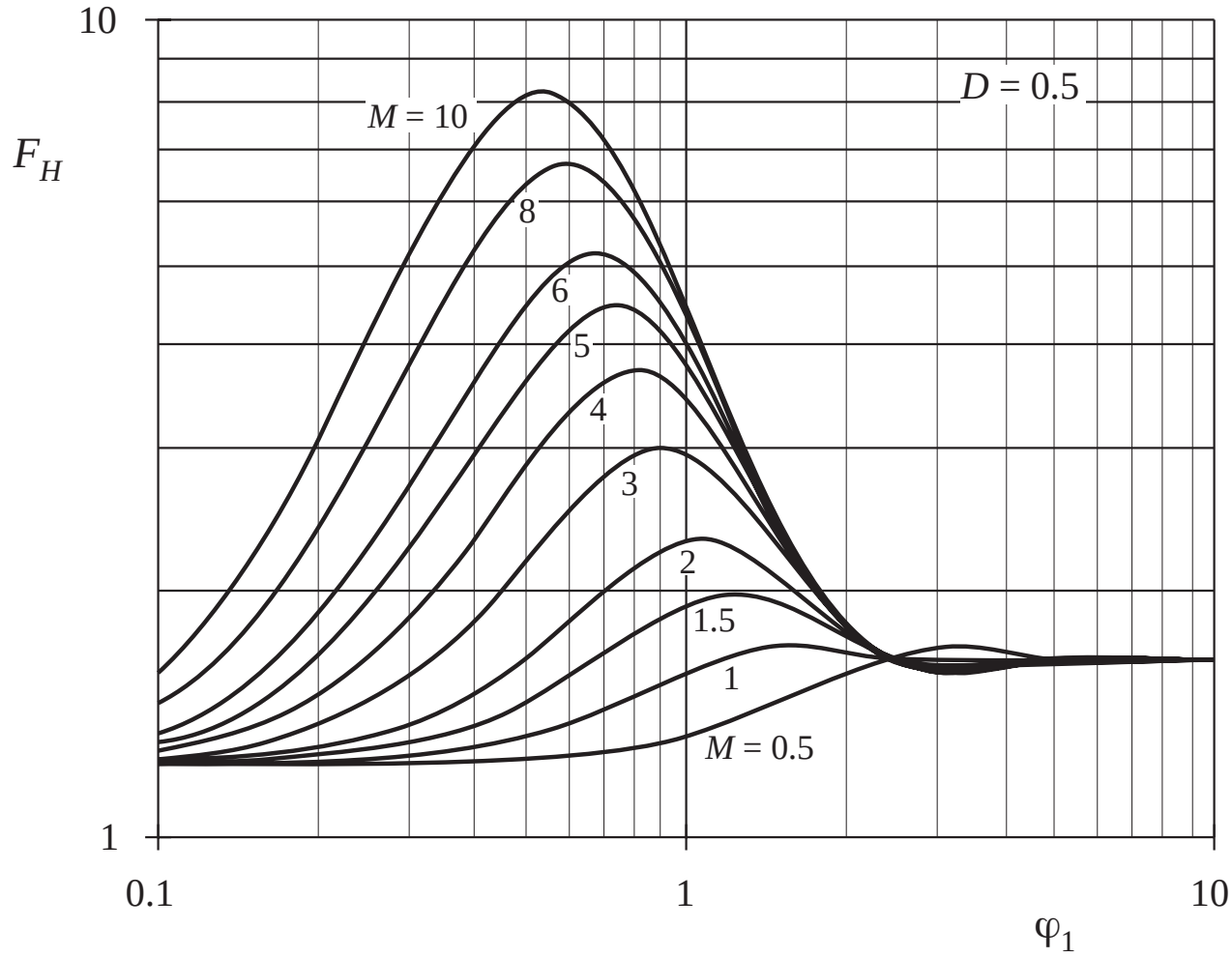
Effect of harmonics: F_H = ratio of total ac copper loss to fundamental copper loss

$$F_H = \frac{\sum_{j=1}^{\infty} P_j}{P_1}$$

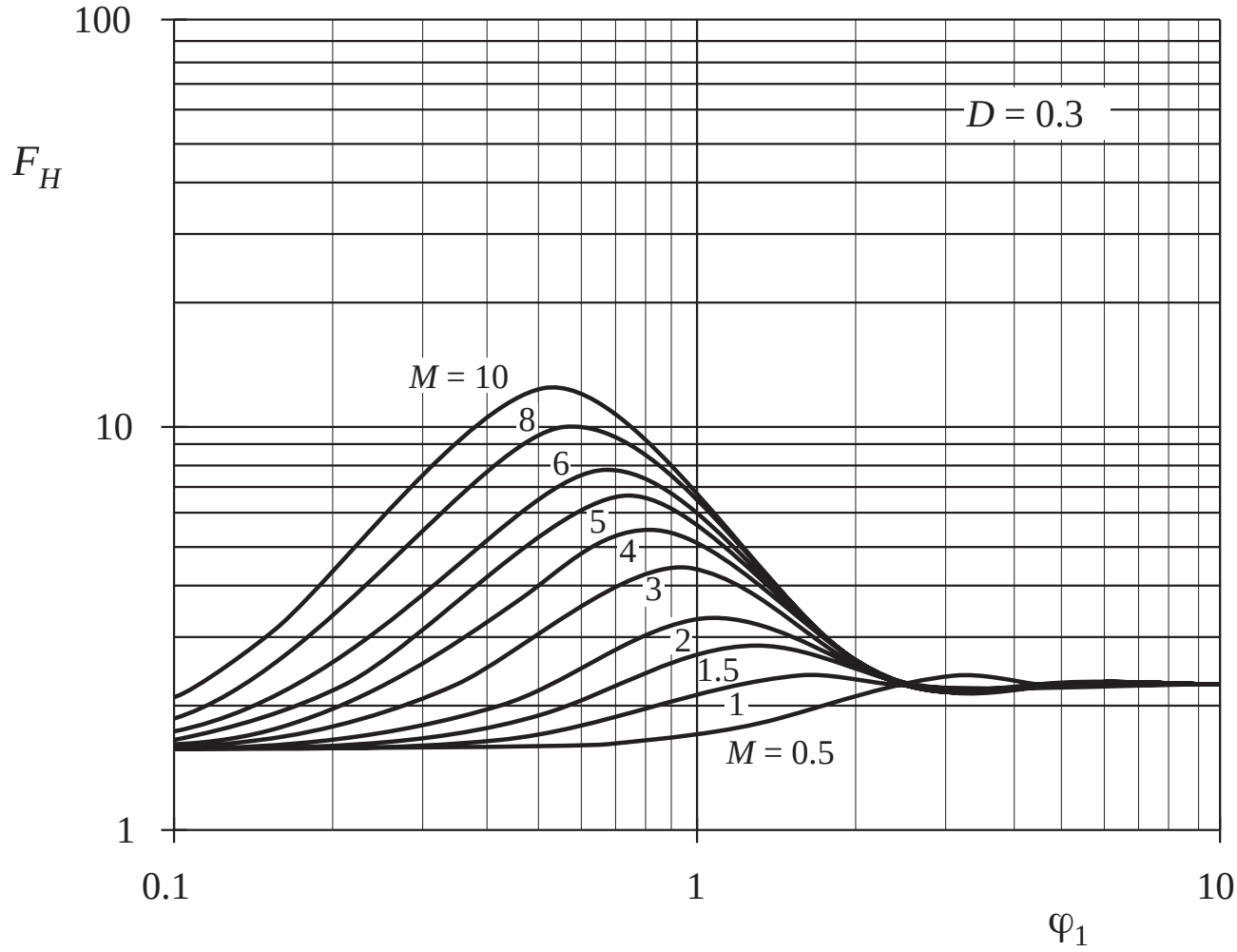
The total winding copper loss can then be written

$$P_{cu} = I_0^2 R_{dc} + F_H F_R I_1^2 R_{dc}$$

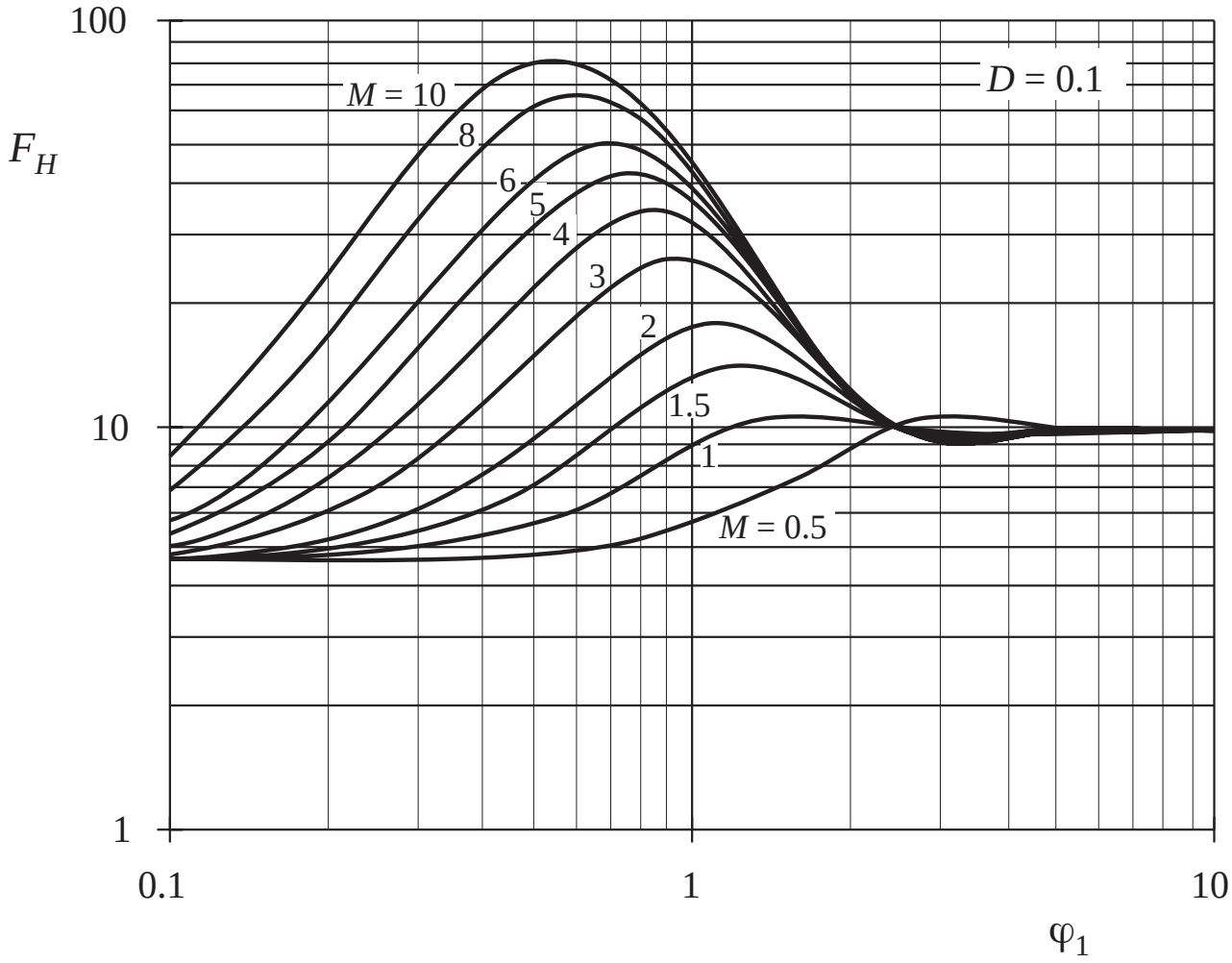
Increased proximity losses induced by PWM waveform harmonics: $D = 0.5$



Increased proximity losses induced by PWM waveform harmonics: D = 0.3



Increased proximity losses induced by PWM waveform harmonics: D = 0.1



Discussion: waveform harmonics

- Harmonic factor F_H accounts for effects of harmonics
- Harmonics are most significant for φ_1 in the vicinity of 1
- Harmonics can radically alter the conclusion regarding optimal wire gauge
- A substantial dc component can drive the design towards larger wire gauge
- Harmonics can increase proximity losses by orders of magnitude, when there are many layers and when φ_1 lies in the vicinity of 1
- For sufficiently small φ_1, F_H tends to the value $1 + (\mathrm{THD})^2$, where the total harmonic distortion of the current is

$$\mathrm{THD} = \frac{\sqrt{\sum_{j=2}^{\infty} I_j^2}}{I_1}$$

13.5. Several types of magnetic devices, their B–H loops, and core vs. copper loss

A key design decision: the choice of maximum operating flux density B_{max}

- Choose B_{max} to avoid saturation of core, or
- Further reduce B_{max}, to reduce core losses

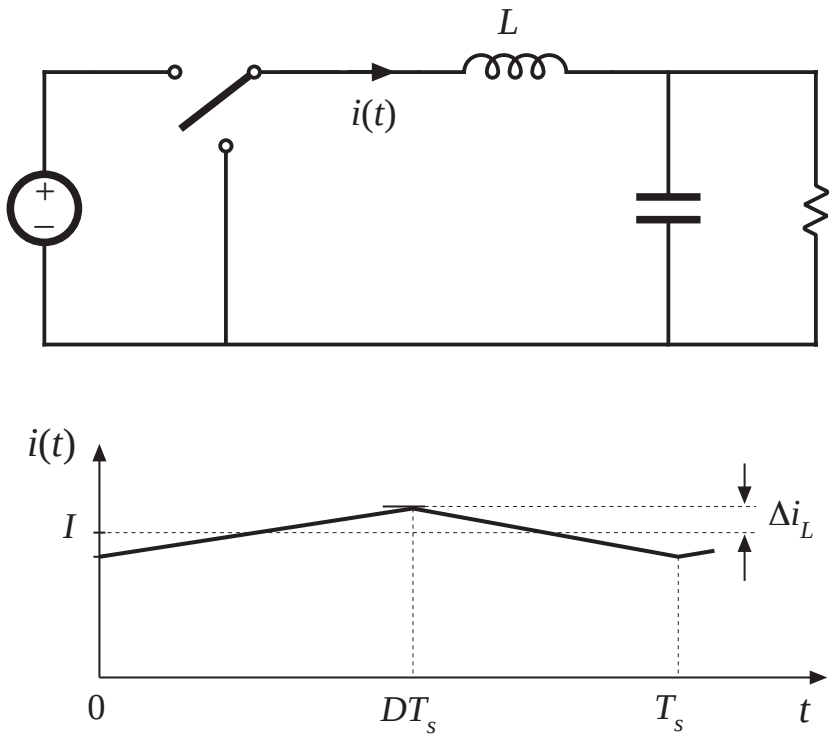
Different design procedures are employed in the two cases.

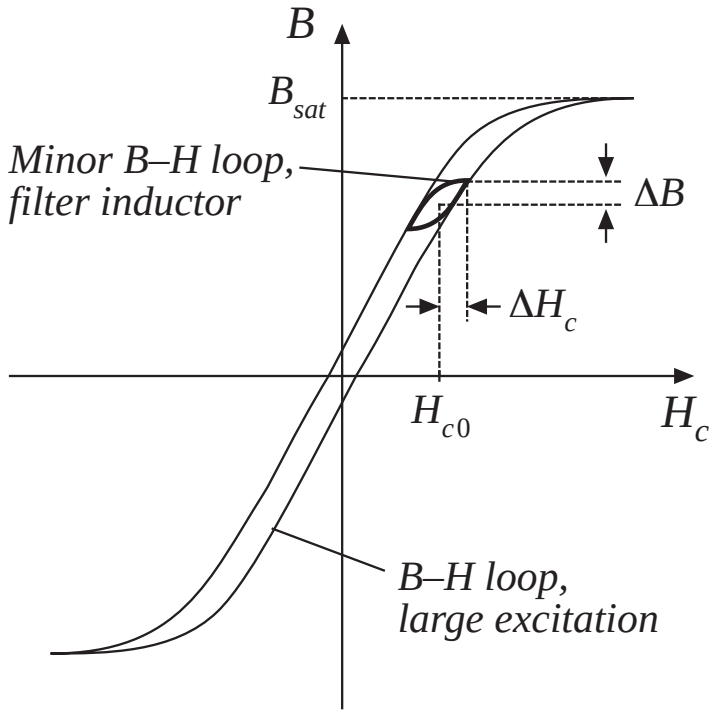
Types of magnetic devices:

Filter inductor	AC inductor
Conventional transformer	Coupled inductor
Flyback transformer	SEPIC transformer
Magnetic amplifier	Saturable reactor

Filter inductor

CCM buck example

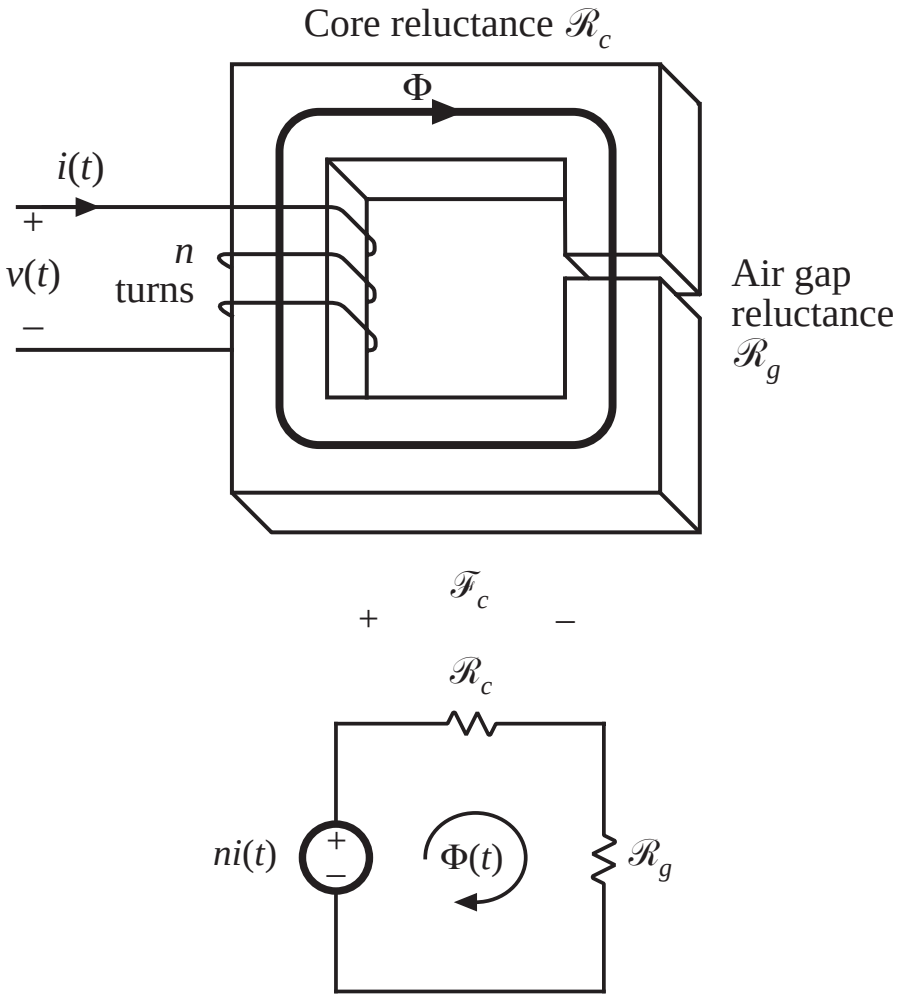




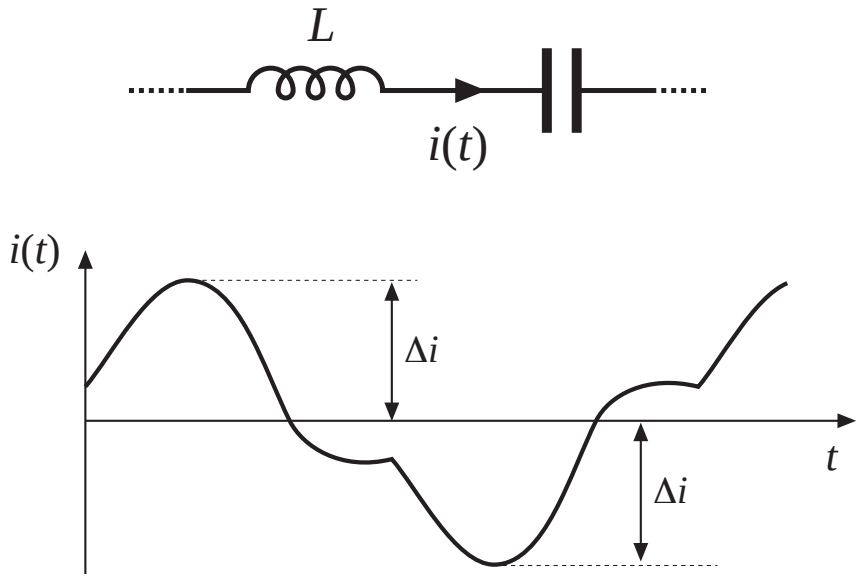
$$H_c(t) = \frac{ni(t)}{\ell_c} \frac{\mathscr{R}_c}{\mathscr{R}_c + \mathscr{R}_g}$$

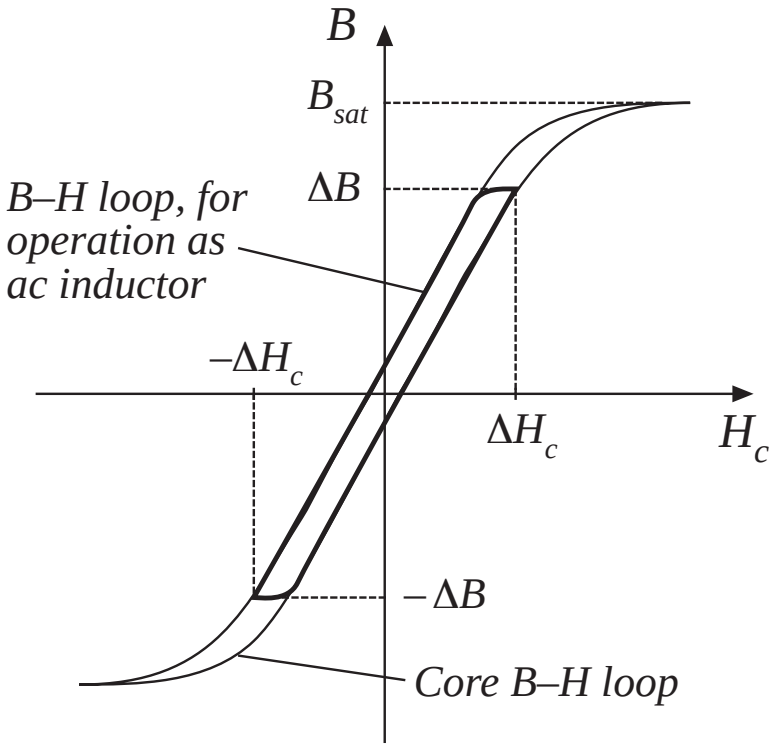
Filter inductor, cont.

- Negligible core loss, negligible proximity loss
- Loss dominated by dc copper loss
- Flux density chosen simply to avoid saturation
- Air gap is employed
- Could use core materials having high saturation flux density (and relatively high core loss), even though converter switching frequency is high



AC inductor

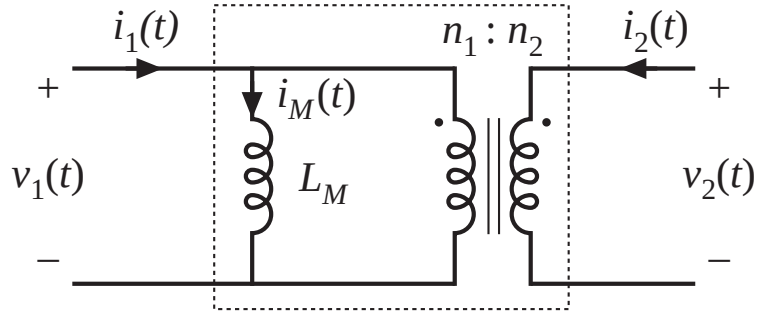

L
i(t)
i(t)
Δi
Δi
t

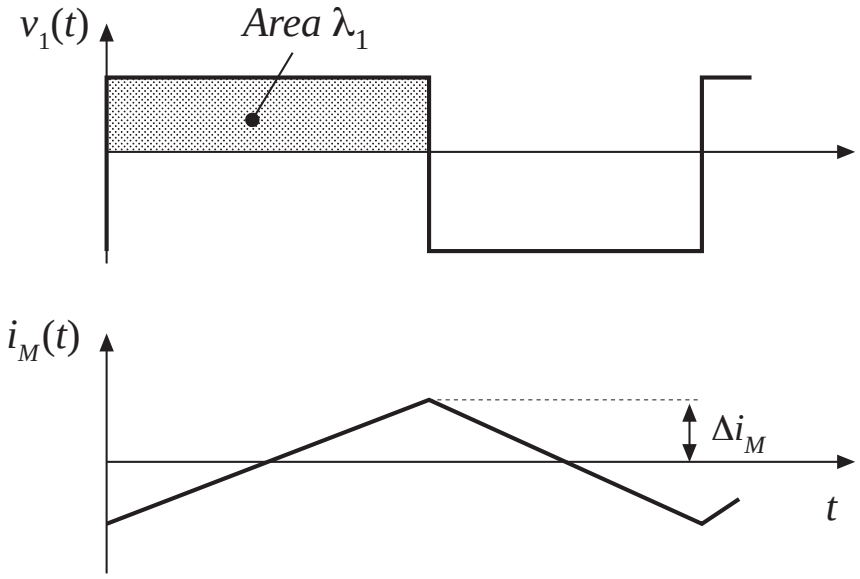

B
B_sat
ΔB
B–H loop, for operation as ac inductor
–ΔH_c
ΔH_c
H_c
–ΔB
Core B–H loop

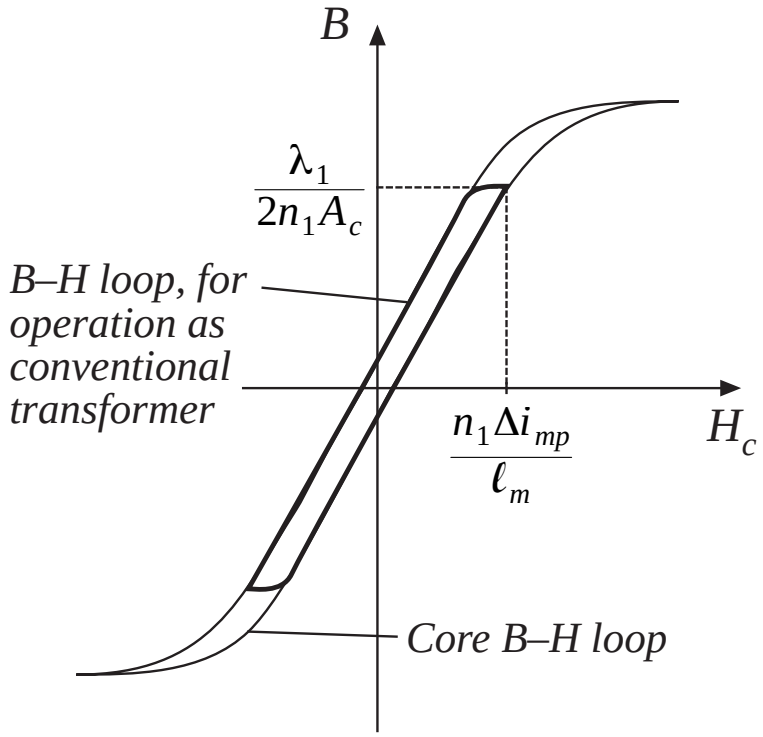
AC inductor, cont.

- Core loss, copper loss, proximity loss are all significant
- An air gap is employed
- Flux density is chosen to reduce core loss
- A high-frequency material (ferrite) must be employed

Conventional transformer







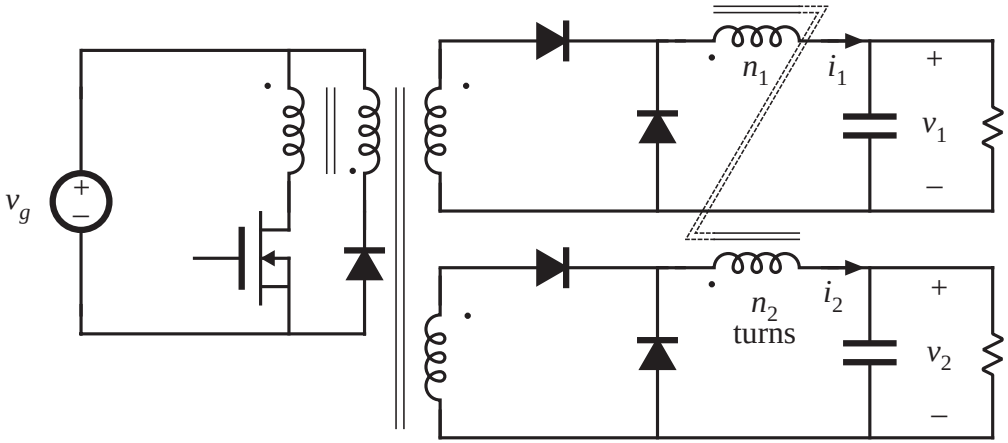
$$H(t) = \frac{ni_M(t)}{\ell_m}$$

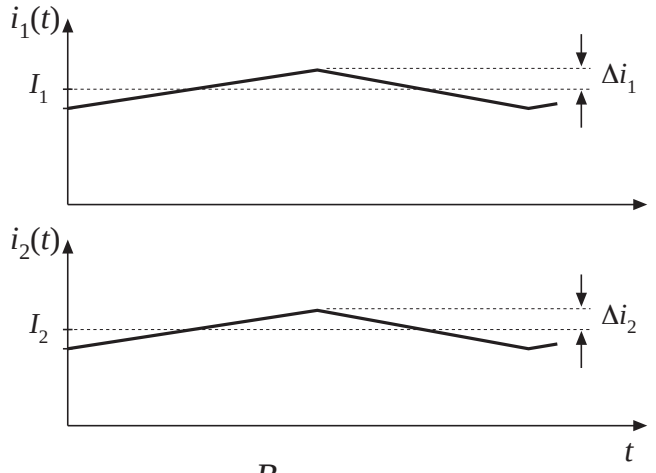
Conventional transformer, cont.

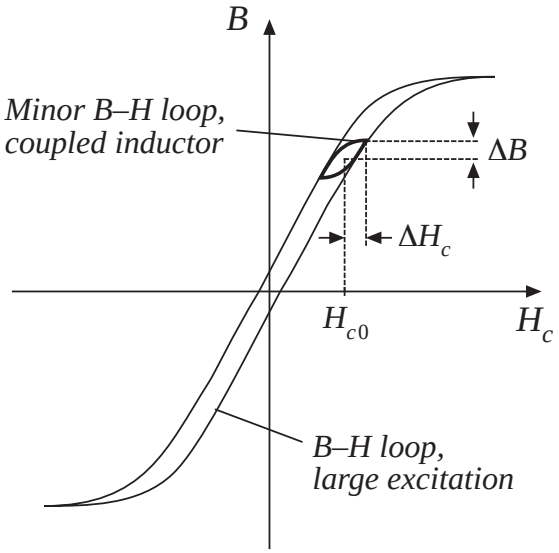
- Core loss, copper loss, and proximity loss are usually significant
- No air gap is employed
- Flux density is chosen to reduce core loss
- A high frequency material (ferrite) must be employed

Coupled inductor

Two-output forward converter example





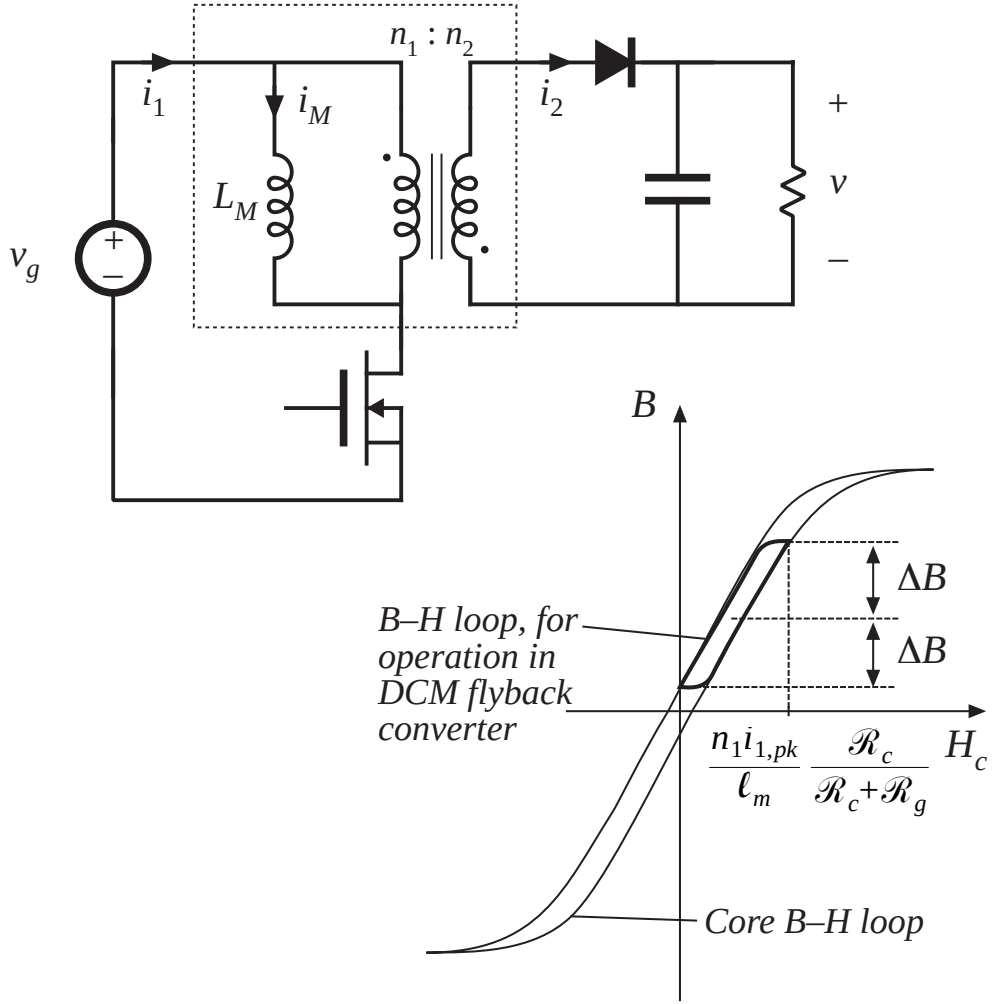


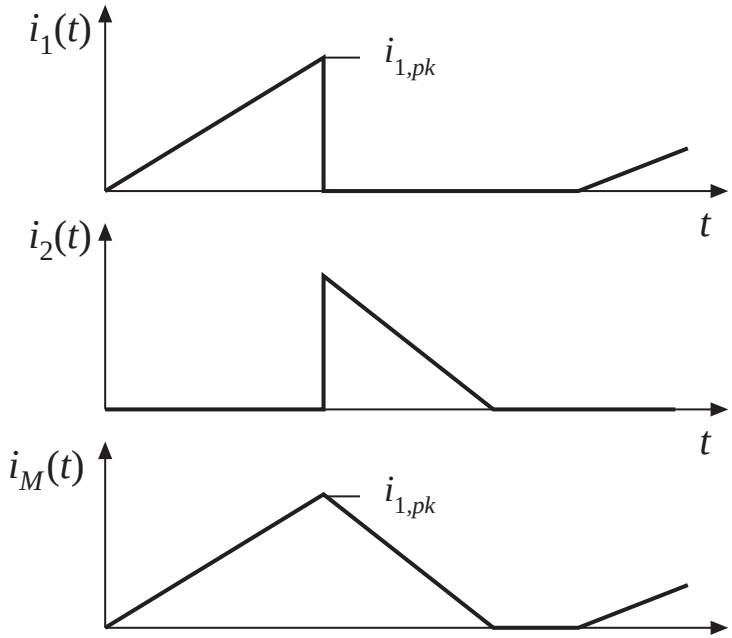
$$H_c(t) = \frac{n_1 i_1(t) + n_2 i_2(t)}{\ell_c} \frac{\mathscr{R}_c}{\mathscr{R}_c + \mathscr{R}_g}$$

Coupled inductor, cont.

- A filter inductor having multiple windings
- Air gap is employed
- Core loss and proximity loss usually not significant
- Flux density chosen to avoid saturation
- Low-frequency core material can be employed

DCM flyback transformer





DCM flyback transformer, cont.

- Core loss, copper loss, proximity loss are significant
- Flux density is chosen to reduce core loss
- Air gap is employed
- A high-frequency core material (ferrite) must be used

Summary of Key Points

1. Magnetic devices can be modeled using lumped-element magnetic circuits, in a manner similar to that commonly used to model electrical circuits. The magnetic analogs of electrical voltage V, current I, and resistance R, are magnetomotive force (MMF) $\mathscr{F}$, flux Φ, and reluctance $\mathscr{R}$ respectively.
2. Faraday's law relates the voltage induced in a loop of wire to the derivative of flux passing through the interior of the loop.
3. Ampere's law relates the total MMF around a loop to the total current passing through the center of the loop. Ampere's law implies that winding currents are sources of MMF, and that when these sources are included, then the net MMF around a closed path is equal to zero.
4. Magnetic core materials exhibit hysteresis and saturation. A core material saturates when the flux density B reaches the saturation flux density B_{sat}.

Summary of key points

5. Air gaps are employed in inductors to prevent saturation when a given maximum current flows in the winding, and to stabilize the value of inductance. The inductor with air gap can be analyzed using a simple magnetic equivalent circuit, containing core and air gap reluctances and a source representing the winding MMF.
6. Conventional transformers can be modeled using sources representing the MMFs of each winding, and the core MMF. The core reluctance approaches zero in an ideal transformer. Nonzero core reluctance leads to an electrical transformer model containing a magnetizing inductance, effectively in parallel with the ideal transformer. Flux that does not link both windings, or "leakage flux," can be modeled using series inductors.
7. The conventional transformer saturates when the applied winding volt-seconds are too large. Addition of an air gap has no effect on saturation. Saturation can be prevented by increasing the core cross-sectional area, or by increasing the number of primary turns.

Summary of key points

8. Magnetic materials exhibit core loss, due to hysteresis of the B–H loop and to induced eddy currents flowing in the core material. In available core materials, there is a tradeoff between high saturation flux density B_{sat} and high core loss P_{fe}. Laminated iron alloy cores exhibit the highest B_{sat} but also the highest P_{fe}, while ferrite cores exhibit the lowest P_{fe} but also the lowest B_{sat}. Between these two extremes are powdered iron alloy and amorphous alloy materials.

9. The skin and proximity effects lead to eddy currents in winding conductors, which increase the copper loss P_{cu} in high-current high-frequency magnetic devices. When a conductor has thickness approaching or larger than the penetration depth δ, magnetic fields in the vicinity of the conductor induce eddy currents in the conductor. According to Lenz's law, these eddy currents flow in paths that tend to oppose the applied magnetic fields.

Summary of key points

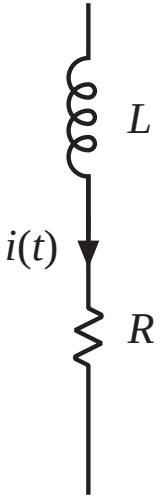
10. The magnetic field strengths in the vicinity of the winding conductors can be determined by use of MMF diagrams. These diagrams are constructed by application of Ampere's law, following the closed paths of the magnetic field lines which pass near the winding conductors. Multiple-layer noninterleaved windings can exhibit high maximum MMFs, with resulting high eddy currents and high copper loss.
11. An expression for the copper loss in a layer, as a function of the magnetic field strengths or MMFs surrounding the layer, is given in Section 13.4.4. This expression can be used in conjunction with the MMF diagram, to compute the copper loss in each layer of a winding. The results can then be summed, yielding the total winding copper loss. When the effective layer thickness is near to or greater than one skin depth, the copper losses of multiple-layer noninterleaved windings are greatly increased.

Summary of key points

12. Pulse-width-modulated winding currents of contain significant total harmonic distortion, which can lead to a further increase of copper loss. The increase in proximity loss caused by current harmonics is most pronounced in multiple-layer non-interleaved windings, with an effective layer thickness near one skin depth.
13. A variety of magnetic devices are commonly used in switching converters. These devices differ in their core flux density variations, as well as in the magnitudes of the ac winding currents. When the flux density variations are small, core loss can be neglected. Alternatively, a low-frequency material can be used, having higher saturation flux density.

Chapter 14 Inductor Design

14.1 Filter inductor design constraints



Objective:

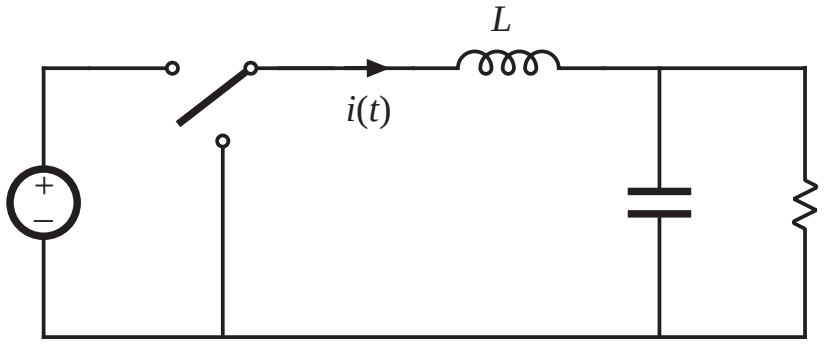
Design inductor having a given inductance L,

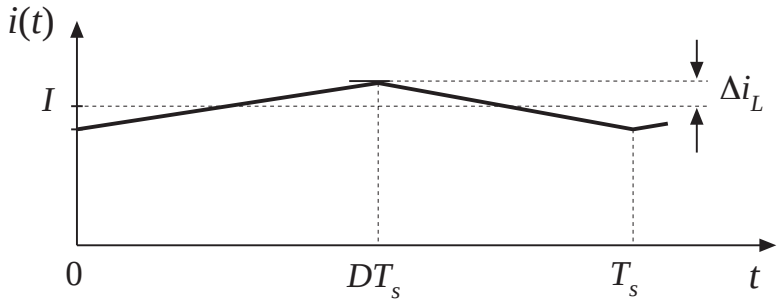
which carries worst-case current I_{max} without saturating,

and which has a given winding resistance R, or, equivalently, exhibits a worst-case copper loss of

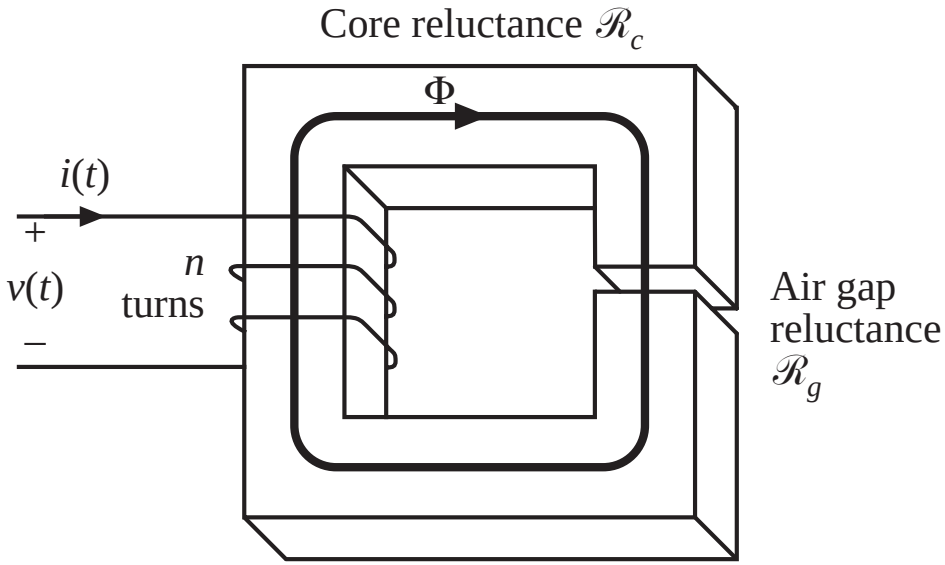
$$P_{cu} = I_{rms}^{\ 2} R$$

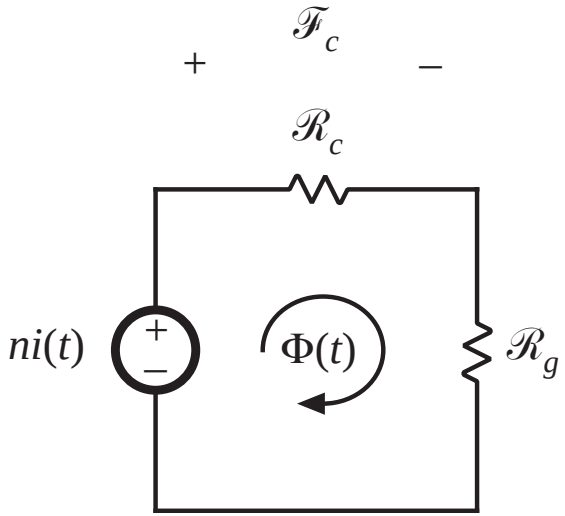
Example: filter inductor in CCM buck converter





Assumed filter inductor geometry





$$\mathscr{R}_c = \frac{\ell_c}{\mu_c A_c}$$

$$\mathscr{R}_g = \frac{\ell_g}{\mu_0 A_c}$$

Solve magnetic circuit:

$$ni = \Phi\left(\mathscr{R}_c + \mathscr{R}_g\right)$$

Usually $\mathscr{R}_c \ll \mathscr{R}_g$ and hence

$$ni \approx \Phi \mathscr{R}_g$$

14.1.1 Constraint: maximum flux density

Given a peak winding current I_{max}, it is desired to operate the core flux density at a peak value B_{max}. The value of B_{max} is chosen to be less than the worst-case saturation flux density B_{sat} of the core material.

From solution of magnetic circuit:

$$ni = BA_c \mathcal{R}_g$$

Let $I = I_{max}$ and $B = B_{max}$:

$$nI_{max} = B_{max} A_c \mathcal{R}_g = B_{max} \frac{\ell_g}{\mu_0}$$

This is constraint #1. The turns ratio n and air gap length ℓ_g are unknown.

14.1.2 Constraint: inductance

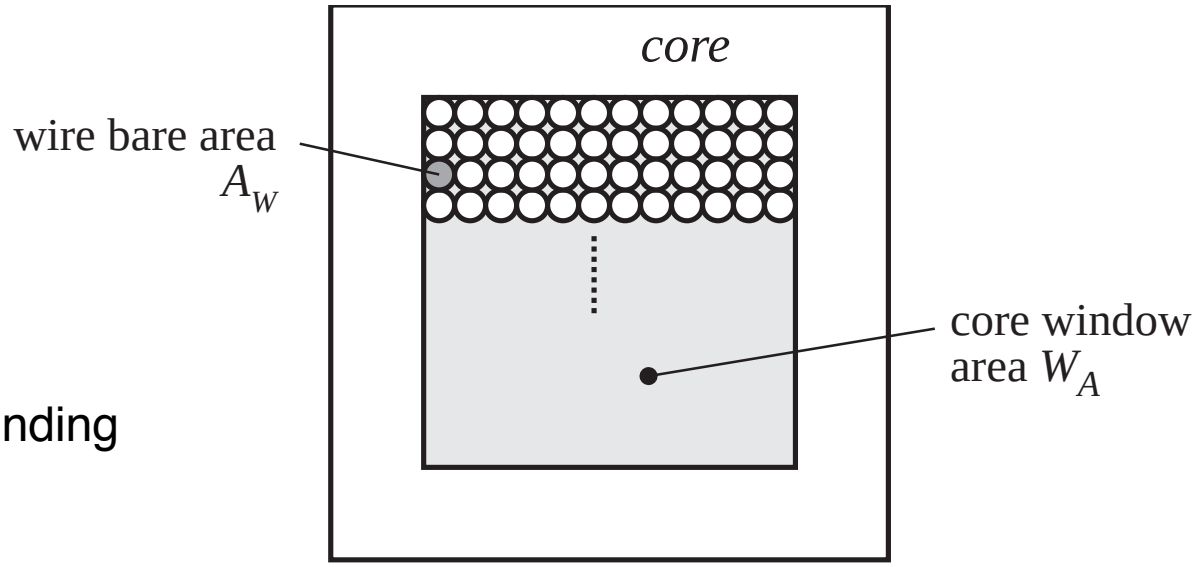
Must obtain specified inductance L. We know that the inductance is

$$L = \frac{n^2}{\mathcal{R}_g} = \frac{\mu_0 A_c n^2}{\ell_g}$$

This is constraint #2. The turns ratio n, core area A_c, and air gap length ℓ_g are unknown.

14.1.3 Constraint: winding area

Wire must fit through core window (i.e., hole in center of core)



Total area of copper in window:

$$nA_W$$

Area available for winding conductors:

$$K_u W_A$$

Third design constraint:

$$K_u W_A \geq nA_W$$

The window utilization factor K_u
also called the "fill factor"

K_u is the fraction of the core window area that is filled by copper

Mechanisms that cause K_u to be less than 1:

- Round wire does not pack perfectly, which reduces K_u by a factor of 0.7 to 0.55 depending on winding technique
- Insulation reduces K_u by a factor of 0.95 to 0.65, depending on wire size and type of insulation
- Bobbin uses some window area
- Additional insulation may be required between windings

Typical values of K_u :

0.5 for simple low-voltage inductor

0.25 to 0.3 for off-line transformer

0.05 to 0.2 for high-voltage transformer (multiple kV)

0.65 for low-voltage foil-winding inductor

14.1.4 Winding resistance

The resistance of the winding is

$$R = \rho \frac{\ell_b}{A_W}$$

where ρ is the resistivity of the conductor material, ℓ_b is the length of the wire, and A_W is the wire bare area. The resistivity of copper at room temperature is $1.724 \cdot 10^{-6}\ \Omega\text{-cm}$. The length of the wire comprising an n-turn winding can be expressed as

$$\ell_b = n(MLT)$$

where (MLT) is the mean-length-per-turn of the winding. The mean-length-per-turn is a function of the core geometry. The above equations can be combined to obtain the fourth constraint:

$$R = \rho \frac{n\,(MLT)}{A_W}$$

14.1.5 The core geometrical constant K_g

The four constraints:

$$nI_{max} = B_{max} A_c \mathcal{R}_g = B_{max} \frac{\ell_g}{\mu_0} \qquad L = \frac{n^2}{\mathcal{R}_g} = \frac{\mu_0 A_c n^2}{\ell_g}$$

$$K_u W_A \geq n A_W \qquad R = \rho \frac{n\,(MLT)}{A_W}$$

These equations involve the quantities

A_c, W_A, and MLT, which are functions of the core geometry,

I_{max}, B_{max} , μ_0, L, K_u, R, and ρ, which are given specifications or other known quantities, and

n, ℓ_g, and A_W, which are unknowns.

Eliminate the three unknowns, leading to a single equation involving the remaining quantities.

Core geometrical constant K_g

Elimination of n, ℓ_g, and A_W leads to

$$\frac{A_c^2 W_A}{(MLT)} \geq \frac{\rho L^2 I_{max}^2}{B_{max}^2 R K_u}$$

- Right-hand side: specifications or other known quantities
- Left-hand side: function of only core geometry

So we must choose a core whose geometry satisfies the above equation.

The core geometrical constant K_g is defined as

$$K_g = \frac{A_c^2 W_A}{(MLT)}$$

Discussion

$$K_g = \frac{A_c^2 W_A}{(MLT)} \geq \frac{\rho L^2 I_{max}^2}{B_{max}^2 R K_u}$$

K_g is a figure-of-merit that describes the effective electrical size of magnetic cores, in applications where the following quantities are specified:

- Copper loss
- Maximum flux density

How specifications affect the core size:

A smaller core can be used by increasing

$B_{max} \Rightarrow$ use core material having higher B_{sat}

$R \Rightarrow$ allow more copper loss

How the core geometry affects electrical capabilities:

A larger K_g can be obtained by increase of

$A_c \Rightarrow$ more iron core material, or

$W_A \Rightarrow$ larger window and more copper

14.2 A step-by-step procedure

The following quantities are specified, using the units noted:

Wire resistivity	ρ	(Ω-cm)
Peak winding current	I_{max}	(A)
Inductance	L	(H)
Winding resistance	R	(Ω)
Winding fill factor	K_u	
Core maximum flux density	B_{max}	(T)

The core dimensions are expressed in cm:

Core cross-sectional area	A_c	(cm^2)
Core window area	W_A	(cm^2)
Mean length per turn	MLT	(cm)

The use of centimeters rather than meters requires that appropriate factors be added to the design equations.

Determine core size

$$K_g \geq \frac{\rho L^2 I_{max}^2}{B_{max}^2 R K_u} \, 10^8 \qquad (\text{cm}^5)$$

Choose a core which is large enough to satisfy this inequality (*see Appendix D for magnetics design tables*).

Note the values of A_c, W_A, and MLT for this core.

Determine air gap length

$$\ell_g = \frac{\mu_0 L I_{max}^2}{B_{max}^2 A_c} 10^4 \quad \text{(m)}$$

with A_c expressed in cm^2. $\mu_0 = 4\pi 10^{-7}$ H/m.

The air gap length is given in meters.

The value expressed above is approximate, and neglects fringing flux and other nonidealities.

A_L

Core manufacturers sell gapped cores. Rather than specifying the air gap length, the equivalent quantity A_L is used.

A_L is equal to the inductance, in mH, obtained with a winding of 1000 turns.

When A_L is specified, it is the core manufacturer's responsibility to obtain the correct gap length.

The required A_L is given by:

$$A_L = \frac{10 B_{max}^2 A_c^2}{L I_{max}^2} \quad \text{(mH/1000 turns)}$$

Units:

A_c cm^2,
L Henries,
B_{max} Tesla.

$$L = A_L \, n^2 \, 10^{-9} \quad \text{(Henries)}$$

Determine number of turns n

$$n = \frac{LI_{max}}{B_{max}A_c} \; 10^4$$

Evaluate wire size

$$A_W \leq \frac{K_u W_A}{n} \quad (\text{cm}^2)$$

Select wire with bare copper area A_W less than or equal to this value. An American Wire Gauge table is included in Appendix D.

As a check, the winding resistance can be computed:

$$R = \frac{\rho n \, (MLT)}{A_w} \quad (\Omega)$$

14.3 Multiple-winding magnetics design using the K_g method

The K_g design method can be extended to multiple-winding magnetic elements such as transformers and coupled inductors.

This method is applicable when

- Copper loss dominates the total loss (i.e. core loss is ignored), or
- The maximum flux density B_{max} is a specification rather than a quantity to be optimized

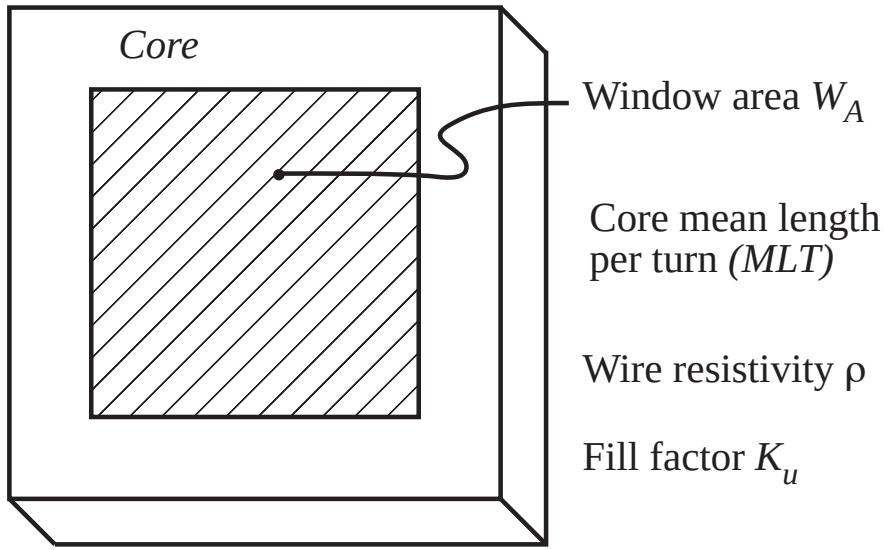
To do this, we must

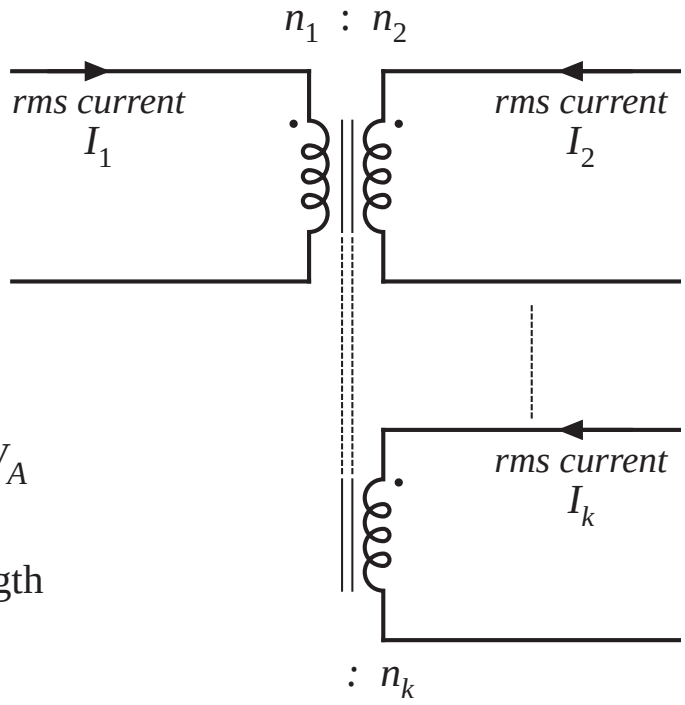
- Find how to allocate the window area between the windings
- Generalize the step-by-step design procedure

14.3.1 Window area allocation

Given: application with k windings having known rms currents and desired turns ratios

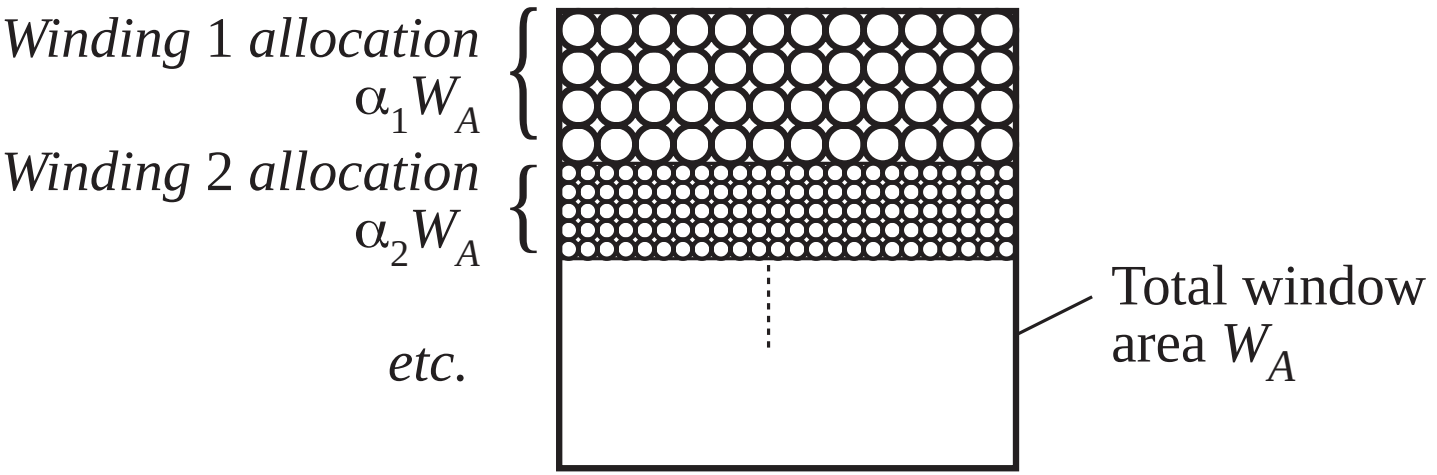
$$\frac{v_1(t)}{n_1} = \frac{v_2(t)}{n_2} = \cdots = \frac{v_k(t)}{n_k}$$





Q: how should the window area W_A be allocated among the windings?

Allocation of winding area



$$0 < \alpha_j < 1$$

$$\alpha_1 + \alpha_2 + \cdots + \alpha_k = 1$$

Copper loss in winding *j*

Copper loss (not accounting for proximity loss) is

$$P_{cu,j} = I_j^2 R_j$$

Resistance of winding *j* is

$$R_j = \rho \frac{\ell_j}{A_{W,j}}$$

with

$$\ell_j = n_j (MLT)$$

length of wire, winding *j*

$$A_{W,j} = \frac{W_A K_u \alpha_j}{n_j}$$

wire area, winding *j*

Hence

$$R_j = \rho \frac{n_j^2 (MLT)}{W_A K_u \alpha_j}$$

$$P_{cu,j} = \frac{n_j^2 i_j^2 \rho (MLT)}{W_A K_u \alpha_j}$$

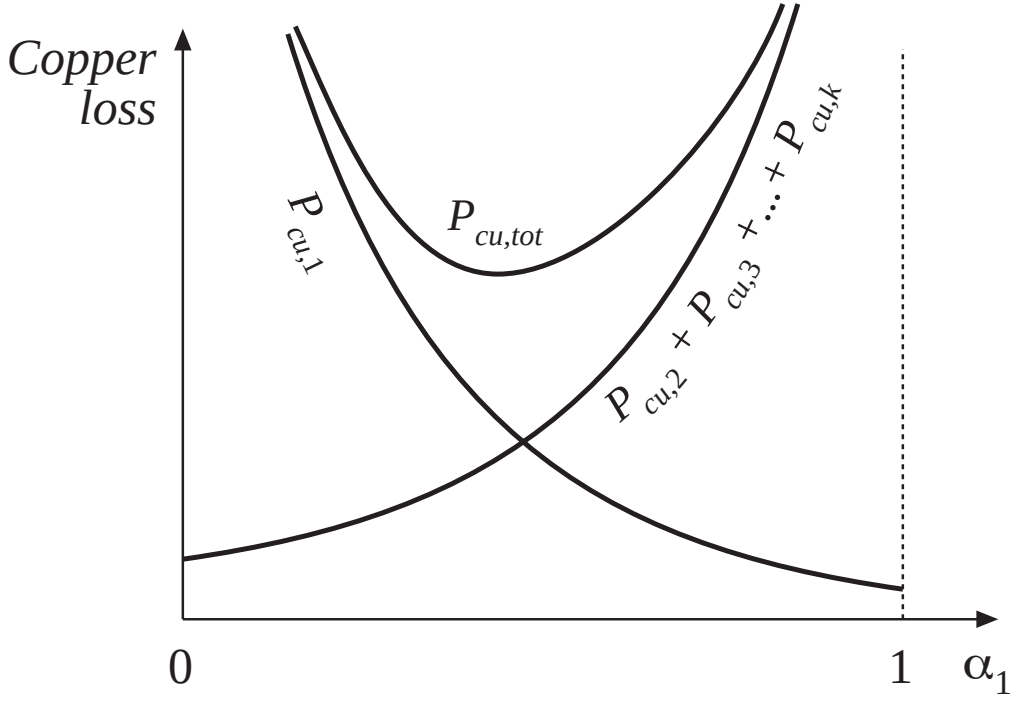
Total copper loss of transformer

Sum previous expression over all windings:

$$P_{cu,tot} = P_{cu,1} + P_{cu,2} + \cdots + P_{cu,k} = \frac{\rho\,(MLT)}{W_A K_u} \sum_{j=1}^{k} \left(\frac{n_j^2 I_j^2}{\alpha_j} \right)$$

Need to select values for $\alpha_1, \alpha_2, \ldots, \alpha_k$ such that the total copper loss is minimized

Variation of copper losses with α_1



For α_1 = 0: wire of winding 1 has zero area. $P_{cu,1}$ tends to infinity

For α_1 = 1: wires of remaining windings have zero area. Their copper losses tend to infinity

There is a choice of α_1 that minimizes the total copper loss

Method of Lagrange multipliers
to minimize total copper loss

Minimize the function

$$P_{cu,tot} = P_{cu,1} + P_{cu,2} + \cdots + P_{cu,k} = \frac{\rho\,(MLT)}{W_A K_u} \sum_{j=1}^{k} \left(\frac{n_j^2 I_j^2}{\alpha_j} \right)$$

subject to the constraint

$$\alpha_1 + \alpha_2 + \cdots + \alpha_k = 1$$

Define the function

$$f(\alpha_1, \alpha_2, \cdots, \alpha_k, \xi) = P_{cu,tot}(\alpha_1, \alpha_2, \cdots, \alpha_k) + \xi\, g(\alpha_1, \alpha_2, \cdots, \alpha_k)$$

where

$$g(\alpha_1, \alpha_2, \cdots, \alpha_k) = 1 - \sum_{j=1}^{k} \alpha_j$$

is the constraint that must equal zero

and ξ is the Lagrange multiplier

Lagrange multipliers
continued

Optimum point is solution of the system of equations

$$\frac{\partial f(\alpha_1, \alpha_2, \cdots, \alpha_k, \xi)}{\partial \alpha_1} = 0$$
$$\frac{\partial f(\alpha_1, \alpha_2, \cdots, \alpha_k, \xi)}{\partial \alpha_2} = 0$$
$$\vdots$$
$$\frac{\partial f(\alpha_1, \alpha_2, \cdots, \alpha_k, \xi)}{\partial \alpha_k} = 0$$
$$\frac{\partial f(\alpha_1, \alpha_2, \cdots, \alpha_k, \xi)}{\partial \xi} = 0$$

Result:

$$\xi = \frac{\rho\,(MLT)}{W_A K_u} \left(\sum_{j=1}^{k} n_j I_j \right)^2 = P_{cu,tot}$$

$$\alpha_m = \frac{n_m I_m}{\sum_{n=1}^{\infty} n_j I_j}$$

An alternate form:

$$\alpha_m = \frac{V_m I_m}{\sum_{n=1}^{\infty} V_j I_j}$$

Interpretation of result

$$\alpha_m = \frac{V_m I_m}{\sum_{n=1}^{\infty} V_j I_j}$$

Apparent power in winding j is

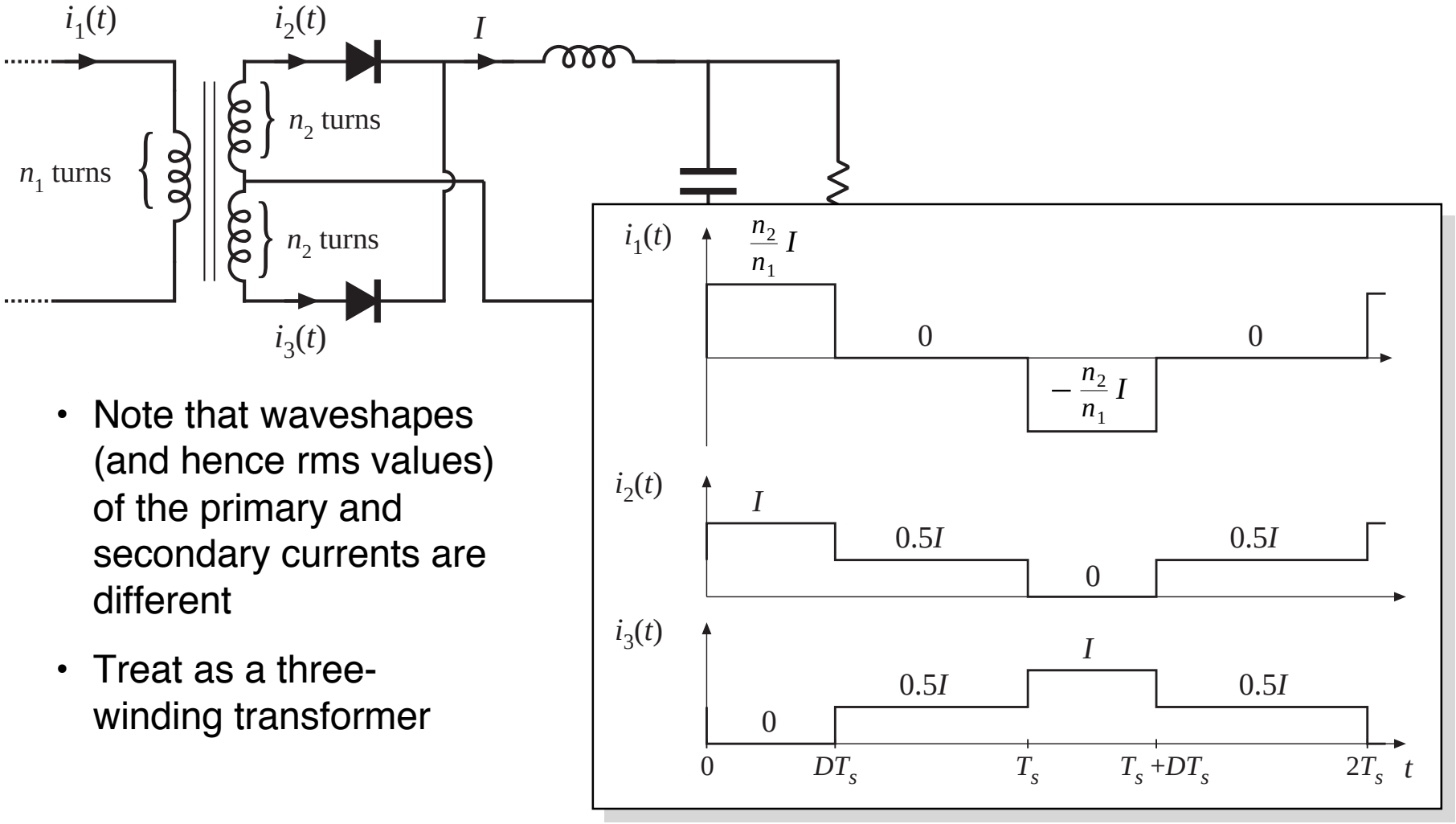
$$V_j I_j$$

where V_j is the rms or peak applied voltage

I_j is the rms current

Window area should be allocated according to the apparent powers of the windings

Example
PWM full-bridge transformer



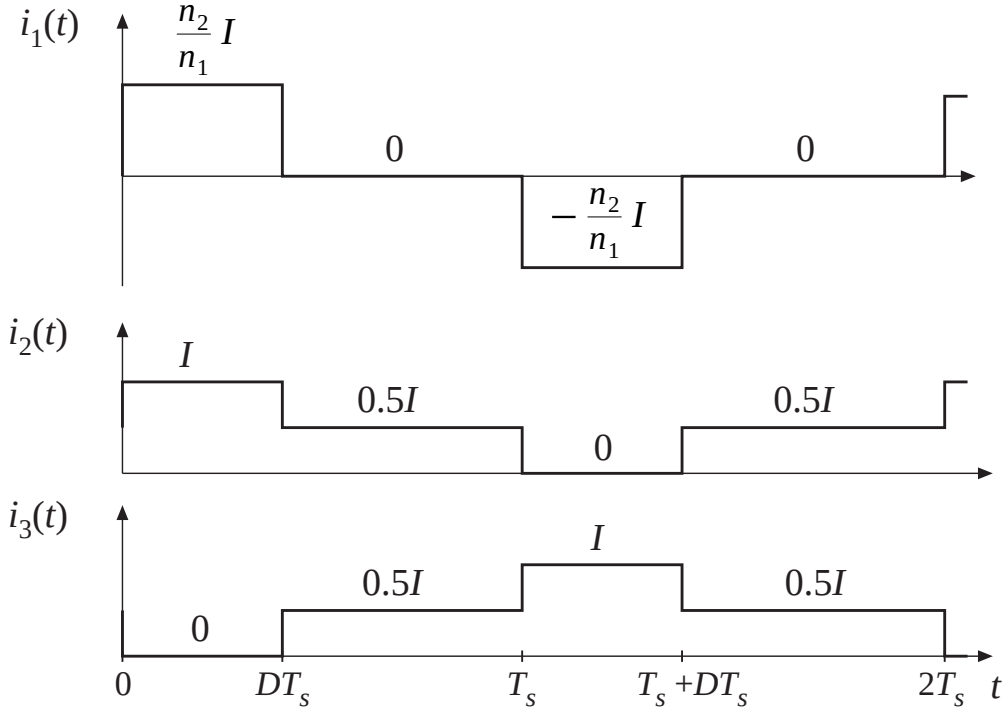
- Note that waveshapes (and hence rms values) of the primary and secondary currents are different
- Treat as a three-winding transformer

Expressions for RMS winding currents

$$I_1 = \sqrt{\frac{1}{2T_s}\int_0^{2T_s} i_1^2(t)\,dt} = \frac{n_2}{n_1} I \sqrt{D}$$

$$I_2 = I_3 = \sqrt{\frac{1}{2T_s}\int_0^{2T_s} i_2^2(t)\,dt} = \frac{1}{2} I \sqrt{1+D}$$

see Appendix A



Allocation of window area:

$$\alpha_m = \frac{V_m I_m}{\sum_{n=1}^{\infty} V_j I_j}$$

Plug in rms current expressions. Result:

$$\alpha_1 = \frac{1}{\left(1 + \sqrt{\frac{1+D}{D}}\right)}$$

Fraction of window area allocated to primary winding

$$\alpha_2 = \alpha_3 = \frac{1}{2} \frac{1}{\left(1 + \sqrt{\frac{D}{1+D}}\right)}$$

Fraction of window area allocated to each secondary winding

Numerical example

Suppose that we decide to optimize the transformer design at the worst-case operating point $D = 0.75$. Then we obtain

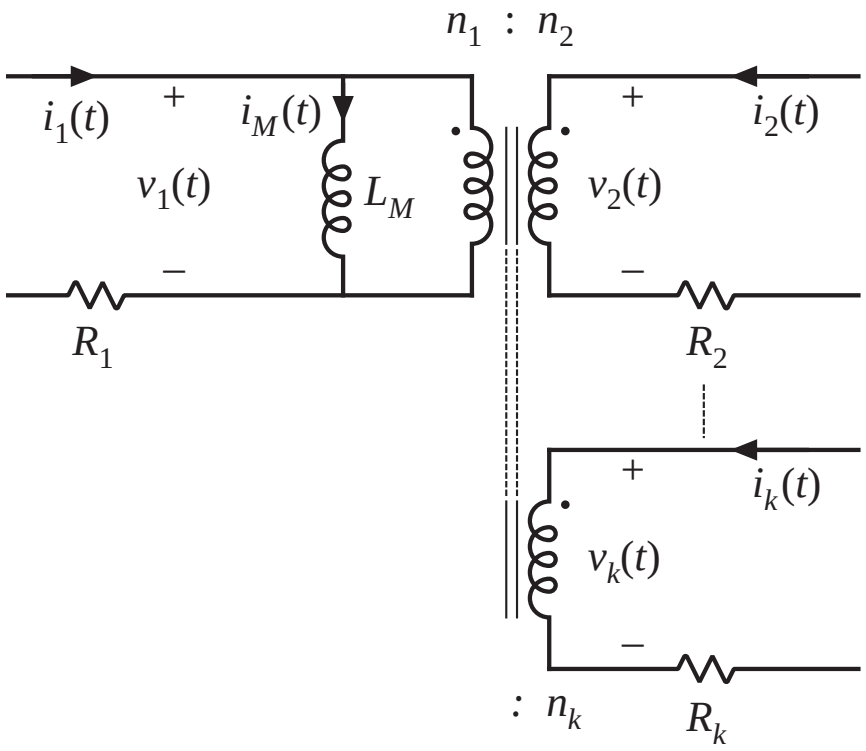
$$\alpha_1 = 0.396$$
$$\alpha_2 = 0.302$$
$$\alpha_3 = 0.302$$

The total copper loss is then given by

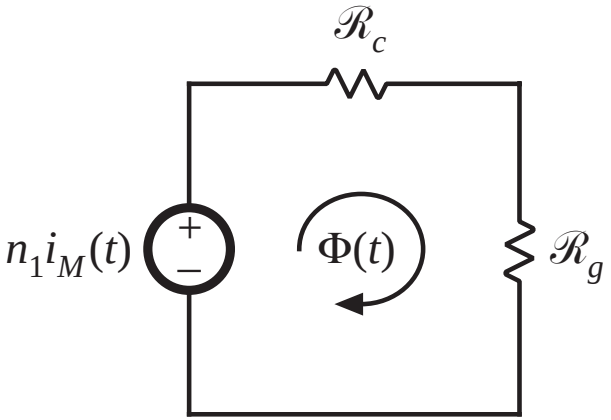
$$P_{cu,tot} = \frac{\rho(MLT)}{W_A K_u} \left(\sum_{j=1}^{3} n_j I_j \right)^2$$
$$= \frac{\rho(MLT) n_2^2 I^2}{W_A K_u} \left(1 + 2D + 2\sqrt{D(1+D)} \right)$$

14.3.2 Coupled inductor design constraints

Consider now the design of a coupled inductor having k windings. We want to obtain a specified value of magnetizing inductance, with specified turns ratios and total copper loss.



Magnetic circuit model:

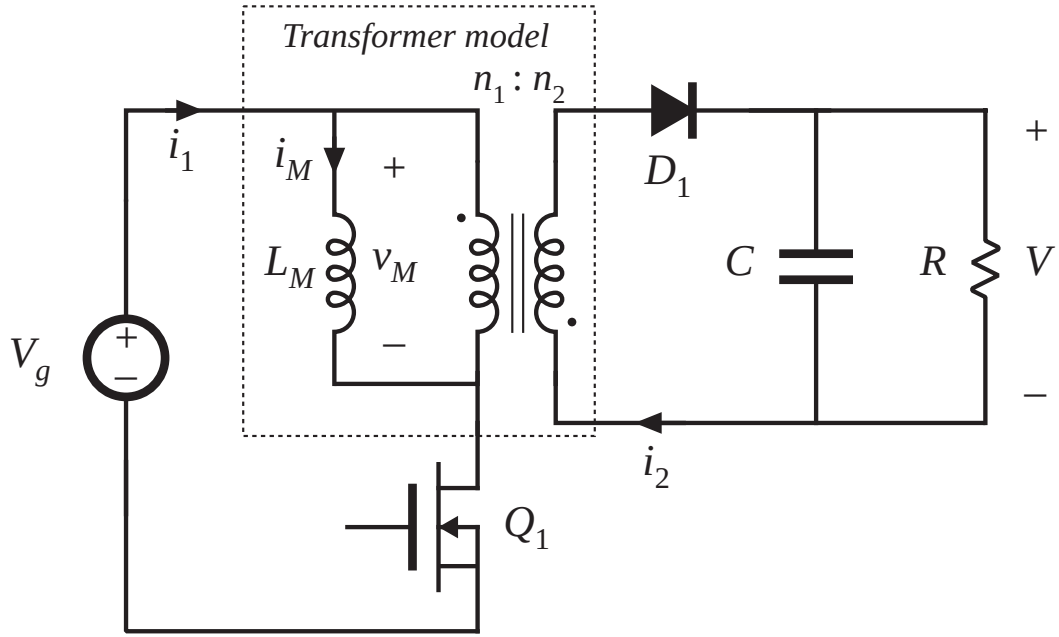


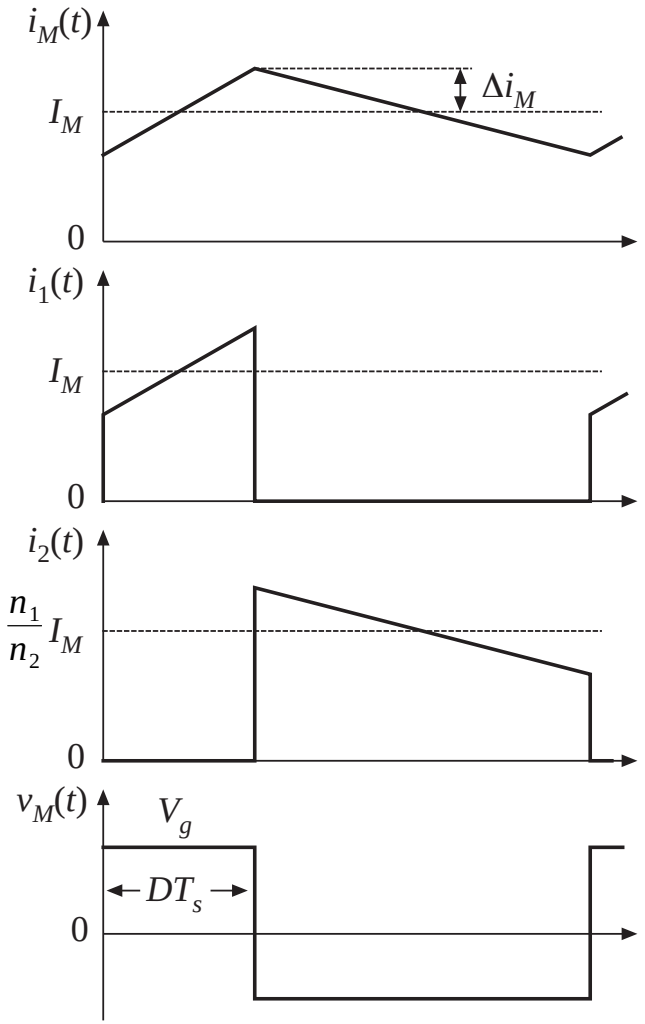
14.4 Examples

14.4.1 Coupled Inductor for a Two-Output Forward Converter

14.4.2 CCM Flyback Transformer

14.4.2 Example 2: CCM flyback transformer





Specifications

Input voltage	$V_g = 200\text{V}$
Output (full load)	20 V at 5 A
Switching frequency	150 kHz
Magnetizing current ripple	20% of dc magnetizing current
Duty cycle	$D = 0.4$
Turns ratio	$n_2/n_1 = 0.15$
Copper loss	1.5 W
Fill factor	$K_u = 0.3$
Maximum flux density	$B_{max} = 0.25$ T

Basic converter calculations

Components of magnetizing current, referred to primary:

$$I_M = \left(\frac{n_2}{n_1}\right)\frac{1}{D'}\frac{V}{R} = 1.25 \text{ A}$$

$$\Delta i_M = \left(20\%\right) I_M = 0.25 \text{ A}$$

$$I_{M,max} = I_M + \Delta i_M = 1.5 \text{ A}$$

Choose magnetizing inductance:

$$L_M = \frac{V_g D T_s}{2\Delta i_M} = 1.07 \text{ mH}$$

RMS winding currents:

$$I_1 = I_M \sqrt{D} \sqrt{1 + \frac{1}{3}\left(\frac{\Delta i_M}{I_M}\right)^2} = 0.796 \text{ A}$$

$$I_2 = \frac{n_1}{n_2} I_M \sqrt{D'} \sqrt{1 + \frac{1}{3}\left(\frac{\Delta i_M}{I_M}\right)^2} = 6.50 \text{ A}$$

$$I_{tot} = I_1 + \frac{n_2}{n_1} I_2 = 1.77 \text{ A}$$

Choose core size

$$K_g \geq \frac{\rho L_M^2 I_{tot}^2 I_{M,max}^2}{B_{max}^2 P_{cu} K_u} 10^8$$

$$= \frac{\left(1.724 \cdot 10^{-6} \Omega\text{-cm}\right)\left(1.07 \cdot 10^{-3}\ \text{H}\right)^2 \left(1.77\ \text{A}\right)^2 \left(1.5\ \text{A}\right)^2}{\left(0.25\ \text{T}\right)^2 \left(1.5\ \text{W}\right)\left(0.3\right)} 10^8$$

$$= 0.049\ \text{cm}^5$$

The smallest EE core that satisfies this inequality (Appendix D) is the EE30.

Choose air gap and turns

$$\ell_g = \frac{\mu_0 L_M I_{M,max}^2}{B_{max}^2 A_c} 10^4$$

$$= \frac{\left(4\pi \cdot 10^{-7}\text{H/m}\right)\left(1.07 \cdot 10^{-3}\text{ H}\right)\left(1.5\text{ A}\right)^2}{\left(0.25\text{ T}\right)^2\left(1.09\text{ cm}^2\right)} 10^4$$

$$= 0.44\text{ mm}$$

$$n_1 = \frac{L_M I_{M,max}}{B_{max} A_c} 10^4$$

$$= \frac{\left(1.07 \cdot 10^{-3}\text{ H}\right)\left(1.5\text{ A}\right)}{\left(0.25\text{ T}\right)\left(1.09\text{ cm}^2\right)} 10^4$$

$$= 58.7\text{ turns}$$

Round to $n_1 = 59$

$$n_2 = \left(\frac{n_2}{n_1}\right) n_1$$

$$= \left(0.15\right) 59$$

$$= 8.81$$

$n_2 = 9$

Wire gauges

$$\alpha_1 = \frac{I_1}{I_{tot}} = \frac{\left(0.796\text{ A}\right)}{\left(1.77\text{ A}\right)} = 0.45$$

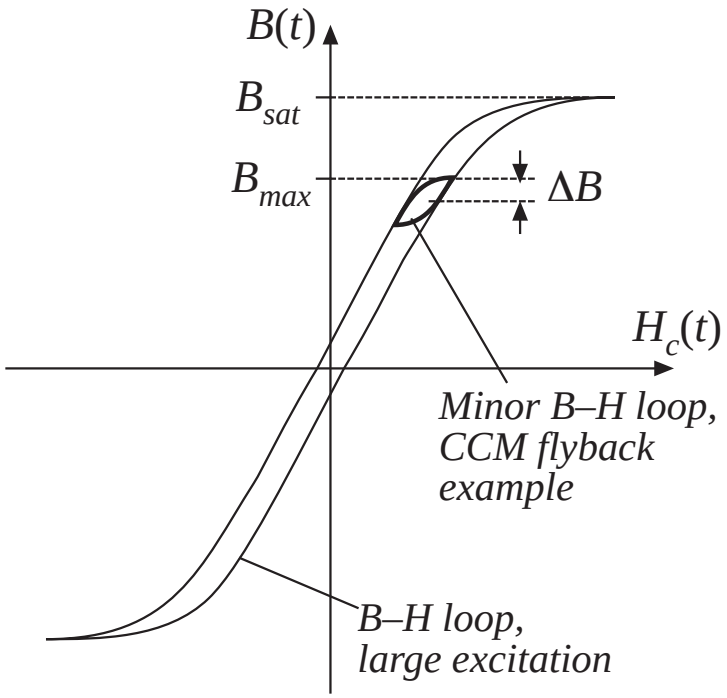
$$\alpha_2 = \frac{n_2 I_2}{n_1 I_{tot}} = \frac{\left(9\right)\left(6.5\text{ A}\right)}{\left(59\right)\left(1.77\text{ A}\right)} = 0.55$$

$$A_{W1} \leq \frac{\alpha_1 K_u W_A}{n_1} = 1.09 \cdot 10^{-3}\text{ cm}^2 \quad \text{— use \#28 AWG}$$

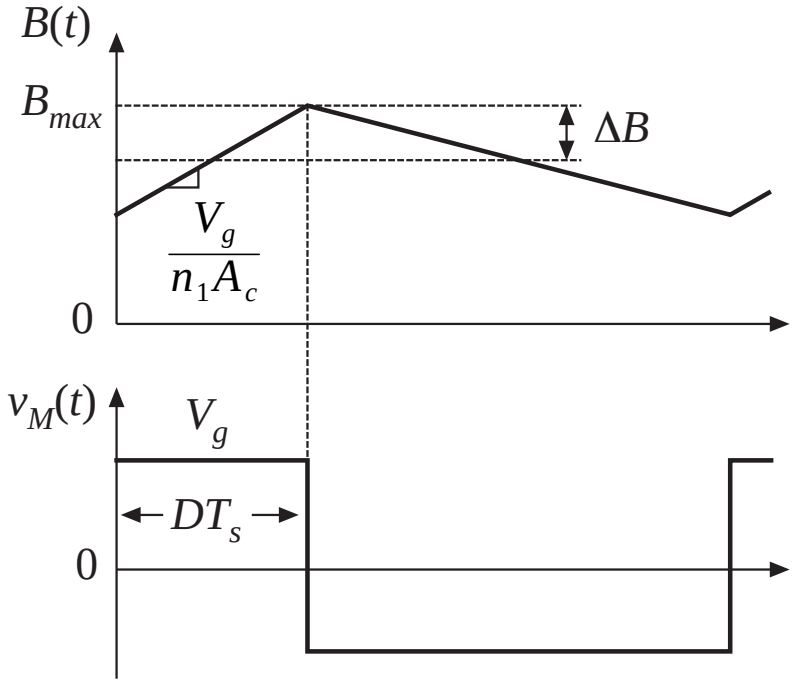
$$A_{W2} \leq \frac{\alpha_2 K_u W_A}{n_2} = 8.88 \cdot 10^{-3}\text{ cm}^2 \quad \text{— use \#19 AWG}$$

Core loss
CCM flyback example

B-H loop for this application:



The relevant waveforms:



$B(t)$ vs. applied voltage, from Faraday's law:

$$\frac{dB(t)}{dt} = \frac{v_M(t)}{n_1 A_c}$$

For the first subinterval:

$$\frac{dB(t)}{dt} = \frac{V_g}{n_1 A_c}$$

Calculation of ac flux density and core loss

Solve for ΔB:

$$\Delta B = \left(\frac{V_g}{n_1 A_c} \right) \left(D T_s \right)$$

Plug in values for flyback example:

$$\Delta B = \frac{\left(200 \text{ V}\right)\left(0.4\right)\left(6.67 \text{ } \mu\text{s}\right)}{2\left(59\right)\left(1.09 \text{ cm}^2\right)} 10^4$$

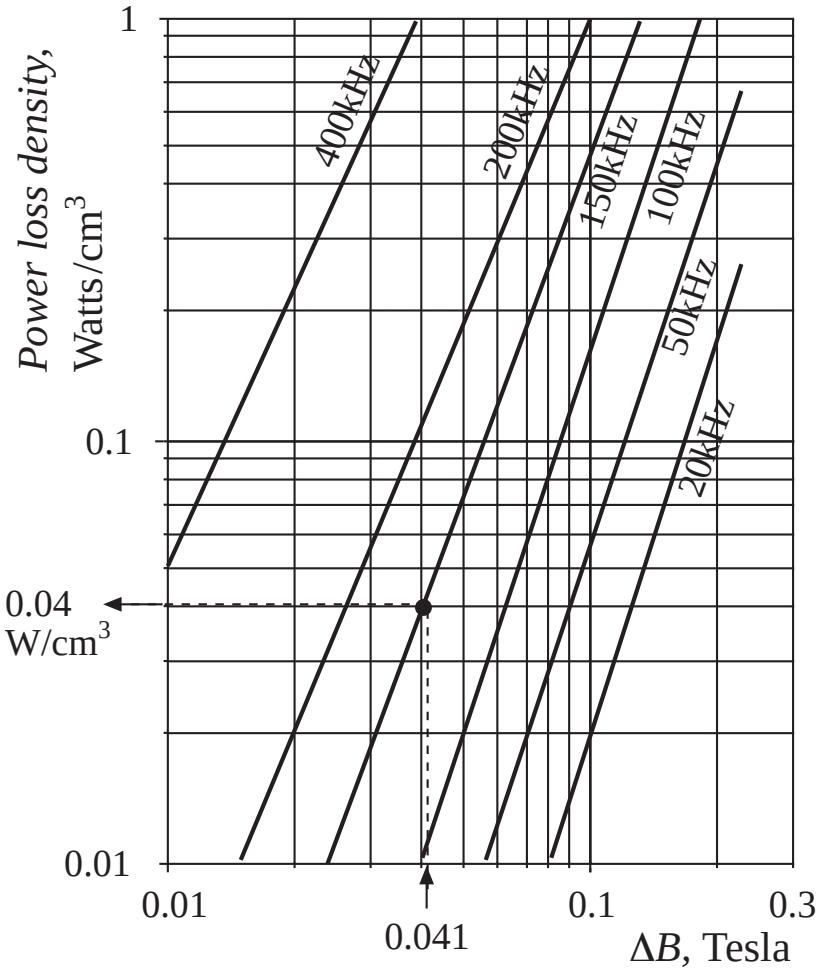
$$= 0.041 \text{ T}$$

From manufacturer's plot of core loss (at left), the power loss density is 0.04 W/cm^3. Hence core loss is

$$P_{fe} = \left(0.04 \text{ W/cm}^3\right)\left(A_c \ell_m\right)$$

$$= \left(0.04 \text{ W/cm}^3\right)\left(1.09 \text{ cm}^2\right)\left(5.77 \text{ cm}\right)$$

$$= 0.25 \text{ W}$$



Comparison of core and copper loss

- Copper loss is 1.5 W
  - does not include proximity losses, which could substantially increase total copper loss
- Core loss is 0.25 W
  - Core loss is small because ripple and ΔB are small
  - It is not a bad approximation to ignore core losses for ferrite in CCM filter inductors
  - Could consider use of a less expensive core material having higher core loss
  - Neglecting core loss is a reasonable approximation for this application
- Design is dominated by copper loss
  - The dominant constraint on flux density is saturation of the core, rather than core loss

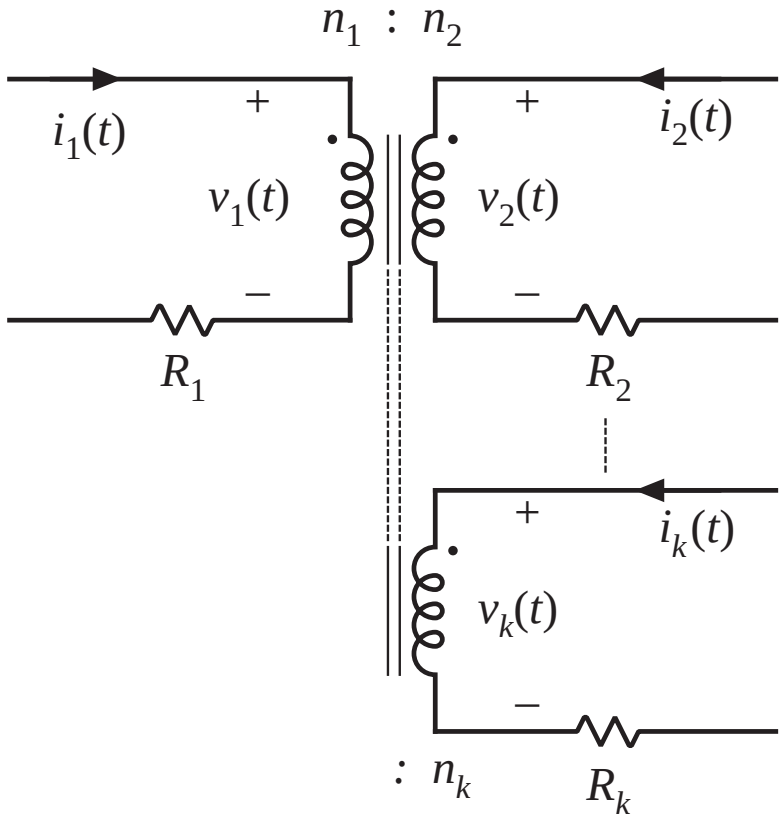
14.5 Summary of key points

1. A variety of magnetic devices are commonly used in switching converters. These devices differ in their core flux density variations, as well as in the magnitudes of the ac winding currents. When the flux density variations are small, core loss can be neglected. Alternatively, a low-frequency material can be used, having higher saturation flux density.
2. The core geometrical constant K_g is a measure of the magnetic size of a core, for applications in which copper loss is dominant. In the K_g design method, flux density and total copper loss are specified.

Chapter 15 Transformer Design

Some more advanced design issues, not considered in previous chapter:

- Inclusion of core loss
- Selection of operating flux density to optimize total loss
- Multiple winding design: as in the coupled-inductor case, allocate the available window area among several windings
- A transformer design procedure
- How switching frequency affects transformer size



Chapter 15 Transformer Design

15.1 Transformer Design:
Basic Constraints

Core loss

$$P_{fe} = K_{fe}(\Delta B)^{\beta} A_c \ell_m$$

Typical value of β for ferrite materials: 2.6 or 2.7

ΔB is the peak value of the ac component of $B(t)$, *i.e.*, the peak ac flux density

So increasing ΔB causes core loss to increase rapidly

This is the first constraint

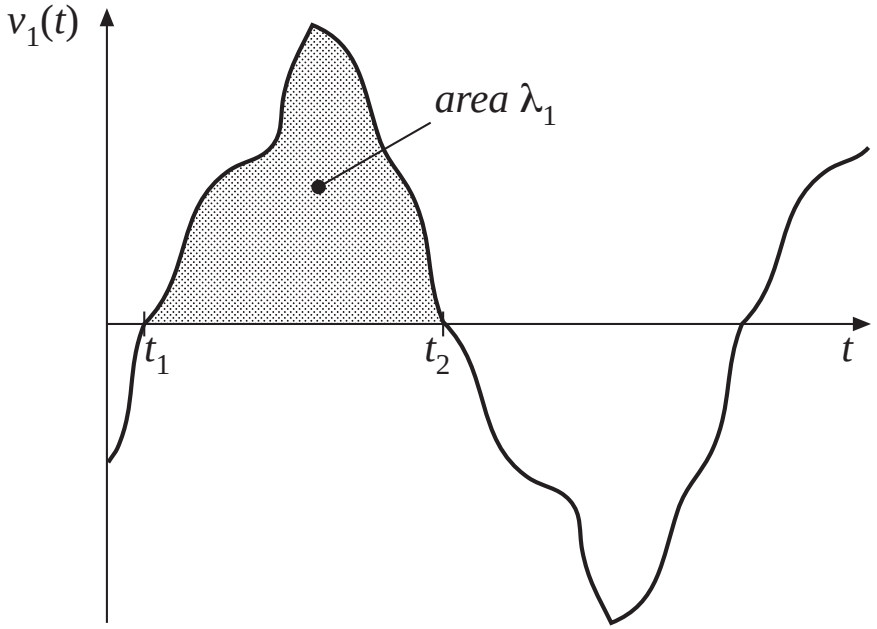
Flux density
Constraint #2

Flux density $B(t)$ is related to the applied winding voltage according to Faraday's Law. Denote the volt-seconds applied to the primary winding during the positive portion of $v_1(t)$ as λ_1:

$$\lambda_1 = \int_{t_1}^{t_2} v_1(t)\,dt$$

This causes the flux to change from its negative peak to its positive peak. From Faraday's law, the peak value of the ac component of flux density is

$$\Delta B = \frac{\lambda_1}{2 n_1 A_c}$$



To attain a given flux density, the primary turns should be chosen according to

$$n_1 = \frac{\lambda_1}{2 \Delta B A_c}$$

Copper loss
Constraint #3

- Allocate window area between windings in optimum manner, as described in previous section
- Total copper loss is then equal to

$$P_{cu} = \frac{\rho (MLT) n_1^2 I_{tot}^2}{W_A K_u}$$

with

$$I_{tot} = \sum_{j=1}^{k} \frac{n_j}{n_1} I_j$$

Eliminate n_1, using result of previous slide:

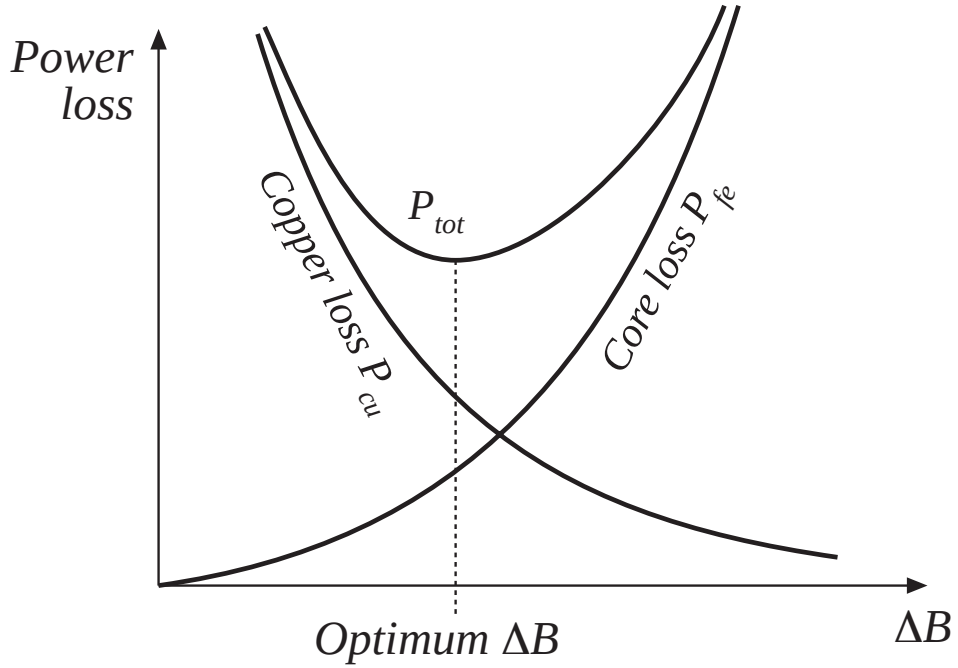
$$P_{cu} = \left(\frac{\rho \lambda_1^2 I_{tot}^2}{4 K_u} \right) \left(\frac{(MLT)}{W_A A_c^2} \right) \left(\frac{1}{\Delta B} \right)^2$$

Note that copper loss decreases rapidly as ΔB is increased

Total power loss

4. $P_{tot} = P_{cu} + P_{fe}$

There is a value of ΔB that minimizes the total power loss



$$P_{tot} = P_{fe} + P_{cu}$$

$$P_{fe} = K_{fe}(\Delta B)^{\beta} A_c \ell_m$$

$$P_{cu} = \left(\frac{\rho \lambda_1^2 I_{tot}^2}{4K_u} \right) \left(\frac{(MLT)}{W_A A_c^2} \right) \left(\frac{1}{\Delta B} \right)^2$$

5. Find optimum flux density ΔB

Given that

$$P_{tot} = P_{fe} + P_{cu}$$

Then, at the ΔB that minimizes P_{tot}, we can write

$$\frac{dP_{tot}}{d(\Delta B)} = \frac{dP_{fe}}{d(\Delta B)} + \frac{dP_{cu}}{d(\Delta B)} = 0$$

Note: optimum does not necessarily occur where $P_{fe} = P_{cu}$. Rather, it occurs where

$$\frac{dP_{fe}}{d(\Delta B)} = -\frac{dP_{cu}}{d(\Delta B)}$$

Take derivatives of core and copper loss

$$P_{fe} = K_{fe}(\Delta B)^{\beta} A_c \ell_m \qquad P_{cu} = \left(\frac{\rho \lambda_1^2 I_{tot}^2}{4K_u}\right)\left(\frac{(MLT)}{W_A A_c^2}\right)\left(\frac{1}{\Delta B}\right)^2$$

$$\frac{dP_{fe}}{d(\Delta B)} = \beta K_{fe}(\Delta B)^{(\beta-1)} A_c \ell_m \qquad \frac{dP_{cu}}{d(\Delta B)} = -2\left(\frac{\rho \lambda_1^2 I_{tot}^2}{4K_u}\right)\left(\frac{(MLT)}{W_A A_c^2}\right)(\Delta B)^{-3}$$

Now, substitute into $\frac{dP_{fe}}{d(\Delta B)} = -\frac{dP_{cu}}{d(\Delta B)}$ and solve for ΔB:

$$\Delta B = \left[\frac{\rho \lambda_1^2 I_{tot}^2}{2K_u}\ \frac{(MLT)}{W_A A_c^3 \ell_m}\ \frac{1}{\beta K_{fe}}\right]^{\left(\frac{1}{\beta+2}\right)}$$

Optimum ΔB for a given core and application

Total loss

Substitute optimum ΔB into expressions for P_{cu} and P_{fe}. The total loss is:

$$P_{tot} = \left[A_c \ell_m K_{fe}\right]^{\left(\frac{2}{\beta+2}\right)} \left[\frac{\rho \lambda_1^2 I_{tot}^2}{4K_u} \frac{(MLT)}{W_A A_c^2}\right]^{\left(\frac{\beta}{\beta+2}\right)} \left[\left(\frac{\beta}{2}\right)^{-\left(\frac{\beta}{\beta+2}\right)} + \left(\frac{\beta}{2}\right)^{\left(\frac{2}{\beta+2}\right)}\right]$$

Rearrange as follows:

$$\frac{W_A \left(A_c\right)^{\left(2(\beta-1)/\beta\right)}}{(MLT)\ell_m^{\left(2/\beta\right)}} \left[\left(\frac{\beta}{2}\right)^{-\left(\frac{\beta}{\beta+2}\right)} + \left(\frac{\beta}{2}\right)^{\left(\frac{2}{\beta+2}\right)}\right]^{-\left(\frac{\beta+2}{\beta}\right)} = \frac{\rho \lambda_1^2 I_{tot}^2 K_{fe}^{\left(2/\beta\right)}}{4K_u \left(P_{tot}\right)^{\left((\beta+2)/\beta\right)}}$$

Left side: terms depend on core geometry

Right side: terms depend on specifications of the application

The core geometrical constant K_{gfe}

Define $$K_{gfe} = \frac{W_A \left(A_c \right)^{\left(2(\beta - 1)/\beta \right)}}{(MLT) \ell_m^{\left(2/\beta \right)}} \left[\left(\frac{\beta}{2} \right)^{-\left(\frac{\beta}{\beta + 2} \right)} + \left(\frac{\beta}{2} \right)^{\left(\frac{2}{\beta + 2} \right)} \right]^{-\left(\frac{\beta + 2}{\beta} \right)}$$

Design procedure: select a core that satisfies

$$K_{gfe} \geq \frac{\rho \lambda_1^2 I_{tot}^2 K_{fe}^{\left(2/\beta \right)}}{4 K_u \left(P_{tot} \right)^{\left((\beta + 2)/\beta \right)}}$$

Appendix D lists the values of K_{gfe} for common ferrite cores

K_{gfe} is similar to the K_g geometrical constant used in Chapter 14:

- K_g is used when B_{max} is specified
- K_{gfe} is used when ΔB is to be chosen to minimize total loss

15.2 Step-by-step transformer design procedure

The following quantities are specified, using the units noted:

Wire effective resistivity	ρ	(Ω-cm)
Total rms winding current, ref to pri	I_{tot}	(A)
Desired turns ratios	n_2/n_1, n_3/n_1, etc.	
Applied pri volt-sec	λ_1	(V-sec)
Allowed total power dissipation	P_{tot}	(W)
Winding fill factor	K_u	
Core loss exponent	β	
Core loss coefficient	K_{fe}	(W/cm^3T^β)

Other quantities and their dimensions:

Core cross-sectional area	A_c	(cm^2)
Core window area	W_A	(cm^2)
Mean length per turn	MLT	(cm)
Magnetic path length	ℓ_e	(cm)
Wire areas	A_{w1}, …	(cm^2)
Peak ac flux density	ΔB	(T)

Procedure

1. Determine core size

$$K_{gfe} \geq \frac{\rho \lambda_1^2 I_{tot}^2 K_{fe}^{(2/\beta)}}{4 K_u \left(P_{tot}\right)^{\left((\beta+2)/\beta\right)}} 10^8$$

Select a core from Appendix D that satisfies this inequality.

It may be possible to reduce the core size by choosing a core material that has lower loss, i.e., lower K_{fe}.

2. Evaluate peak ac flux density

$$\Delta B = \left[10^8 \; \frac{\rho \lambda_1^2 I_{tot}^2}{2K_u} \; \frac{(MLT)}{W_A A_c^3 \ell_m} \; \frac{1}{\beta K_{fe}} \right]^{\left(\frac{1}{\beta + 2}\right)}$$

At this point, one should check whether the saturation flux density is exceeded. If the core operates with a flux dc bias B_{dc}, then $\Delta B + B_{dc}$ should be less than the saturation flux density B_{sat}.

If the core will saturate, then there are two choices:

- Specify ΔB using the K_g method of Chapter 14, or
- Choose a core material having greater core loss, then repeat steps 1 and 2

3. and 4. Evaluate turns

Primary turns:

$$n_1 = \frac{\lambda_1}{2\Delta B A_c} \; 10^4$$

Choose secondary turns according to desired turns ratios:

$$n_2 = n_1 \left(\frac{n_2}{n_1} \right)$$

$$n_3 = n_1 \left(\frac{n_3}{n_1} \right)$$

$$\vdots$$

5. and 6. Choose wire sizes

Fraction of window area assigned to each winding:

$$\alpha_1 = \frac{n_1 I_1}{n_1 I_{tot}}$$

$$\alpha_2 = \frac{n_2 I_2}{n_1 I_{tot}}$$

$$\vdots$$

$$\alpha_k = \frac{n_k I_k}{n_1 I_{tot}}$$

Choose wire sizes according to:

$$A_{w1} \le \frac{\alpha_1 K_u W_A}{n_1}$$

$$A_{w2} \le \frac{\alpha_2 K_u W_A}{n_2}$$

$$\vdots$$

Check: computed transformer model

Predicted magnetizing inductance, referred to primary:

$$L_M = \frac{\mu n_1^2 A_c}{\ell_m}$$

Peak magnetizing current:

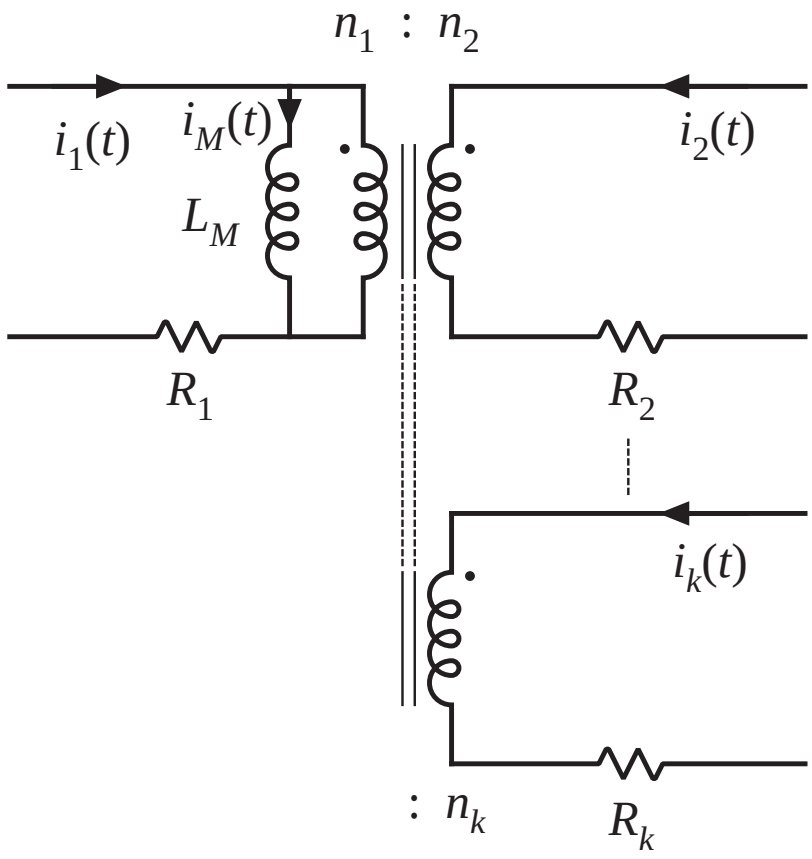
$$i_{M,\,pk} = \frac{\lambda_1}{2L_M}$$

Predicted winding resistances:

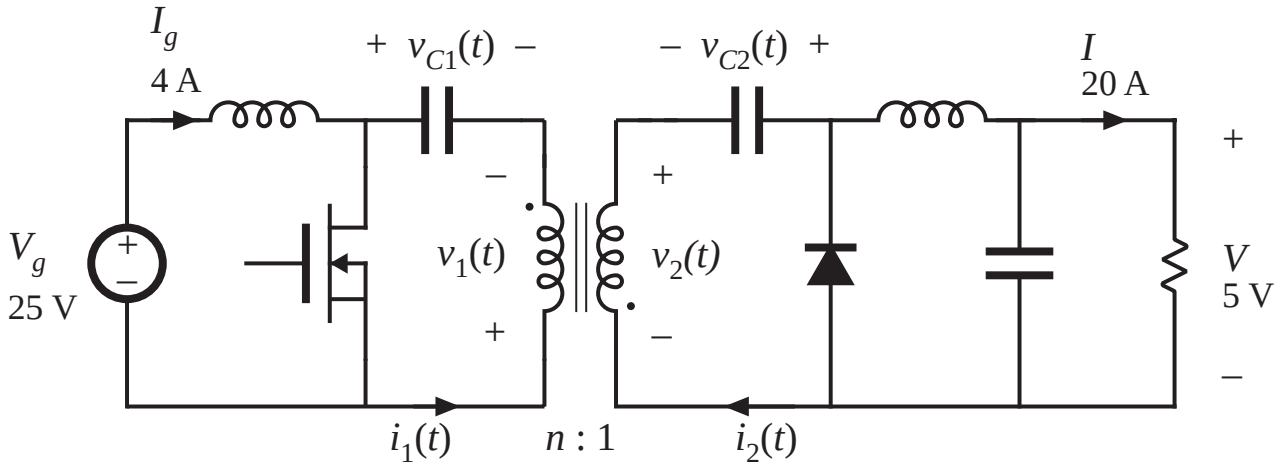
$$R_1 = \frac{\rho n_1 (MLT)}{A_{w1}}$$

$$R_2 = \frac{\rho n_2 (MLT)}{A_{w2}}$$

$$\vdots$$



15.4.1 Example 1: Single-output isolated Cuk converter



100 W

$f_s = 200$ kHz

$D = 0.5$

$n = 5$

$K_u = 0.5$

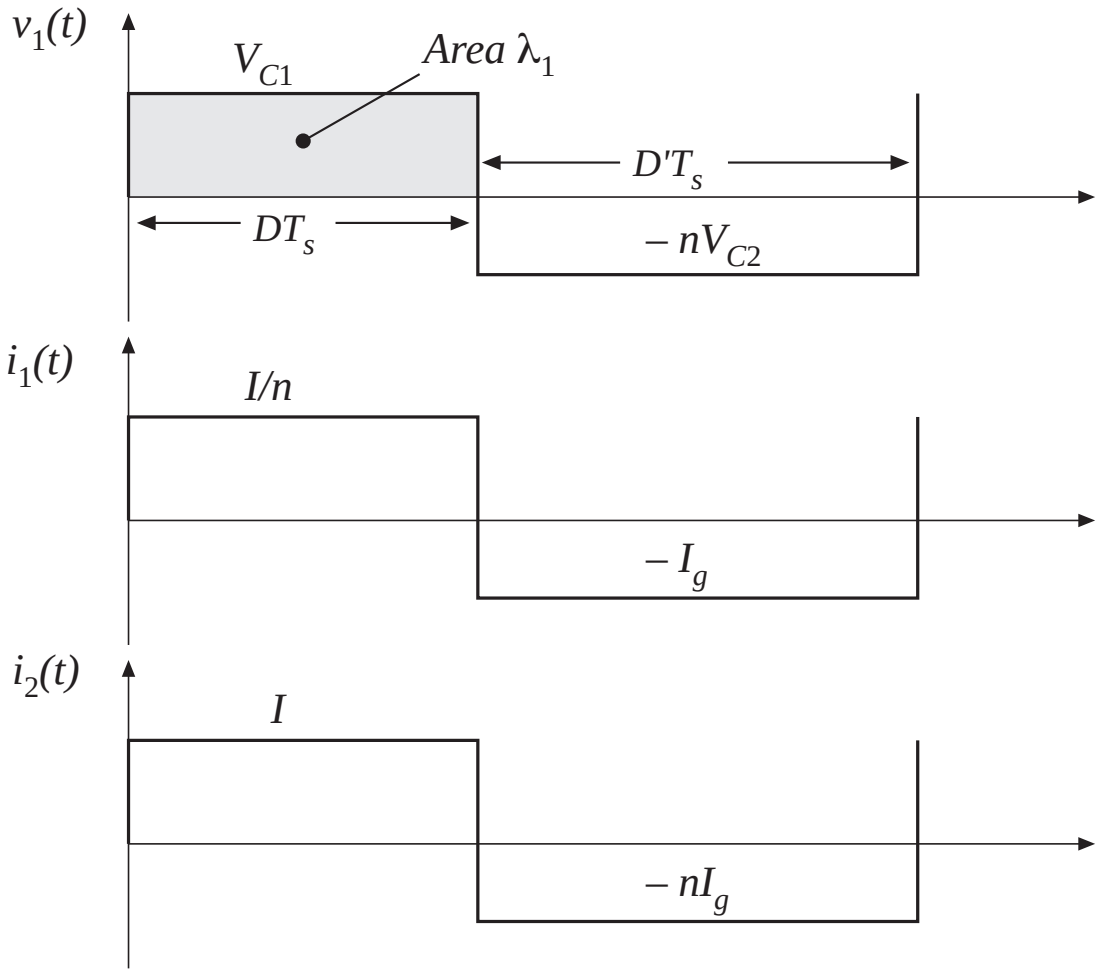
Allow $P_{tot} = 0.25$ W

Use a ferrite pot core, with Magnetics Inc. P material. Loss parameters at 200 kHz are

$K_{fe} = 24.7$

$\beta = 2.6$

Waveforms



Applied primary volt-seconds:

$$\lambda_1 = DT_s V_{c1} = (0.5)\ (5\ \mu\text{sec}\ )\ (25\ \text{V})$$
$$= 62.5\ \text{V–}\mu\text{sec}$$

Applied primary rms current:

$$I_1 = \sqrt{D\left(\frac{I}{n}\right)^2 + D'\left(I_g\right)^2} = 4\ \text{A}$$

Applied secondary rms current:

$$I_2 = nI_1 = 20\ \text{A}$$

Total rms winding current:

$$I_{tot} = I_1 + \frac{1}{n} I_2 = 8\ \text{A}$$

Choose core size

$$K_{gfe} \geq \frac{(1.724 \cdot 10^{-6})(62.5 \cdot 10^{-6})^2 (8)^2 (24.7)^{(2/2.6)}}{4\ (0.5)\ (0.25)^{(4.6/2.6)}}\ 10^8$$

$$= 0.00295$$

Pot core data of Appendix D lists 2213 pot core with

$$K_{gfe} = 0.0049$$

Next smaller pot core is not large enough.

Evaluate peak ac flux density

$$\Delta B = \left[10^8 \frac{(1.724 \cdot 10^{-6})(62.5 \cdot 10^{-6})^2 (8)^2}{2\,(0.5)} \frac{(4.42)}{(0.297)(0.635)^3(3.15)} \frac{1}{(2.6)(24.7)} \right]^{(1/4.6)}$$

$$= 0.0858 \text{ Tesla}$$

This is much less than the saturation flux density of approximately 0.35 T. Values of ΔB in the vicinity of 0.1 T are typical for ferrite designs that operate at frequencies in the vicinity of 100 kHz.

Evaluate turns

$$n_1 = 10^4 \frac{(62.5 \cdot 10^{-6})}{2(0.0858)(0.635)}$$

$$= 5.74 \text{ turns}$$

$$n_2 = \frac{n_1}{n} = 1.15 \text{ turns}$$

In practice, we might select

$n_1 = 5$ and $n_2 = 1$

This would lead to a slightly higher flux density and slightly higher loss.

Determine wire sizes

Fraction of window area allocated to each winding:

$$\alpha_1 = \frac{\left(4\text{ A}\right)}{\left(8\text{ A}\right)} = 0.5$$

$$\alpha_2 = \frac{\left(\frac{1}{5}\right)\left(20\text{ A}\right)}{\left(8\text{ A}\right)} = 0.5$$

(Since, in this example, the ratio of winding rms currents is equal to the turns ratio, equal areas are allocated to each winding)

Wire areas:

$$A_{w1} = \frac{(0.5)(0.5)(0.297)}{(5)} = 14.8{\cdot}10^{-3}\text{ cm}^2$$

From wire table, Appendix D:

AWG #16

$$A_{w2} = \frac{(0.5)(0.5)(0.297)}{(1)} = 74.2{\cdot}10^{-3}\text{ cm}^2$$

AWG #9

Wire sizes: discussion

Primary

5 turns #16 AWG

Secondary

1 turn #9 AWG

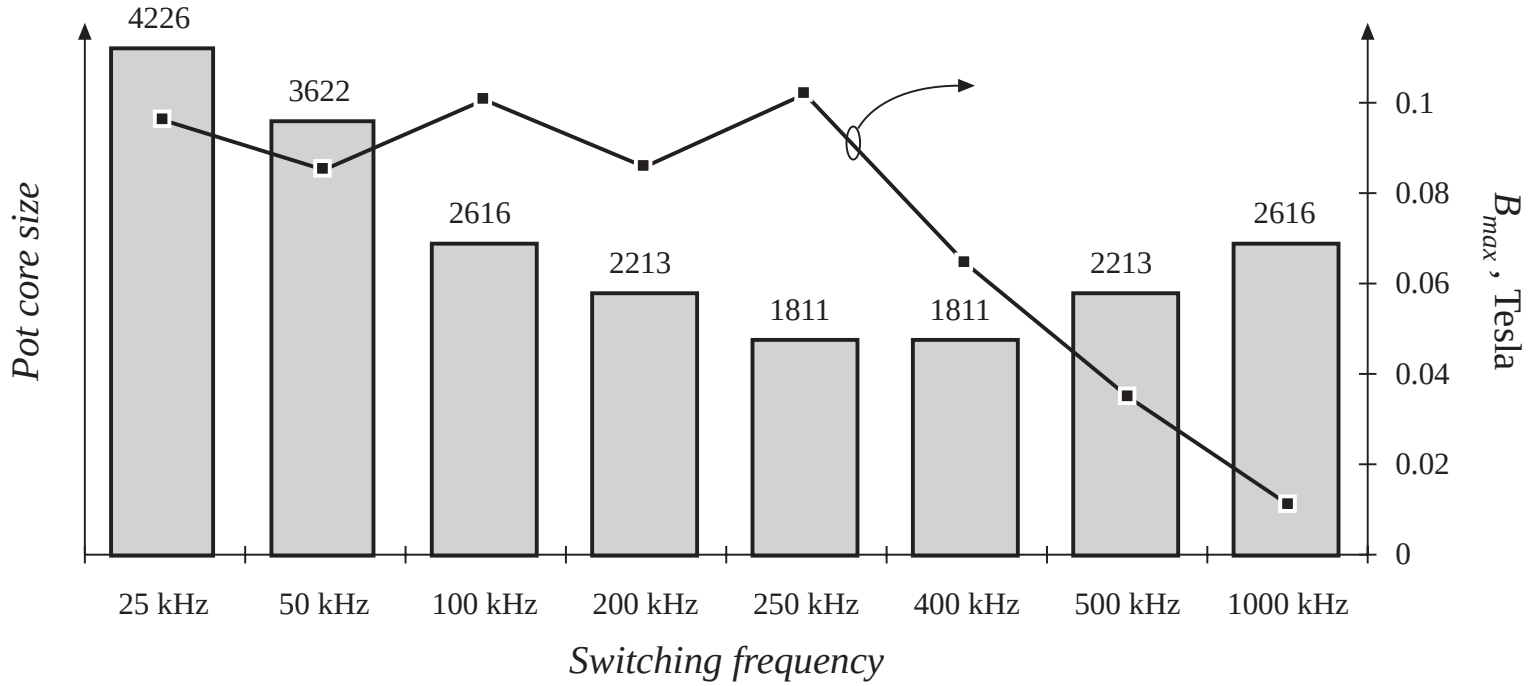
- Very large conductors!
- One turn of #9 AWG is not a practical solution

Some alternatives

- Use foil windings
- Use Litz wire or parallel strands of wire

Effect of switching frequency on transformer size

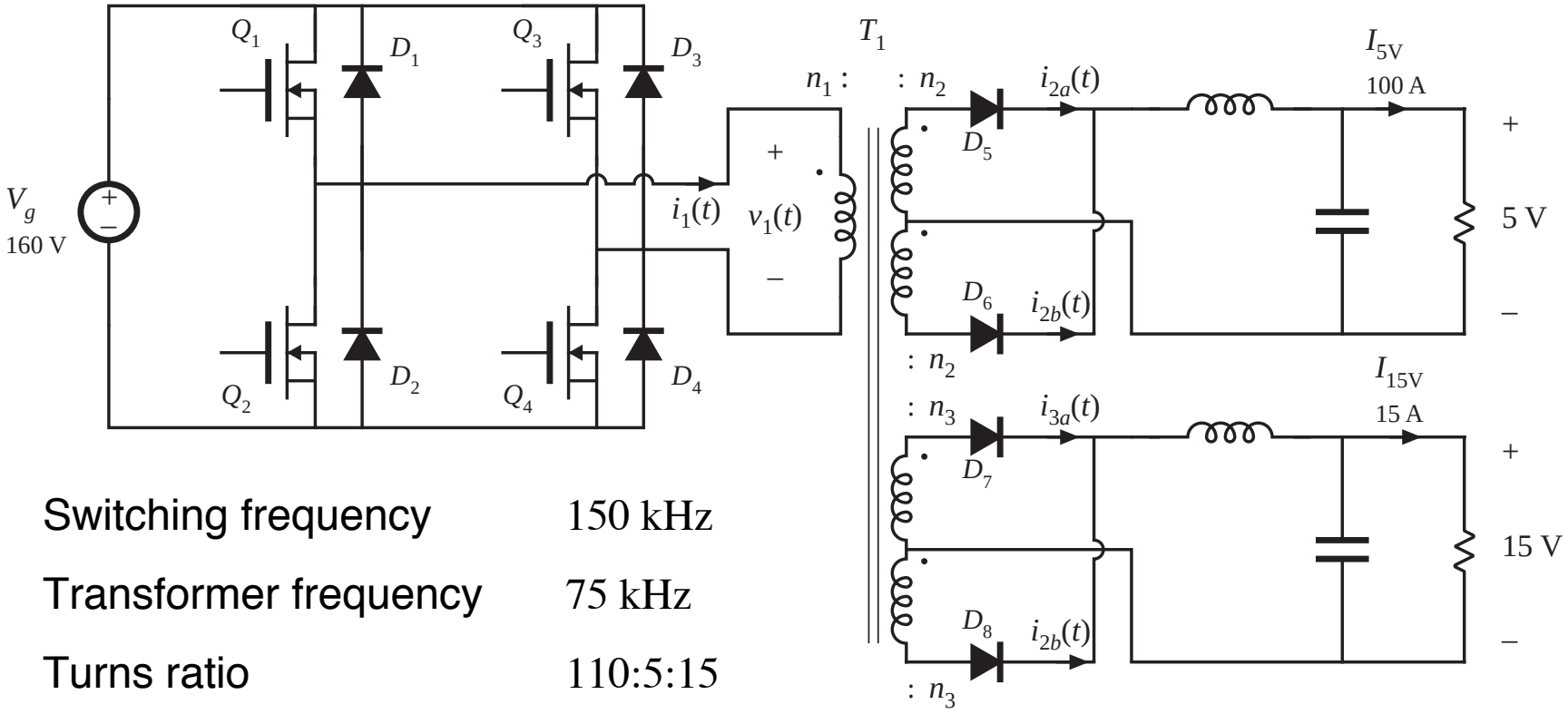
for this P-material Cuk converter example



- As switching frequency is increased from 25 kHz to 250 kHz, core size is dramatically reduced
- As switching frequency is increased from 400 kHz to 1 MHz, core size increases

15.3.2 Example 2

Multiple-Output Full-Bridge Buck Converter



Switching frequency	150 kHz
Transformer frequency	75 kHz
Turns ratio	110:5:15
Optimize transformer at	D = 0.75

Other transformer design details

Use Magnetics, Inc. ferrite P material. Loss parameters at 75 kHz:

$K_{fe} = 7.6$ W/T$^{\beta}$cm^3

$\beta = 2.6$

Use E-E core shape

Assume fill factor of

$K_u = 0.25$ (reduced fill factor accounts for added insulation required in multiple-output off-line application)

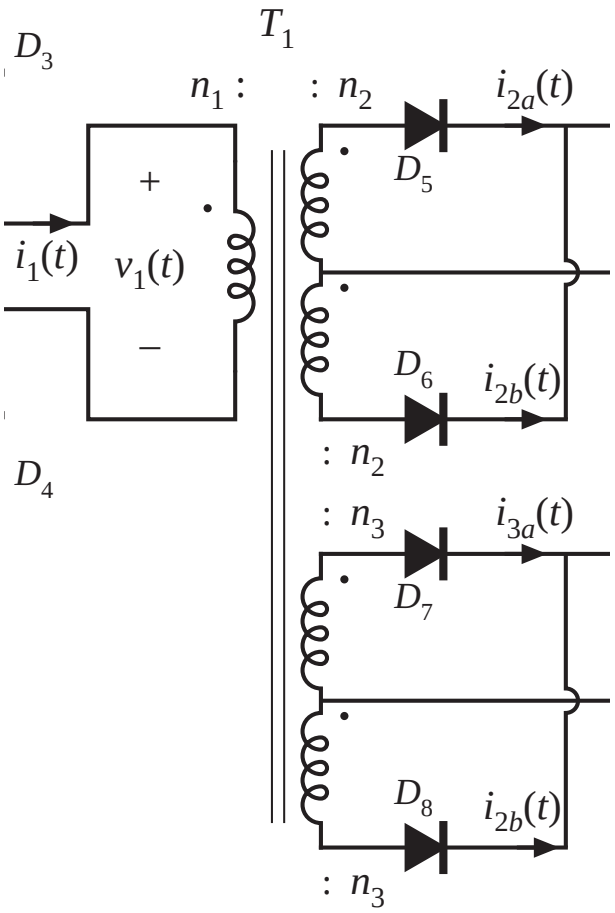
Allow transformer total power loss of

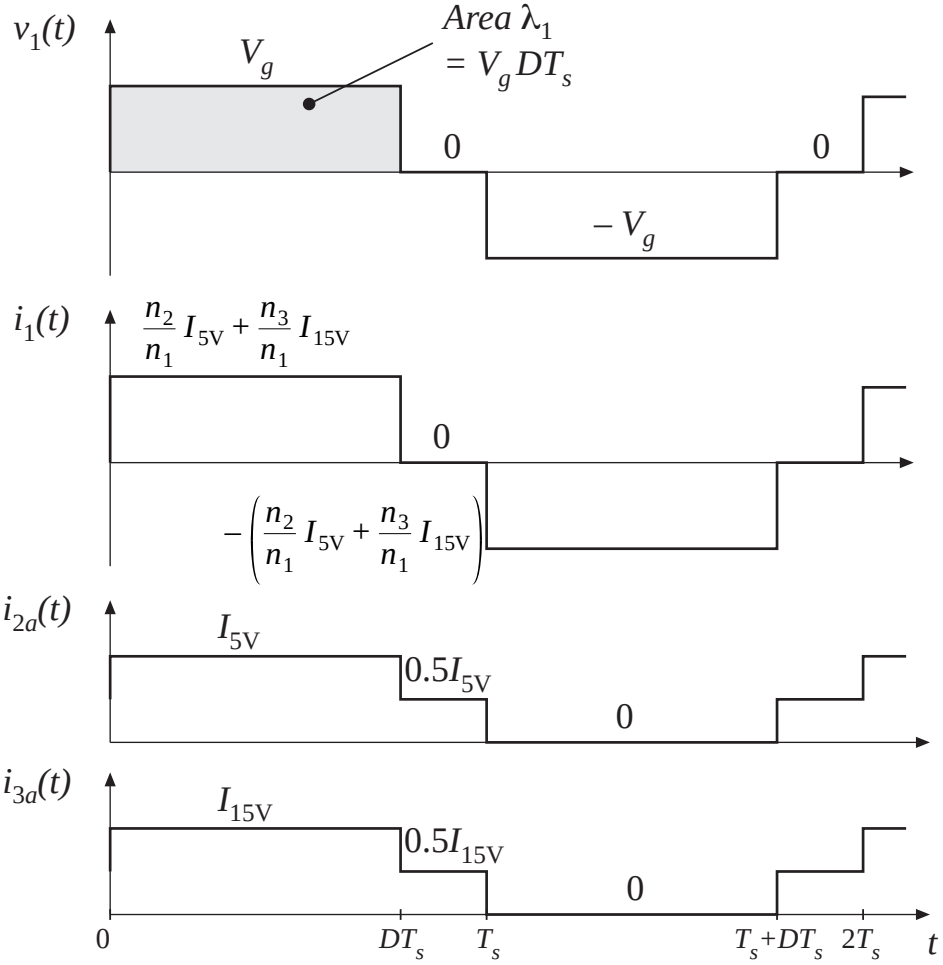
$P_{tot} = 4$ W (approximately 0.5% of total output power)

Use copper wire, with

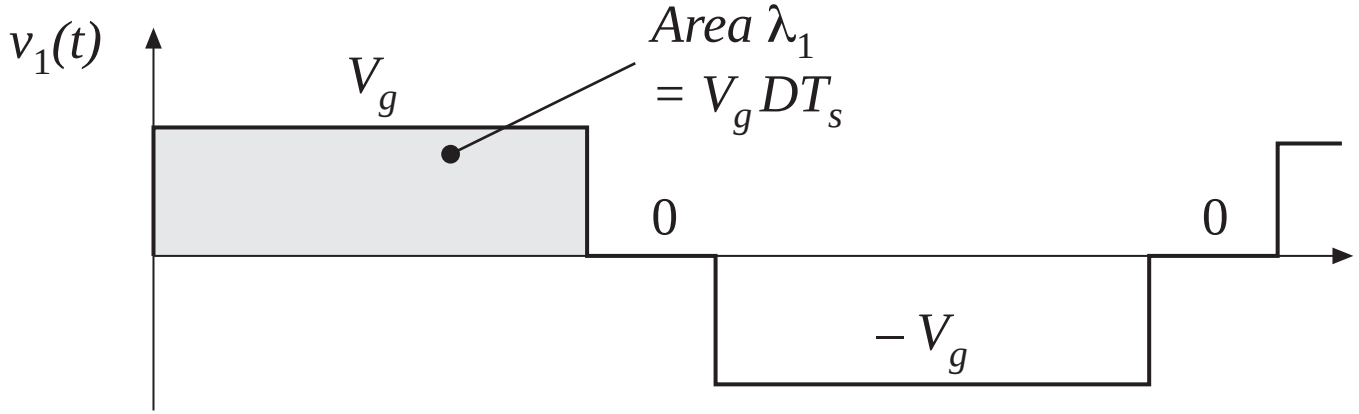
$\rho = 1.724 \cdot 10^{-6}$ Ω-cm

Applied transformer waveforms



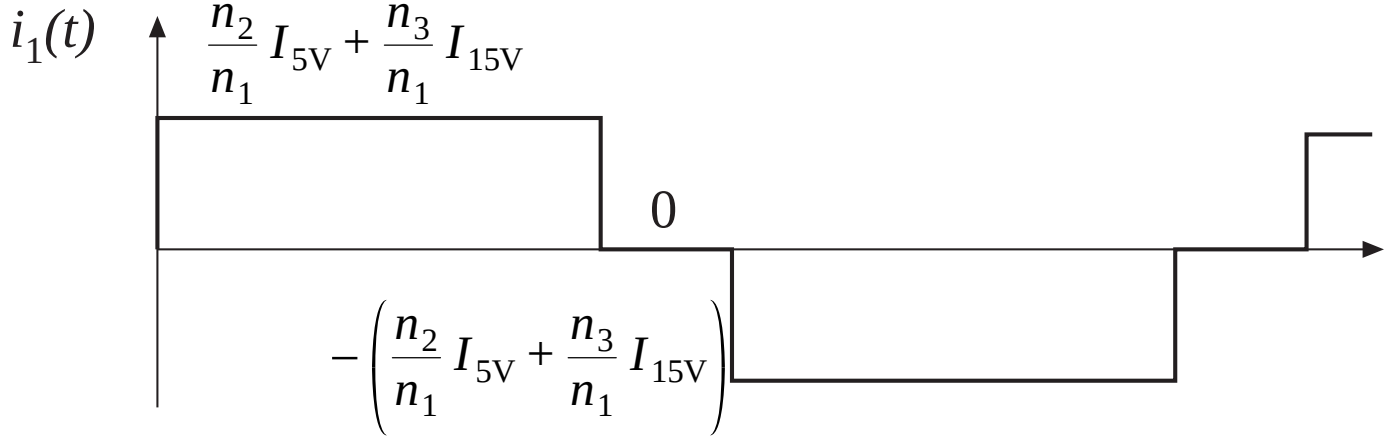


Applied primary volt-seconds



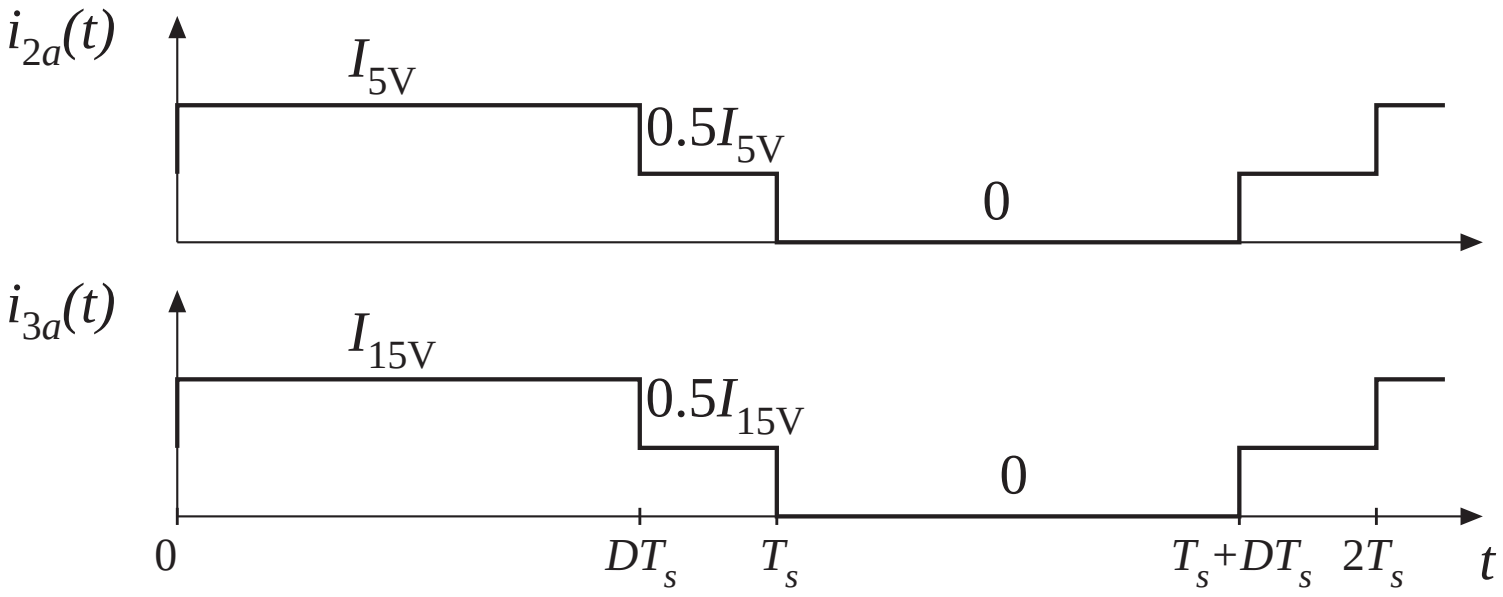
$$\lambda_1 = DT_s V_g = (0.75)\,(6.67\ \mu\text{sec})\,(160\ \text{V}) = 800\ \text{V–}\mu\text{sec}$$

Applied primary rms current



$$I_1 = \left(\frac{n_2}{n_1} I_{5V} + \frac{n_3}{n_1} I_{15V} \right) \sqrt{D} = 5.7 \text{ A}$$

Applied rms current, secondary windings



$$I_2 = \frac{1}{2} I_{5V} \sqrt{1 + D} = 66.1 \text{ A}$$

$$I_3 = \frac{1}{2} I_{15V} \sqrt{1 + D} = 9.9 \text{ A}$$

I_{tot}

RMS currents, summed over all windings and referred to primary

$$I_{tot} = \sum_{\substack{all\ 5 \\ windings}} \frac{n_j}{n_1} I_j = I_1 + 2\,\frac{n_2}{n_1} I_2 + 2\,\frac{n_3}{n_1} I_3$$

$$= \left(5.7\text{ A}\right) + \frac{5}{110}\left(66.1\text{ A}\right) + \frac{15}{110}\left(9.9\text{ A}\right)$$

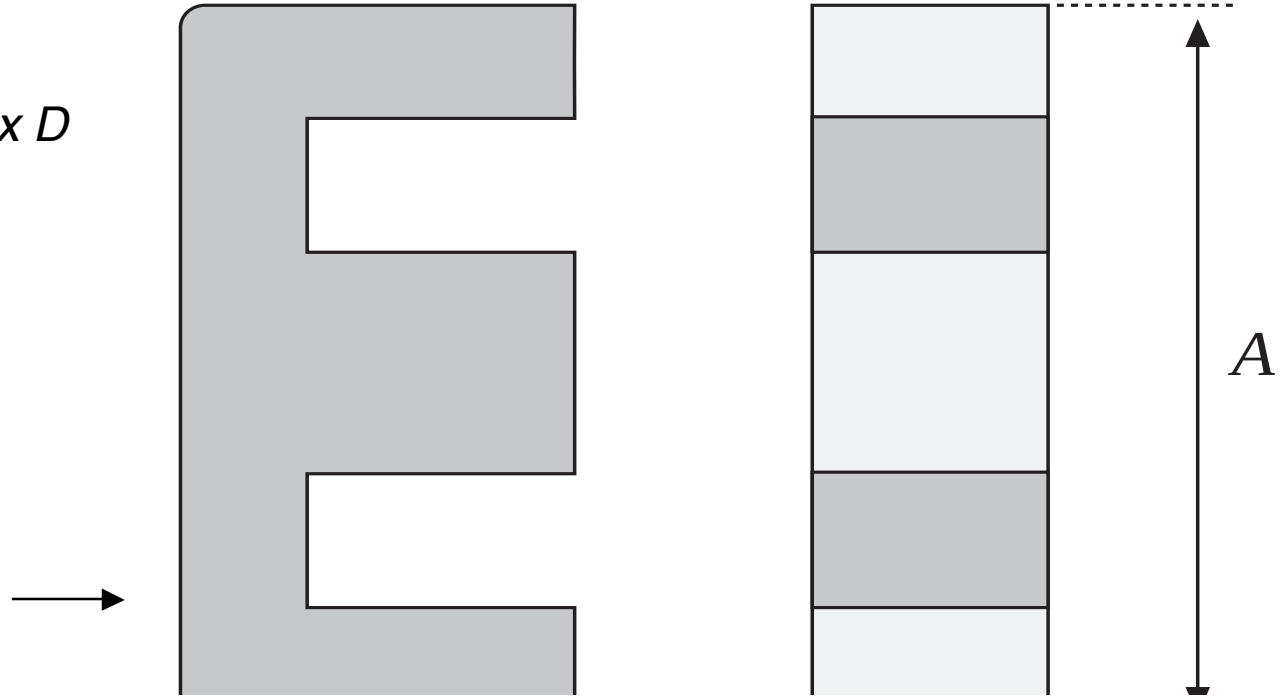
$$= 14.4\text{ A}$$

Select core size

$$K_{gfe} \geq \frac{(1.724 \cdot 10^{-6})(800 \cdot 10^{-6})^2 (14.4)^2 (7.6)^{(2/2.6)}}{4\ (0.25)\ (4)^{(4.6/2.6)}}\ 10^8$$

$$= 0.00937$$

From Appendix D



Evaluate ac flux density ΔB

Eq. (15.20):

$$B_{max} = \left[10^8 \; \frac{\rho \lambda_1^2 I_{tot}^2}{2K_u} \; \frac{(MLT)}{W_A A_c^3 l_m} \; \frac{1}{\beta K_{fe}} \right]^{\left(\frac{1}{\beta + 2}\right)}$$

Plug in values:

$$\Delta B = \left[10^8 \; \frac{(1.724 \cdot 10^{-6})(800 \cdot 10^{-6})^2 (14.4)^2}{2(0.25)} \; \frac{(8.5)}{(1.1)(1.27)^3 (7.7)} \; \frac{1}{(2.6)(7.6)} \right]^{(1/4.6)}$$

$$= 0.23 \text{ Tesla}$$

This is less than the saturation flux density of approximately 0.35 T

Evaluate turns

Choose n_1 according to Eq. (15.21):

$$n_1 = \frac{\lambda_1}{2\Delta B A_c} \; 10^4$$

$$n_1 = 10^4 \frac{(800 \cdot 10^{-6})}{2(0.23)(1.27)}$$

$$= 13.7 \text{ turns}$$

Choose secondary turns according to desired turns ratios:

$$n_2 = \frac{5}{110} n_1 = 0.62 \text{ turns}$$

$$n_3 = \frac{15}{110} n_1 = 1.87 \text{ turns}$$

Rounding the number of turns

To obtain desired turns ratio of

110:5:15

we might round the actual turns to

22:1:3

Increased n_1 would lead to

- Less core loss
- More copper loss
- Increased total loss

Loss calculation
with rounded turns

With $n_1 = 22$, the flux density will be reduced to

$$\Delta B = \frac{(800 \cdot 10^{-6})}{2(22)(1.27)} 10^4 = 0.143 \text{ Tesla}$$

The resulting losses will be

$$P_{fe} = (7.6)(0.143)^{2.6}(1.27)(7.7) = 0.47 \text{ W}$$

$$P_{cu} = \frac{(1.724 \cdot 10^{-6})(800 \cdot 10^{-6})^2 (14.4)^2}{4\,(0.25)} \frac{(8.5)}{(1.1)(1.27)^2} \frac{1}{(0.143)^2} 10^8$$

$$= 5.4 \text{ W}$$

$$P_{tot} = P_{fe} + P_{cu} = 5.9 \text{ W}$$

Which exceeds design goal of 4 W by 50%. So use next larger core size: EE50.

Calculations with EE50

Repeat previous calculations for EE50 core size. Results:

$$\Delta B = 0.14 \text{ T}, n_1 = 12, P_{tot} = 2.3 \text{ W}$$

Again round n_1 to 22. Then

$$\Delta B = 0.08 \text{ T}, P_{cu} = 3.89 \text{ W}, P_{fe} = 0.23 \text{ W}, P_{tot} = 4.12 \text{ W}$$

Which is close enough to 4 W.

Wire sizes for EE50 design

Window allocations

$$\alpha_1 = \frac{I_1}{I_{tot}} = \frac{5.7}{14.4} = 0.396$$

$$\alpha_2 = \frac{n_2 I_2}{n_1 I_{tot}} = \frac{5}{110}\,\frac{66.1}{14.4} = 0.209$$

$$\alpha_3 = \frac{n_3 I_3}{n_1 I_{tot}} = \frac{15}{110}\,\frac{9.9}{14.4} = 0.094$$

Wire gauges

$$A_{w1} = \frac{\alpha_1 K_u W_A}{n_1} = \frac{(0.396)(0.25)(1.78)}{(22)} = 8.0 \cdot 10^{-3}\ \text{cm}^2$$

$$\Rightarrow \text{AWG \#19}$$

$$A_{w2} = \frac{\alpha_2 K_u W_A}{n_2} = \frac{(0.209)(0.25)(1.78)}{(1)} = 93.0 \cdot 10^{-3}\ \text{cm}^2$$

$$\Rightarrow \text{AWG \#8}$$

$$A_{w3} = \frac{\alpha_3 K_u W_A}{n_3} = \frac{(0.094)(0.25)(1.78)}{(3)} = 13.9 \cdot 10^{-3}\ \text{cm}^2$$

$$\Rightarrow \text{AWG \#16}$$

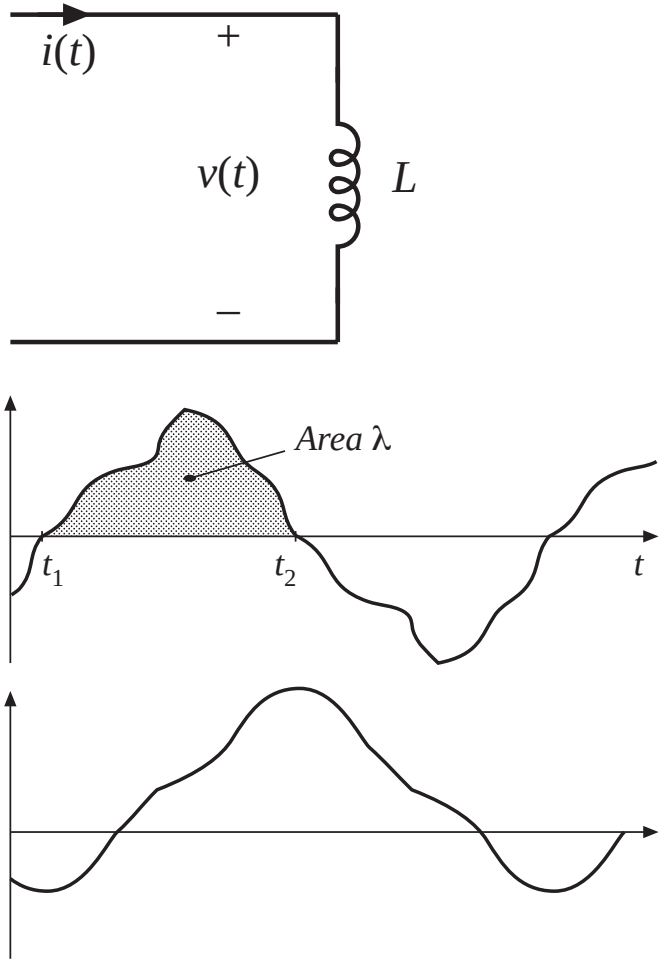
Might actually use foil or Litz wire for secondary windings

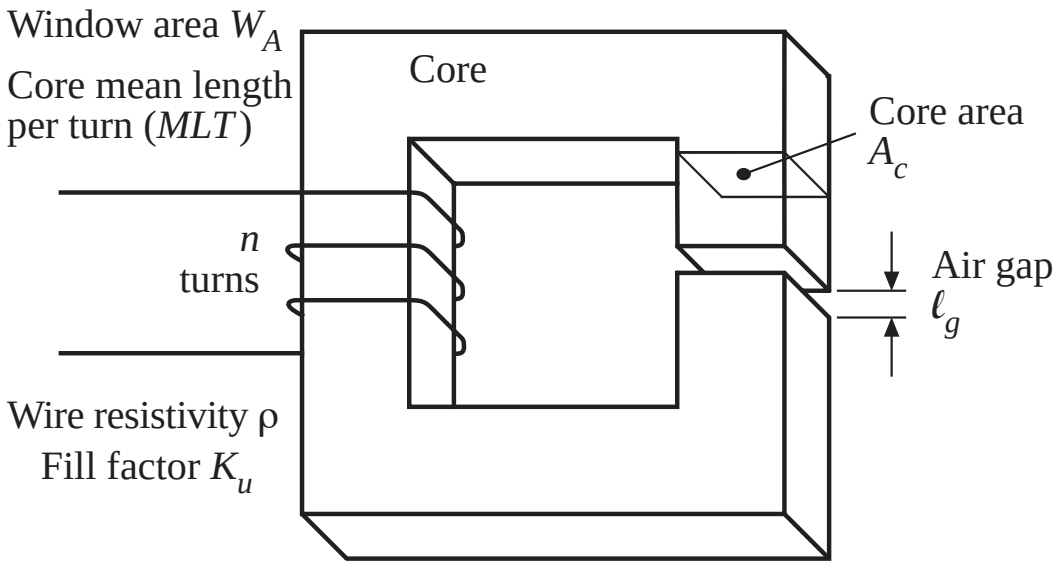
Discussion: Transformer design

- Process is iterative because of round-off of physical number of turns and, to a lesser extent, other quantities
- Effect of proximity loss
  - Not included in design process yet
  - Requires additional iterations
- Can modify procedure as follows:
  - After a design has been calculated, determine number of layers in each winding and then compute proximity loss
  - Alter effective resistivity of wire to compensate: define

    $\rho_{eff} = \rho \cdot P_{cu}/P_{dc}$ where P_{cu} is the total copper loss (including proximity effects) and P_{dc} is the copper loss predicted by the dc resistance.
  - Apply transformer design procedure using this effective wire resistivity, and compute proximity loss in the resulting design. Further iterations may be necessary if the specifications are not met.

15.4 AC Inductor Design





Design a single-winding inductor, having an air gap, accounting for core loss

(note that the previous design procedure of this chapter did not employ an air gap, and inductance was not a specification)

Outline of key equations

Obtain specified inductance:

$$L = \frac{\mu_0 A_c n^2}{\ell_g}$$

Relationship between applied volt-seconds and peak ac flux density:

$$\Delta B = \frac{\lambda}{2 n A_c}$$

Copper loss (using dc resistance):

$$P_{cu} = \frac{\rho n^2 (MLT)}{K_u W_A} I^2$$

Total loss is minimized when

$$\Delta B = \left[\frac{\rho \lambda^2 I^2}{2 K_u} \; \frac{(MLT)}{W_A A_c^3 \ell_m} \; \frac{1}{\beta K_{fe}} \right]^{\left(\frac{1}{\beta + 2}\right)}$$

Must select core that satisfies

$$K_{gfe} \geq \frac{\rho \lambda^2 I^2 K_{fe}^{(2/\beta)}}{2 K_u \left(P_{tot}\right)^{\left((\beta + 2)/\beta\right)}}$$

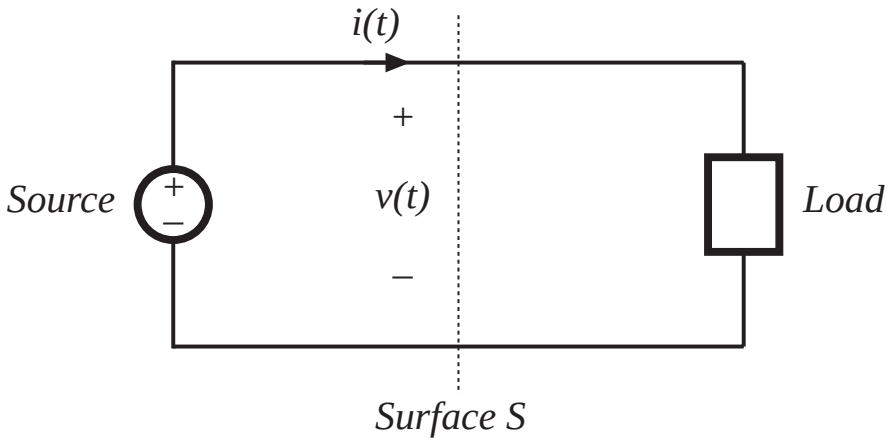
See Section 15.4.2 for step-by-step design equations

Part IV
Modern Rectifiers and Power System Harmonics

Chapter 16
Power And Harmonics in Nonsinusoidal Systems

16.1. Average power

Observe transmission of energy through surface S



Express voltage and current as Fourier series:

$$v(t) = V_0 + \sum_{n=1}^{\infty} V_n \cos\left(n\omega t - \varphi_n\right)$$

$$i(t) = I_0 + \sum_{n=1}^{\infty} I_n \cos\left(n\omega t - \theta_n\right)$$

relate energy transmission to harmonics

Energy transmittted to load, per cycle

$$W_{cycle} = \int_0^T v(t) i(t) dt$$

This is related to average power as follows:

$$P_{av} = \frac{W_{cycle}}{T} = \frac{1}{T} \int_0^T v(t) i(t) dt$$

Investigate influence of harmonics on average power: substitute Fourier series

$$P_{av} = \frac{1}{T} \int_0^T \left(V_0 + \sum_{n=1}^{\infty} V_n \cos\left(n\omega t - \varphi_n\right) \right) \left(I_0 + \sum_{n=1}^{\infty} I_n \cos\left(n\omega t - \theta_n\right) \right) dt$$

Evaluation of integral

Orthogonality of harmonics: Integrals of cross-product terms are zero

$$\int_0^T \left(V_n \cos\left(n\omega t - \varphi_n\right)\right)\left(I_m \cos\left(m\omega t - \theta_m\right)\right) dt = \begin{cases} 0 & \text{if } n \neq m \\ \frac{V_n I_n}{2} \cos\left(\varphi_n - \theta_n\right) & \text{if } n = m \end{cases}$$

Expression for average power becomes

$$P_{av} = V_0 I_0 + \sum_{n=1}^{\infty} \frac{V_n I_n}{2} \cos\left(\varphi_n - \theta_n\right)$$

So net energy is transmitted to the load only when the Fourier series of *v(t)* and *i(t)* contain terms at the same frequency. For example, if the voltage and current both contain third harmonic, then they lead to the average power

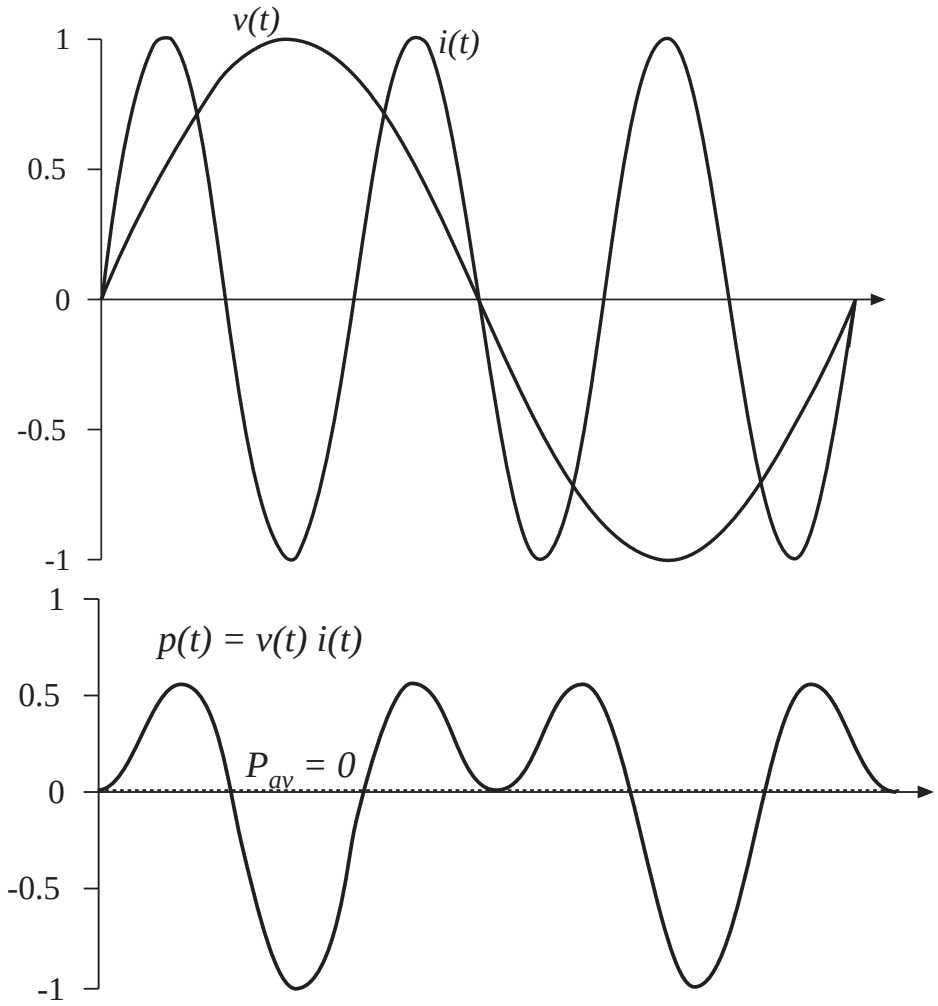
$$\frac{V_3 I_3}{2} \cos\left(\varphi_3 - \theta_3\right)$$

Example 1

Voltage: fundamental only

Current: third harmonic only

Power: zero average

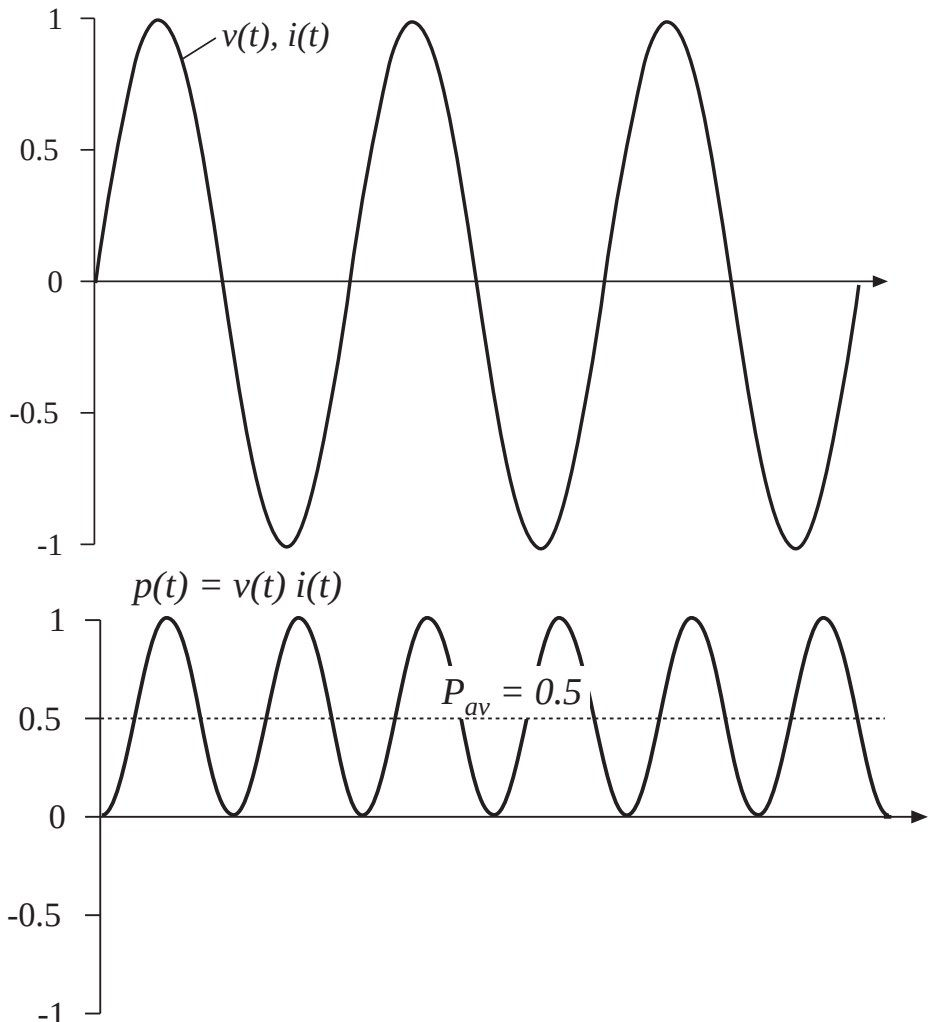


Example 2

Voltage: third harmonic only

Current: third harmonic only, in phase with voltage

Power: nonzero average



Example 3

Fourier series:

$$v(t) = 1.2 \cos(\omega t) + 0.33 \cos(3\omega t) + 0.2 \cos(5\omega t)$$
$$i(t) = 0.6 \cos(\omega t + 30°) + 0.1 \cos(5\omega t + 45°) + 0.1 \cos(7\omega t + 60°)$$

Average power calculation:

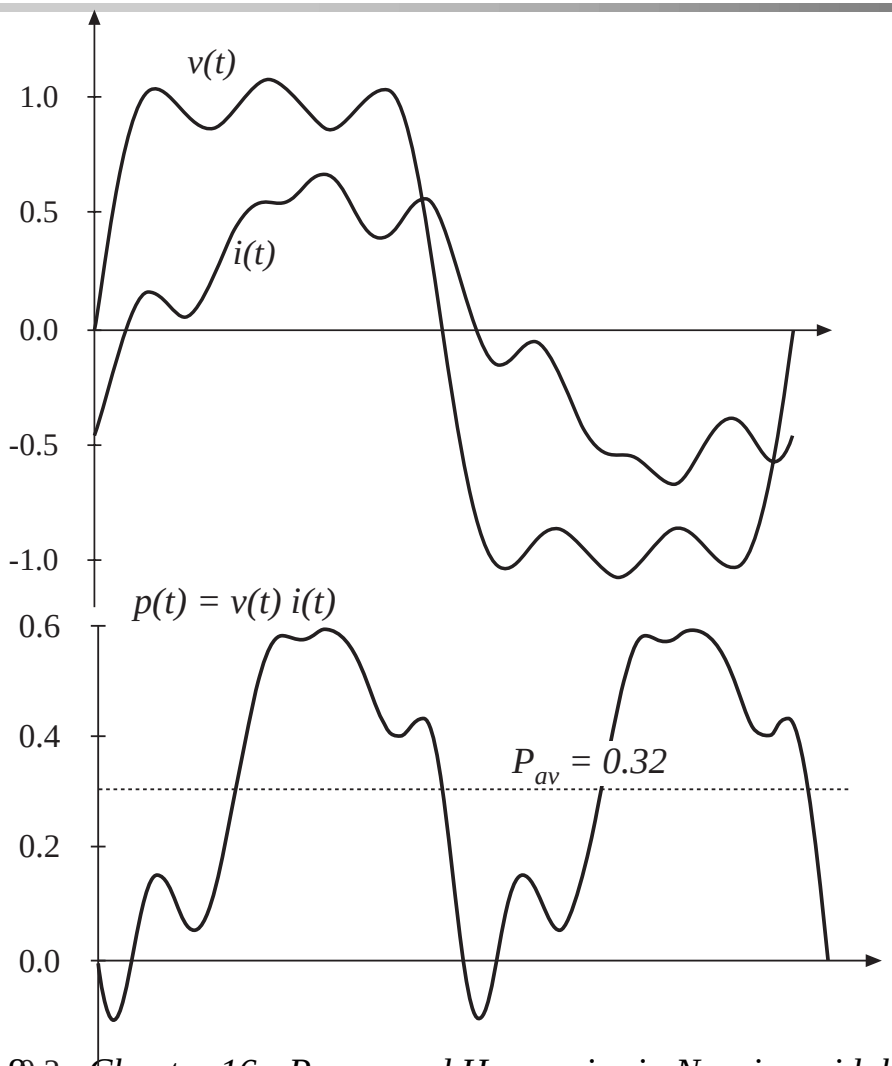
$$P_{av} = \frac{(1.2)(0.6)}{2} \cos(30°) + \frac{(0.2)(0.1)}{2} \cos(45°) = 0.32$$

Example 3

Voltage: 1st, 3rd, 5th

Current: 1st, 5th, 7th

Power: net energy is transmitted at fundamental and fifth harmonic frequencies



16.2. Root-mean-square (RMS) value of a waveform, in terms of Fourier series

$$\text{(rms value)} = \sqrt{\frac{1}{T}\int_0^T v^2(t)\,dt}$$

Insert Fourier series. Again, cross-multiplication terms have zero average. Result is

$$\text{(rms value)} = \sqrt{V_0^2 + \sum_{n=1}^{\infty} \frac{V_n^2}{2}}$$

- Similar expression for current
- Harmonics always increase rms value
- Harmonics do not necessarily increase average power
- Increased rms values mean increased losses

16.3. Power factor

For efficient transmission of energy from a source to a load, it is desired to maximize average power, while minimizing rms current and voltage (and hence minimizing losses).

Power factor is a figure of merit that measures how efficiently energy is transmitted. It is defined as

$$\text{power factor} = \frac{\text{(average power)}}{\text{(rms voltage) (rms current)}}$$

Power factor always lies between zero and one.

16.3.1. Linear resistive load, nonsinusoidal voltage

Then current harmonics are in phase with, and proportional to, voltage harmonics. All harmonics result in transmission of energy to load, and unity power factor occurs.

$$I_n = \frac{V_n}{R} \qquad \theta_n = \varphi_n \qquad \text{so} \quad \cos(\theta_n - \varphi_n) = 1$$

$$\text{(rms voltage)} = \sqrt{V_0^2 + \sum_{n=1}^{\infty} \frac{V_n^2}{2}}$$

$$\text{(rms current)} = \sqrt{I_0^2 + \sum_{n=1}^{\infty} \frac{I_n^2}{2}} = \sqrt{\frac{V_0^2}{R^2} + \sum_{n=1}^{\infty} \frac{V_n^2}{2R^2}}$$

$$= \frac{1}{R} \text{(rms voltage)}$$

$$P_{av} = V_0 I_0 + \sum_{n=1}^{\infty} \frac{V_n I_n}{2} \cos(\varphi_n - \theta_n)$$

16.3.2. Nonlinear dynamical load, sinusoidal voltage

With a sinusoidal voltage, current harmonics do not lead to average power. However, current harmonics do increase the rms current, and hence they decrease the power factor.

$$P_{av} = \frac{V_1 I_1}{2} \cos(\varphi_1 - \theta_1)$$

$$\text{(rms current)} = \sqrt{I_0^2 + \sum_{n=1}^{\infty} \frac{I_n^2}{2}}$$

$$\text{(power factor)} = \left(\frac{\frac{I_1}{\sqrt{2}}}{\sqrt{I_0^2 + \sum_{n=1}^{\infty} \frac{I_n^2}{2}}} \right) \left(\cos(\varphi_1 - \theta_1) \right)$$

$$= \text{(distortion factor) (displacement factor)}$$

Distortion factor

Defined only for sinusoidal voltage.

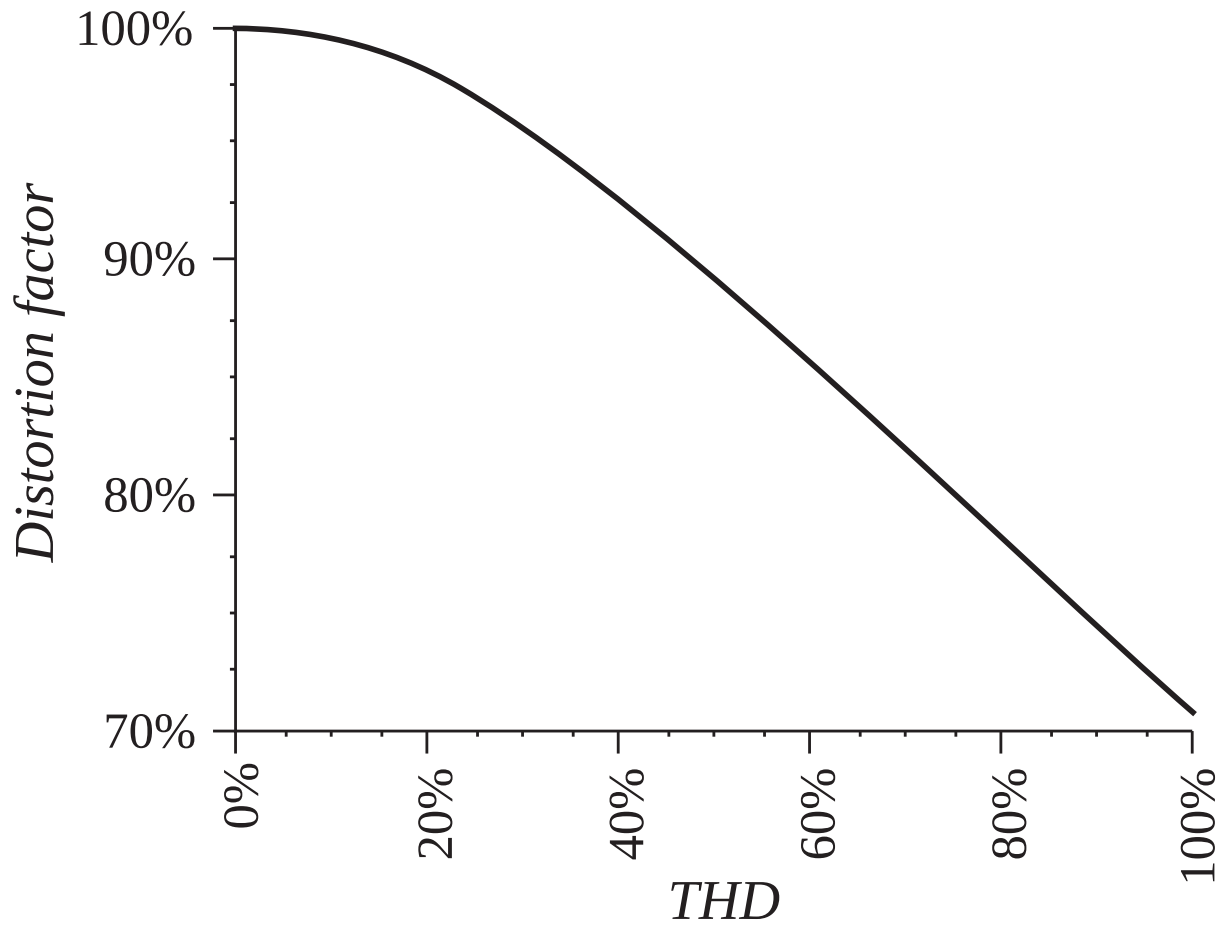
$$\text{(distortion factor)} = \left(\frac{\frac{I_1}{\sqrt{2}}}{\sqrt{I_0^2 + \sum_{n=1}^{\infty} \frac{I_n^2}{2}}} \right) = \frac{\text{(rms fundamental current)}}{\text{(rms current)}}$$

Related to Total Harmonic Distortion (THD):

$$\text{(THD)} = \frac{\sqrt{\sum_{n=2}^{\infty} I_n^2}}{I_1}$$

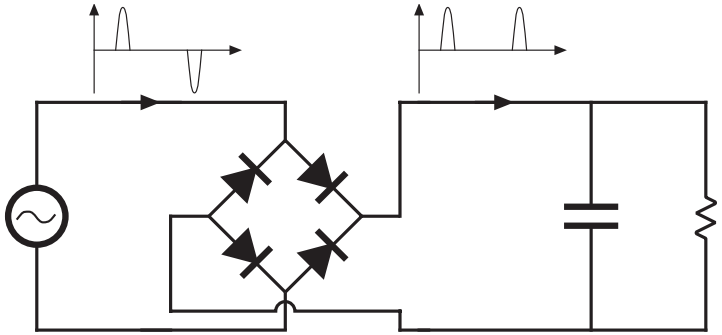
$$\text{(distortion factor)} = \frac{1}{\sqrt{1 + (\text{THD})^2}}$$

Distortion factor vs. THD

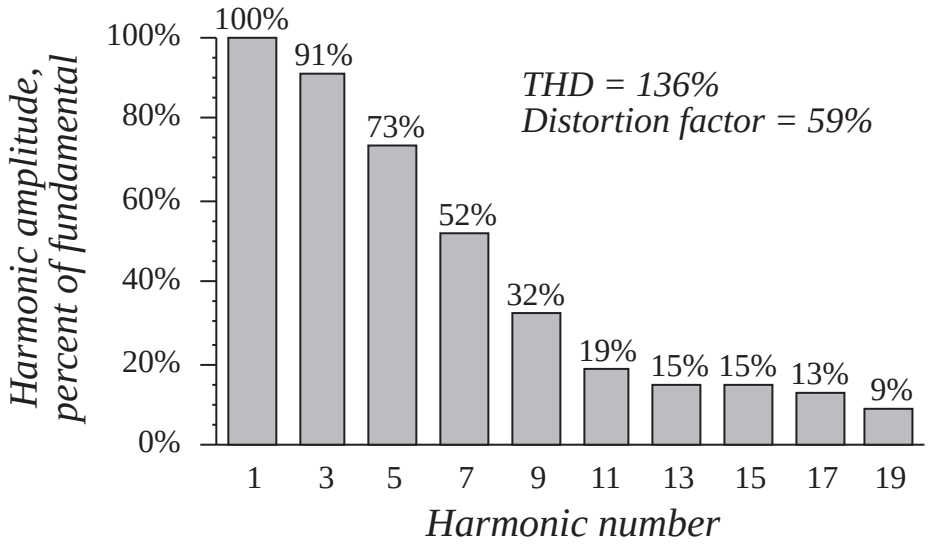


Peak detection rectifier example

Conventional single-phase peak detection rectifier



Typical ac line current spectrum



Maximum power obtainable from 120V 15A wall outlet

with peak detection rectifier

(ac voltage) (derated breaker current) (power factor) (rectifier efficiency)
= (120 V) (80% of 15 A) (0.55) (0.98)
= 776 W

at unity power factor

(ac voltage) (derated breaker current) (power factor) (rectifier efficiency)
= (120 V) (80% of 15 A) (0.99) (0.93)
= 1325 W

16.4. Power phasors in sinusoidal systems

Apparent power is the product of the rms voltage and rms current

- It is easily measured —simply the product of voltmeter and ammeter readings
- Unit of apparent power is the volt-ampere, or VA
- Many elements, such as transformers, are rated according to the VA that they can supply

So power factor is the ratio of average power to apparent power

With sinusoidal waveforms (no harmonics), we can also define the

real power P *reactive power* Q *complex power* $\boldsymbol{S}$

If the voltage and current are represented by phasors $\boldsymbol{V}$ and $\boldsymbol{I}$, then

$$\boldsymbol{S} = \boldsymbol{V}\boldsymbol{I}^* = P + jQ$$

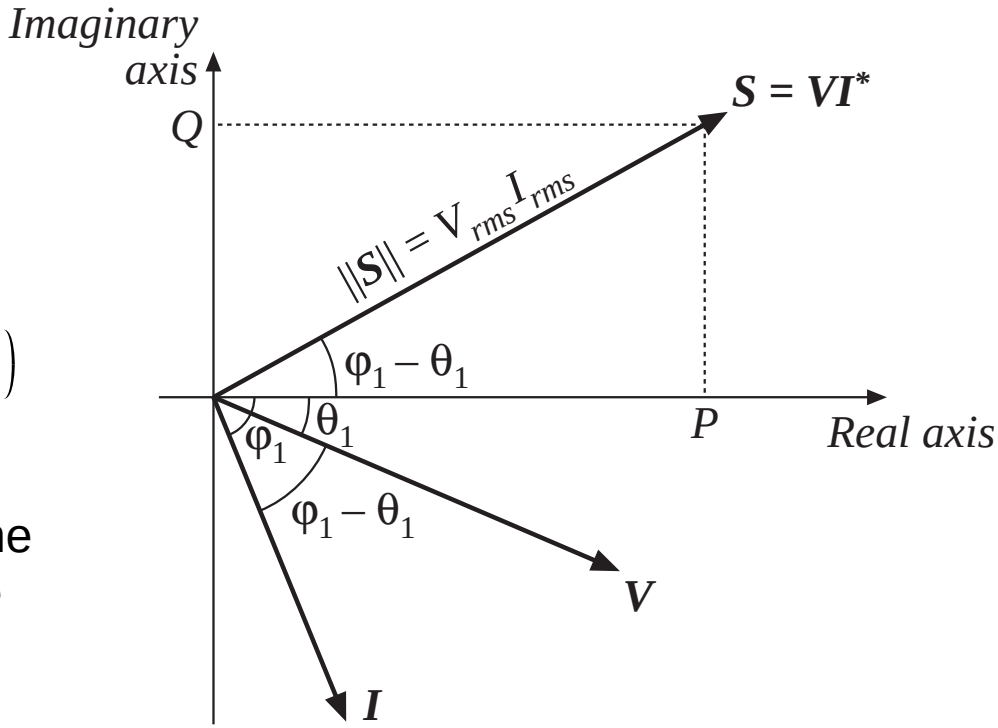
with $\boldsymbol{I}^*$ = complex conjugate of $\boldsymbol{I}$, j = square root of -1. The magnitude of $\boldsymbol{S}$ is the apparent power (VA). The real part of $\boldsymbol{S}$ is the average power P (watts). The imaginary part of $\boldsymbol{S}$ is the reactive power Q (reactive volt-amperes, or VARs).

Example: power phasor diagram

The phase angle between the voltage and current, or $(\varphi_1 - \theta_1)$, coincides with the angle of $\boldsymbol{S}$. The power factor is

$$\text{power factor} = \frac{P}{\|\boldsymbol{S}\|} = \cos\left(\varphi_1 - \theta_1\right)$$

In this purely sinusoidal case, the distortion factor is unity, and the power factor coincides with the displacement factor.



Reactive power Q

The reactive power Q does not lead to net transmission of energy between the source and load. When $Q \neq 0$, the rms current and apparent power are greater than the minimum amount necessary to transmit the average power P.

Inductor: current lags voltage by 90°, hence displacement factor is zero.

The alternate storing and releasing of energy in an inductor leads to current flow and nonzero apparent power, but $P = 0$.

Just as resistors consume real (average) power P, inductors can be viewed as consumers of reactive power Q.

Capacitor: current leads voltage by 90°, hence displacement factor is zero.

Capacitors supply reactive power Q.

They are often placed in the utility power distribution system near inductive loads. If Q supplied by capacitor is equal to Q consumed by inductor, then the net current (flowing from the source into the capacitor-inductive-load combination) is in phase with the voltage, leading to unity power factor and minimum rms current magnitude.

Lagging fundamental current of phase-controlled rectifiers

It will be seen in the next chapter that phase-controlled rectifiers produce a nonsinusoidal current waveform whose fundamental component lags the voltage.

This lagging current does not arise from energy storage, but it does nonetheless lead to a reduced displacement factor, and to rms current and apparent power that are greater than the minimum amount necessary to transmit the average power.

At the fundamental frequency, phase-controlled rectifiers can be viewed as consumers of reactive power Q, similar to inductive loads.

16.5. Harmonic currents in three phase systems

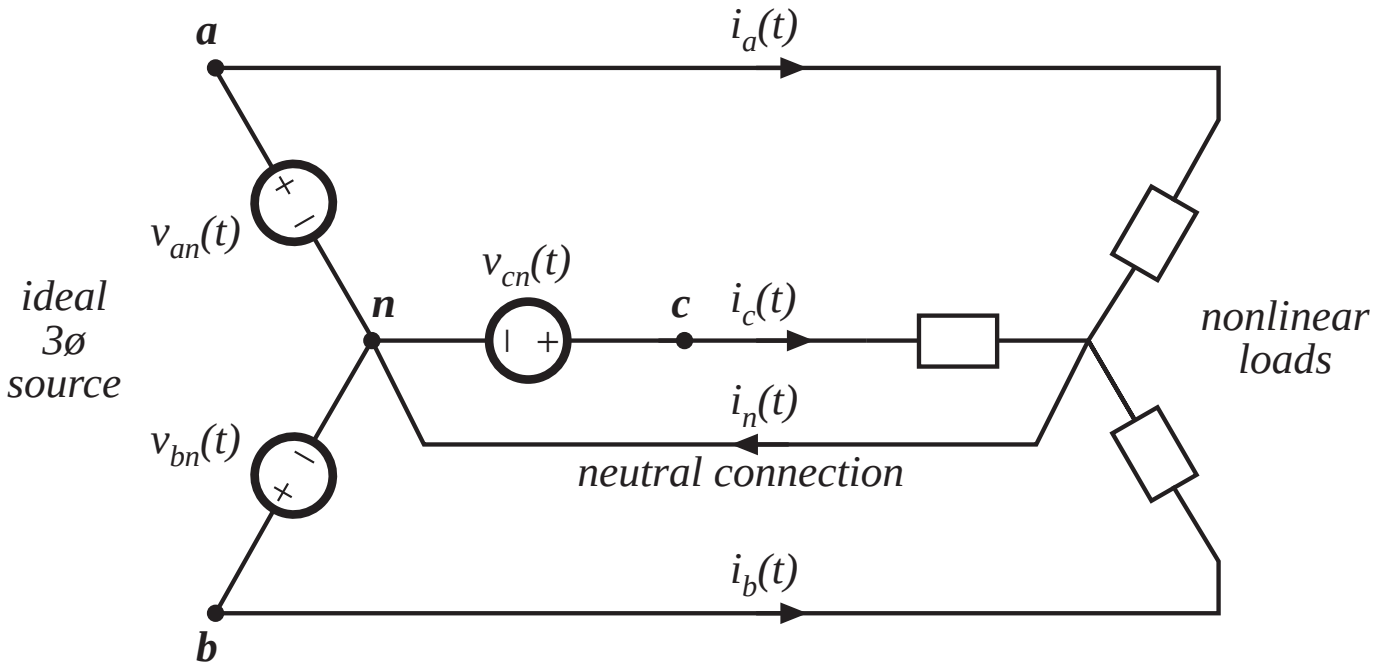
The presence of harmonic currents can also lead to some special problems in three-phase systems:

- In a four-wire three-phase system, harmonic currents can lead to large currents in the neutral conductors, which may easily exceed the conductor rms current rating
- Power factor correction capacitors may experience significantly increased rms currents, causing them to fail

In this section, these problems are examined, and the properties of harmonic current flow in three-phase systems are derived:

- Harmonic neutral currents in 3ø four-wire networks
- Harmonic neutral voltages in 3ø three-wire wye-connected loads

16.5.1. Harmonic currents in three-phase four-wire networks



Fourier series of line currents and voltages:

$$i_a(t) = I_{a0} + \sum_{k=1}^{\infty} I_{ak} \cos\left(k\omega t - \theta_{ak}\right)$$

$$i_b(t) = I_{b0} + \sum_{k=1}^{\infty} I_{bk} \cos\left(k(\omega t - 120^\circ) - \theta_{bk}\right)$$

$$i_c(t) = I_{c0} + \sum_{k=1}^{\infty} I_{ck} \cos\left(k(\omega t + 120^\circ) - \theta_{ck}\right)$$

$$v_{an}(t) = V_m \cos(\omega t)$$

$$v_{bn}(t) = V_m \cos(\omega t - 120^\circ)$$

$$v_{cn}(t) = V_m \cos(\omega t + 120^\circ)$$

Neutral current

$$i_n(t) = I_{a0} + I_{b0} + I_{c0} +$$

$$\sum_{k=1}^{\infty} \left[I_{ak} \cos\left(k\omega t - \theta_{ak}\right) + I_{bk} \cos\left(k(\omega t - 120^\circ) - \theta_{bk}\right) + I_{ck} \cos\left(k(\omega t + 120^\circ) - \theta_{ck}\right) \right]$$

If the load is unbalanced, then there is nothing more to say. The neutral connection may contain currents having spectrum similar to the line currents.

In the balanced case, $I_{ak} = I_{bk} = I_{ck} = I_k$ and $\theta_{ak} = \theta_{bk} = \theta_{ck} = \theta_k$, for all k; i.e., the harmonics of the three phases all have equal amplitudes and phase shifts. The neutral current is then

$$i_n(t) = 3I_0 + \sum_{k = 3,6,9,\cdots}^{\infty} 3I_k \cos\left(k\omega t - \theta_k\right)$$

Neutral currents

$$i_n(t) = 3I_0 + \sum_{k = 3,6,9,\cdots}^{\infty} 3I_k \cos\left(k\omega t - \theta_k\right)$$

- Fundamental and most harmonics cancel out
- Triplen (triple-n, or 0, 3, 6, 9, ...) harmonics do not cancel out, but add. Dc components also add.
- Rms neutral current is

$$i_{n,\,rms} = 3\sqrt{I_0^2 + \sum_{k = 3,6,9,\cdots}^{\infty} \frac{I_k^2}{2}}$$

Example

A balanced nonlinear load produces line currents containing fundamental and 20% third harmonic: $i_{an}(t) = I_1 \cos(\omega t - \theta_1) + 0.2\, I_1 \cos(3\omega t - \theta_3)$. Find the rms neutral current, and compare its amplitude to the rms line current amplitude.

Solution

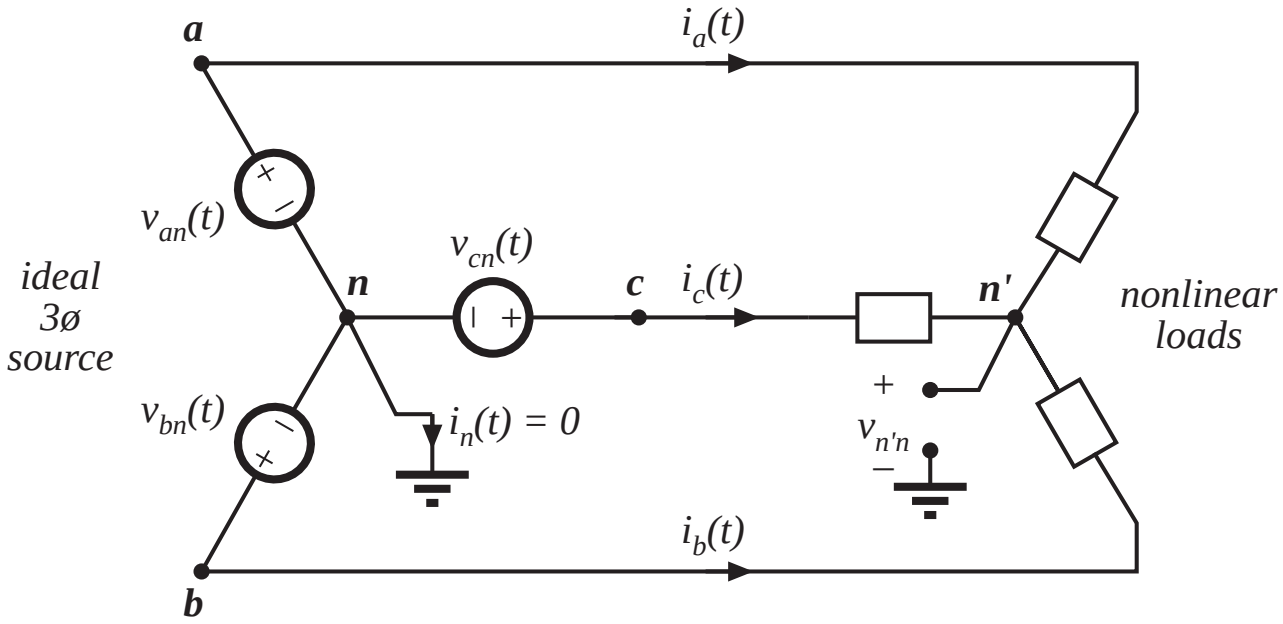
$$i_{n,\,rms} = 3\sqrt{\frac{(0.2I_1)^2}{2}} = \frac{0.6\, I_1}{\sqrt{2}}$$

$$i_{1,\,rms} = \sqrt{\frac{I_1^2 + (0.2I_1)^2}{2}} = \frac{I_1}{\sqrt{2}}\sqrt{1 + 0.04} \approx \frac{I_1}{\sqrt{2}}$$

- The neutral current magnitude is 60% of the line current magnitude!
- The triplen harmonics in the three phases add, such that 20% third harmonic leads to 60% third harmonic neutral current.
- Yet the presence of the third harmonic has very little effect on the rms value of the line current. Significant unexpected neutral current flows.

16.5.2. Harmonic currents in three-phase three-wire networks

Wye-connected nonlinear load, no neutral connection:



No neutral connection

If the load is balanced, then it is still true that

$$i_n(t) = 3I_0 + \sum_{k = 3,6,9,\cdots}^{\infty} 3I_k \cos(k\omega t - \theta_k)$$

But $i_n(t) = 0$, since there is no neutral connection.

So the ac line currents cannot contain dc or triplen harmonics.

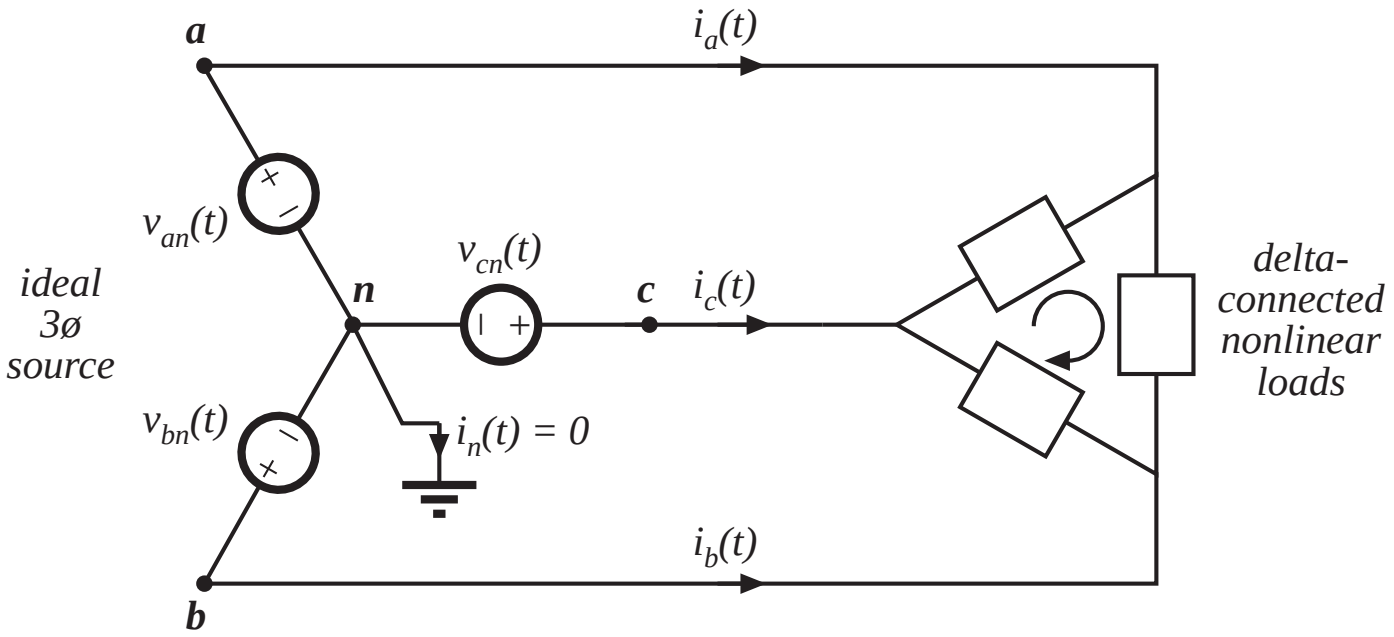
What happens:

A voltage is induced at the load neutral point, that causes the line current dc and triplen harmonics to become zero.

The load neutral point voltage contains dc and triplen harmonics.

With an unbalanced load, the line currents can still contain dc and triplen harmonics.

Delta-connected load

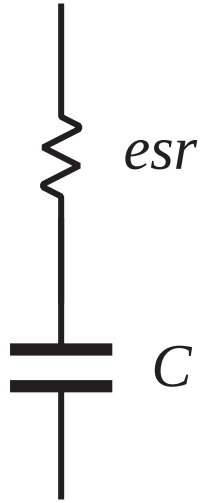


- There is again no neutral connection, so the ac line currents contain no dc or triplen harmonics
- The load currents may contain dc and triplen harmonics: with a balanced nonlinear load, these circulate around the delta.

Harmonic currents in power factor correction capacitors

PFC capacitors are usually not intended to conduct significant harmonic currents.

Heating in capacitors is a function of capacitor equivalent series resistance (esr) and rms current. The maximum allowable rms current then leads to the capacitor rating:



$$\text{rated rms voltage } V_{rms} = \frac{I_{rms}}{2\pi f C}$$

$$\text{rated reactive power} = \frac{I_{rms}^2}{2\pi f C}$$

16.6. AC line current harmonic standards

US MIL-STD-461B

International Electrotechnical Commission Standard 1000

IEEE/ANSI Standard 519

US MIL-STD-461B

- An early attempt to regulate ac line current harmonics generated by nonlinear loads
- For loads of 1kW or greater, no current harmonic magnitude may be greater than 3% of the fundamental magnitude.
- For the nth harmonic with $n > 33$, the harmonic magnitude may not exceed $(1/n)$ times the fundamental magnitude.
- Harmonic limits are now employed by all of the US armed forces. The specific limits are often tailored to the specific application.
- The shipboard application is a good example of the problems faced in a relatively small stand-alone power system having a large fraction of electronic loads.

International Electrotechnical Commission Standard 1000

- First draft of their IEC-555 standard:1982. It has since undergone a number of revisions. Recent reincarnation: IEC-1000-3-2
- Enforcement of IEC-1000 is the prerogative of each individual country, and hence it has been sometimes difficult to predict whether and where this standard will actually be given the force of law.
- Nonetheless, IEC-1000 is now enforced in Europe, making it a de facto standard for commercial equipment intended to be sold worldwide.
- IEC-1000 covers a number of different types of low power equipment, with differing harmonic limits. Harmonics for equipment having an input current of up to 16A, connected to 50 or 60 Hz, 220V to 240V single phase circuits (two or three wire), as well as 380V to 415V three phase (three or four wire) circuits, are limited.

Low-power harmonic limits

- In a city environment such as a large building, a large fraction of the total power system load can be nonlinear
- Example: a major portion of the electrical load in a building is comprised of fluorescent lights, which present a very nonlinear characteristic to the utility system.
- A modern office may also contain a large number of personal computers, printers, copiers, etc., each of which may employ peak detection rectifiers.
- Although each individual load is a negligible fraction of the total local load, these loads can collectively become significant.

IEC-1000: Class A and B

Class A: Balanced three-phase equipment, and any equipment which does not fit into the other categories. This class includes low harmonic rectifiers for computer and other office equipment. These limits are given in Table 16.1, and are absolute ampere limits.

Class B: Portable tools, and similar devices. The limits are equal to the Table 16.1 limits, multiplied by 1.5.

Classes C, D, and E: For other types of equipment, including lighting (Class C) and equipment having a “special waveshape” (Class D).

Class A limits

Table 16.1. IEC-1000 Harmonic current limits, Class A

Odd harmonics		*Even harmonics*	
Harmonic number	*Maximum current*	*Harmonic number*	*Maximum curre*
3	2.30A	2	1.08A
5	1.14A	4	0.43A
7	0.77A	6	0.30A
9	0.40A	$8 \le n \le 40$	$0.23\text{A} \cdot (8/n)$
11	0.33A		
13	0.21A		
$15 \le n \le 39$	$0.15\text{A} \cdot (15/n)$		

16.6.2. IEEE / ANSI Standard 519

- In 1993, the IEEE published a revised draft standard limiting the amplitudes of current harmonics, *IEEE Guide for Harmonic Control and Reactive Compensation of Static Power Converters*.
- Harmonic limits are based on the ratio of the fundamental component of the load current IL to the short circuit current at the point of common (PCC) coupling at the utility I_{sc}.
- Stricter limits are imposed on large loads than on small loads. The limits are similar in magnitude to IEC-1000, and cover high voltage loads (of much higher power) not addressed by IEC-1000. Enforcement of this standard is presently up to the local utility company.
- The odd harmonic limits are listed in Table 16.2. The limits for even harmonics are 25% of the odd harmonic limits. Dc current components and half-wave rectifiers are not allowed.

IEEE-519 current limits, low voltage systems

Table 16.2. IEEE-519 Maximum odd harmonic current limits for general distribution systems, 120V through 69kV

I_{SC}/I_L	$n < 11$	$11 \le n < 17$	$17 \le n < 23$	$23 \le n < 35$	$35 \le n$	*THD*
<20	4.0%	2.0%	1.5%	0.6%	0.3%	5.0%
20–50	7.0%	3.5%	2.5%	1.0%	0.5%	8.0%
50–100	10.0%	4.5%	4.0%	1.5%	0.7%	12.0%
100–1000	12.0%	5.5%	5.0%	2.0%	1.0%	15.0%
>1000	15.0%	7.0%	6.0%	2.5%	1.4%	20.0%

IEEE-519 voltage limits

Table 16.3. IEEE-519 voltage distortion limits

Bus voltage at PCC	*Individual harmonics*	*THD*
69kV and below	3.0%	5.0%
69.001kV–161kV	1.5%	2.5%
above 161kV	1.0%	1.5%

It is the responsibility of the utility to meet these limits.

Chapter 17

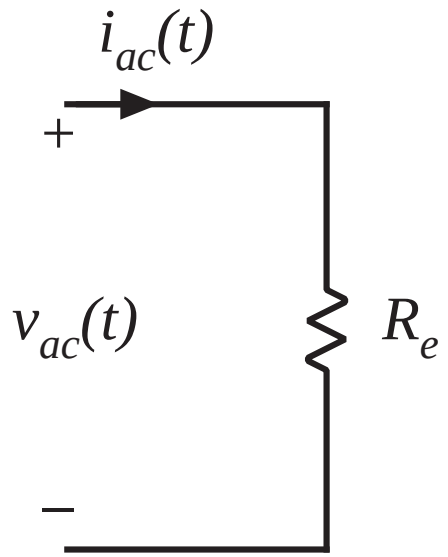
The Ideal Rectifier

17.1 Properties of the ideal rectifier

It is desired that the rectifier present a resistive load to the ac power system. This leads to

- unity power factor
- ac line current has same waveshape as voltage

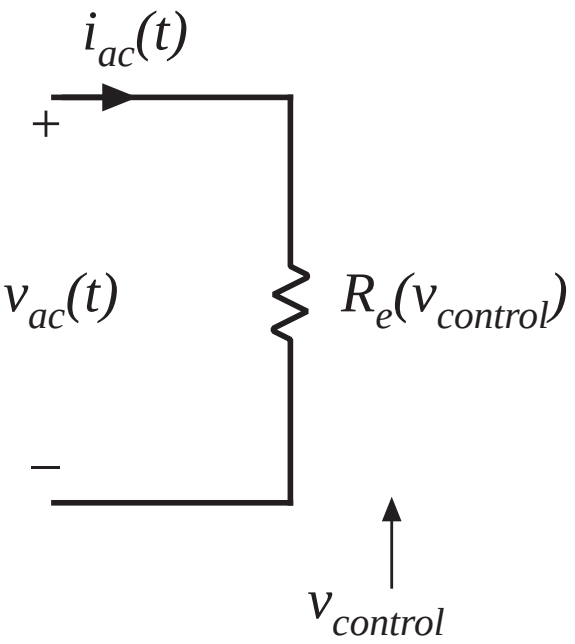
$$i_{ac}(t) = \frac{v_{ac}(t)}{R_e}$$



R_e is called the *emulated resistance*

Control of power throughput

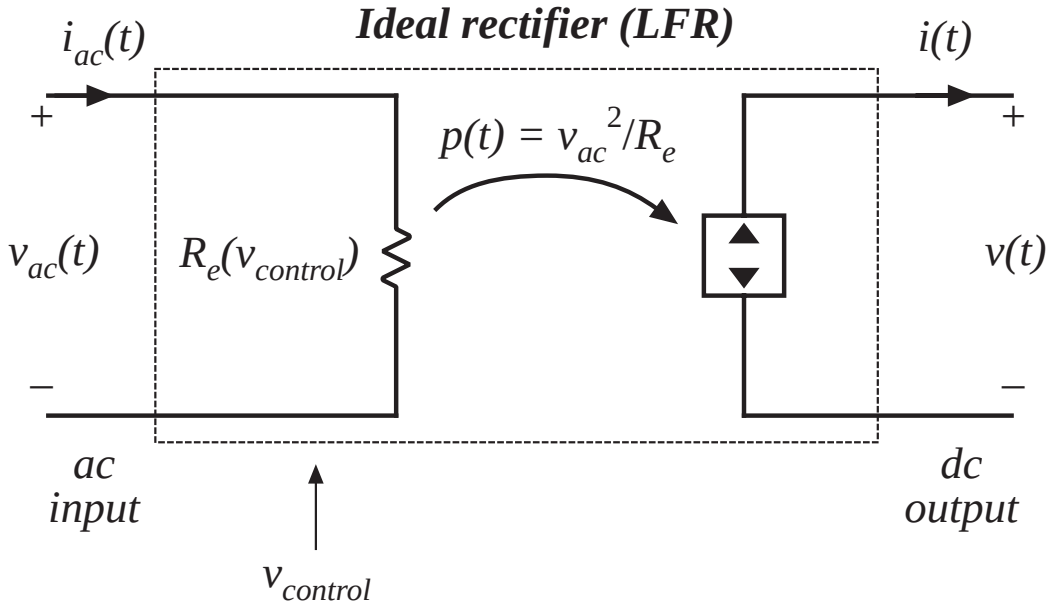
$$P_{av} = \frac{V_{ac,rms}^2}{R_e(v_{control})}$$



Power apparently "consumed" by R_e is actually transferred to rectifier dc output port. To control the amount of output power, it must be possible to adjust the value of R_e.

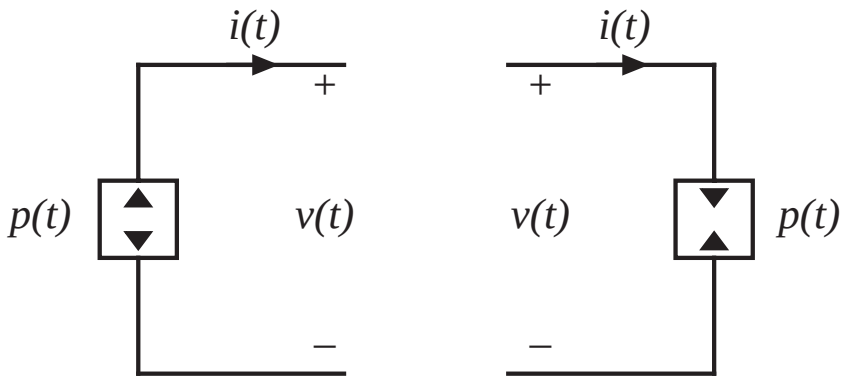
Output port model

The ideal rectifier is lossless and contains no internal energy storage. Hence, the instantaneous input power equals the instantaneous output power. Since the instantaneous power is independent of the dc load characteristics, the output port obeys a power source characteristic.



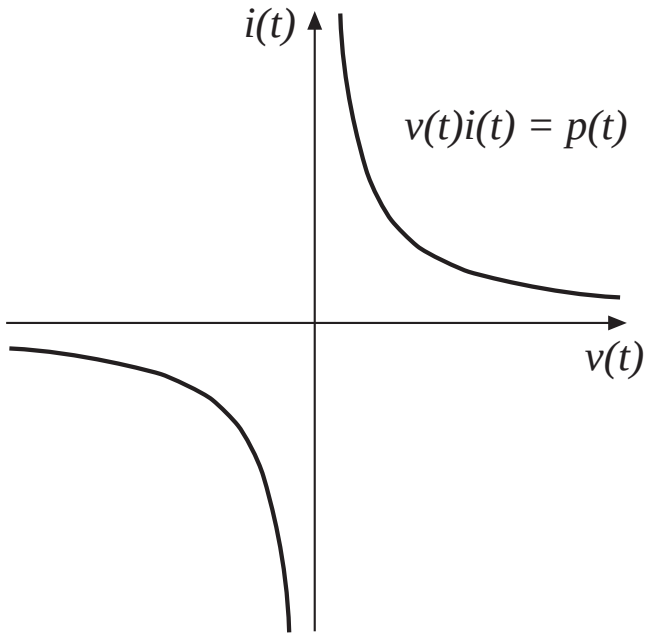
$$p(t) = \frac{v_{ac}^2(t)}{R_e(v_{control}(t))} \qquad v(t)i(t) = p(t) = \frac{v_{ac}^2(t)}{R_e}$$

The dependent power source



power source

power sink



i-v characteristic

Equations of the ideal rectifier / LFR

Defining equations of the ideal rectifier:

$$i_{ac}(t) = \frac{v_{ac}(t)}{R_e(v_{control})}$$

$$v(t)i(t) = p(t)$$

$$p(t) = \frac{v_{ac}^2(t)}{R_e(v_{control}(t))}$$

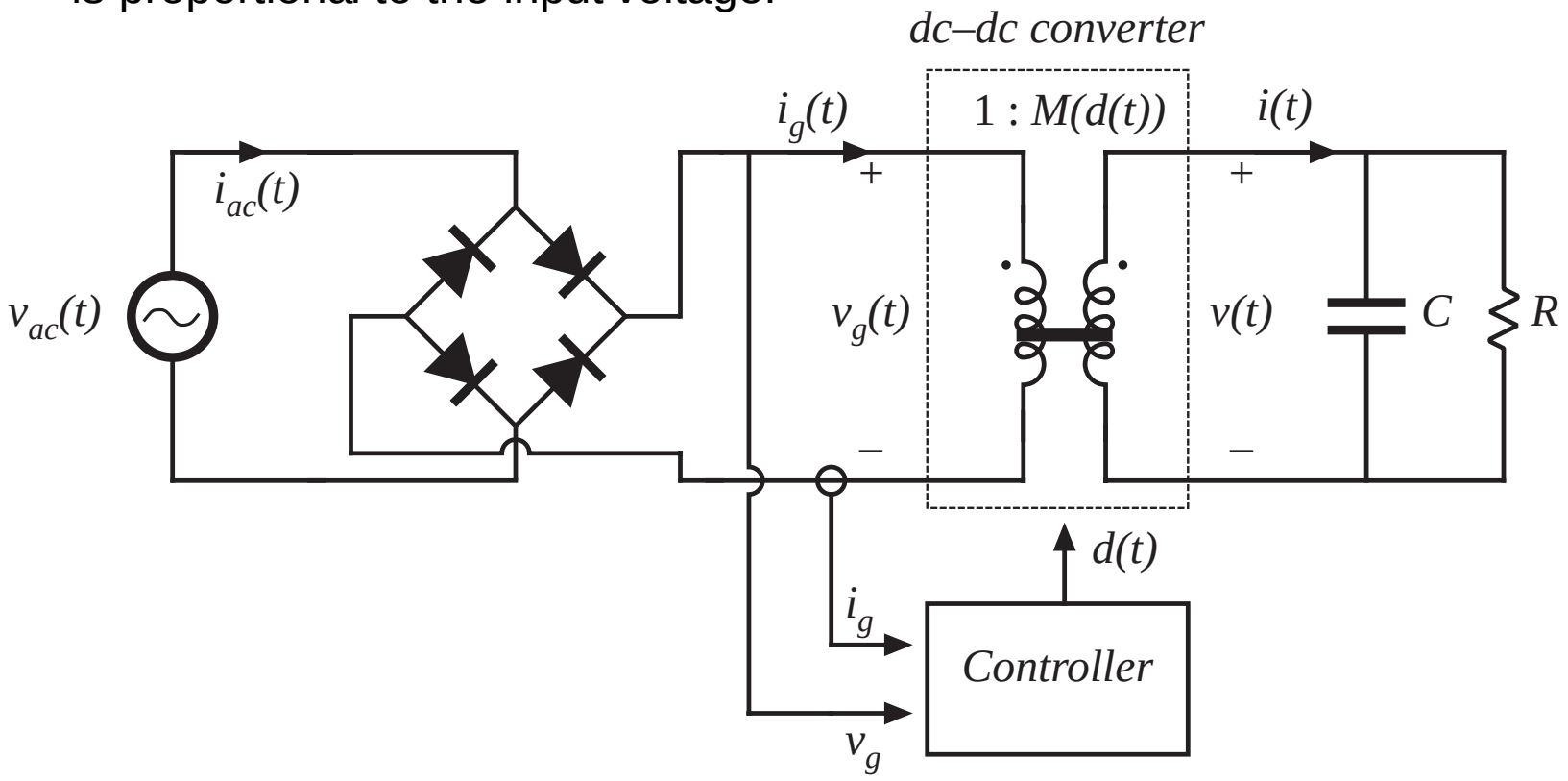
When connected to a resistive load of value R, the input and output rms voltages and currents are related as follows:

$$\frac{V_{rms}}{V_{ac,rms}} = \sqrt{\frac{R}{R_e}}$$

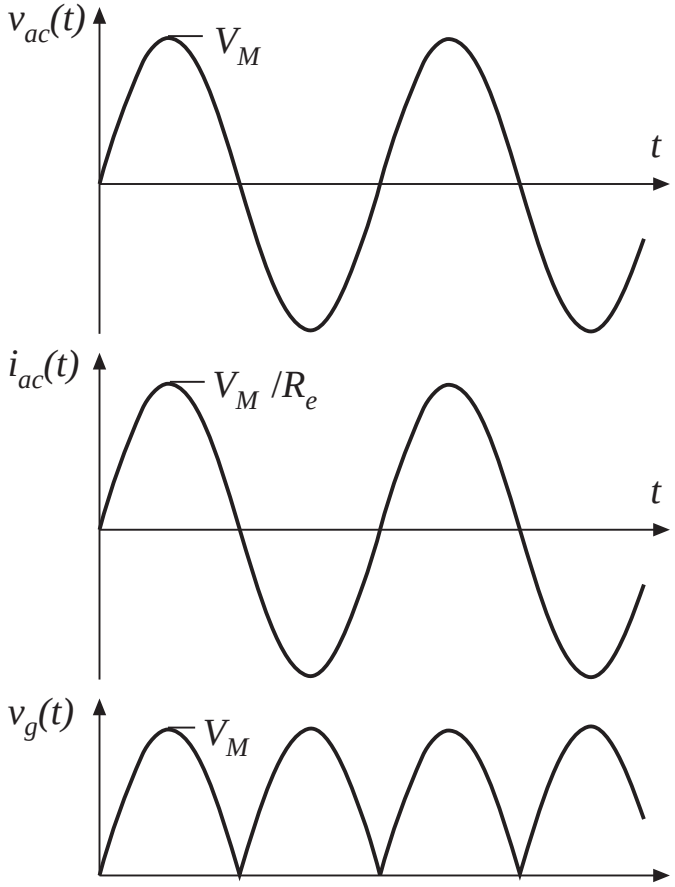
$$\frac{I_{ac,rms}}{I_{rms}} = \sqrt{\frac{R}{R_e}}$$

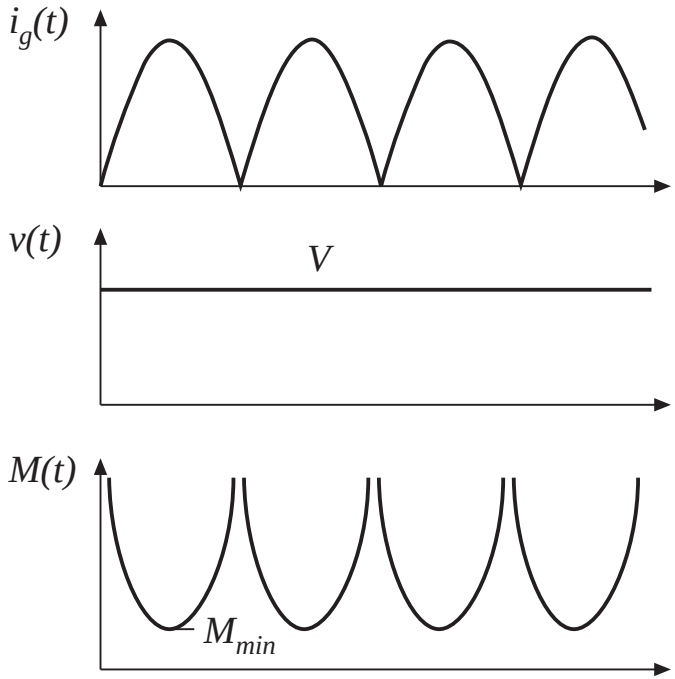
17.2 Realization of a near-ideal rectifier

Control the duty cycle of a dc-dc converter, such that the input current is proportional to the input voltage:



Waveforms





$$v_{ac}(t) = V_M \sin(\omega t)$$

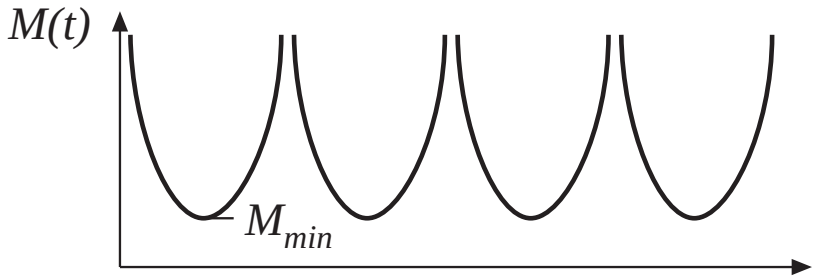
$$v_g(t) = V_M \left| \sin(\omega t) \right|$$

$$M(d(t)) = \frac{v(t)}{v_g(t)} = \frac{V}{V_M \left| \sin(\omega t) \right|}$$

$$M_{min} = \frac{V}{V_M}$$

Choice of converter

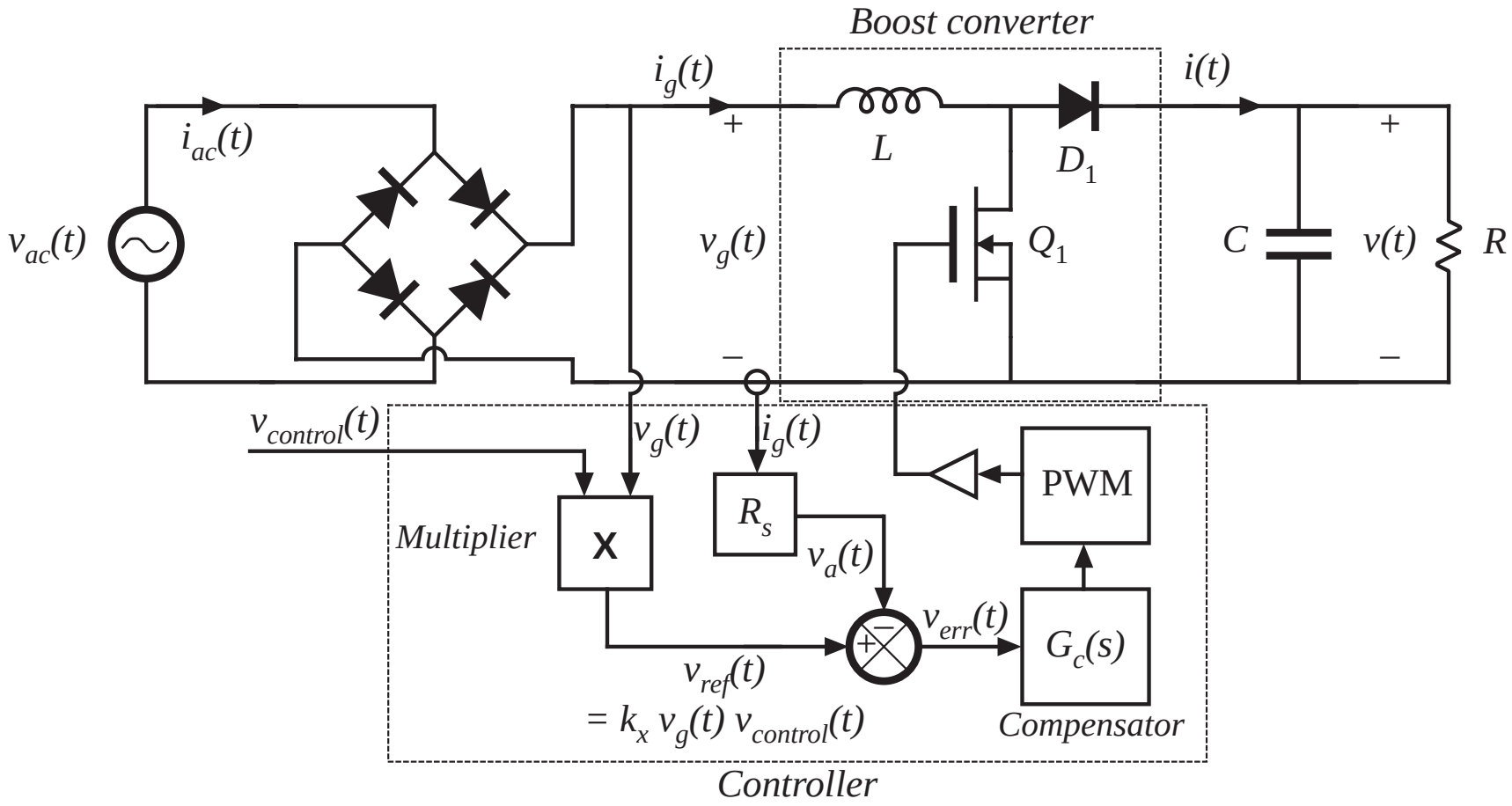
$$M(d(t)) = \frac{v(t)}{v_g(t)} = \frac{V}{V_M \left| \sin(\omega t) \right|}$$



- To avoid distortion near line voltage zero crossings, converter should be capable of producing $M(d(t))$ approaching infinity
- Above expression neglects converter dynamics
- Boost, buck-boost, Cuk, SEPIC, and other converters with similar conversion ratios are suitable
- We will see that the boost converter exhibits lowest transistor stresses. For this reason, it is most often chosen

Boost converter

with controller to cause input current to follow input voltage



Variation of duty cycle in boost rectifier

$$M(d(t)) = \frac{v(t)}{v_g(t)} = \frac{V}{V_M \left| \sin(\omega t) \right|}$$

Since $M \geq 1$ in the boost converter, it is required that $V \geq V_M$

If the converter operates in CCM, then

$$M(d(t)) = \frac{1}{1 - d(t)}$$

The duty ratio should therefore follow

$$d(t) = 1 - \frac{v_g(t)}{V}$$ in CCM

CCM/DCM boundary, boost rectifier

Inductor current ripple is

$$\Delta i_g(t) = \frac{v_g(t) d(t) T_s}{2L}$$

Low-frequency (average) component of inductor current waveform is

$$\left\langle i_g(t) \right\rangle_{T_s} = \frac{v_g(t)}{R_e}$$

The converter operates in CCM when

$$\left\langle i_g(t) \right\rangle_{T_s} > \Delta i_g(t) \quad \Rightarrow \quad d(t) < \frac{2L}{R_e T_s}$$

Substitute CCM expression for $d(t)$:

$$R_e < \frac{2L}{T_s \left(1 - \frac{v_g(t)}{V} \right)} \quad \text{for CCM}$$

CCM/DCM boundary

$$R_e < \frac{2L}{T_s\left(1 - \frac{v_g(t)}{V}\right)} \quad \text{for CCM}$$

Note that $v_g(t)$ varies with time, between 0 and V_M. Hence, this equation may be satisfied at some points on the ac line cycle, and not at others. The converter always operates in CCM provided that

$$R_e < \frac{2L}{T_s}$$

The converter always operates in DCM provided that

$$R_e > \frac{2L}{T_s\left(1 - \frac{V_M}{V}\right)}$$

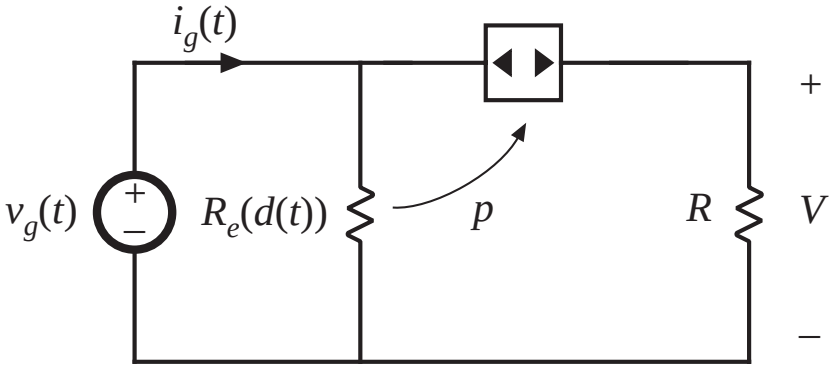
For R_e between these limits, the converter operates in DCM when $v_g(t)$ is near zero, and in CCM when $v_g(t)$ approaches V_M.

Static input characteristics of the boost converter

A plot of input current $i_g(t)$ vs input voltage $v_g(t)$, for various duty cycles $d(t)$. In CCM, the boost converter equilibrium equation is

$$\frac{v_g(t)}{V} = 1 - d(t)$$

The input characteristic in DCM is found by solution of the averaged DCM model (Fig. 10.12(b)):



Solve for input current:

$$i_g(t) = \frac{v_g(t)}{R_e(d(t))} + \frac{p(t)}{V - v_g(t)}$$

with $$p(t) = \frac{v_g^2(t)}{R_e(d(t))}$$

$$R_e(d(t)) = \frac{2L}{d^2(t)T_s}$$

Beware! This DCM $R_e(d)$ from Chapter 10 is not the same as the rectifier emulated resistance $R_e = v_g/i_g$

Static input characteristics of the boost converter

Now simplify DCM current expression, to obtain

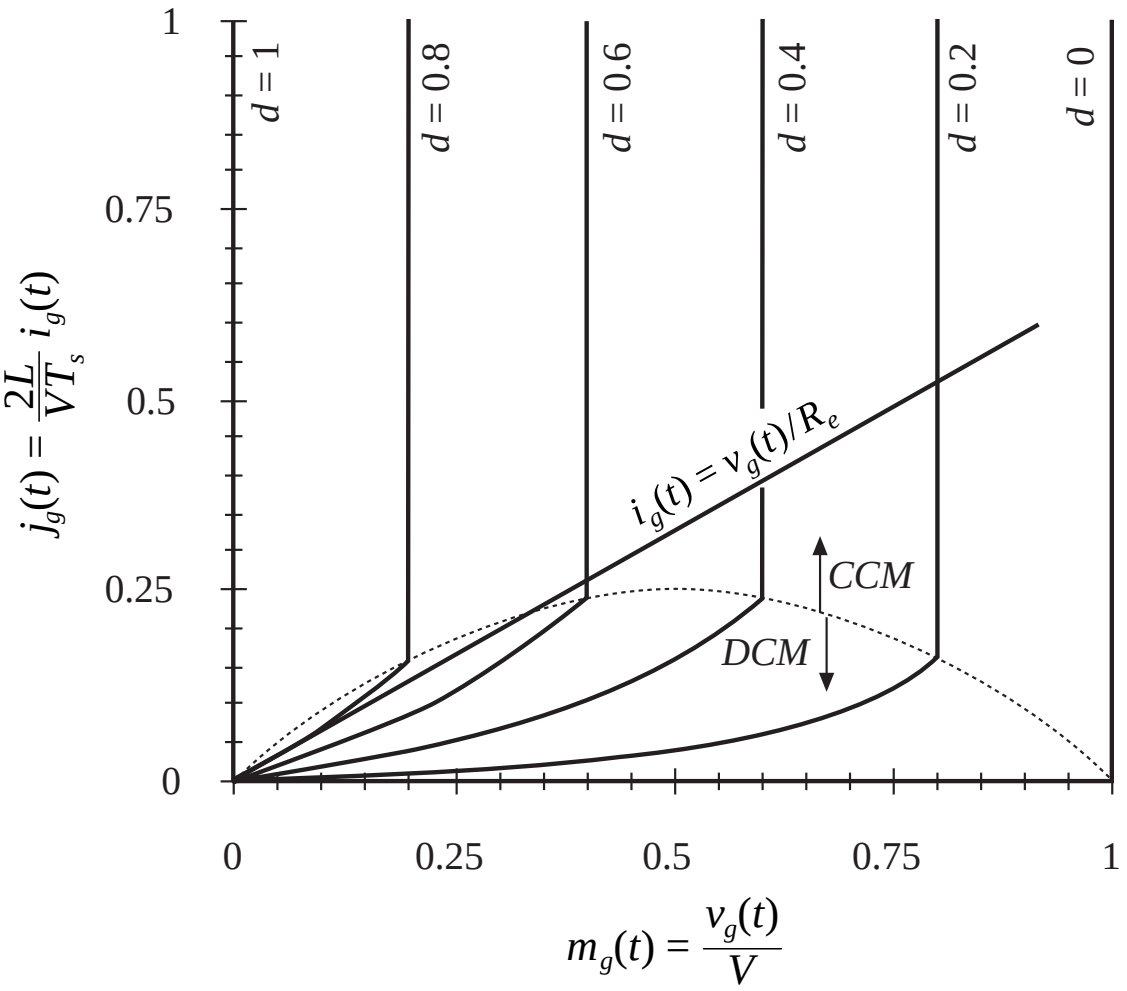
$$\frac{2L}{VT_s}\, i_g(t) \left(1 - \frac{v_g(t)}{V} \right) = d^2(t)\, \frac{v_g(t)}{V}$$

CCM/DCM mode boundary, in terms of $v_g(t)$ and $i_g(t)$:

$$\frac{2L}{VT_s}\, i_g(t) > \left(\frac{v_g(t)}{V} \right) \left(1 - \frac{v_g(t)}{V} \right)$$

Boost input characteristics

with superimposed resistive characteristic



CCM:

$$\frac{v_g(t)}{V} = 1 - d(t)$$

DCM:

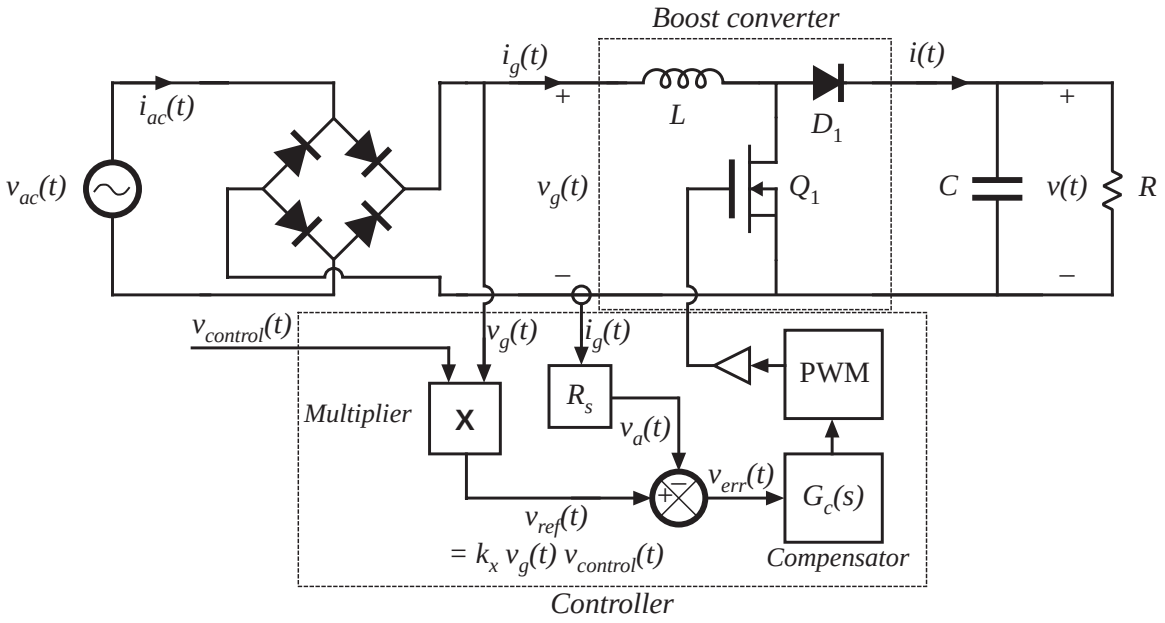
$$\frac{2L}{VT_s} i_g(t) \left(1 - \frac{v_g(t)}{V}\right) = d^2(t) \frac{v_g(t)}{V}$$

CCM when

$$\frac{2L}{VT_s} i_g(t) > \left(\frac{v_g(t)}{V}\right) \left(1 - \frac{v_g(t)}{V}\right)$$

R_e of the multiplying (average current) controller

Solve circuit to find R_e:



Current sensor gain

$$v_a(t) = i_g(t) R_s$$

when the error signal is small,

$$v_a(t) \approx v_{ref}(t)$$

multiplier equation

$$v_{ref}(t) = k_x v_g(t) v_{control}(t)$$

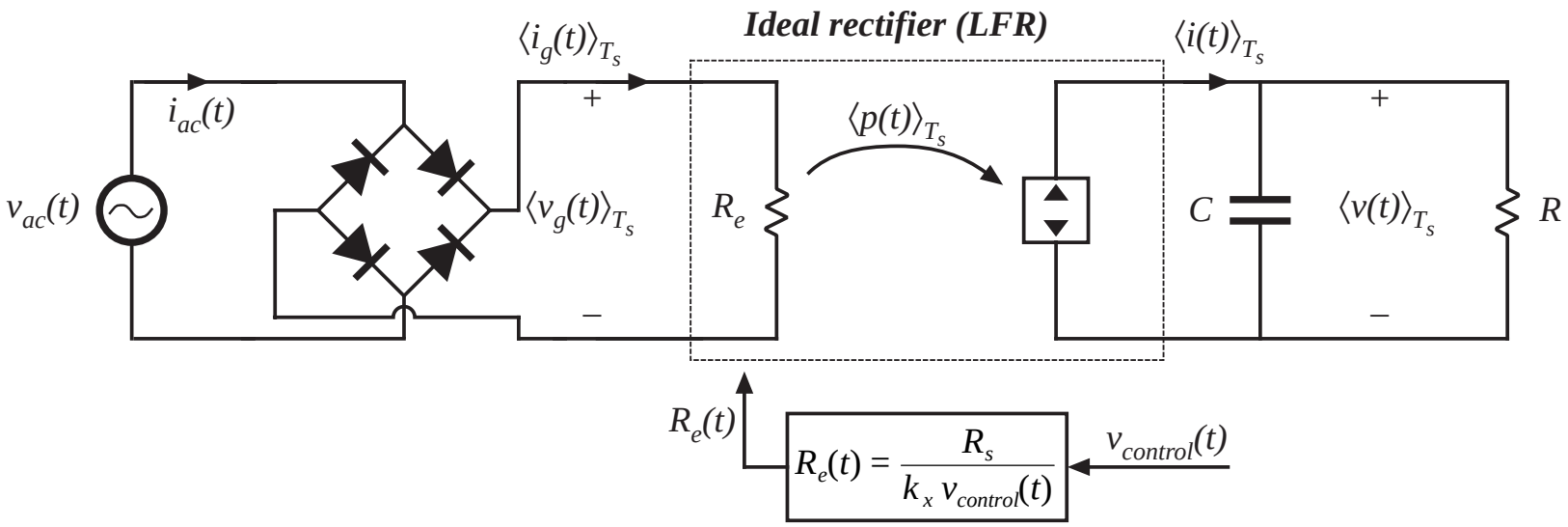
then R_e is

$$R_e = \frac{v_g(t)}{i_g(t)} = \frac{\left(\dfrac{v_{ref}(t)}{k_x v_{control}(t)} \right)}{\left(\dfrac{v_a(t)}{R_s} \right)}$$

simplify:

$$R_e(v_{control}(t)) = \frac{R_s}{k_x v_{control}(t)}$$

Low frequency system model



$$R_e(v_{control}(t)) = \frac{R_s}{k_x v_{control}(t)}$$

This model also applies to other converters that are controlled in the same manner, including buck-boost, Cuk, and SEPIC.

Open-loop DCM approach

We found in Chapter 10 that the buck-boost, SEPIC, and Cuk converters, when operated open-loop in DCM, inherently behave as loss-free resistors. This suggests that they could also be used as near-ideal rectifiers, without need for a multiplying controller.

Advantage: simple control

Disadvantages: higher peak currents, larger input current EMI

Like other DCM applications, this approach is usually restricted to low power (< 200W).

The boost converter can also be operated in DCM as a low harmonic rectifier. Input characteristic is

$$\left\langle i_g(t) \right\rangle_{T_s} = \frac{v_g(t)}{R_e} + \frac{v_g^2(t)}{R_e \left(v(t) - v_g(t) \right)}$$

Input current contains harmonics. If v is sufficiently greater than v_g, then harmonics are small.

17.3 Single-phase converter systems containing ideal rectifiers

- It is usually desired that the output voltage $v(t)$ be regulated with high accuracy, using a wide-bandwidth feedback loop
- For a given constant load characteristic, the instantaneous load current and power are then also constant:

$$p_{load}(t) = v(t)i(t) = VI$$

- The instantaneous input power of a single-phase ideal rectifier is not constant:

$$p_{ac}(t) = v_g(t)i_g(t)$$

with

$$v_g(t) = V_M \left| \sin(\omega t) \right| \qquad i_g(t) = \frac{v_g(t)}{R_e}$$

so

$$p_{ac}(t) = \frac{V_M^2}{R_e} \sin^2(\omega t) = \frac{V_M^2}{2R_e} \left(1 - \cos(2\omega t)\right)$$

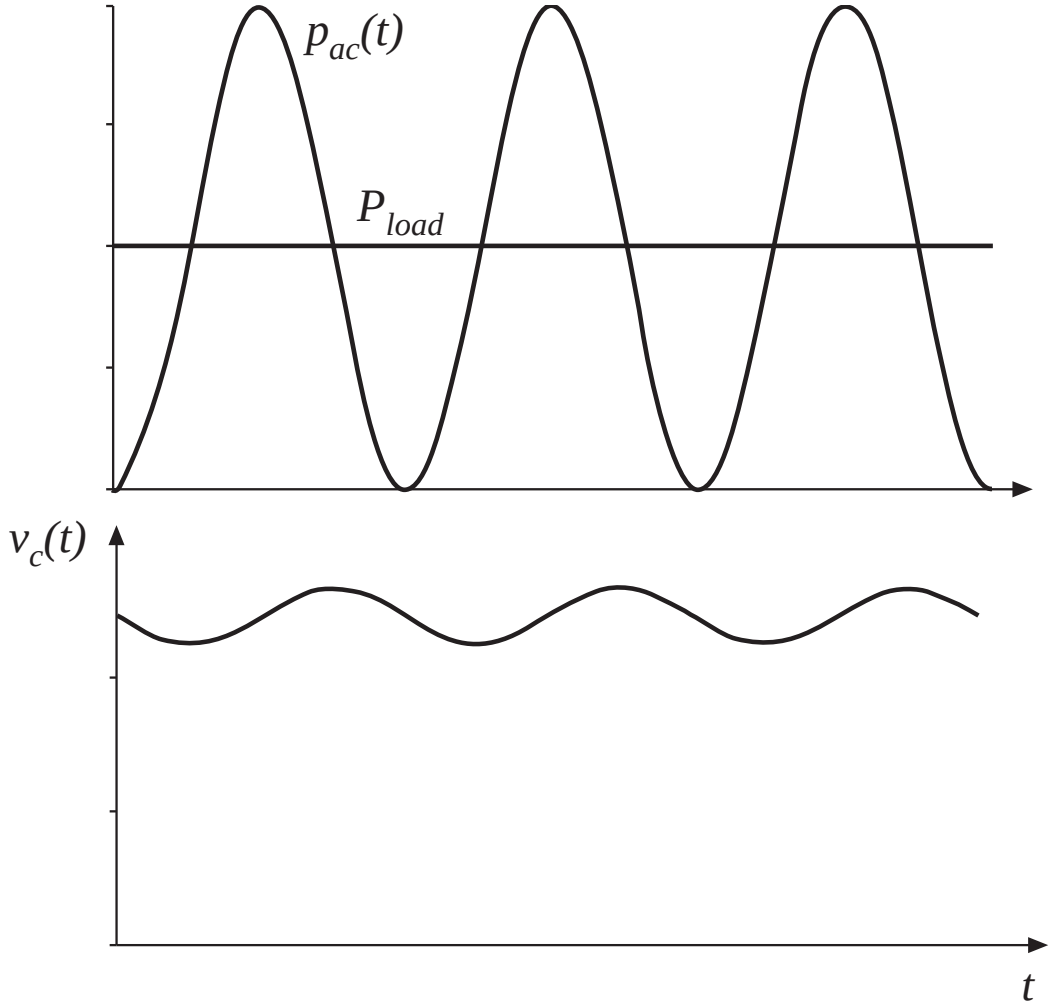
Power flow in single-phase ideal rectifier system

- Ideal rectifier is lossless, and contains no internal energy storage.
- Hence instantaneous input and output powers must be equal
- An energy storage element must be added
- Capacitor energy storage: instantaneous power flowing into capacitor is equal to difference between input and output powers:

$$p_C(t) = \frac{dE_C(t)}{dt} = \frac{d\left(\frac{1}{2} C v_C^2(t)\right)}{dt} = p_{ac}(t) - p_{load}(t)$$

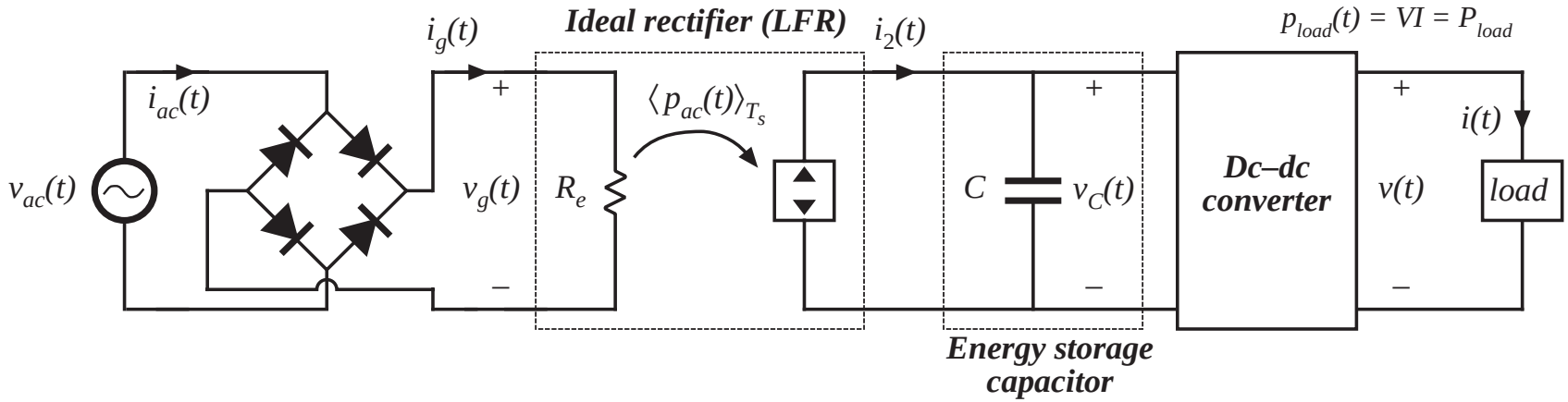
Energy storage capacitor voltage must be allowed to vary, in accordance with this equation

Capacitor energy storage in 1ø system



$$\frac{d\left(\frac{1}{2} C v_C^2(t)\right)}{dt} = p_{ac}(t) - p_{load}(t)$$

Single-phase system with internal energy storage



Energy storage capacitor voltage $v_C(t)$ must be independent of input and output voltage waveforms, so that it can vary according to

$$\frac{d\left(\frac{1}{2} C v_C^2(t)\right)}{dt} = p_{ac}(t) - p_{load}(t)$$

This system is capable of

- Wide-bandwidth control of output voltage
- Wide-bandwidth control of input current waveform
- Internal independent energy storage

Hold up time

Internal energy storage allows the system to function in other situations where the instantaneous input and output powers differ.

A common example: continue to supply load power in spite of failure of ac line for short periods of time.

Hold up time: the duration which the dc output voltage $v(t)$ remains regulated after $v_{ac}(t)$ has become zero

A typical hold-up time requirement: supply load for one complete missing ac line cycle, or 20msec in a 50Hz system

During the hold-up time, the load power is supplied entirely by the energy storage capacitor

Energy storage element

Instead of a capacitor, and inductor or higher-order LC network could store the necessary energy.

But, inductors are not good energy-storage elements

Example

100V 100μF capacitor

100A 100μH inductor

each store 1 Joule of energy

But the capacitor is considerably smaller, lighter, and less expensive

So a single big capacitor is the best solution

Inrush current

A problem caused by the large energy storage capacitor: the large inrush current observed during system startup, necessary to charge the capacitor to its equilibrium value.

Boost converter is not capable of controlling this inrush current.

Even with $d = 0$, a large current flows through the boost converter diode to the capacitor, as long as $v(t) < v_g(t)$.

Additional circuitry is needed to limit the magnitude of this inrush current.

Converters having buck-boost characteristics are capable of controlling the inrush current. Unfortunately, these converters exhibit higher transistor stresses.

Universal input

The capability to operate from the ac line voltages and frequencies found everywhere in the world:

50Hz and 60Hz

Nominal rms line voltages of 100V to 260V:

100V, 110V, 115V, 120V, 132V, 200V, 220V, 230V, 240V, 260V

Regardless of the input voltage and frequency, the near-ideal rectifier produces a constant nominal dc output voltage. With a boost converter, this voltage is 380 or 400V.

Low-frequency model of dc-dc converter

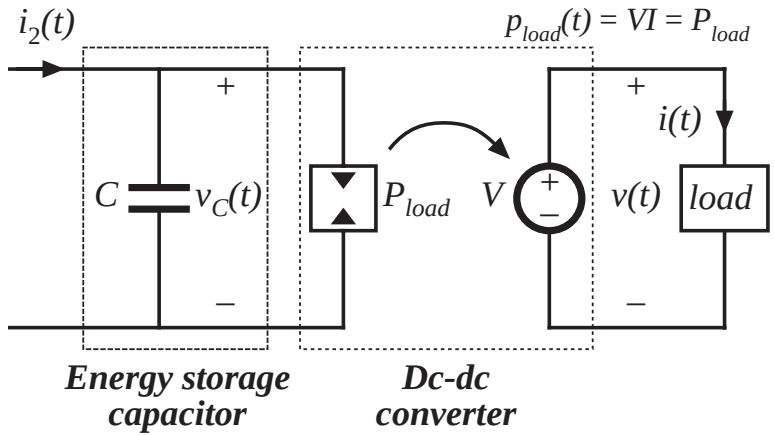
Dc-dc converter produces well-regulated dc load voltage V.

Load therefore draws constant current I.

Load power is therefore the constant value $P_{load} = VI$.

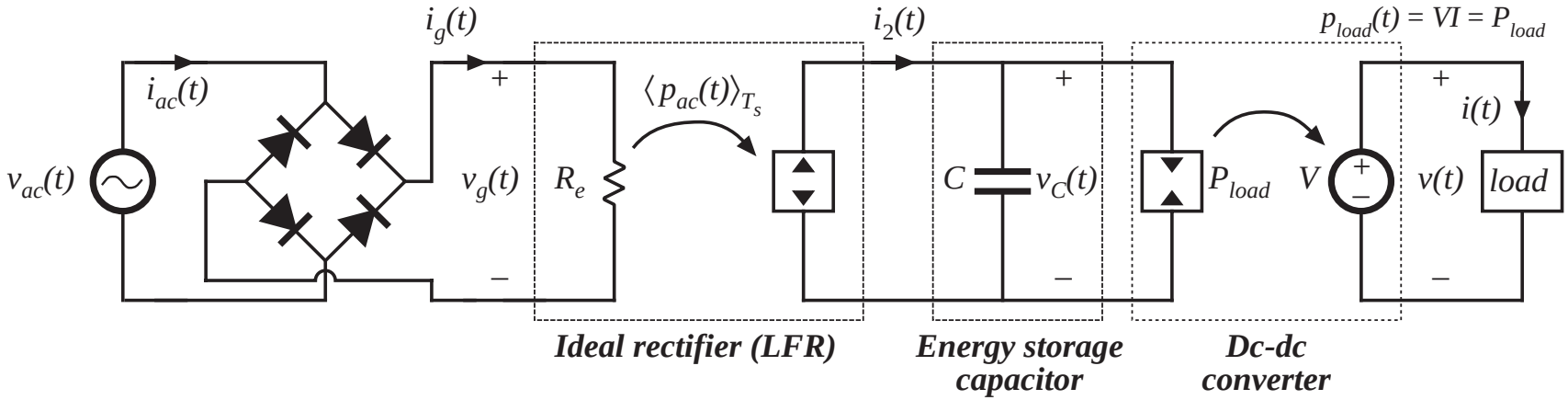
To the extent that dc-dc converter losses can be neglected, then dc-dc converter input power is P_{load} , regardless of capacitor voltage $v_c(t)$.

Dc-dc converter input port behaves as a power sink. A low frequency converter model is



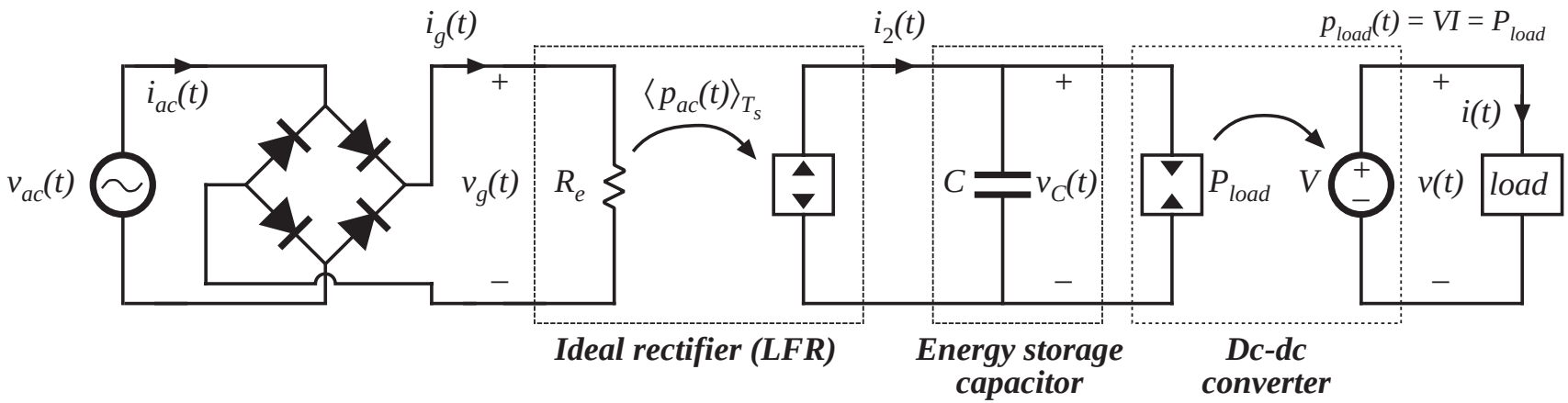
Low-frequency energy storage process, 1ø system

A complete low-frequency system model:



- Difference between rectifier output power and dc-dc converter input power flows into capacitor
- In equilibrium, average rectifier and load powers must be equal
- But the system contains no mechanism to accomplish this
- An additional feeback loop is necessary, to adjust R_e such that the rectifier average power is equal to the load power

Obtaining average power balance

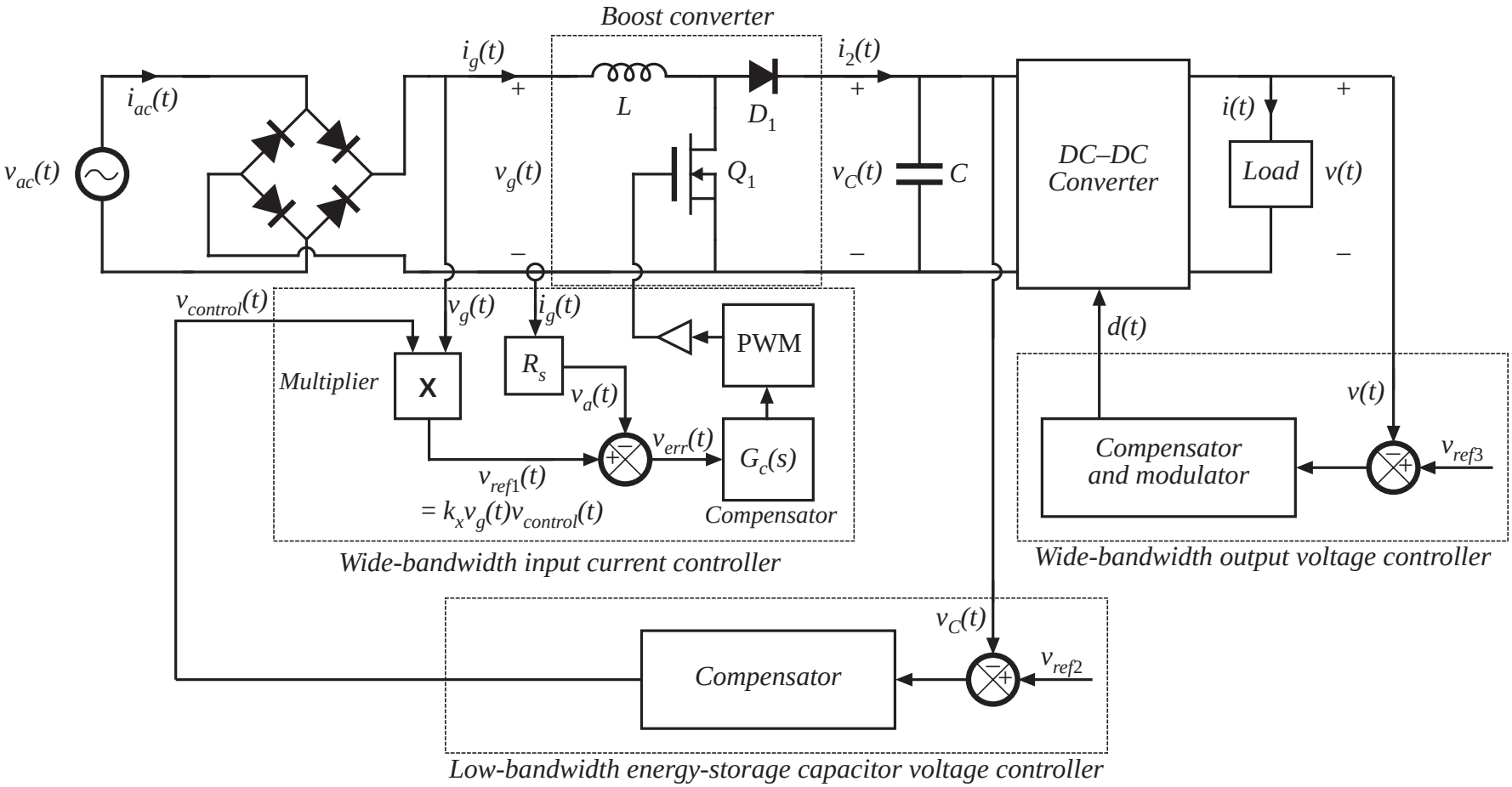


If the load power exceeds the average rectifier power, then there is a net discharge in capacitor energy and voltage over one ac line cycle.

There is a net increase in capacitor charge when the reverse is true.

This suggests that rectifier and load powers can be balanced by regulating the energy storage capacitor voltage.

A complete 1ø system
containing three feedback loops



Bandwidth of capacitor voltage loop

- The energy-storage-capacitor voltage feedback loop causes the dc component of $v_c(t)$ to be equal to some reference value
- Average rectifier power is controlled by variation of R_e.
- R_e must not vary too quickly; otherwise, ac line current harmonics are generated
- Extreme limit: loop has infinite bandwidth, and $v_c(t)$ is perfectly regulated to be equal to a constant reference value
  - Energy storage capacitor voltage then does not change, and this capacitor does not store or release energy
  - Instantaneous load and ac line powers are then equal
  - Input current becomes

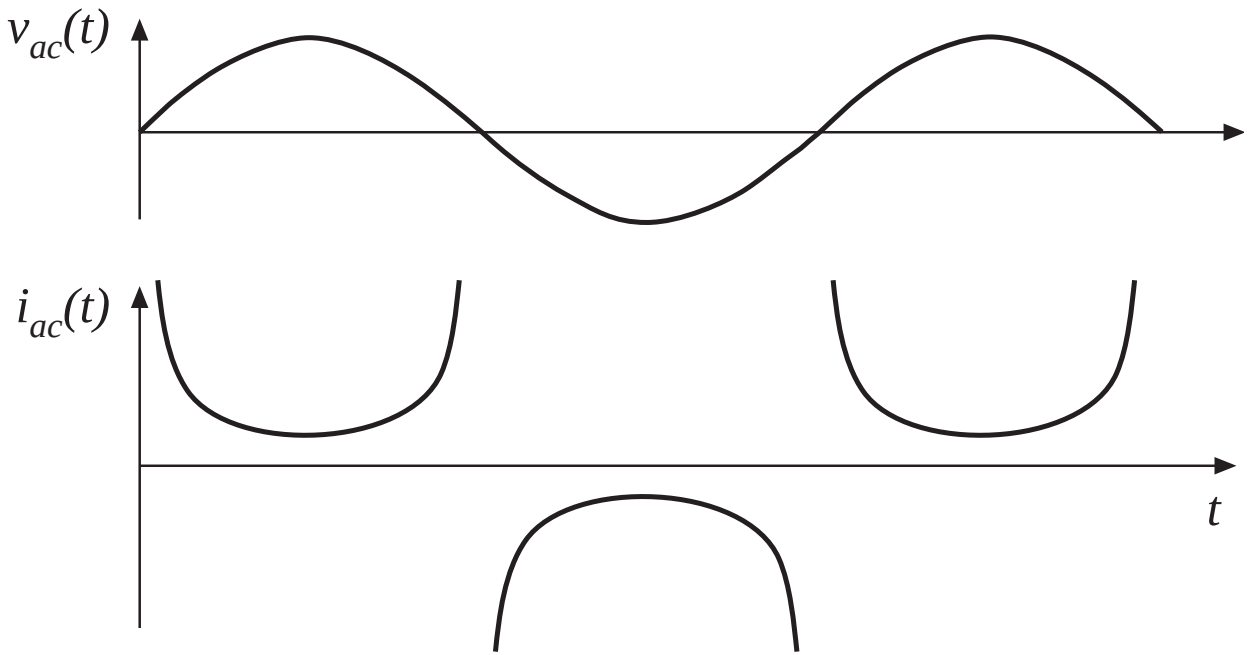
$$i_{ac}(t) = \frac{p_{ac}(t)}{v_{ac}(t)} = \frac{p_{load}(t)}{v_{ac}(t)} = \frac{P_{load}}{V_M \sin\left(\omega t\right)}$$

Input current waveform, extreme limit

$$i_{ac}(t) = \frac{p_{ac}(t)}{v_{ac}(t)} = \frac{p_{load}(t)}{v_{ac}(t)} = \frac{P_{load}}{V_M \sin\left(\omega t\right)}$$

THD → ∞

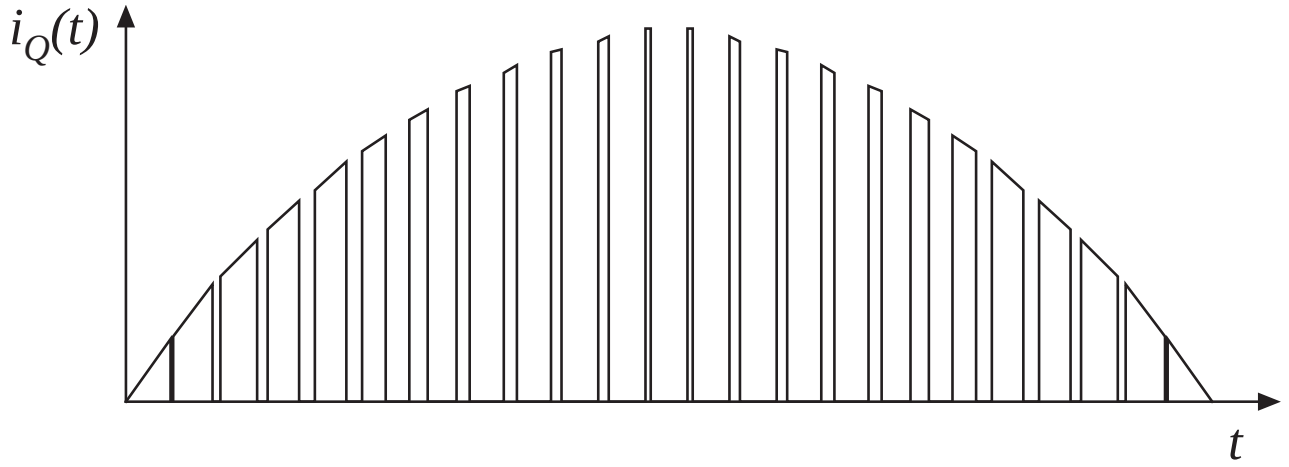
Power factor → 0



So bandwidth of capacitor voltage loop must be limited, and THD increases rapidly with increasing bandwidth

17.4 RMS values of rectifier waveforms

Doubly-modulated transistor current waveform, boost rectifier:



Computation of rms value of this waveform is complex and tedious

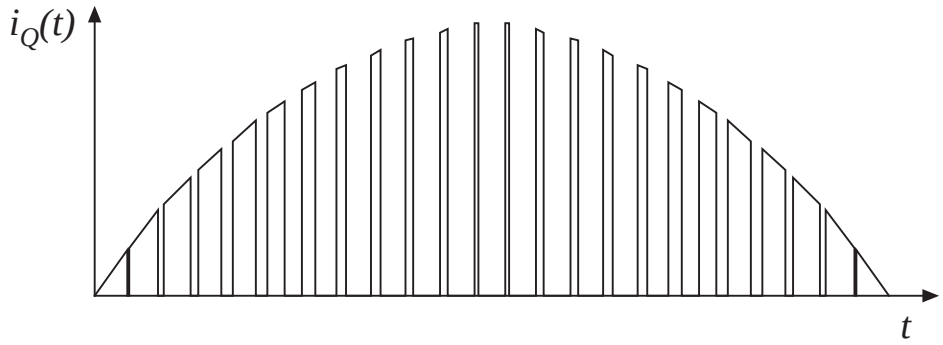
Approximate here using double integral

Generate tables of component rms and average currents for various rectifier converter topologies, and compare

RMS transistor current

RMS transistor current is

$$I_{Qrms} = \sqrt{\frac{1}{T_{ac}} \int_0^{T_{ac}} i_Q^2(t)\, dt}$$



Express as sum of integrals over all switching periods contained in one ac line period:

$$I_{Qrms} = \sqrt{\frac{1}{T_{ac}} T_s \sum_{n=1}^{T_{ac}/T_s} \left(\frac{1}{T_s} \int_{(n\text{-}1)T_s}^{nT_s} i_Q^2(t)\, dt \right)}$$

Quantity in parentheses is the value of i_Q^2, averaged over the n^{th} switching period.

Approximation of RMS expression

$$I_{Qrms} = \sqrt{\frac{1}{T_{ac}} T_s \sum_{n=1}^{T_{ac}/T_s} \left(\frac{1}{T_s} \int_{(n\text{-}1)T_s}^{nT_s} i_Q^2(t)\,dt \right)}$$

When $T_s << T_{ac}$, then the summation can be approximated by an integral, which leads to the double-average:

$$I_{Qrms} \approx \sqrt{\frac{1}{T_{ac}} \lim_{T_s \to 0} \left[T_s \sum_{n=1}^{T_{ac}/T_s} \left(\frac{1}{T_s} \int_{(n\text{-}1)T_s}^{nT_s} i_Q^2(\tau)\,d\tau \right) \right]}$$

$$= \sqrt{\frac{1}{T_{ac}} \int_0^{T_{ac}} \frac{1}{T_s} \int_t^{t+T_s} i_Q^2(\tau)\,d\tau\,dt}$$

$$= \sqrt{\left\langle \left\langle i_Q^2(t) \right\rangle_{T_s} \right\rangle_{T_{ac}}}$$

17.4.1 Boost rectifier example

For the boost converter, the transistor current $i_Q(t)$ is equal to the input current when the transistor conducts, and is zero when the transistor is off. The average over one switching period of $i_Q^2(t)$ is therefore

$$\left\langle i_Q^2 \right\rangle_{T_s} = \frac{1}{T_s} \int_t^{t+T_s} i_Q^2(t)\, dt$$

$$= d(t) i_{ac}^2(t)$$

If the input voltage is

$$v_{ac}(t) = V_M \left| \sin \omega t \right|$$

then the input current will be given by

$$i_{ac}(t) = \frac{V_M}{R_e} \left| \sin \omega t \right|$$

and the duty cycle will ideally be

$$\frac{V}{v_{ac}(t)} = \frac{1}{1 - d(t)}$$

(this neglects converter dynamics)

Boost rectifier example

Duty cycle is therefore

$$d(t) = 1 - \frac{V_M}{V} \left| \sin \omega t \right|$$

Evaluate the first integral:

$$\left\langle i_Q^2 \right\rangle_{T_s} = \frac{V_M^2}{R_e^2} \left(1 - \frac{V_M}{V} \left| \sin \omega t \right| \right) \sin^2 \left(\omega t \right)$$

Now plug this into the RMS formula:

$$I_{Qrms} = \sqrt{\frac{1}{T_{ac}} \int_0^{T_{ac}} \left\langle i_Q^2 \right\rangle_{T_s} dt}$$

$$= \sqrt{\frac{1}{T_{ac}} \int_0^{T_{ac}} \frac{V_M^2}{R_e^2} \left(1 - \frac{V_M}{V} \left| \sin \omega t \right| \right) \sin^2 \left(\omega t \right) dt}$$

$$I_{Qrms} = \sqrt{\frac{2}{T_{ac}} \frac{V_M^2}{R_e^2} \int_0^{T_{ac}/2} \left(\sin^2 \left(\omega t \right) - \frac{V_M}{V} \sin^3 \left(\omega t \right) \right) dt}$$

Integration of powers of sin θ over complete half-cycle

$$\frac{1}{\pi}\int_0^{\pi} sin^n(\theta)d\theta = \begin{cases} \frac{2}{\pi}\frac{2\cdot 4\cdot 6\cdots(n-1)}{1\cdot 3\cdot 5\cdots n} & \text{if } n \text{ is odd} \\ \frac{1\cdot 3\cdot 5\cdots(n-1)}{2\cdot 4\cdot 6\cdots n} & \text{if } n \text{ is even} \end{cases}$$

n	$\frac{1}{\pi}\int_0^{\pi} sin^n(\theta)d\theta$
1	$\frac{2}{\pi}$
2	$\frac{1}{2}$
3	$\frac{4}{3\pi}$
4	$\frac{3}{8}$
5	$\frac{16}{15\pi}$
6	$\frac{15}{48}$

Boost example: Transistor RMS current

$$I_{Qrms} = \frac{V_M}{\sqrt{2} R_e} \sqrt{1 - \frac{8}{3\pi} \frac{V_M}{V}} = I_{ac\ rms} \sqrt{1 - \frac{8}{3\pi} \frac{V_M}{V}}$$

Transistor RMS current is minimized by choosing V as small as possible: $V = V_M$. This leads to

$$I_{Qrms} = 0.39 I_{ac\ rms}$$

When the dc output voltage is not too much greater than the peak ac input voltage, the boost rectifier exhibits very low transistor current. Efficiency of the boost rectifier is then quite high, and 95% is typical in a 1kW application.

Table of rectifier current stresses for various topologies

Table 17.2 Summary of rectifier current stresses for several converter topologies

	rms	*Average*	*Peak*
CCM boost			
Transistor	$I_{ac\,rms}\sqrt{1-\frac{8}{3\pi}\frac{V_M}{V}}$	$I_{ac\,rms}\frac{2\sqrt{2}}{\pi}\left(1-\frac{\pi}{8}\frac{V_M}{V}\right)$	$I_{ac\,rms}\sqrt{2}$
Diode	$I_{dc}\sqrt{\frac{16}{3\pi}\frac{V}{V_M}}$	I_{dc}	$2\,I_{dc}\frac{V}{V_M}$
Inductor	$I_{ac\,rms}$	$I_{ac\,rms}\frac{2\sqrt{2}}{\pi}$	$I_{ac\,rms}\sqrt{2}$
CCM flyback, with *n*:1 isolation transformer and input filter			
Transistor, xfmr primary	$I_{ac\,rms}\sqrt{1+\frac{8}{3\pi}\frac{V_M}{nV}}$	$I_{ac\,rms}\frac{2\sqrt{2}}{\pi}$	$I_{ac\,rms}\sqrt{2}\left(1+\frac{V}{n}\right.$
L_1	$I_{ac\,rms}$	$I_{ac\,rms}\frac{2\sqrt{2}}{\pi}$	$I_{ac\,rms}\sqrt{2}$
C_1	$I_{ac\,rms}\sqrt{\frac{8}{3\pi}\frac{V_M}{nV}}$	0	$I_{ac\,rms}\sqrt{2}\max\left(1,\frac{V_M}{nV}\right.$
Diode, xfmr secondary	$I_{dc}\sqrt{\frac{3}{2}+\frac{16}{3\pi}\frac{nV}{V_M}}$	I_{dc}	$2I_{dc}\left(1+\frac{nV}{V_M}\right)$

Table of rectifier current stresses
continued

CCM SEPIC, nonisolated			
Transistor	$I_{ac\,rms}\sqrt{1+\frac{8}{3\pi}\frac{V_M}{V}}$	$I_{ac\,rms}\frac{2\sqrt{2}}{\pi}$	$I_{ac\,rms}\sqrt{2}\left(1+\frac{V_M}{V}\right.$
L_1	$I_{ac\,rms}$	$I_{ac\,rms}\frac{2\sqrt{2}}{\pi}$	$I_{ac\,rms}\sqrt{2}$
C_1	$I_{ac\,rms}\sqrt{\frac{8}{3\pi}\frac{V_M}{V}}$	0	$I_{ac\,rms}\max\left(1,\frac{V_M}{V}\right.$
L_2	$I_{ac\,rms}\frac{V_M}{V}\frac{\sqrt{3}}{2}$	$\frac{I_{ac\,rms}}{\sqrt{2}}\frac{V_M}{V}$	$I_{ac\,rms}\frac{V_M}{V}\sqrt{2}$
Diode	$I_{dc}\sqrt{\frac{3}{2}+\frac{16}{3\pi}\frac{V}{V_M}}$	I_{dc}	$2I_{dc}\left(1+\frac{V}{V_M}\right)$
CCM SEPIC, with n:1 isolation transformer			
transistor	$I_{ac\,rms}\sqrt{1+\frac{8}{3\pi}\frac{V_M}{nV}}$	$I_{ac\,rms}\frac{2\sqrt{2}}{\pi}$	$I_{ac\,rms}\sqrt{2}\left(1+\frac{V_M}{nV}\right.$
L_1	$I_{ac\,rms}$	$I_{ac\,rms}\frac{2\sqrt{2}}{\pi}$	$I_{ac\,rms}\sqrt{2}$
C_1, xfmr primary	$I_{ac\,rms}\sqrt{\frac{8}{3\pi}\frac{V_M}{nV}}$	0	$I_{ac\,rms}\sqrt{2}\max\left(1,\right.$
Diode, xfmr secondary	$I_{dc}\sqrt{\frac{3}{2}+\frac{16}{3\pi}\frac{nV}{V_M}}$	I_{dc}	$2I_{dc}\left(1+\frac{nV}{V_M}\right)$

with, in all cases, $\frac{I_{ac\,rms}}{I_{dc}}=\sqrt{2}\,\frac{V}{V_M}$, ac input voltage = $V_M\sin(\omega t)$

dc output voltage = V

Comparison of rectifier topologies

Boost converter

- Lowest transistor rms current, highest efficiency
- Isolated topologies are possible, with higher transistor stress
- No limiting of inrush current
- Output voltage must be greater than peak input voltage

Buck-boost, SEPIC, and Cuk converters

- Higher transistor rms current, lower efficiency
- Isolated topologies are possible, without increased transistor stress
- Inrush current limiting is possible
- Output voltage can be greater than or less than peak input voltage

Comparison of rectifier topologies

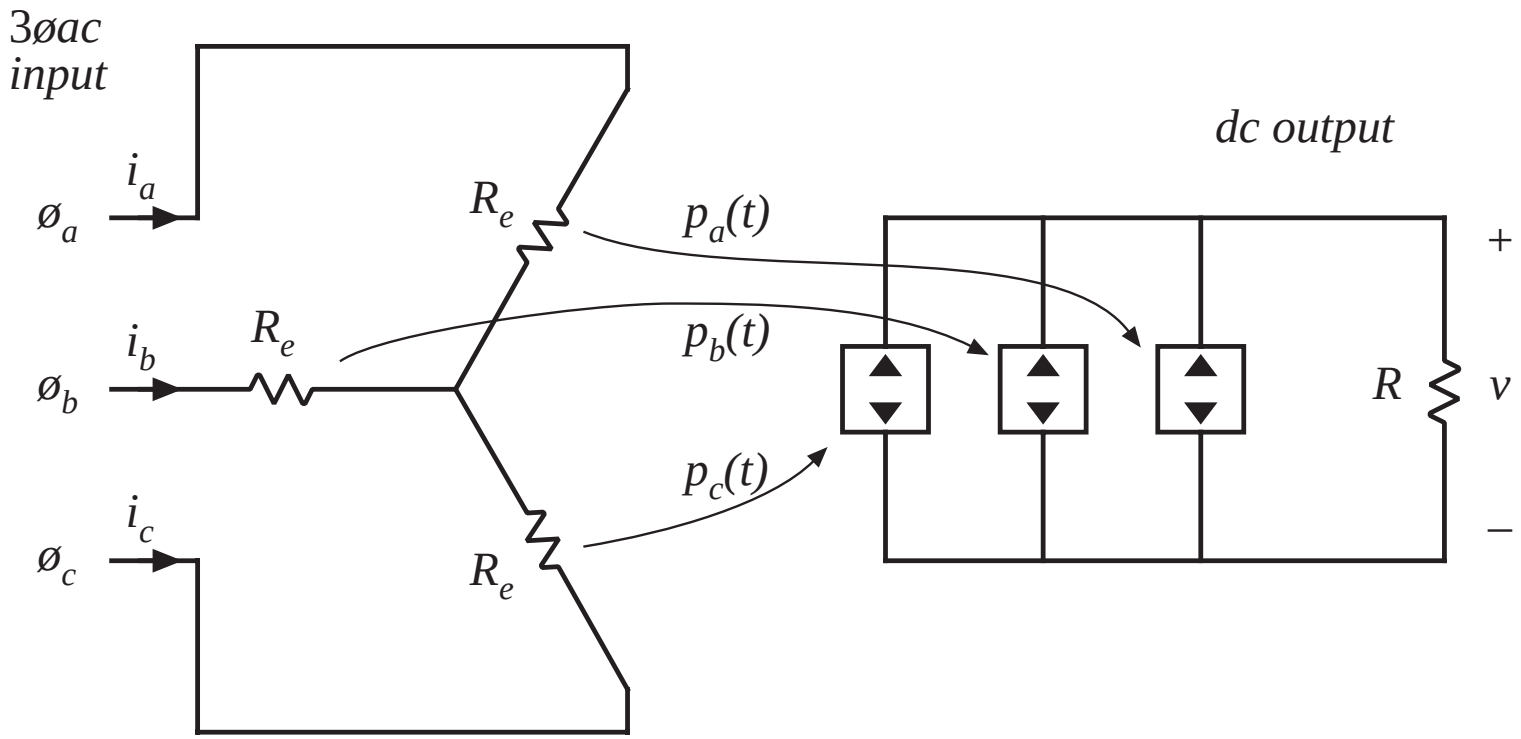
1kW, 240Vrms example. Output voltage: 380Vdc. Input current: 4.2Arms

Converter	Transistor rms current	Transistor voltage	Diode rms current	Transistor rms current, 120V	Diode rms current, 120V
Boost	2 A	380 V	3.6 A	6.6 A	5.1 A
Nonisolated SEPIC	5.5 A	719 V	4.85 A	9.8 A	6.1 A
Isolated SEPIC	5.5 A	719 V	36.4 A	11.4 A	42.5 A

Isolated SEPIC example has 4:1 turns ratio, with 42V 23.8A dc load

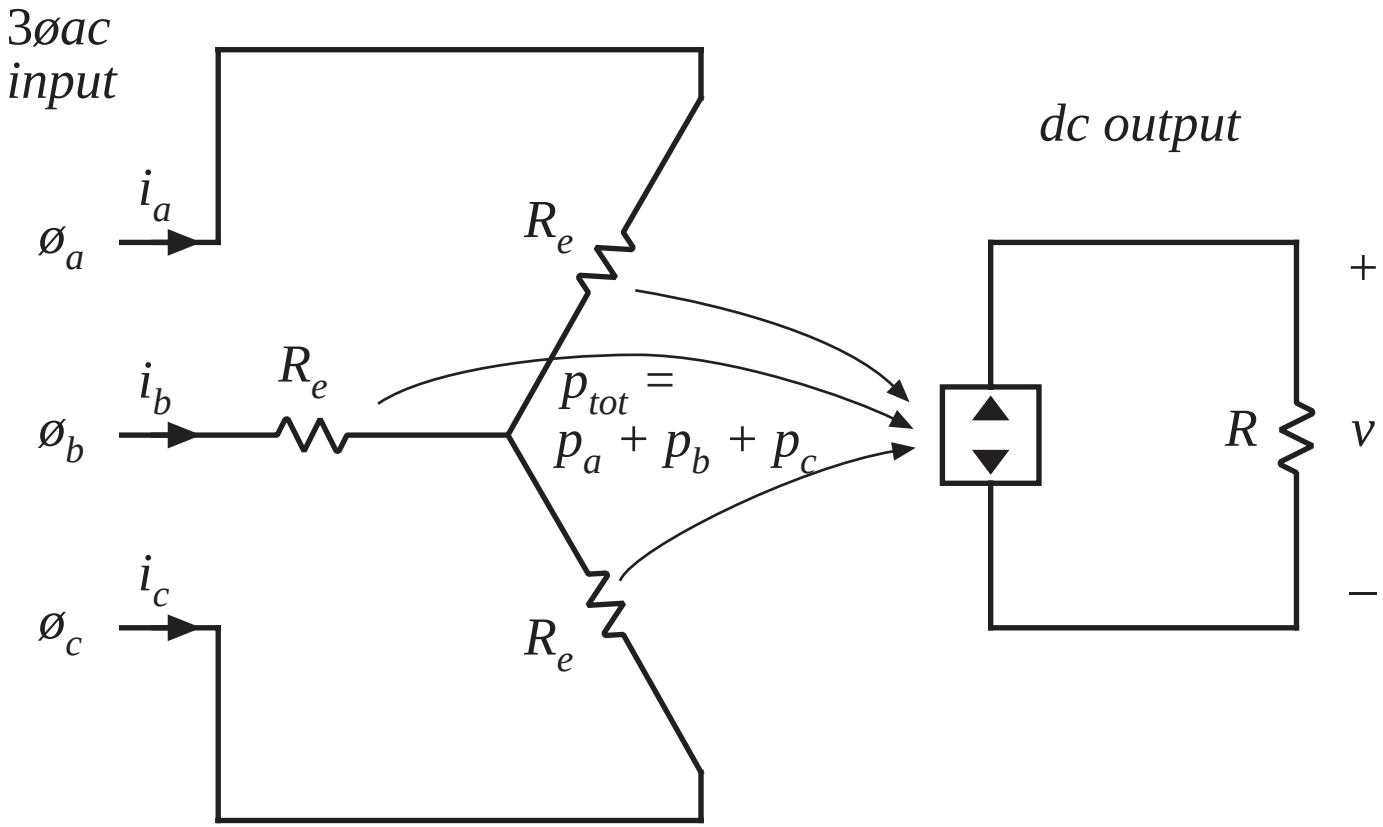
17.5 Ideal three-phase rectifiers

Ideal 3ø rectifier, modeled as three 1ø ideal rectifiers:



Ideal 3ø rectifier model

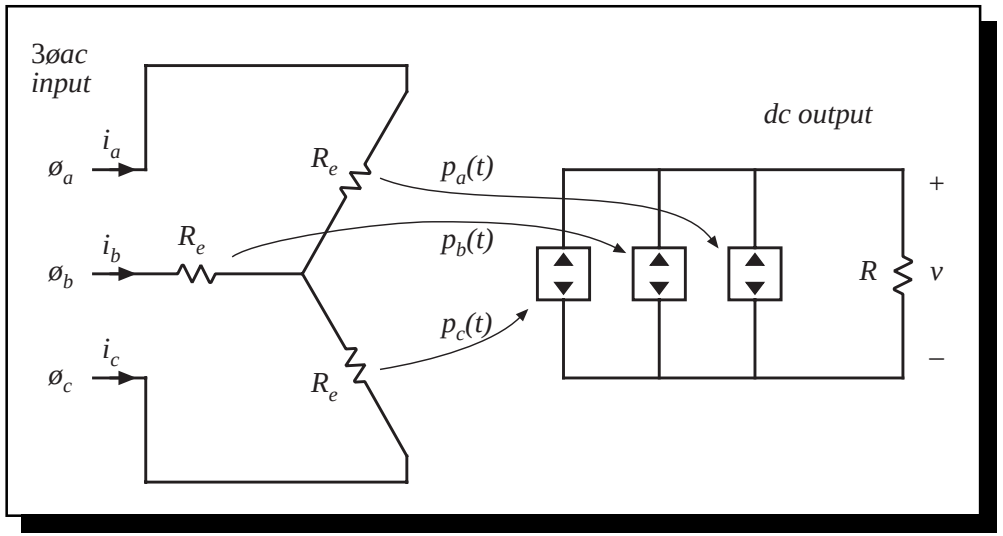
Combine parallel-connected power sources into a single source $p_{tot}(t)$:



Value of $p_{tot}(t)$

Ac input voltages:

$$v_{an}(t) = V_M \sin\left(\omega t\right)$$
$$v_{bn}(t) = V_M \sin\left(\omega t - 120°\right)$$
$$v_{cn}(t) = V_M \sin\left(\omega t - 240°\right)$$



Instantaneous phase powers:

$$p_a(t) = \frac{v_{an}^2(t)}{R_e} = \frac{V_M^2}{2R_e}\left(1 - \cos\left(2\omega t\right)\right)$$
$$p_b(t) = \frac{v_{bn}^2(t)}{R_e} = \frac{V_M^2}{2R_e}\left(1 - \cos\left(2\omega t - 240°\right)\right)$$
$$p_c(t) = \frac{v_{cn}^2(t)}{R_e} = \frac{V_M^2}{2R_e}\left(1 - \cos\left(2\omega t - 120°\right)\right)$$

Total 3ø instantaneous power:

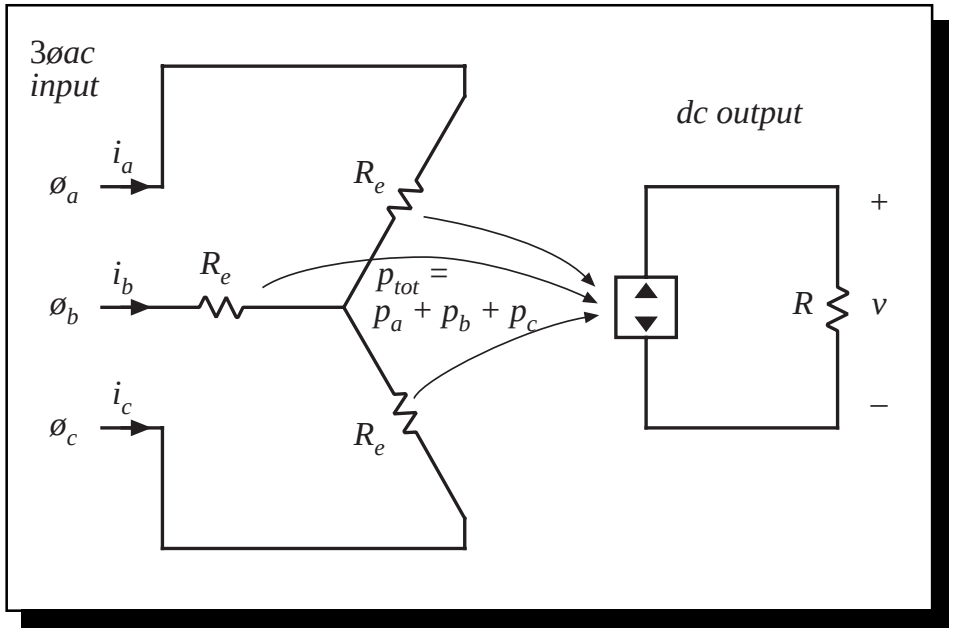
$$p_{tot}(t) = p_a(t) + p_b(t) + p_c(t) = \frac{3}{2}\frac{V_M^2}{R_e}$$

- 2nd harmonic terms add to zero
- total 3ø power $p_{tot}(t)$ is constant

Instantaneous power in ideal 3ø rectifier

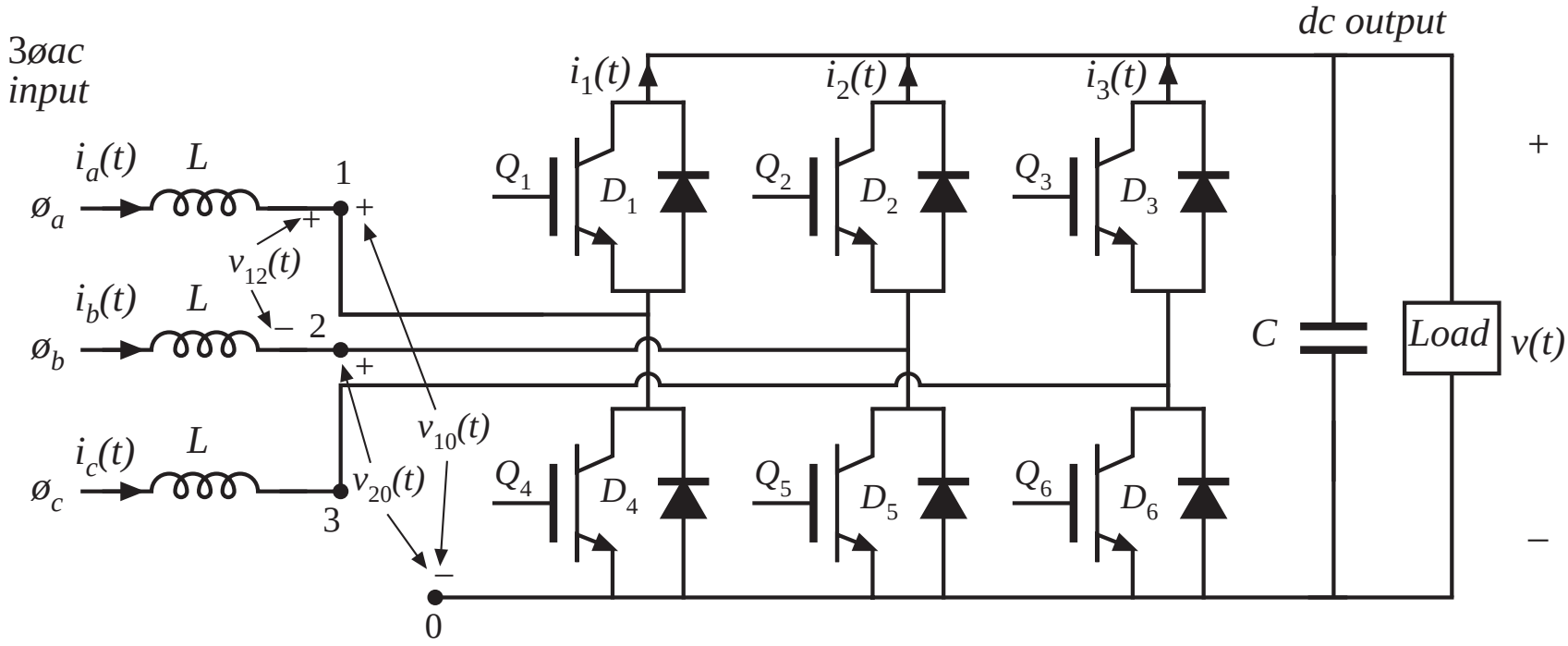
$$p_{tot}(t) = p_a(t) + p_b(t) + p_c(t) = \frac{3}{2}\frac{V_M^2}{R_e}$$

- In a balanced system, the ideal 3ø rectifier supplies constant power to its dc output
- a constant power load can be supplied, without need for low-frequency internal energy storage



17.5.1 Three-phase rectifiers operating in CCM

3øac–dc boost rectifier



- Uses six current-bidirectional switches
- Operation of each individual phase is similar to the 1ø boost rectifier

The 3øac–dc boost rectifier

- Voltage-source inverter, operated backwards as a rectifier
- Converter is capable of bidirectional power flow
- Dc output voltage V must be greater than peak ac line-line voltage $V_{L,pk}$.
- Ac input currents are nonpulsating. In CCM, input EMI filtering is relatively easy
- Very low RMS transistor currents and conduction loss
- The leading candidate to replace uncontrolled 3ø rectifiers
- Requires six active devices
- Cannot regulate output voltage down to zero:

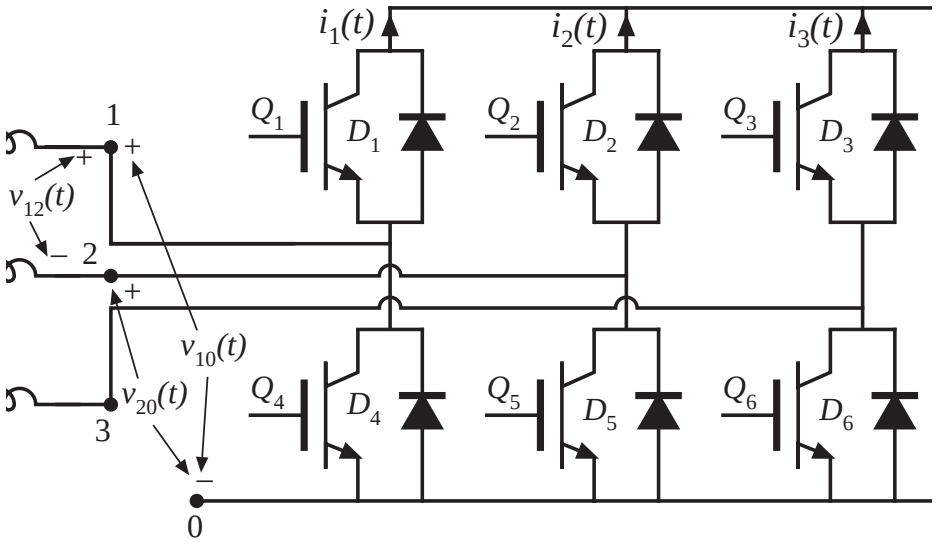
  no current limiting

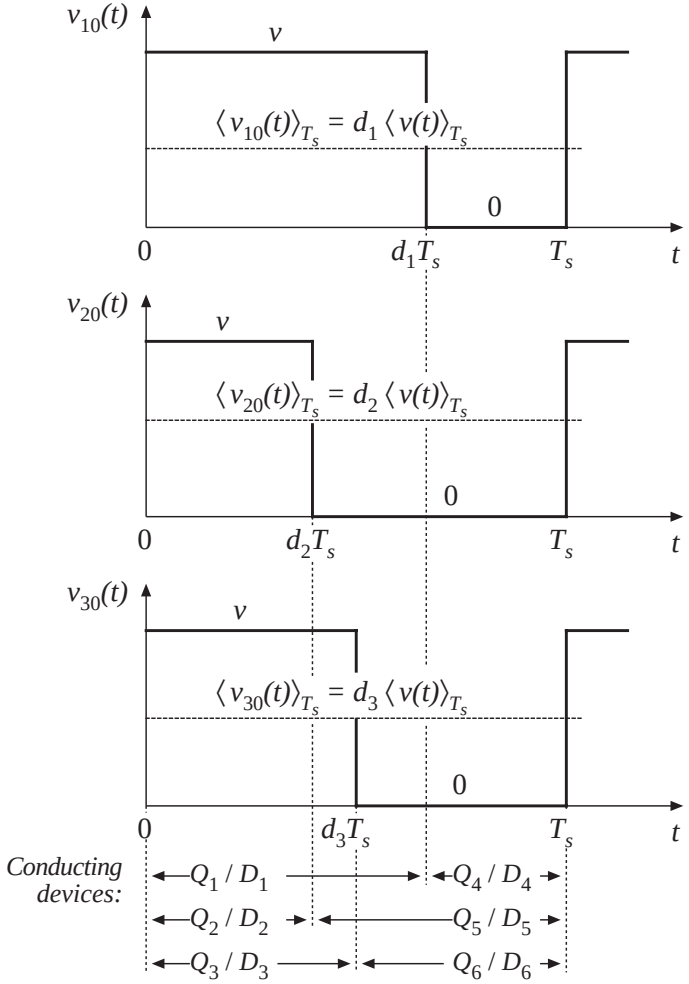
  cannot replace traditional buck-type controlled rectifiers

Control of switches in CCM 3øac-dc boost rectifier

Pulse-width modulation:

Drive lower transistors ($Q_4 - Q_6$) with complements of duty cycles of respective upper transistors ($Q_1 - Q_3$). Each phase operates independently, with its own duty cycle.





Average switch waveforms

Average the switch voltages:

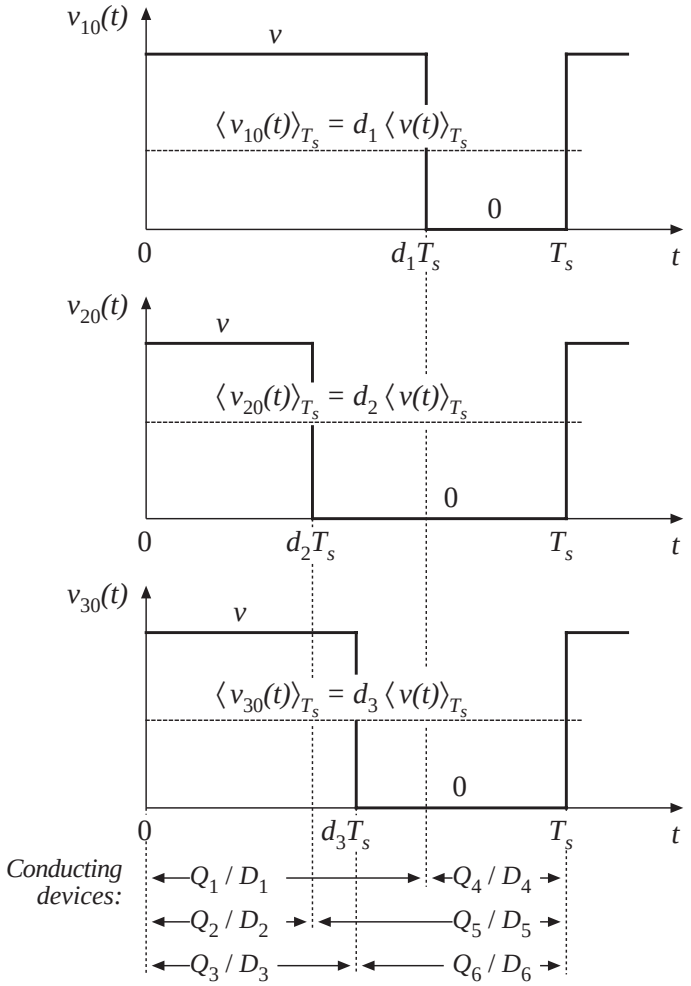
$$\left\langle v_{10}(t) \right\rangle_{T_s} = d_1(t) \left\langle v(t) \right\rangle_{T_s}$$
$$\left\langle v_{20}(t) \right\rangle_{T_s} = d_2(t) \left\langle v(t) \right\rangle_{T_s}$$
$$\left\langle v_{30}(t) \right\rangle_{T_s} = d_3(t) \left\langle v(t) \right\rangle_{T_s}$$

Average line-line voltages:

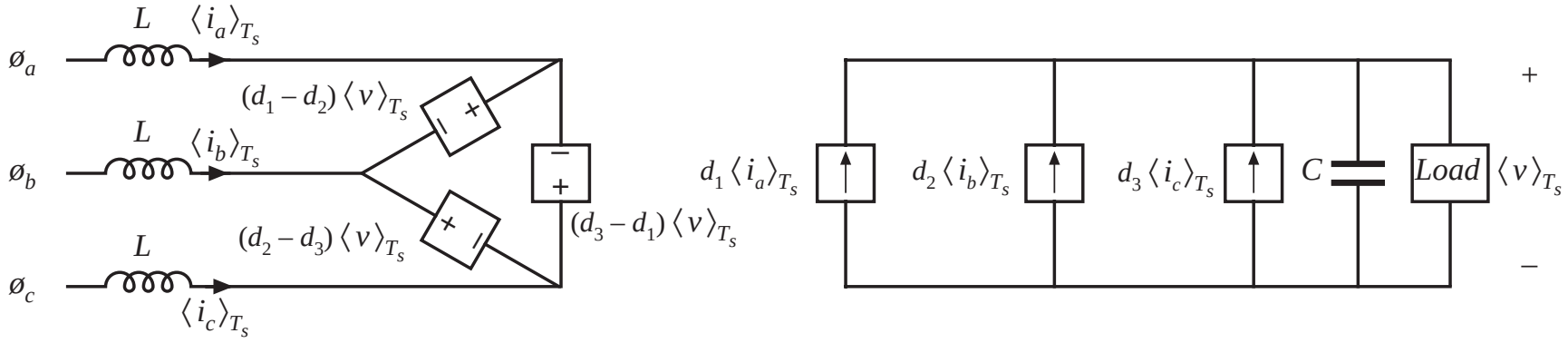
$$\left\langle v_{12}(t) \right\rangle_{T_s} = \left\langle v_{10}(t) \right\rangle_{T_s} - \left\langle v_{20}(t) \right\rangle_{T_s} = \left(d_1(t) - d_2(t) \right) \left\langle v(t) \right\rangle_{T_s}$$
$$\left\langle v_{23}(t) \right\rangle_{T_s} = \left\langle v_{20}(t) \right\rangle_{T_s} - \left\langle v_{30}(t) \right\rangle_{T_s} = \left(d_2(t) - d_3(t) \right) \left\langle v(t) \right\rangle_{T_s}$$
$$\left\langle v_{31}(t) \right\rangle_{T_s} = \left\langle v_{30}(t) \right\rangle_{T_s} - \left\langle v_{10}(t) \right\rangle_{T_s} = \left(d_3(t) - d_1(t) \right) \left\langle v(t) \right\rangle_{T_s}$$

Average switch output-side currents:

$$\left\langle i_1(t) \right\rangle_{T_s} = d_1(t) \left\langle i_a(t) \right\rangle_{T_s}$$
$$\left\langle i_2(t) \right\rangle_{T_s} = d_2(t) \left\langle i_b(t) \right\rangle_{T_s}$$
$$\left\langle i_3(t) \right\rangle_{T_s} = d_3(t) \left\langle i_c(t) \right\rangle_{T_s}$$



Averaged circuit model



$$\left\langle v_{12}(t)\right\rangle_{T_s} = \left\langle v_{10}(t)\right\rangle_{T_s} - \left\langle v_{20}(t)\right\rangle_{T_s} = \left(d_1(t) - d_2(t)\right)\left\langle v(t)\right\rangle_{T_s}$$

$$\left\langle v_{23}(t)\right\rangle_{T_s} = \left\langle v_{20}(t)\right\rangle_{T_s} - \left\langle v_{30}(t)\right\rangle_{T_s} = \left(d_2(t) - d_3(t)\right)\left\langle v(t)\right\rangle_{T_s}$$

$$\left\langle v_{31}(t)\right\rangle_{T_s} = \left\langle v_{30}(t)\right\rangle_{T_s} - \left\langle v_{10}(t)\right\rangle_{T_s} = \left(d_3(t) - d_1(t)\right)\left\langle v(t)\right\rangle_{T_s}$$

$$\left\langle i_1(t)\right\rangle_{T_s} = d_1(t)\left\langle i_a(t)\right\rangle_{T_s}$$

$$\left\langle i_2(t)\right\rangle_{T_s} = d_2(t)\left\langle i_b(t)\right\rangle_{T_s}$$

$$\left\langle i_3(t)\right\rangle_{T_s} = d_3(t)\left\langle i_c(t)\right\rangle_{T_s}$$

Q: How to vary $d(t)$ such that the desired ac and dc waveforms are obtained?

Solution is not unique.

Sinusoidal PWM

A simple modulation scheme: Sinusoidal PWM

Vary duty cycles sinusoidally, in synchronism with ac line

$$d_1(t) = D_0 + \tfrac{1}{2} D_m \sin\left(\omega t - \varphi\right)$$

$$d_2(t) = D_0 + \tfrac{1}{2} D_m \sin\left(\omega t - \varphi - 120°\right)$$

$$d_3(t) = D_0 + \tfrac{1}{2} D_m \sin\left(\omega t - \varphi - 240°\right)$$

where

ω is the ac line frequency

D_0 is a dc bias

D_m is the *modulation index*

For $D_0 = 0.5$, D_m in the above equations must be less than 1.

The modulation index is defined as one-half of the peak amplitude of the fundamental component of the duty cycle modulation. In some other modulation schemes, it is possible that $D_m > 1$.

Solution, linear sinusoidal PWM

If the switching frequency is high, then the inductors can be small and have negligible effect at the ac line frequency. The averaged switch voltage and ac line voltage are then equal:

$$\left\langle v_{12}(t) \right\rangle_{T_s} = \left(d_1(t) - d_2(t) \right) \left\langle v(t) \right\rangle_{T_s} \approx v_{ab}(t)$$

Substitute expressions for duty cycle and ac line voltage variations:

$$\tfrac{1}{2} D_m \left[\sin\left(\omega t - \varphi\right) - \sin\left(\omega t - \varphi - 120^\circ\right) \right] \left\langle v(t) \right\rangle_{T_s} = V_M \left[\sin\left(\omega t\right) - \sin\left(\omega t - 120^\circ\right) \right]$$

For small L, φ tends to zero. The expression then becomes

$$\tfrac{1}{2} D_m V = V_M$$

Solve for the output voltage:

$$V = \frac{2V_M}{D_m} \qquad V = \frac{2}{\sqrt{3}} \frac{V_{L,pk}}{D_m} = 1.15 \frac{V_{L,pk}}{D_m}$$

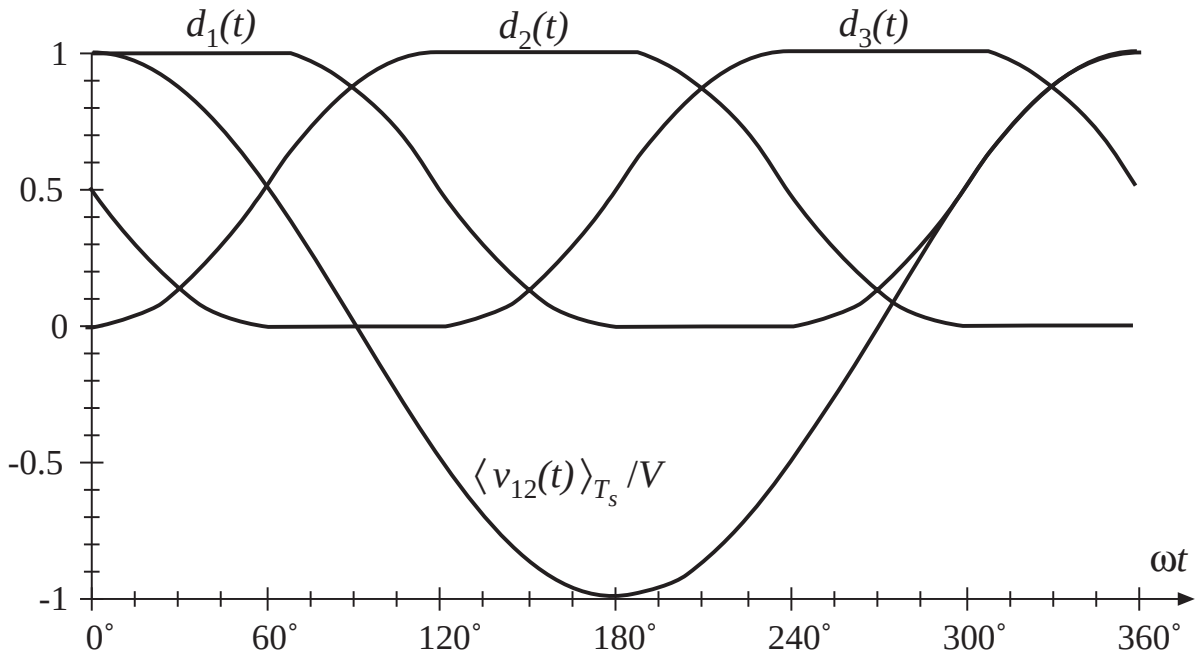
Boost rectifier with sinusoidal PWM

$$V = \frac{2}{\sqrt{3}} \frac{V_{L,pk}}{D_m} = 1.15 \frac{V_{L,pk}}{D_m}$$

With sinusoidal PWM, the dc output voltage must be greater than 1.15 times the peak line-line input voltage. Hence, the boost rectifier increases the voltage magnitude.

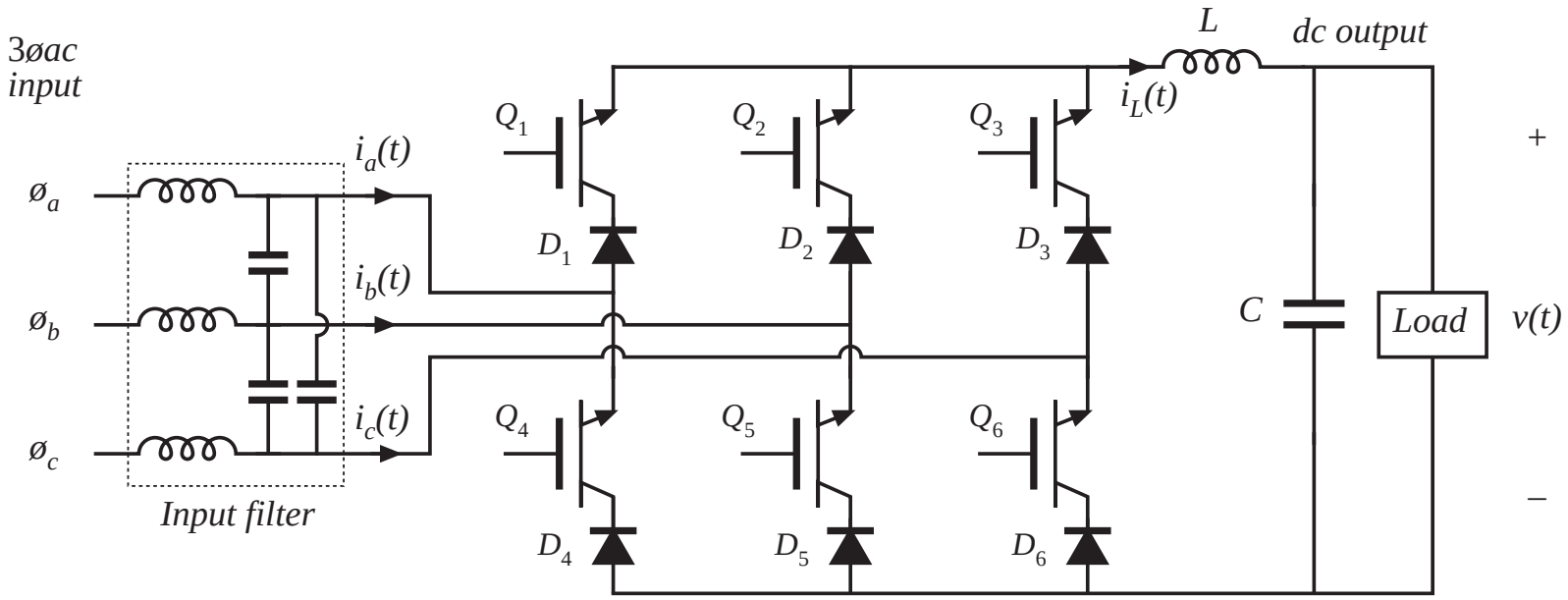
Nonlinear modulation

- Triplen harmonics can be added to the duty ratio modulation, without appearing in the line-line voltages.
- *Overmodulation*, in which the modulation index D_m is increased beyond 1, also



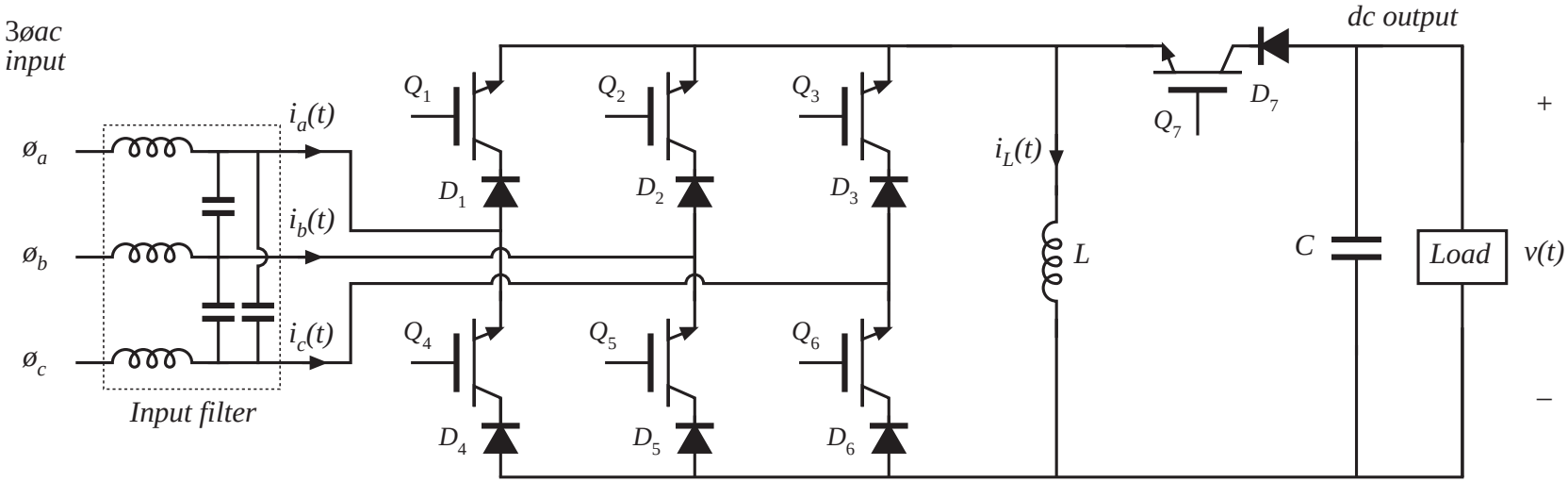
leads to undistorted line-line voltages provided that $D_m \leq 1.15$. The pulse width modulator saturates, but the duty ratio variations contain only triplen harmonics. $V = V_{L,pk}$ is obtained at $D_m = 1.15$. Further increases in D_m cause distorted ac line waveforms.

Buck-type 3øac–dc rectifier

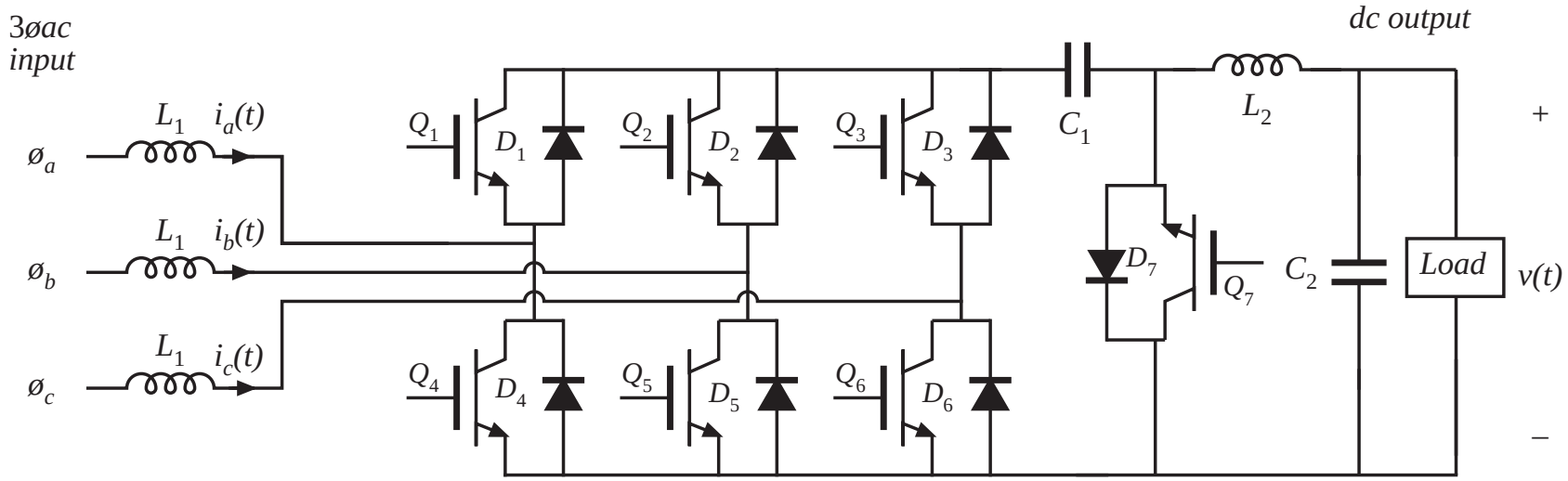


- Can produce controlled dc output voltages in the range $0 \le V \le V_{L,pk}$
- Requires two-quadrant voltage-bidirectional switches
- Exhibits greater active semiconductor stress than boost topology
- Can operate in inverter mode by reversal of output voltage polarity

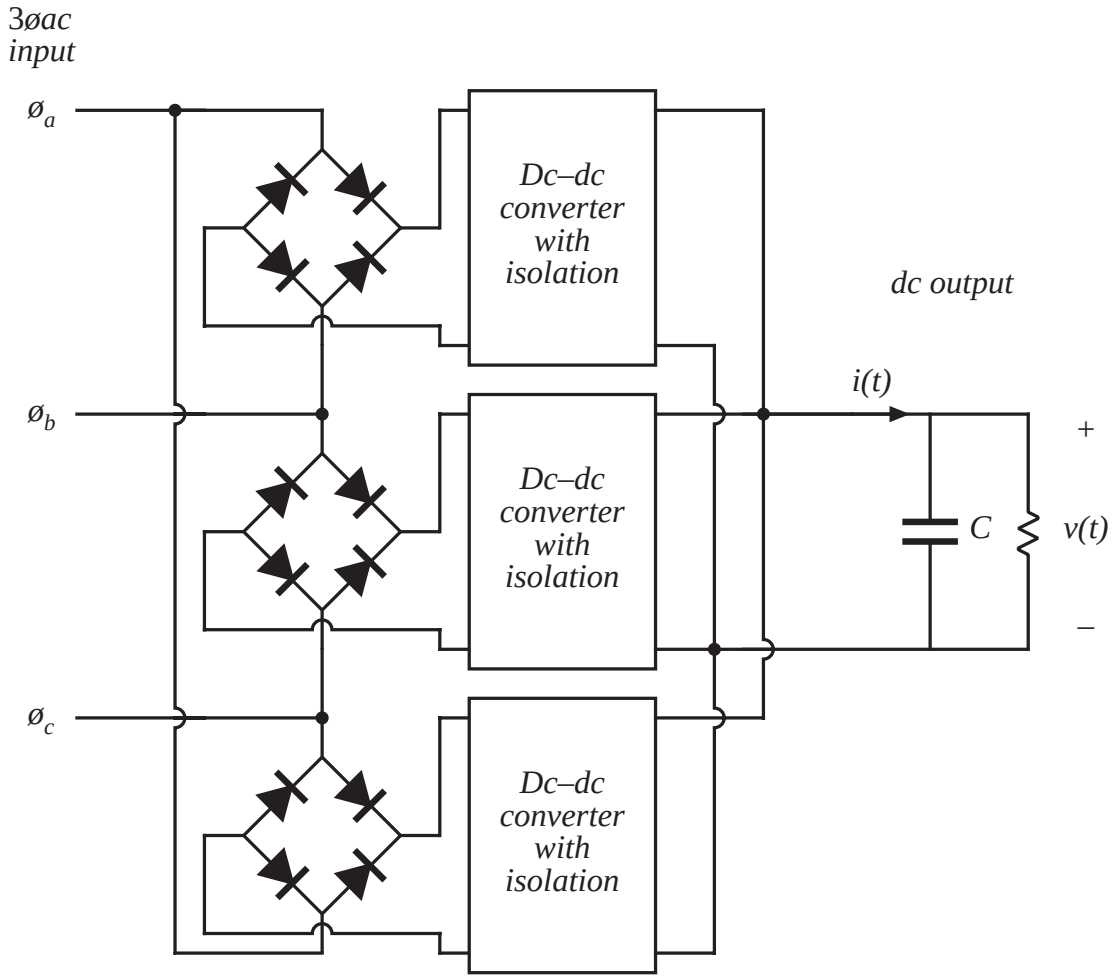
Buck–boost topology



Cuk topology



Use of three single-phase rectifiers



- Each rectifier must include isolation between input and output
- Isolation transformers must be rated to carry the pulsating single-phase ac power $p_{ac}(t)$
- Outputs can be connected in series or parallel
- Because of the isolation requirement, semiconductor stresses are greater than in 3ø boost rectifier

17.5.2 Some other approaches to three-phase rectification

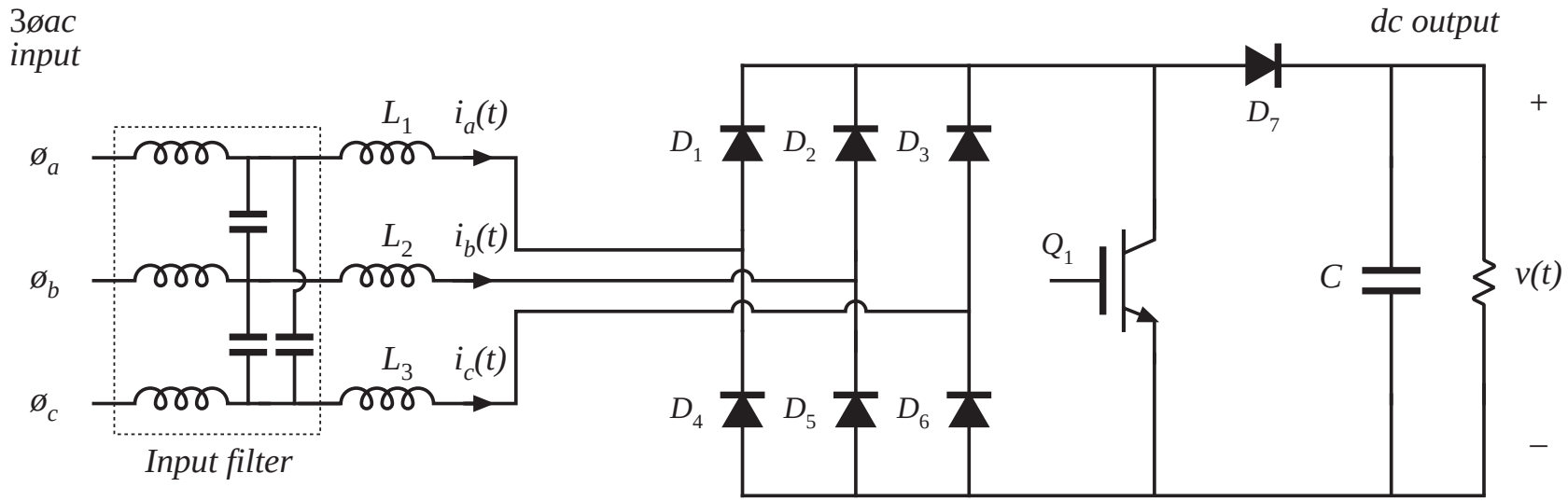
Low-harmonic rectification requires active semiconductor devices that are much more expensive than simple peak-detection diode rectifiers.

What is the minimum active silicon required to perform the function of 3ø low-harmonic rectification?

- No active devices are needed: diodes and harmonic traps will do the job, but these require low-frequency reactive elements
- When control of the output voltage is needed, then there must be at least one active device
- To avoid low-frequency reactive elements, at least one high-frequency switch is needed

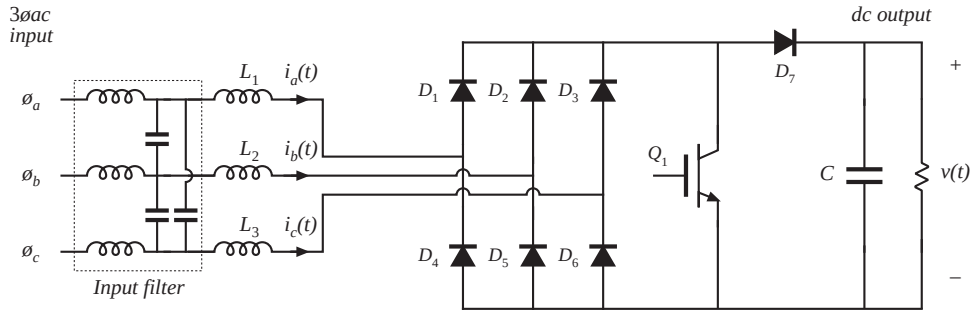
So let's search for approaches that use just one active switch, and only high-frequency reactive elements

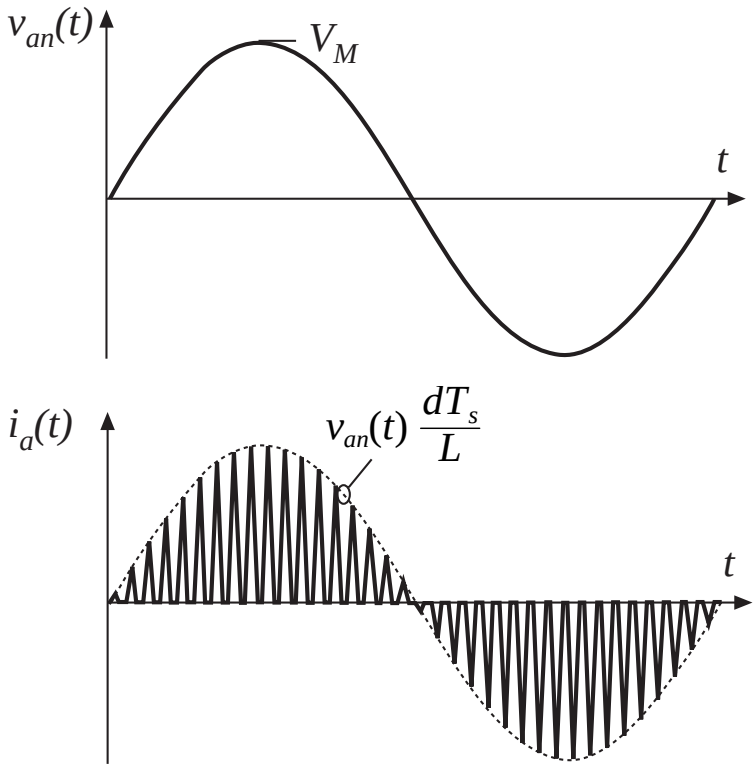
The single-switch DCM boost 3ø rectifier



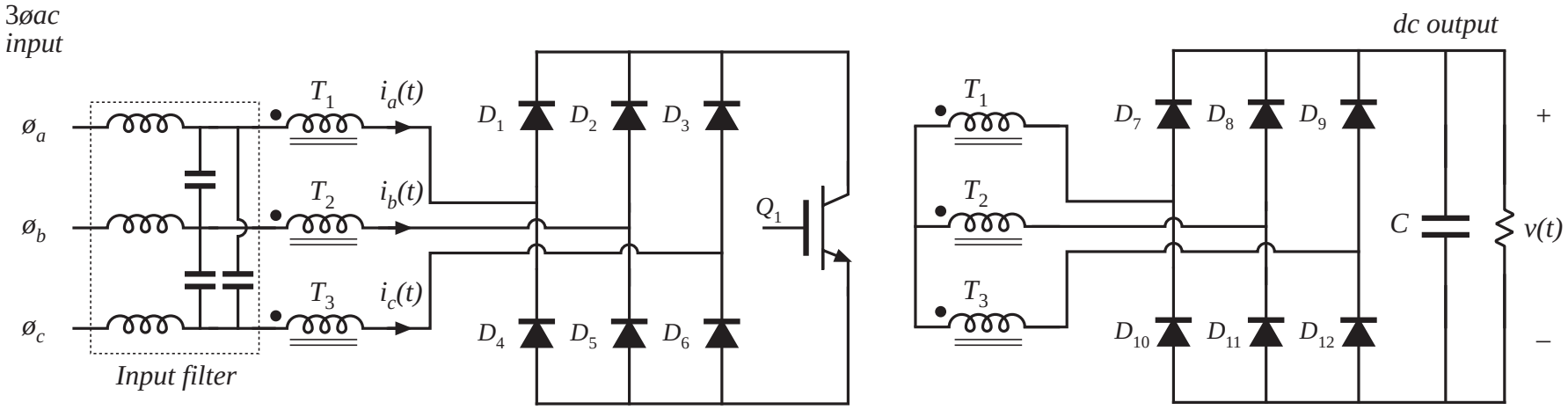
Inductors L_1 to L_3 operate in discontinuous conduction mode, in conjunction with diodes D_1 to D_6. Average input currents $\langle i_a(t) \rangle_{Ts}$, $\langle i_b(t) \rangle_{Ts}$, and $\langle i_c(t) \rangle_{Ts}$ are approximately proportional to the instantaneous input line-neutral voltages. Transistor is operated with constant duty cycle; slow variation of the duty cycle allows control of output power.

The single-switch DCM boost 3ø rectifier





The single-switch 3ø DCM flyback rectifier



The single-switch 3ø DCM flyback rectifier

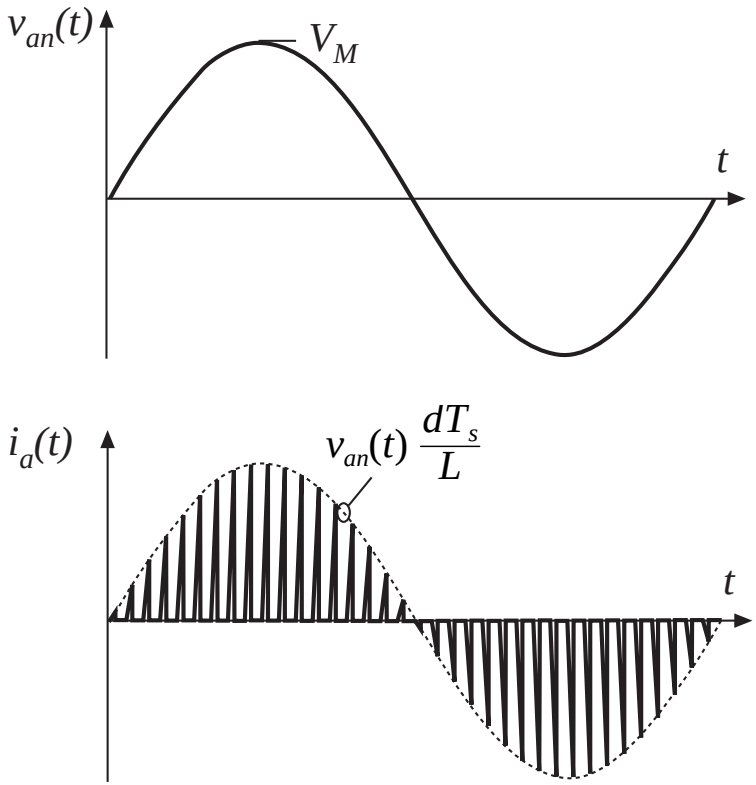
This converter is effectively three independent single-phase DCM flyback converters that share a common switch.

Since the open-loop DCM flyback converter can be modeled as a Loss-Free Resistor, three-phase low-harmonic rectification is obtained naturally.

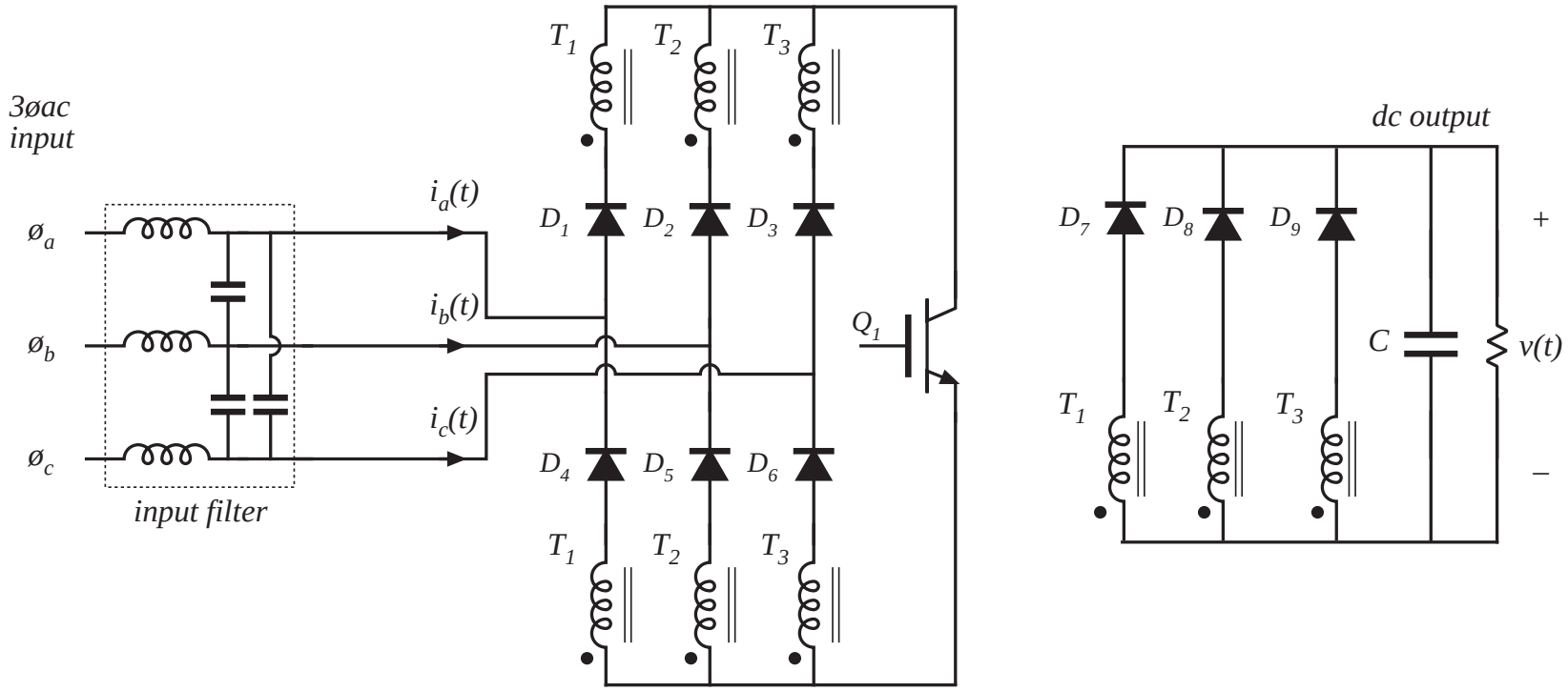
Basic converter has a boost characteristic, but buck-boost characteristic is possible (next slide).

Inrush current limiting and isolation are obtained easily.

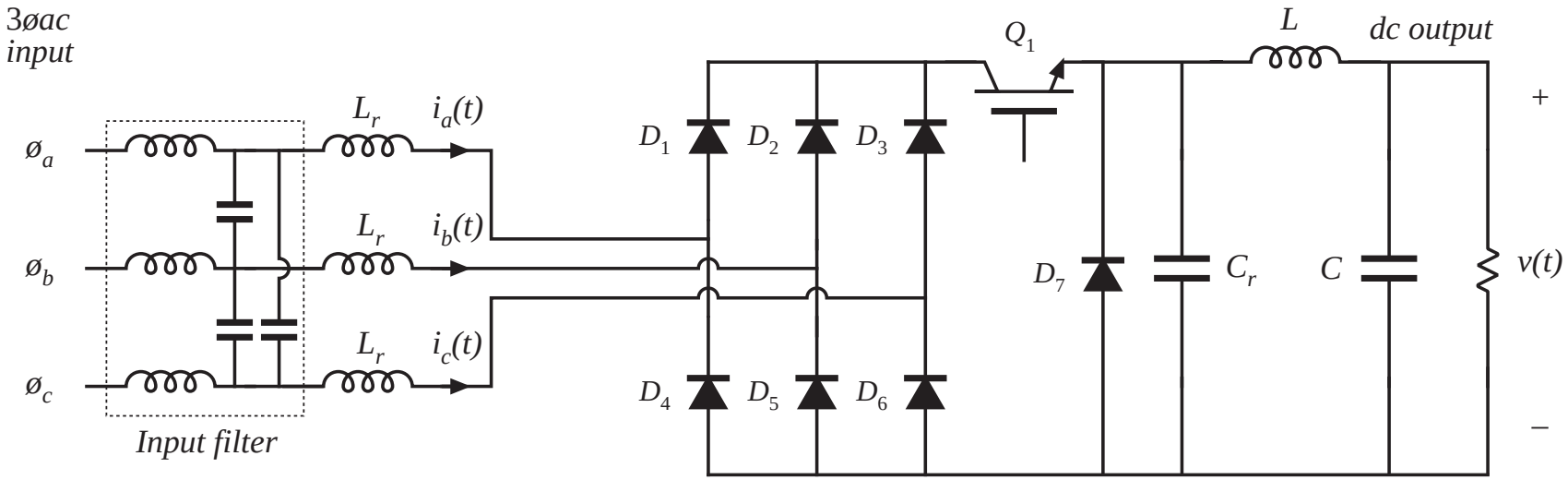
High peak currents, needs an input EMI filter



3ø Flyback rectifier with buck-boost conversion ratio



Single-switch three-phase zero-current-switching quasi-resonant buck rectifier

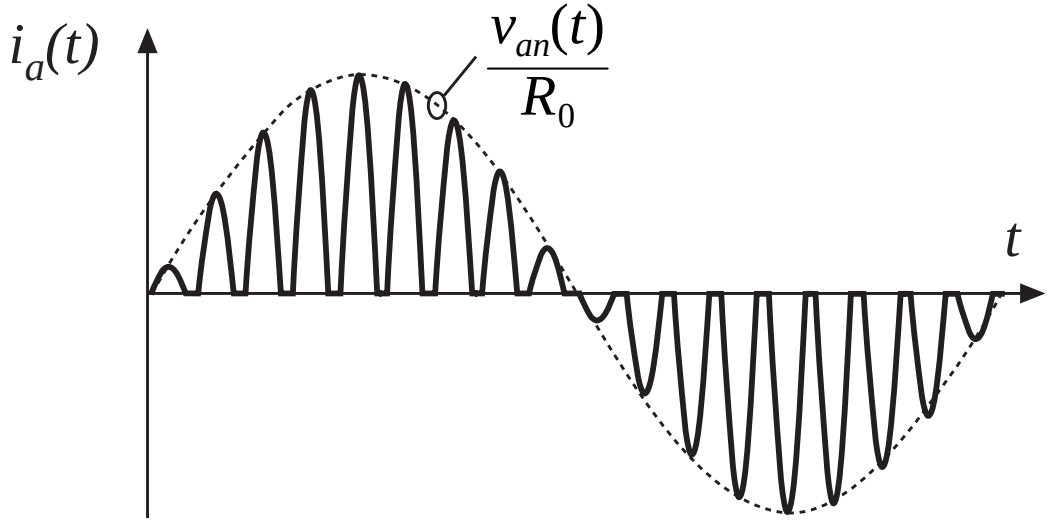


Inductors L_r and capacitor C_r form resonant tank circuits, having resonant frequency slightly greater than the switching frequency.

Turning on Q_1 initiates resonant current pulses, whose amplitudes depend on the instantaneous input line-neutral voltages.

When the resonant current pulses return to zero, diodes D_1 to D_6 are reverse-biased. Transistor Q_1 can then be turned off at zero current.

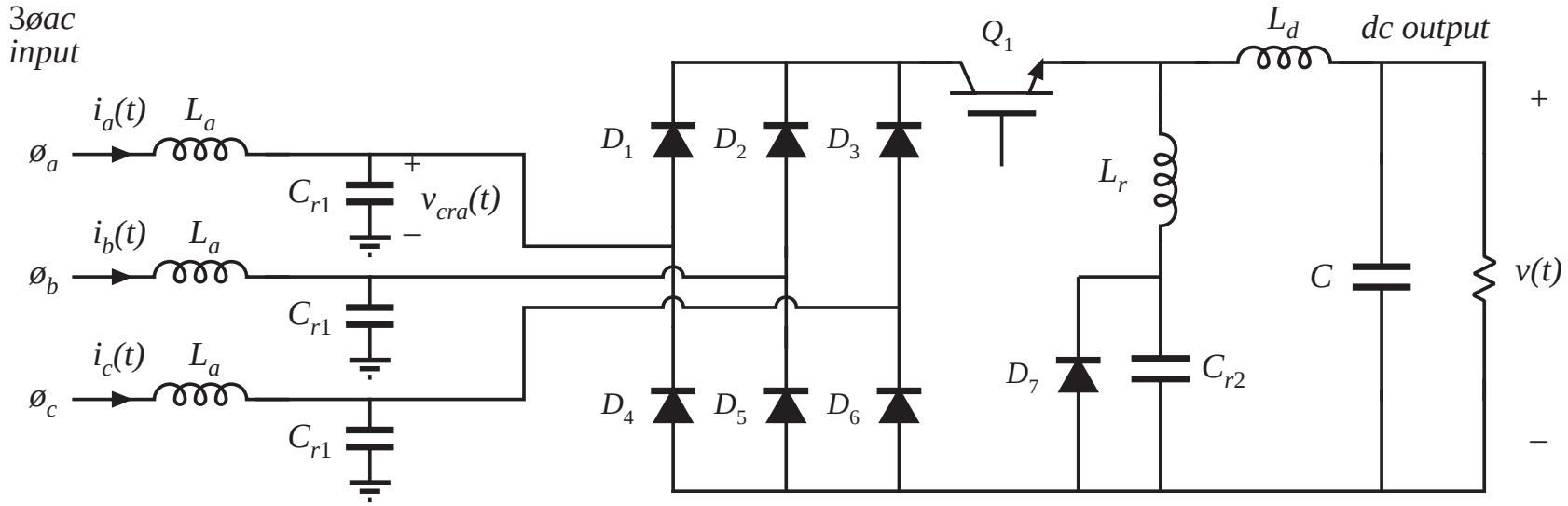
Single-switch three-phase zero-current-switching quasi-resonant buck rectifier



Input line currents are approximately sinusoidal pulses, whose amplitudes follow the input line-neutral voltages.

Lowest total active semiconductor stress of all buck-type 3ø low harmonic rectifiers

Multiresonant single-switch zero-current switching 3ø buck rectifier

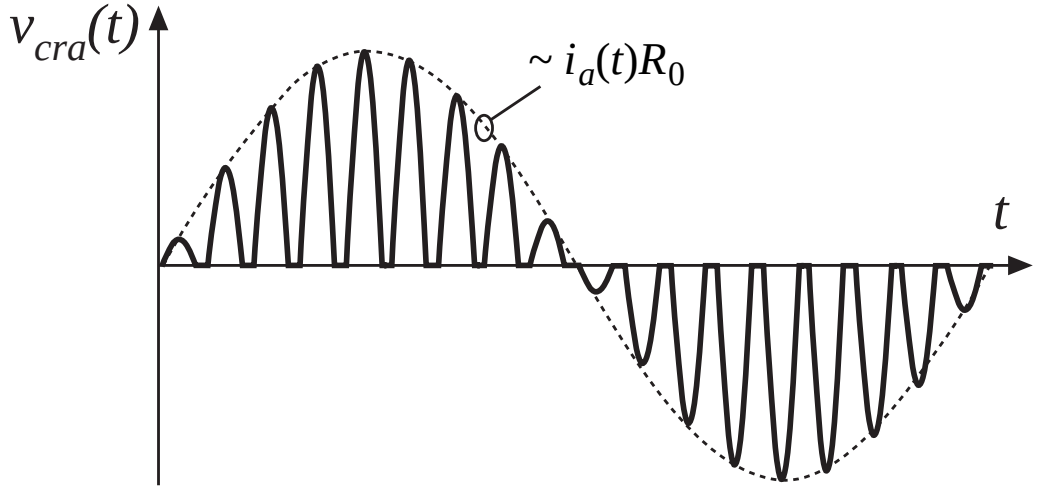


Inductors L_r and capacitors C_{r1} and C_{r2} form resonant tank circuits, having resonant frequency slightly greater than the switching frequency.

Turning on Q_1 initiates resonant voltage pulses in $v_{cra}(t)$, whose amplitudes depend on the instantaneous input line-neutral currents $i_a(t)$ to $i_c(t)$.

All diodes switch off when their respective tank voltages reach zero. Transistor Q_1 is turned off at zero current.

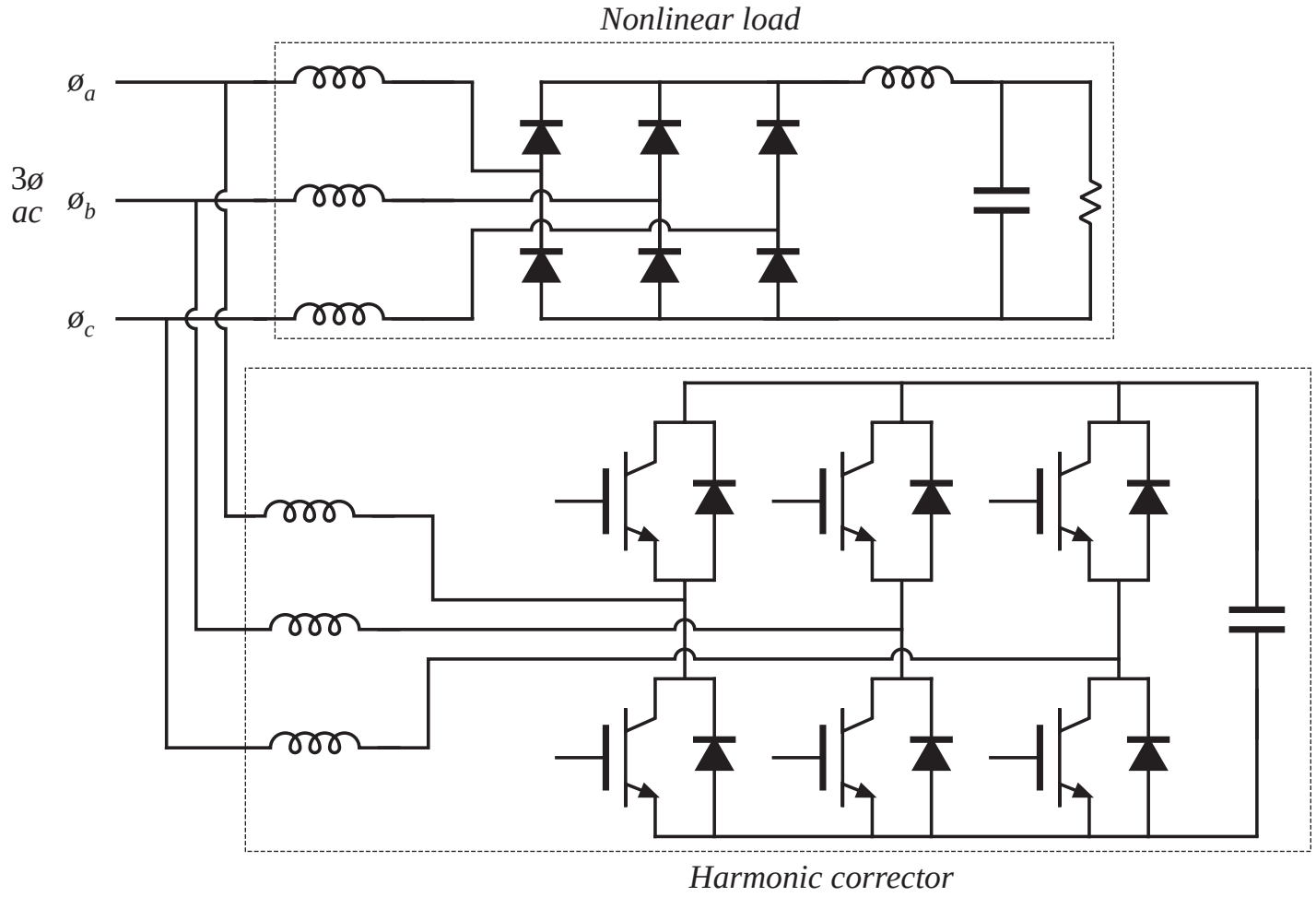
Multiresonant single-switch zero-current switching 3ø buck rectifier



Input-side resonant voltages are approximately sinusoidal pulses, whose amplitudes follow the input currents. Input filter inductors operate in CCM.

Higher total active semiconductor stress than previous approach, but less EMI filtering is needed. Low THD: < 4% THD can be obtained.

Harmonic correction



Harmonic correction

- An active filter that is controlled to cancel the harmonic currents created by a nonlinear load.
- Does not need to conduct the average load power.
- Total active semiconductor stress is high when the nonlinear load generates large harmonic currents having high THD.
- In the majority of applications, this approach exhibits greater total active semiconductor stress than the simple 3ø CCM boost rectifier.

17.6 Summary of key points

1. The ideal rectifier presents an effective resistive load, the emulated resistance R_e, to the ac power system. The power apparently "consumed" by R_e is transferred to the dc output port. In a three-phase ideal rectifier, input resistor emulation is obtained in each phase. In both the single-phase and three-phase cases, the output port follows a power source characteristic, dependent on the instantaneous ac input power. Ideal rectifiers can perform the function of low-harmonic rectification, without need for low-frequency reactive elements.

2. The dc-dc boost converter, as well as other converters capable of increasing the voltage, can be adapted to the ideal rectifier application. A control system causes the input current to be proportional to the input voltage. The converter may operate in CCM, DCM, or in both modes. The mode boundary is expressed as a function of R_e , $2L/T_s$, and the instantaneous voltage ratio $v_g(t)/V$. A well-designed average current controller leads to resistor emulation regardless of the operating mode; however, other schemes discussed in the next chapter may lead to distorted current waveforms when the mode boundary is crossed.

Summary of key points

3. In a single-phase system, the instantaneous ac input power is pulsating, while the dc load power is constant. Whenever the instantaneous input and output powers are not equal, the ideal rectifier system must contain energy storage. A large capacitor is commonly employed; the voltage of this capacitor must be allowed to vary independently, as necessary to store and release energy. A slow feedback loop regulates the dc component of the capacitor voltage, to ensure that the average ac input power and dc load power are balanced.
4. RMS values of rectifiers waveforms can be computed by double integration. In the case of the boost converter, the rms transistor current can be as low as 39% of the rms ac input current, when V is close in value to V_M. Other converter topologies such as the buck-boost, SEPIC, and Cuk converters exhibit significantly higher rms transistor currents but are capable of limiting the converter inrush current.

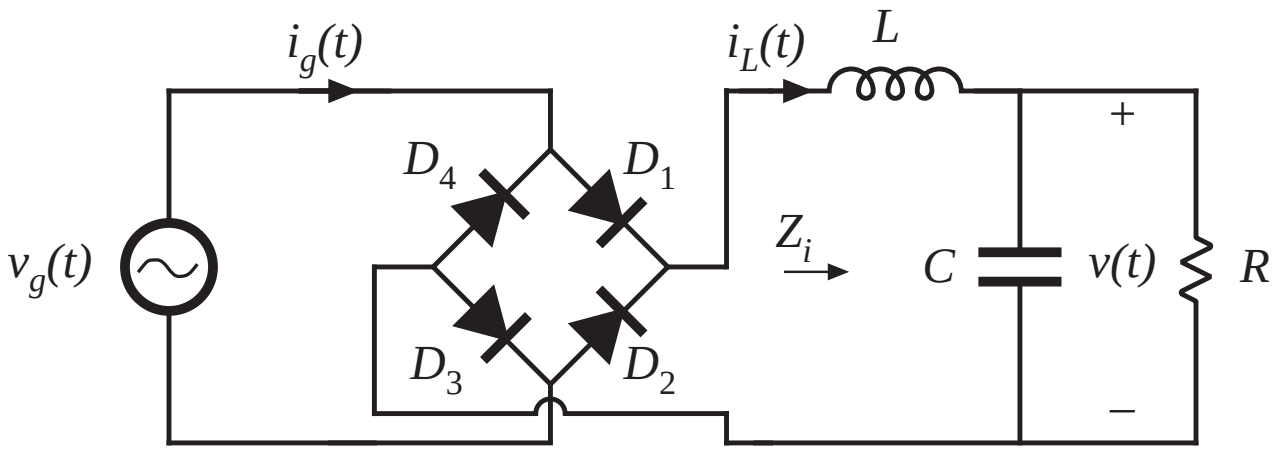
Summary of key points

5. In the three-phase case, a boost-type rectifier based on the PWM voltage-source inverter also exhibits low rms transistor currents. This approach requires six active switching elements, and its dc output voltage must be greater than the peak input line-to-line voltage. Average current control can be used to obtain input resistor emulation. An equivalent circuit can be derived by averaging the switch waveforms. The converter operation can be understood by assuming that the switch duty cycles vary sinusoidally; expressions for the average converter waveforms can then be derived.
6. Other three-phase rectifier topologies are known, including six-switch rectifiers having buck and buck-boost characteristics. In addition, three-phase low-harmonic rectifiers having a reduced number of active switches, as few as one, are discussed here.

Chapter 17

Line-Commutated Rectifiers

17.1 The single-phase full-wave rectifier



Full-wave rectifier with dc-side L-C filter

Two common reasons for including the dc-side L-C filter:

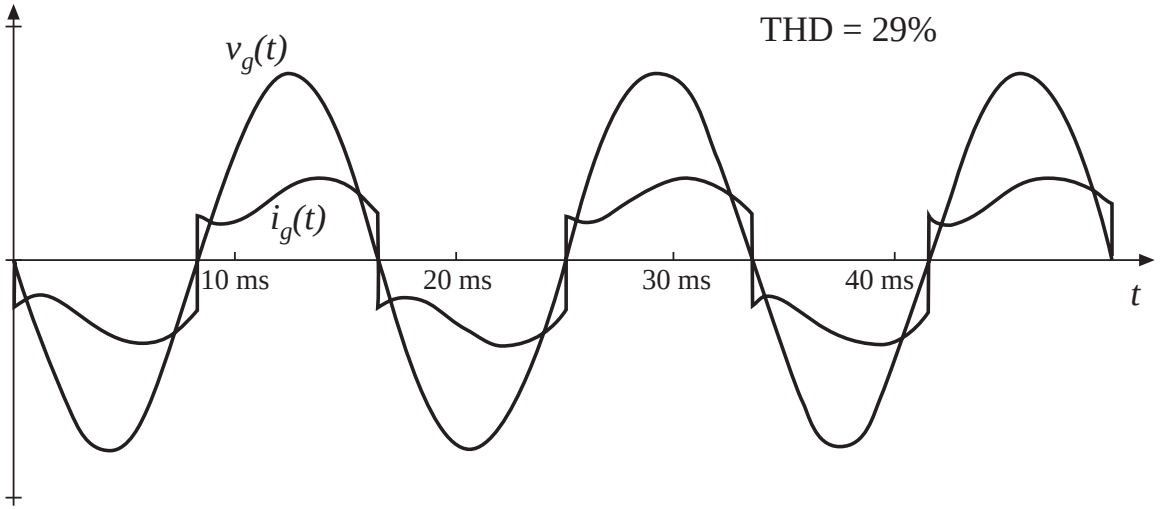
- Obtain good dc output voltage (large C) and acceptable ac line current waveform (large L)
- Filter conducted EMI generated by dc load (small L and C)

17.1.1 Continuous conduction mode

Large L

Typical ac line waveforms for CCM :

As $L \rightarrow \infty$, ac line current approaches a square wave



CCM results, for $L \rightarrow \infty$:

$$\text{distortion factor} = \frac{I_{1,\,rms}}{I_{rms}} = \frac{4}{\pi\sqrt{2}} = 90.0\%$$

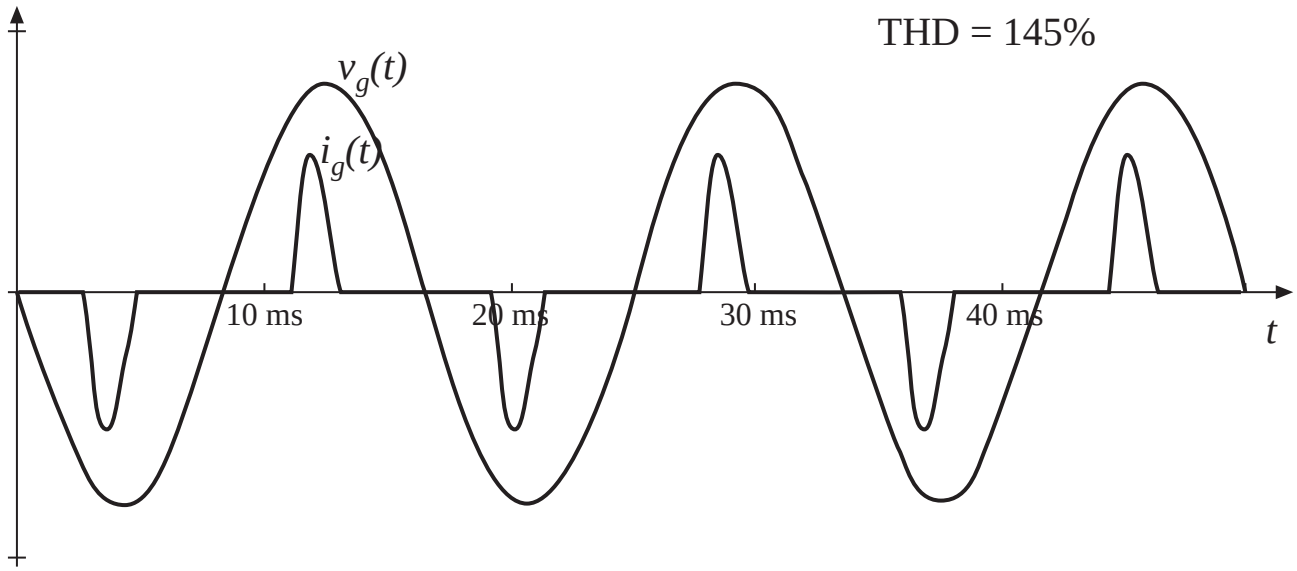
$$\text{THD} = \sqrt{\left(\frac{1}{\text{distortion factor}}\right)^2 - 1} = 48.3\%$$

17.1.2 Discontinuous conduction mode

Small L

Typical ac line waveforms for DCM :

As $L \rightarrow 0$, ac line current approaches impulse functions (peak detection)



As the inductance is reduced, the THD rapidly increases, and the distortion factor decreases.

Typical distortion factor of a full-wave rectifier with no inductor is in the range 55% to 65%, and is governed by ac system inductance.

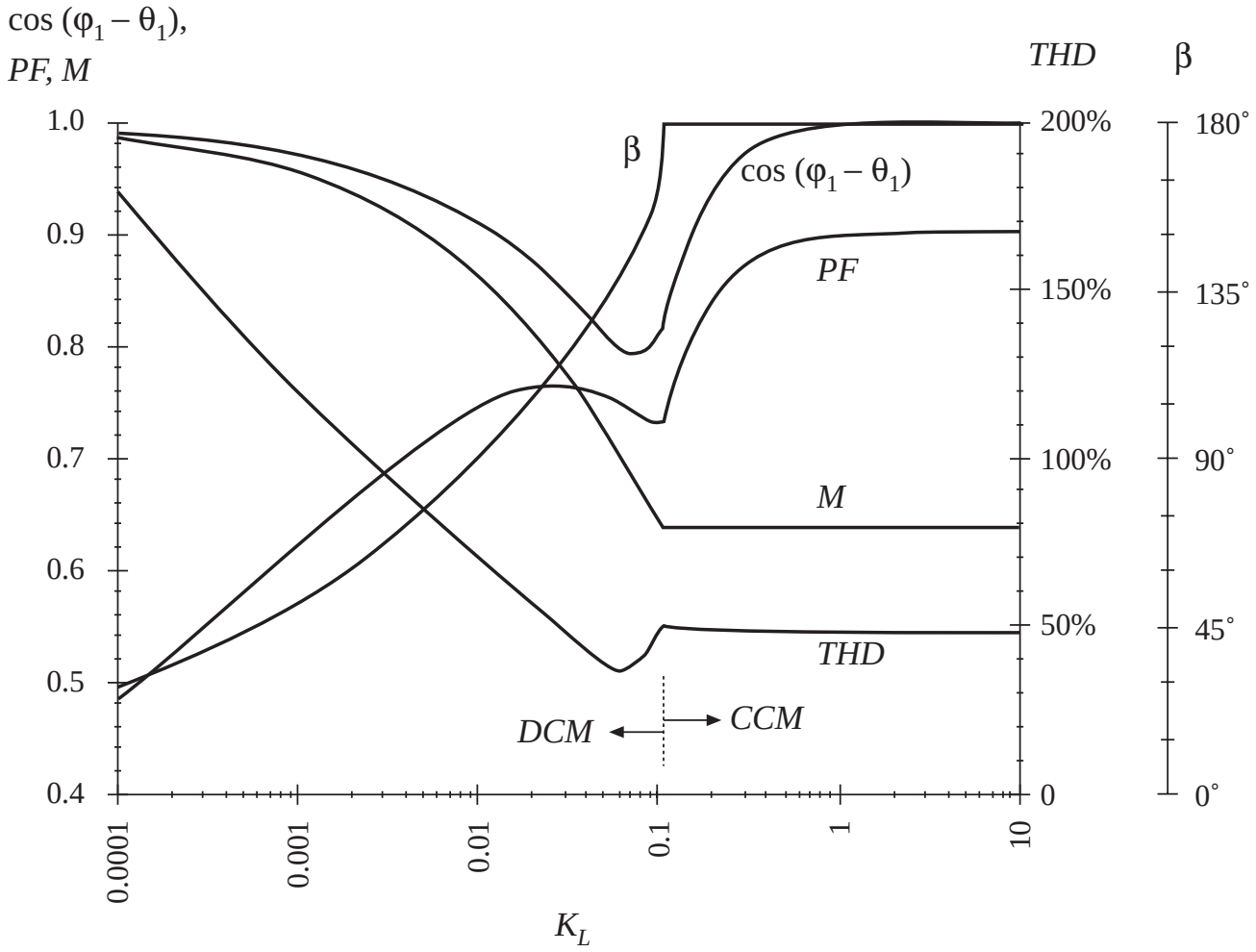
17.1.3 Behavior when *C* is large

Solution of the full-wave rectifier circuit for infinite *C*:

Define

$$K_L = \frac{2L}{RT_L}$$

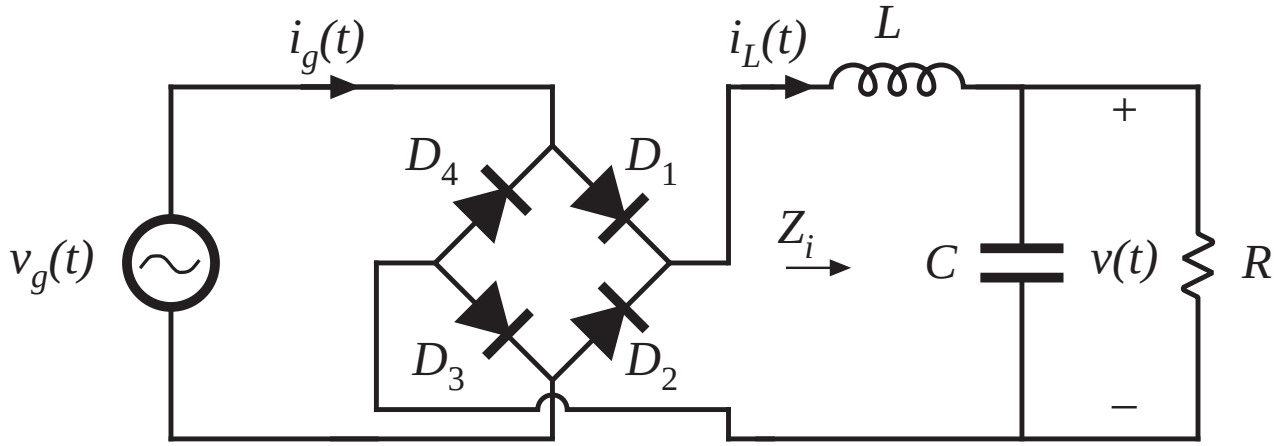
$$M = \frac{V}{V_m}$$



17.1.4 Minimizing *THD* when *C* is small

Sometimes the *L*-*C* filter is present only to remove high-frequency conducted EMI generated by the dc load, and is not intended to modify the ac line current waveform. If *L* and *C* are both zero, then the load resistor is connected directly to the output of the diode bridge, and the ac line current waveform is purely sinusoidal.

An approximate argument: the *L*-*C* filter has negligible effect on the ac line current waveform provided that the filter input impedance Z_i has zero phase shift at the second harmonic of the ac line frequency, $2\,f_L$.



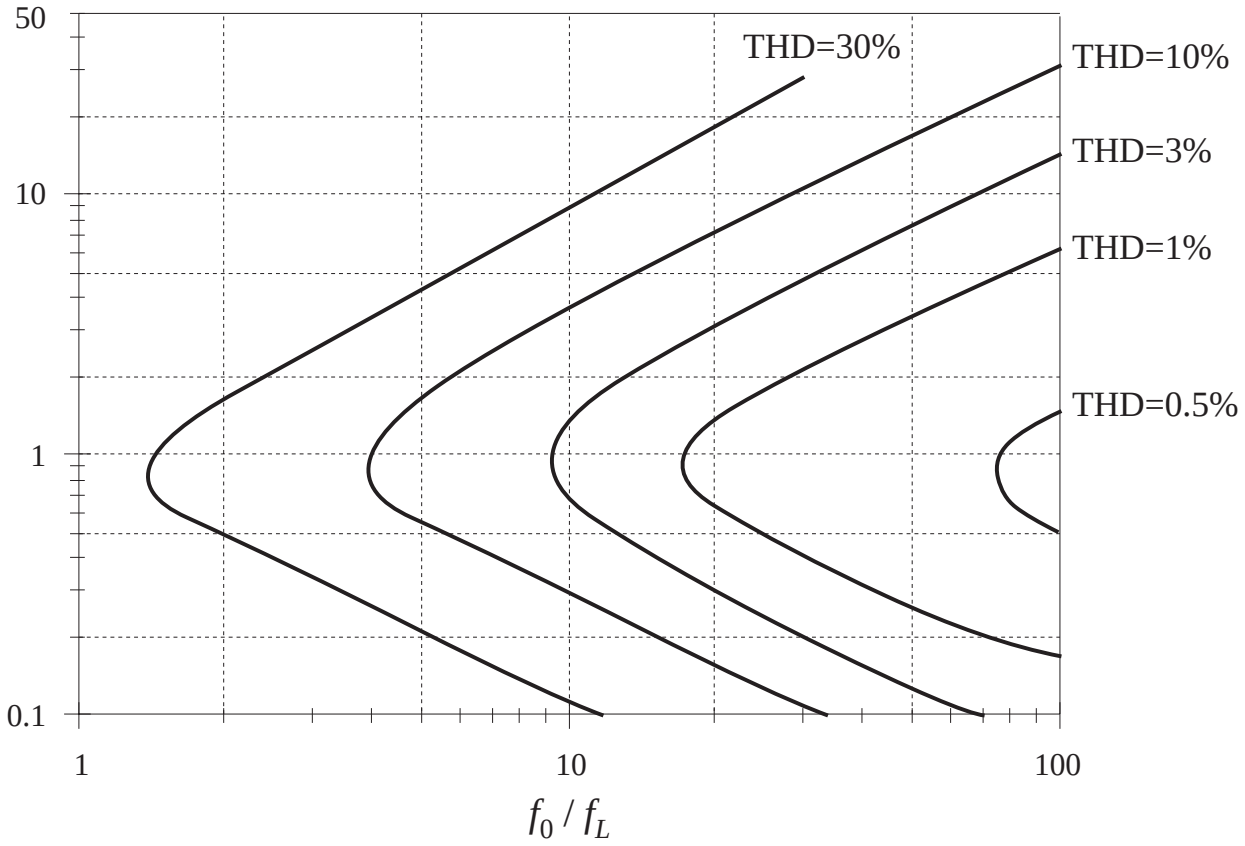
Approximate THD

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

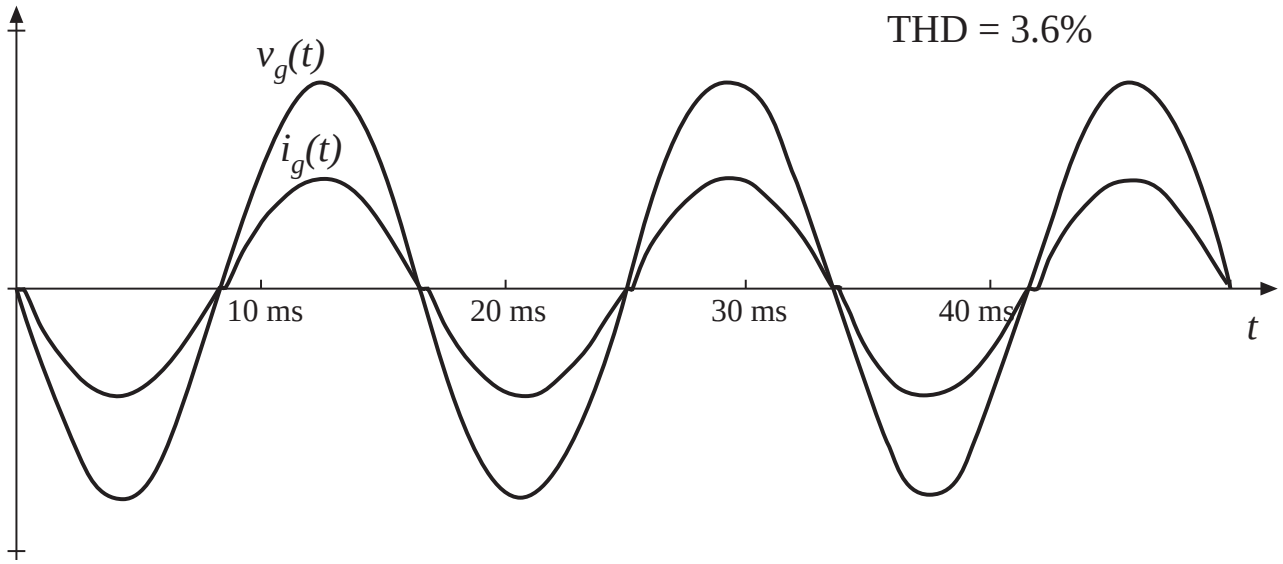
$$R_0 = \sqrt{\frac{L}{C}}$$

$$Q = \frac{R}{R_0}$$

$$f_p = \frac{1}{2\pi RC} = \frac{f_0}{Q}$$

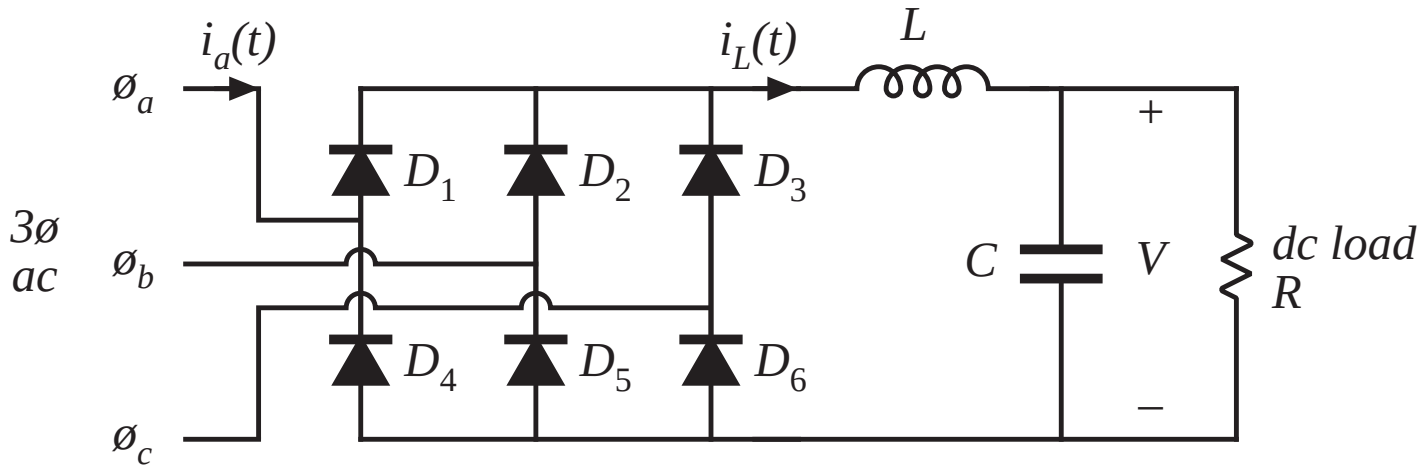


Example

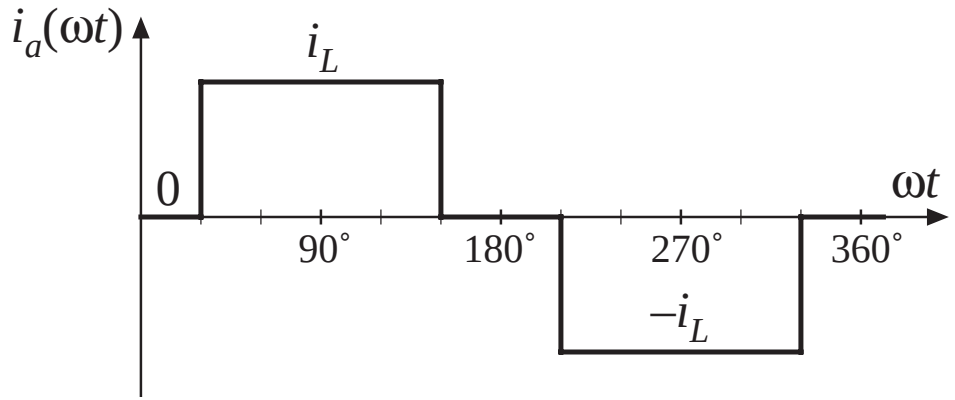


Typical ac line current and voltage waveforms, near the boundary between continuous and discontinuous modes and with small dc filter capacitor. $f_0/f_L = 10$, $Q = 1$

17.2 The Three-Phase Bridge Rectifier



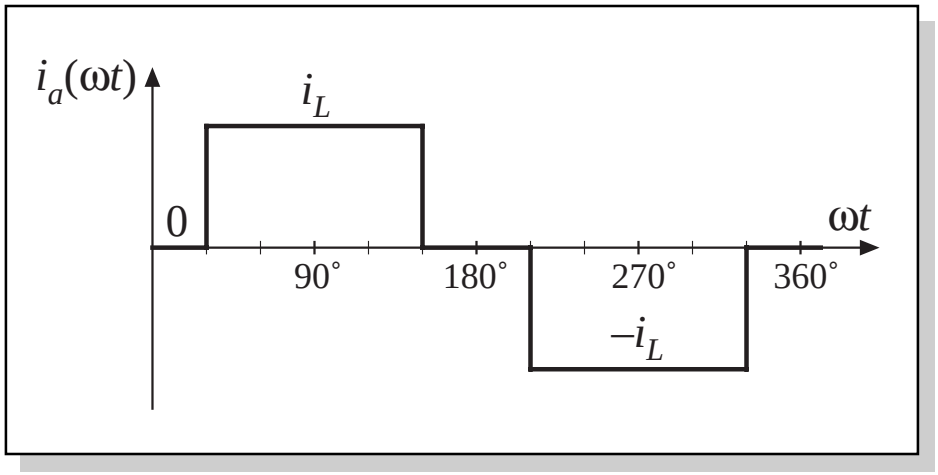
Line current waveform for infinite L



17.2.1 Continuous conduction mode

Fourier series:

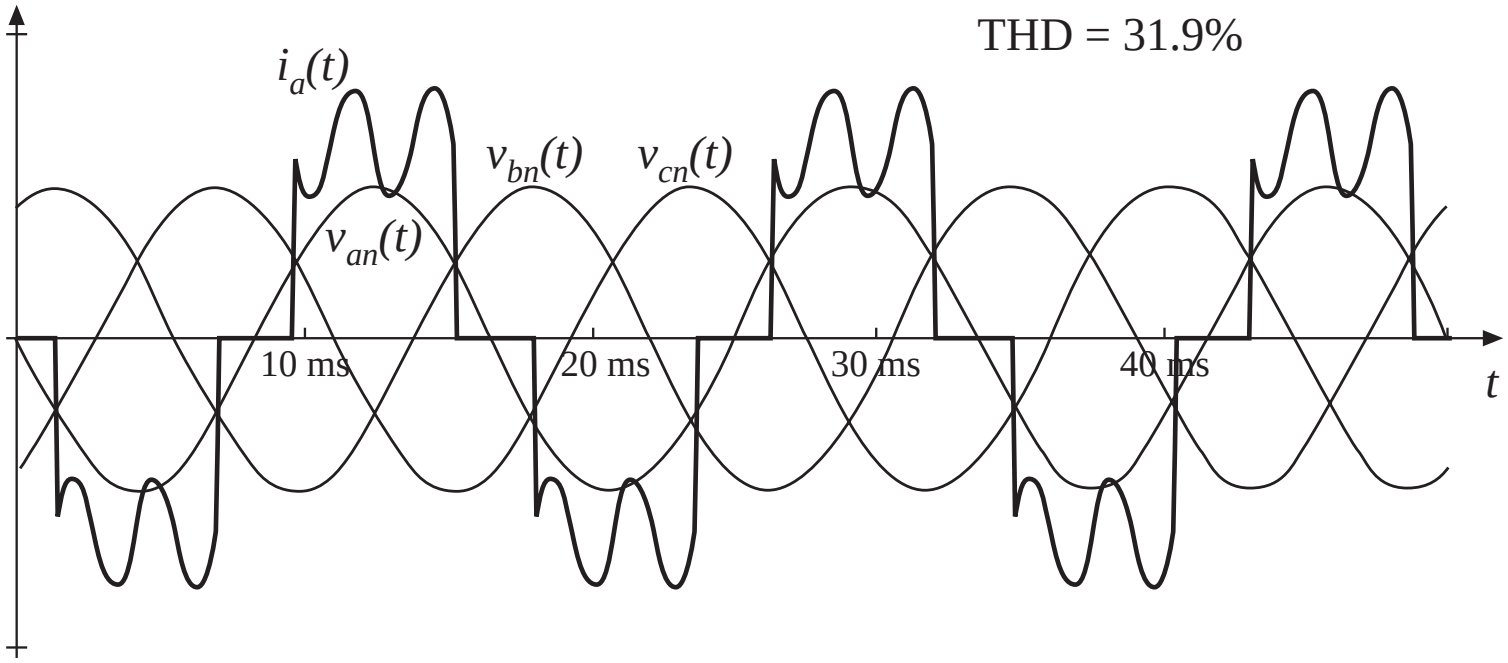
$$i_a(t) = \sum_{n = 1,5,7,11,\ldots}^{\infty} \frac{4}{n\pi} I_L \sin\left(\frac{n\pi}{2}\right) \sin\left(\frac{n\pi}{3}\right) \sin\left(n\omega t\right)$$



- Similar to square wave, but missing triplen harmonics
- THD = 31%
- Distortion factor = $3/\pi$ = 95.5%
- In comparison with single phase case:

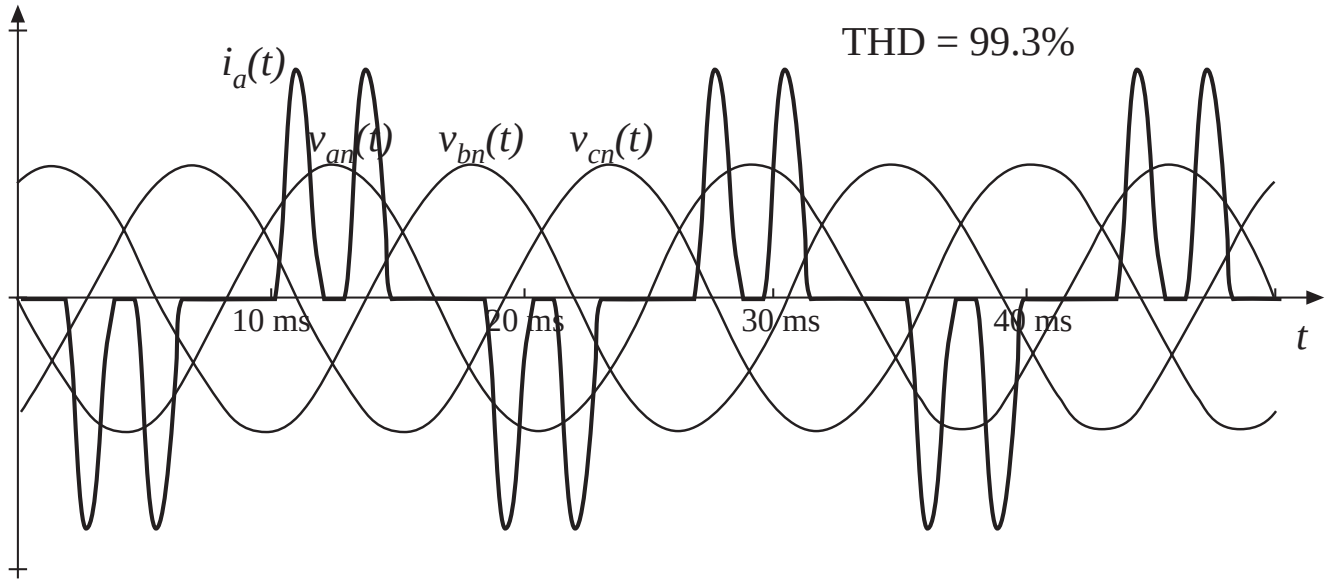
  the missing 60° of current improves the distortion factor from 90% to 95%, because the triplen harmonics are removed

A typical CCM waveform



Inductor current contains sixth harmonic ripple (360 Hz for a 60 Hz ac system). This ripple is superimposed on the ac line current waveform, and influences the fifth and seventh harmonic content of $i_a(t)$.

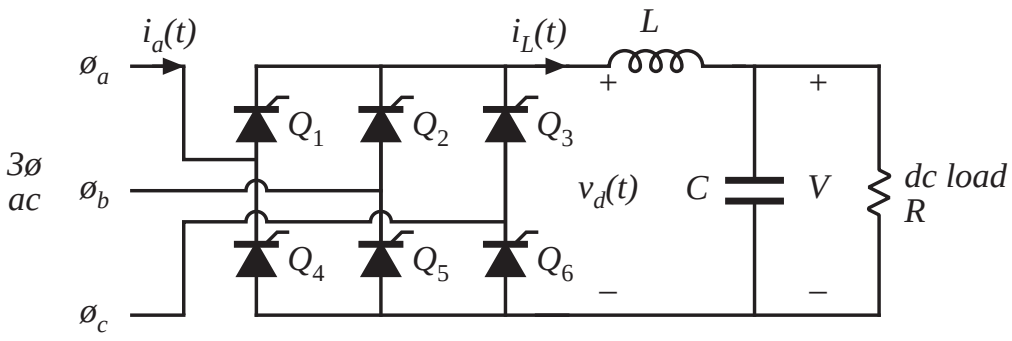
17.2.2 Discontinuous conduction mode



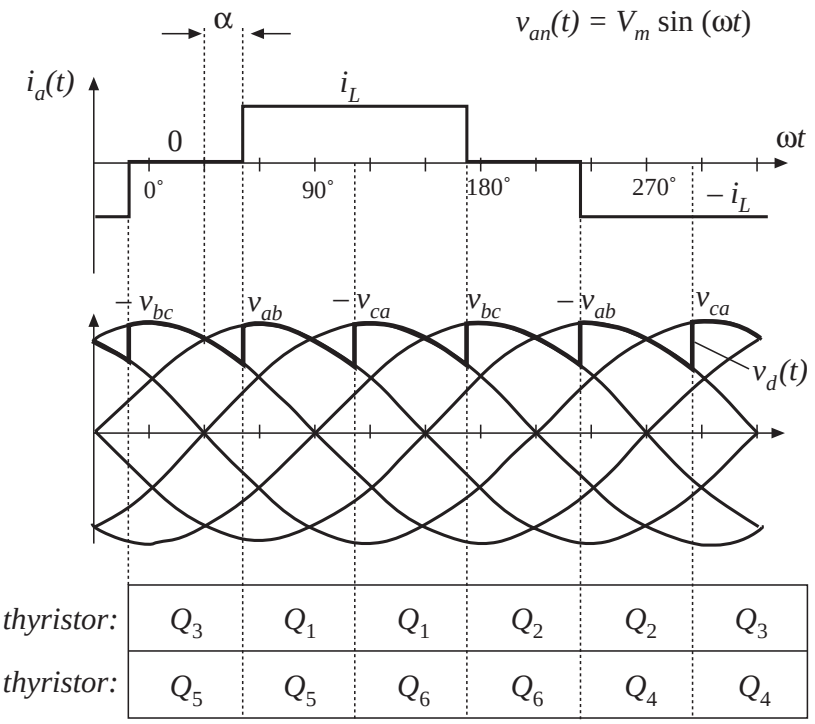
Phase *a* current contains pulses at the positive and negative peaks of the line-to-line voltages $v_{ab}(t)$ and $v_{ac}(t)$. Distortion factor and THD are increased. Distortion factor of the typical waveform illustrated above is 71%.

17.3 Phase control

Replace diodes with SCRs:



Phase control waveforms:

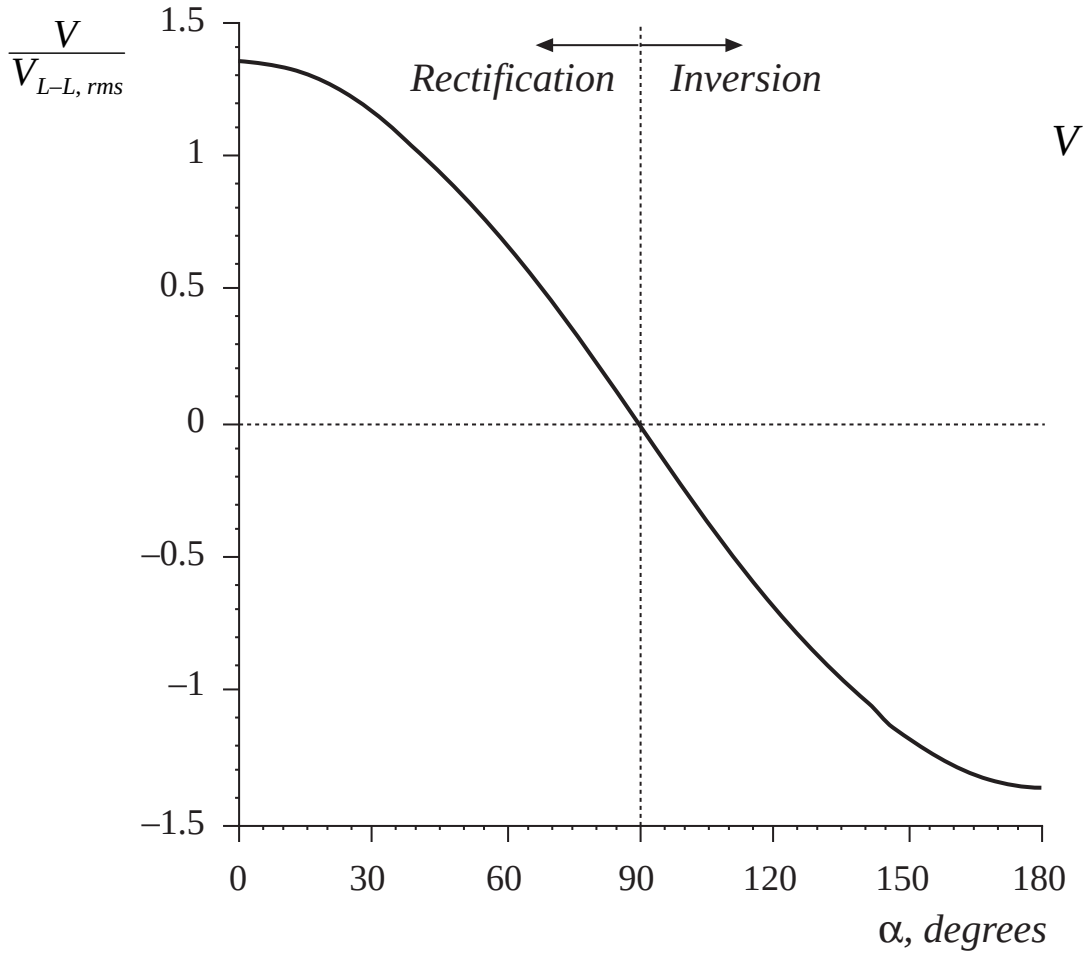


Average (dc) output voltage:

$$V = \frac{3}{\pi} \int_{30^\circ+\alpha}^{90^\circ+\alpha} \sqrt{3}\, V_m \sin(\theta + 30^\circ) d\theta$$

$$= \frac{3\sqrt{2}}{\pi} V_{L\text{-}L,\, rms} \cos \alpha$$

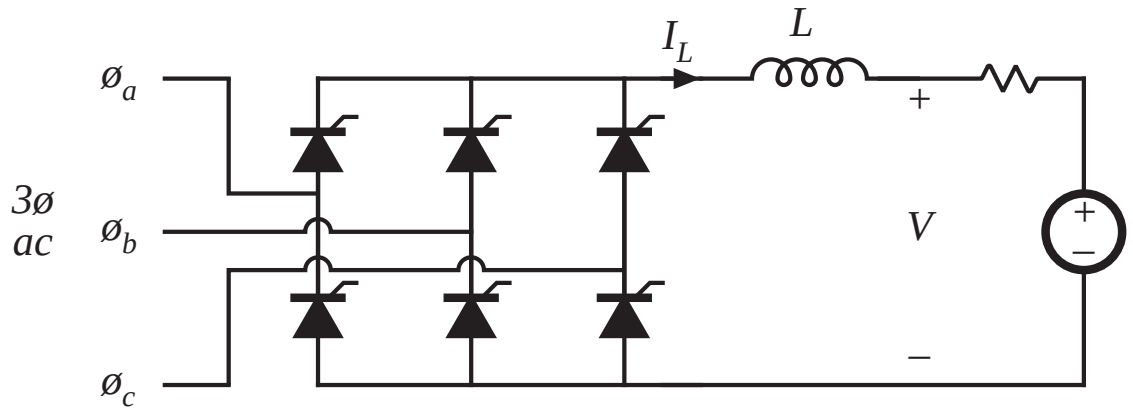
Dc output voltage vs. delay angle α



$$V = \frac{3}{\pi} \int_{30^\circ+\alpha}^{90^\circ+\alpha} \sqrt{3}\, V_m \sin(\theta + 30^\circ) d\theta$$

$$= \frac{3\sqrt{2}}{\pi} V_{L\text{-}L,\,rms} \cos \alpha$$

17.3.1 Inverter mode



If the load is capable of supplying power, then the direction of power flow can be reversed by reversal of the dc output voltage V. The delay angle α must be greater than 90°. The current direction is unchanged.

17.3.2 Harmonics and power factor

Fourier series of ac line current waveform, for large dc-side inductance:

$$i_a(t) = \sum_{n = 1,5,7,11,\ldots}^{\infty} \frac{4}{n\pi} I_L \sin\left(\frac{n\pi}{2}\right) \sin\left(\frac{n\pi}{3}\right) \sin(n\omega t - n\alpha)$$

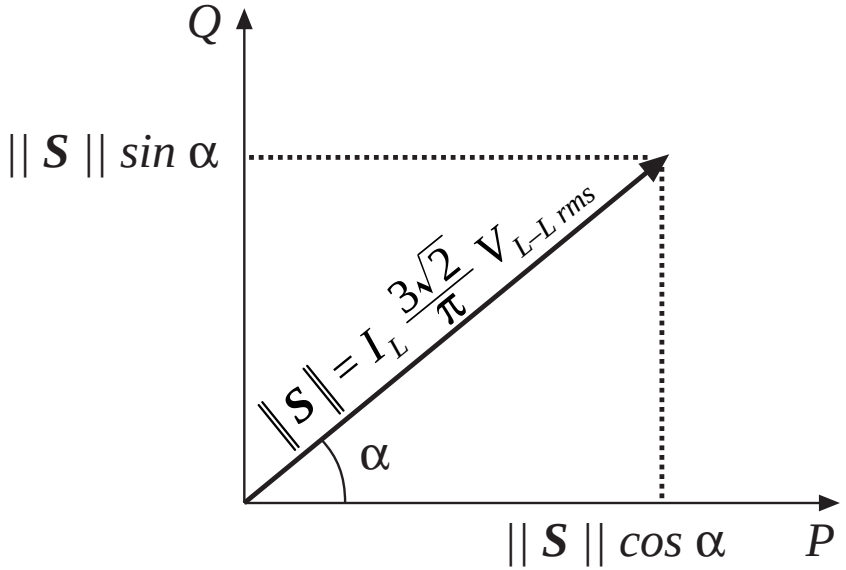
Same as uncontrolled rectifier case, except that waveform is delayed by the angle α. This causes the current to lag, and decreases the displacement factor. The power factor becomes:

$$\text{power factor} = 0.955 \left| \cos(\alpha) \right|$$

When the dc output voltage is small, then the delay angle α is close to 90° and the power factor becomes quite small. The rectifier apparently consumes reactive power, as follows:

$$Q = \sqrt{3}\, I_{a,\,rms} V_{L\text{-}L,\,rms} \sin\alpha = I_L \frac{3\sqrt{2}}{\pi} V_{L\text{-}L,\,rms} \sin\alpha$$

Real and reactive power in controlled rectifier
at fundamental frequency

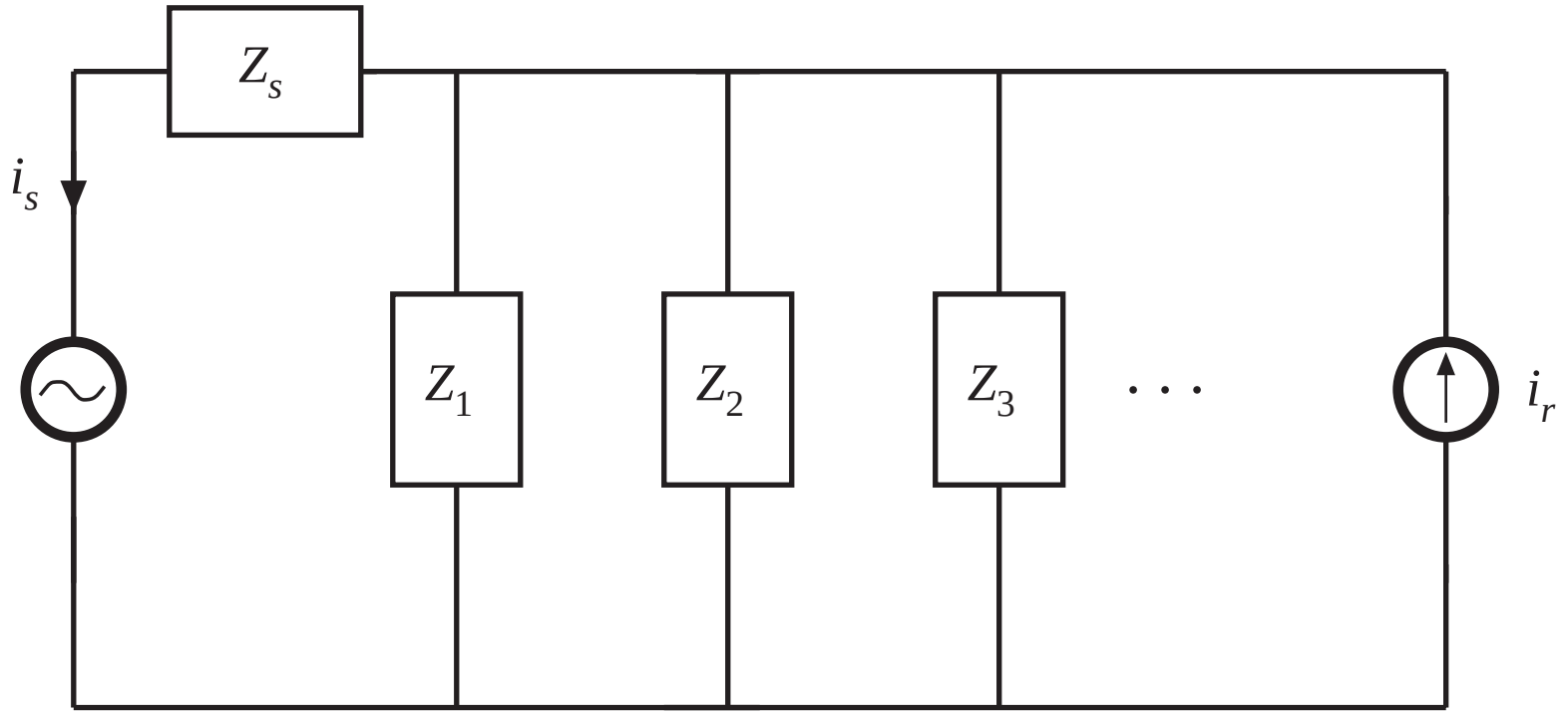


$$P = I_L \frac{3\sqrt{2}}{\pi} V_{L\text{-}L,\,rms} \cos\alpha$$

$$Q = \sqrt{3}\, I_{a,\,rms} V_{L\text{-}L,\,rms} \sin\alpha = I_L \frac{3\sqrt{2}}{\pi} V_{L\text{-}L,\,rms} \sin\alpha$$

17.4 Harmonic trap filters

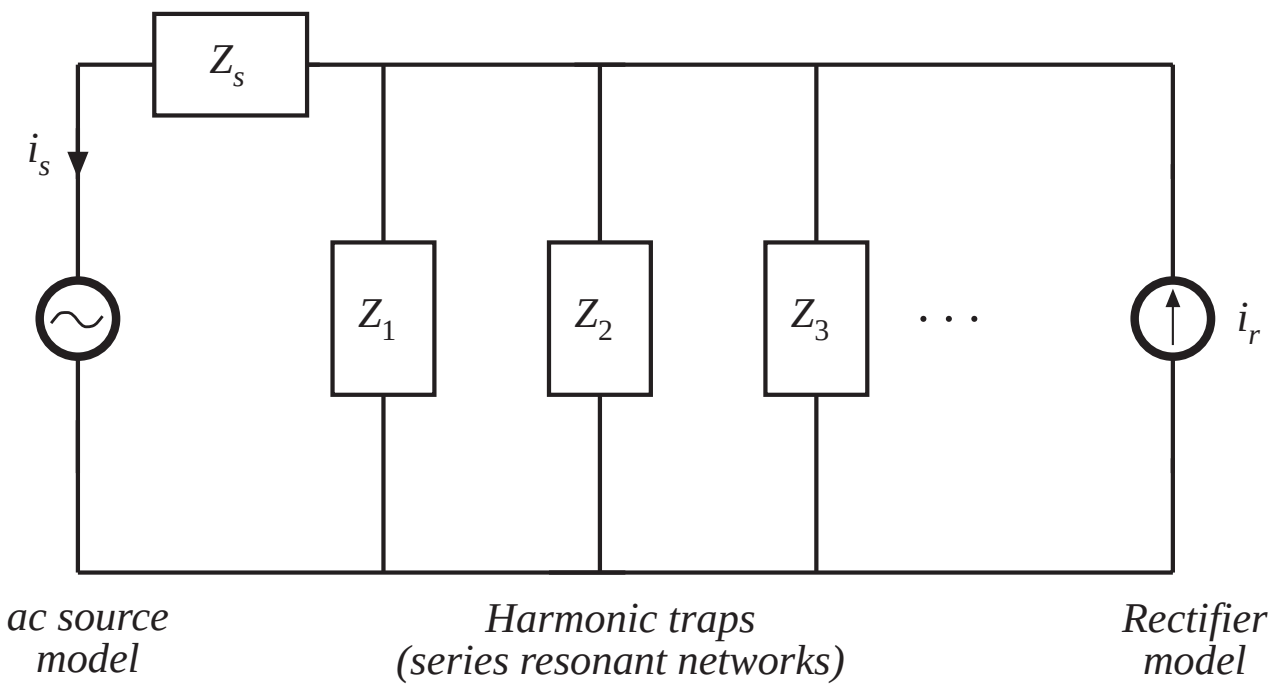
A passive filter, having resonant zeroes tuned to the harmonic frequencies



Harmonic trap

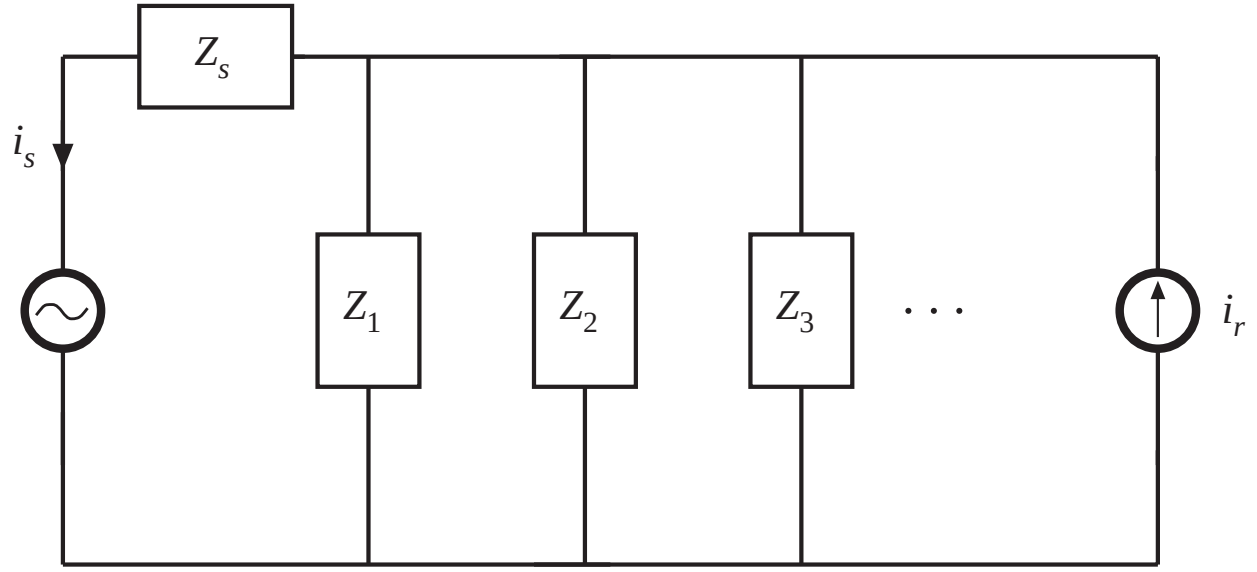
Ac source: model with Thevenin-equiv voltage source and impedance Z_s'(s). Filter often contains series inductor sL_s'. Lump into effective impedance $Z_s(s)$:

$$Z_s(s) = Z_s'(s) + sL_s'$$

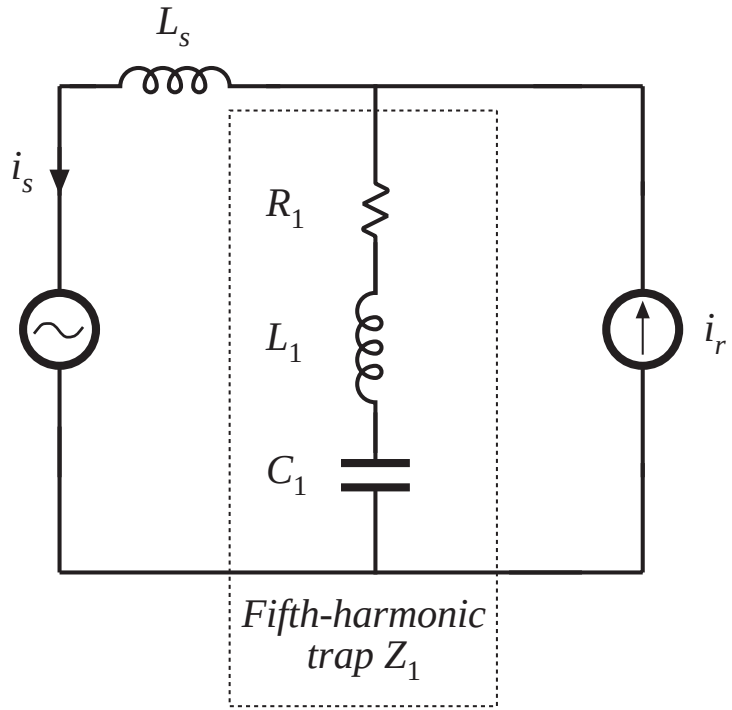


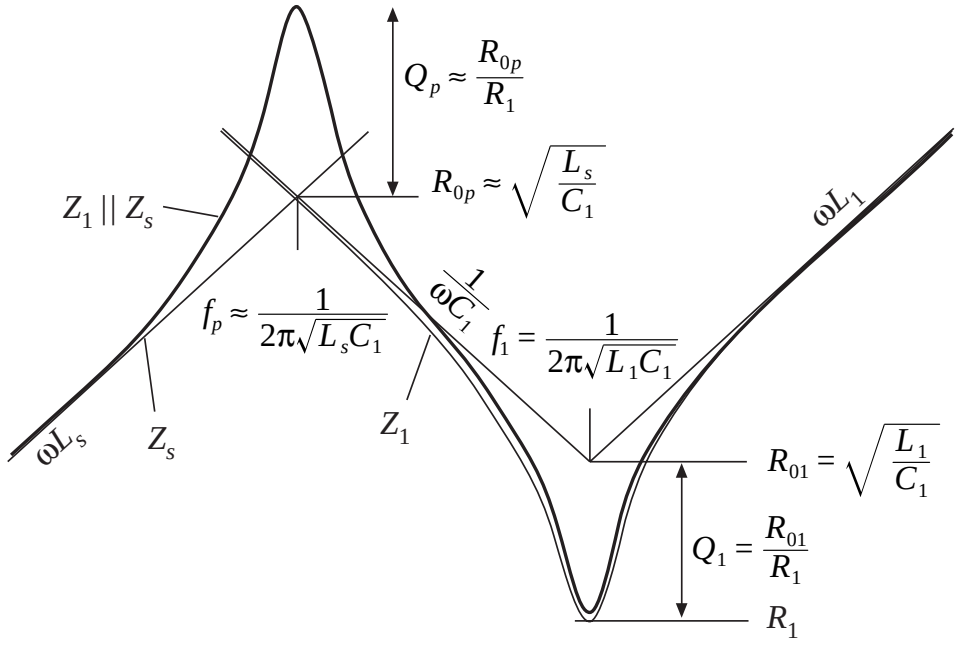
Filter transfer function

$$H(s) = \frac{i_s(s)}{i_R(s)} = \frac{Z_1 \parallel Z_2 \parallel \cdots}{Z_s + Z_1 \parallel Z_2 \parallel \cdots} \quad \text{or} \quad H(s) = \frac{i_s(s)}{i_R(s)} = \frac{Z_s \parallel Z_1 \parallel Z_2 \parallel \cdots}{Z_s}$$

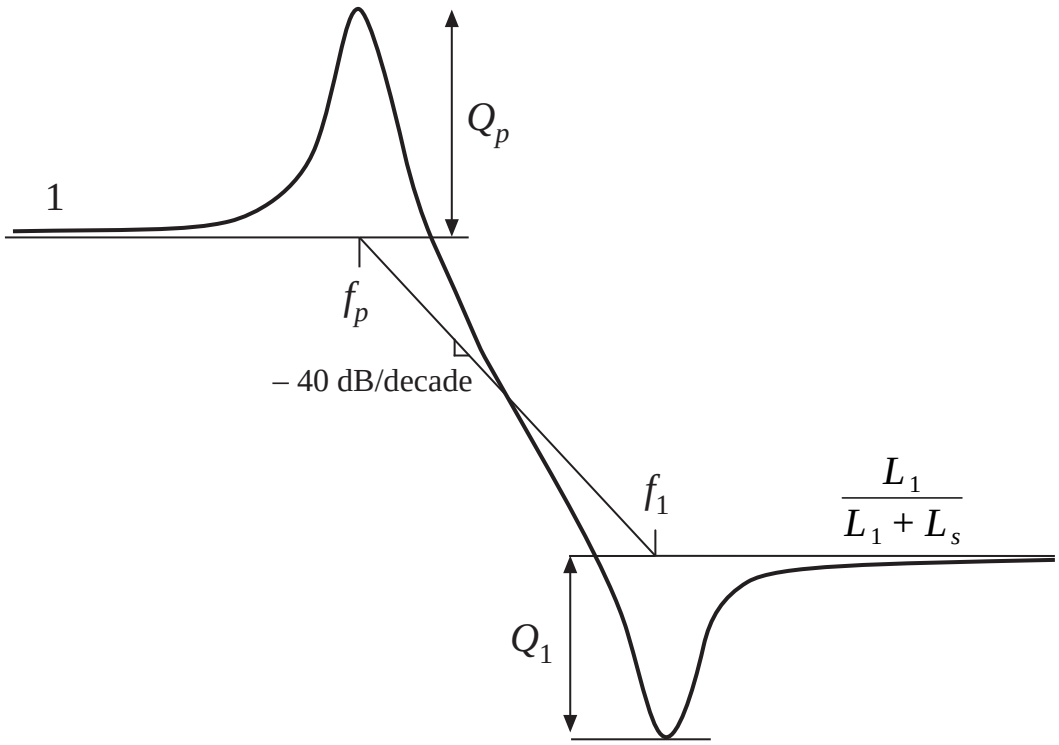


Simple example



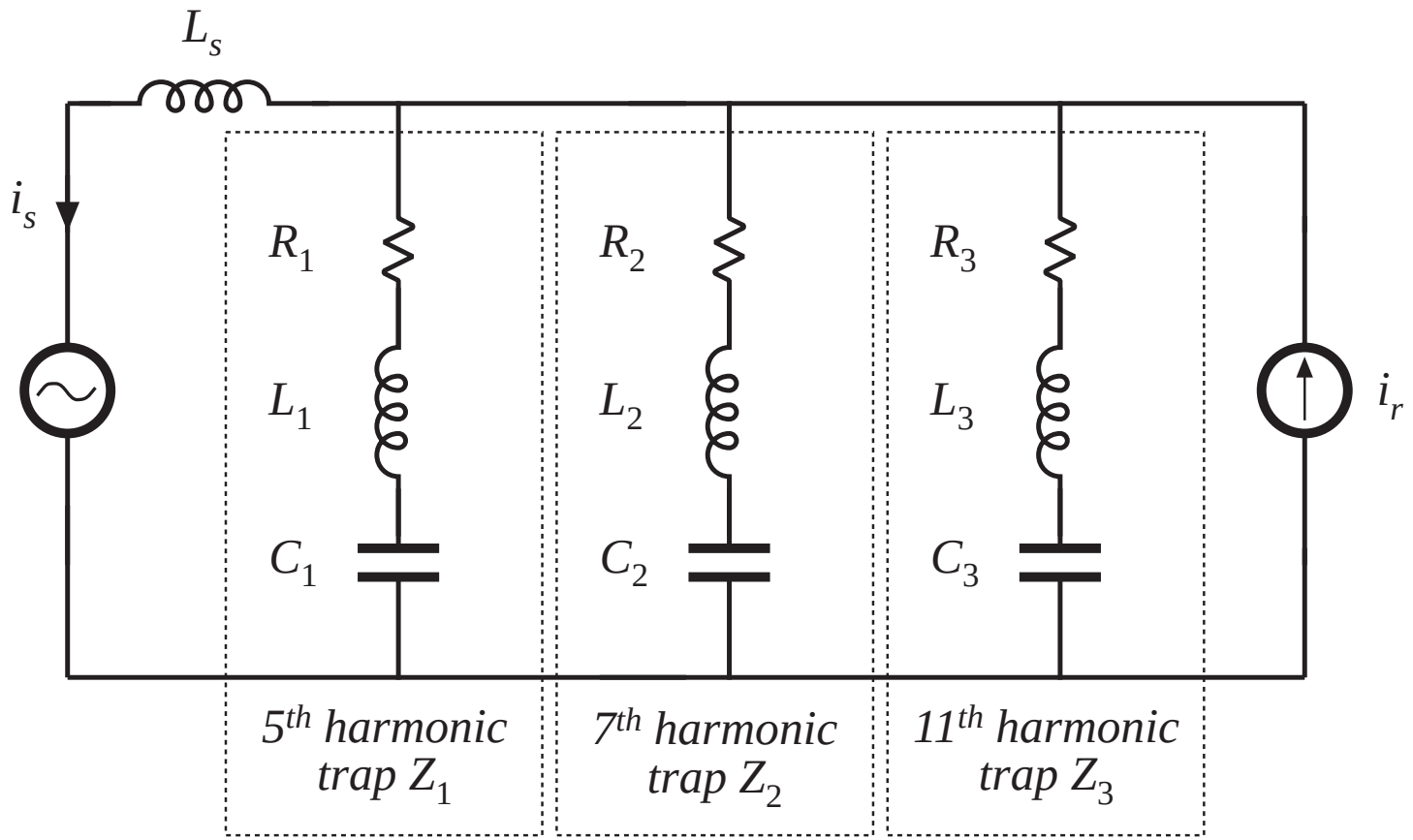


Simple example: transfer function

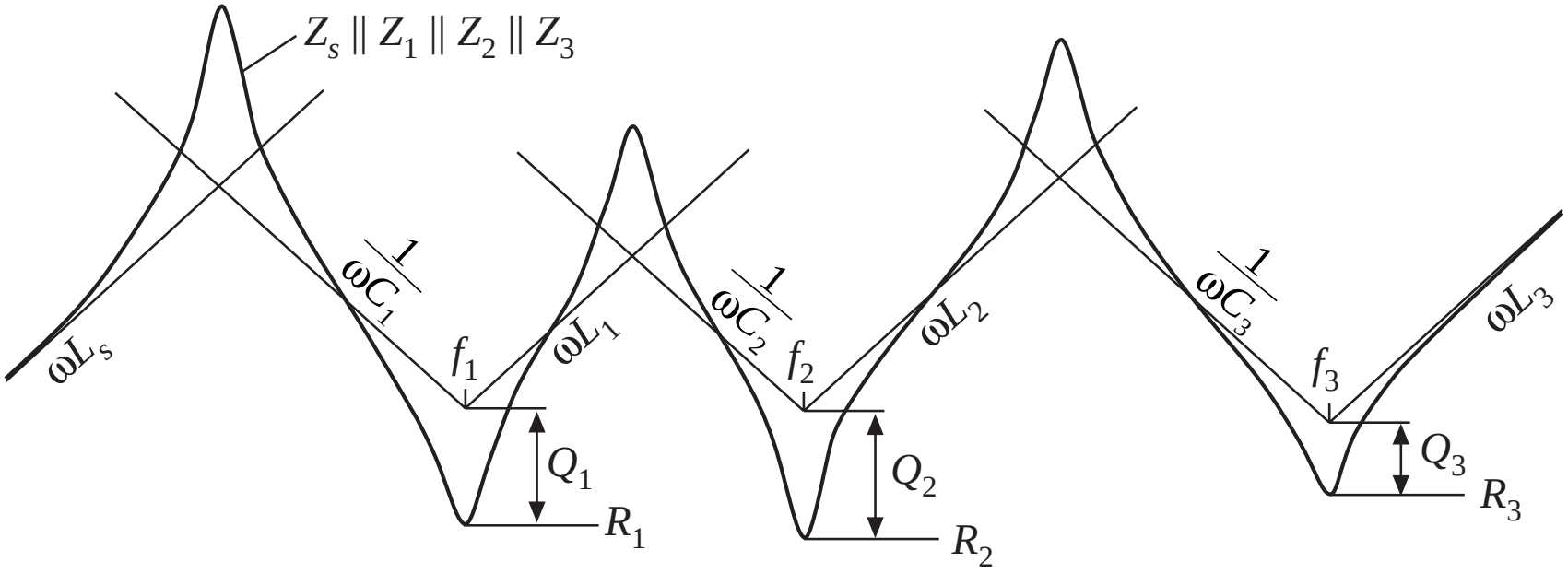


- Series resonance: fifth harmonic trap
- Parallel resonance: C_1 and L_s
- Parallel resonance tends to increase amplitude of third harmonic
- Q of parallel resonance is larger than Q of series resonance

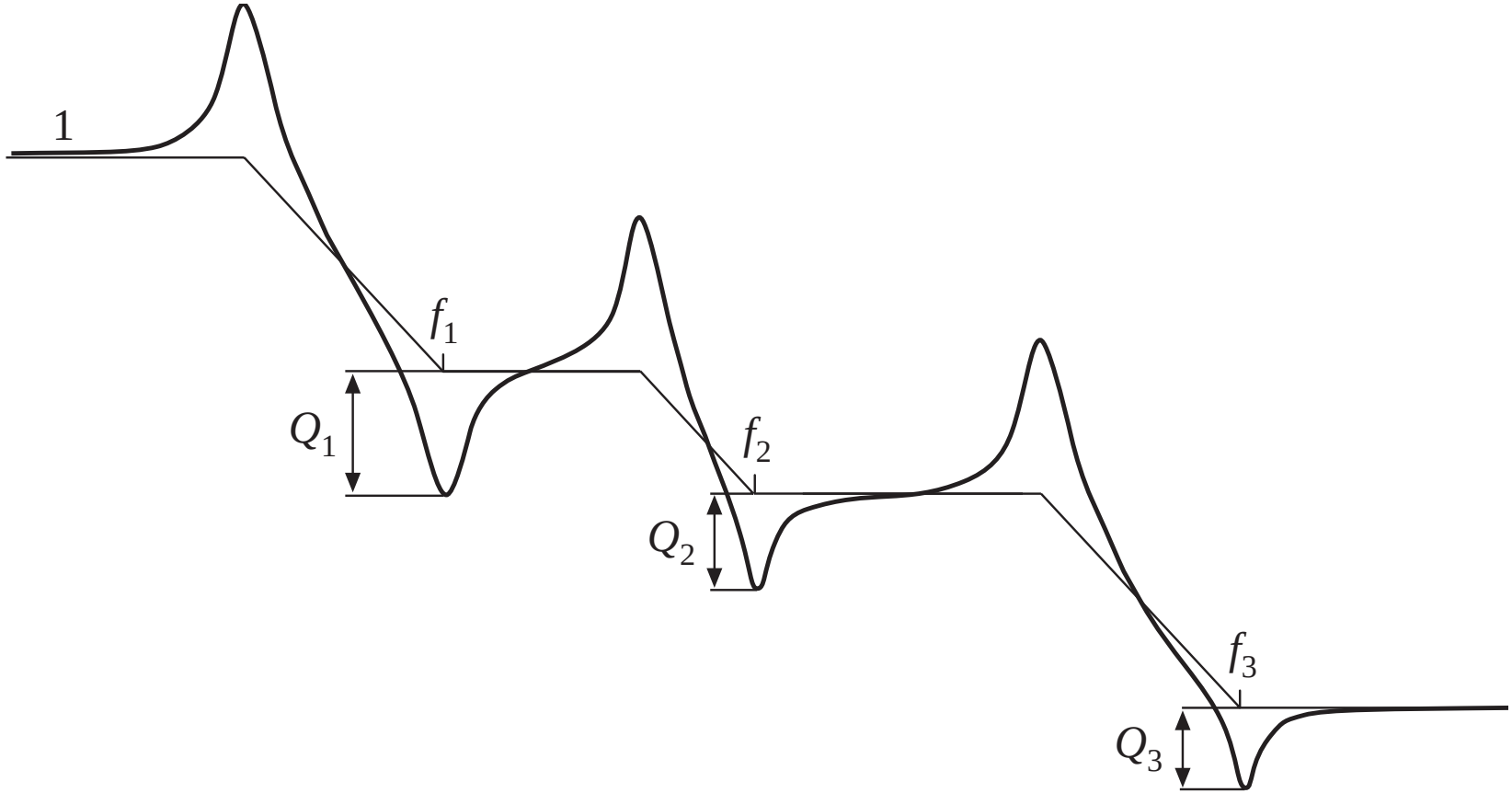
Example 2


L_s
i_s
R_1
L_1
C_1
R_2
L_2
C_2
R_3
L_3
C_3
i_r
5^{th} harmonic trap Z_1
7^{th} harmonic trap Z_2
11^{th} harmonic trap Z_3

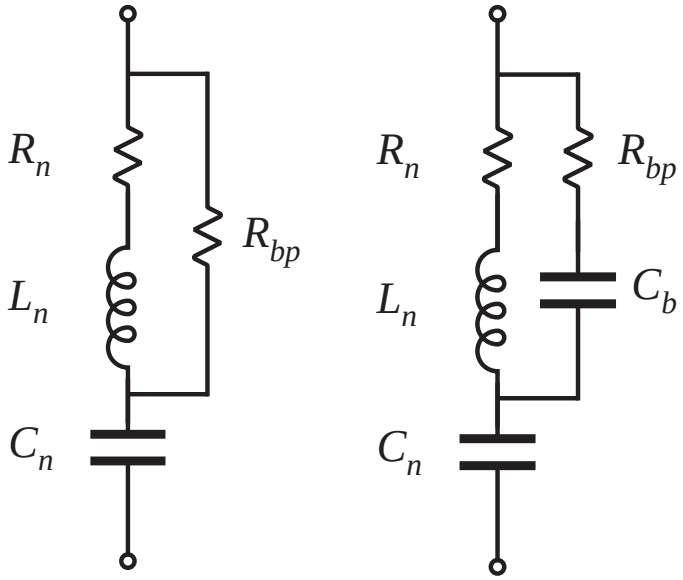
Approximate impedance asymptotes

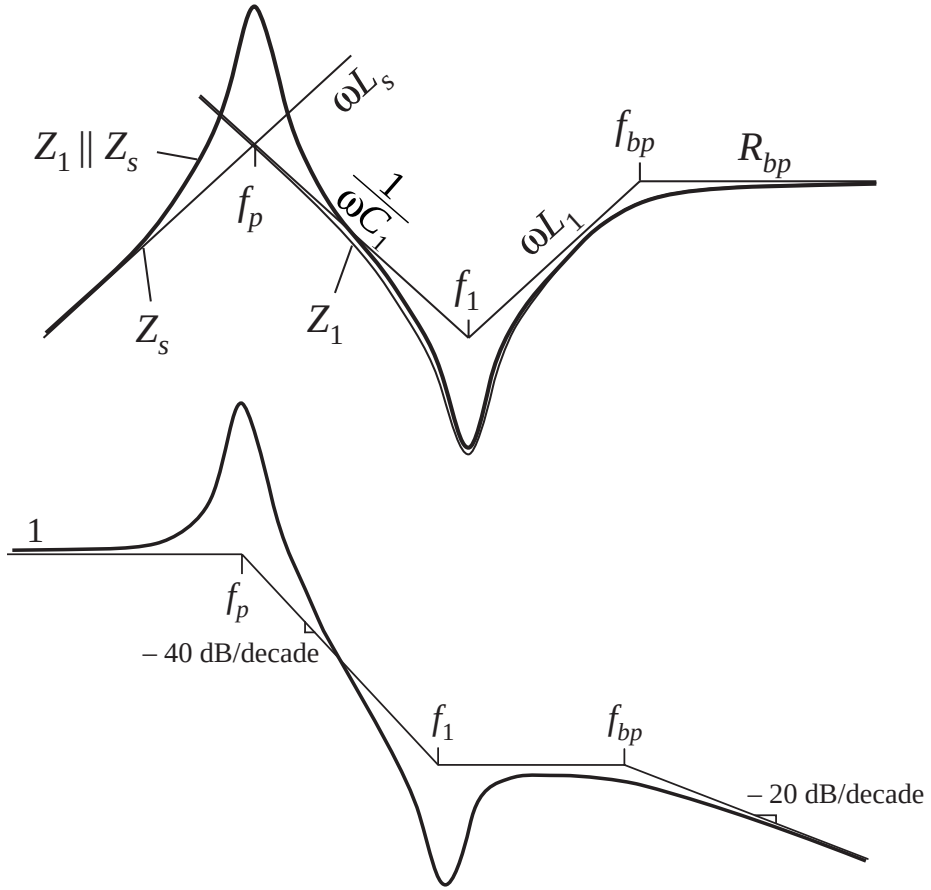


Transfer function asymptotes

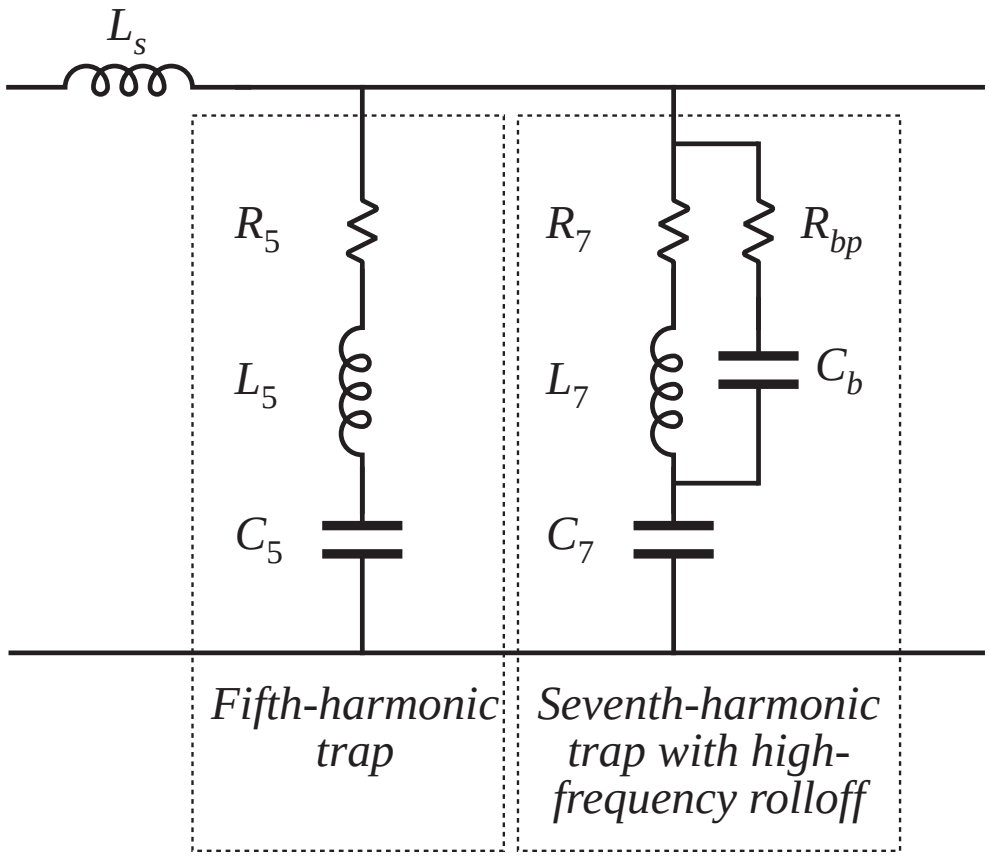


Bypass resistor





Harmonic trap filter with high-frequency roll-off

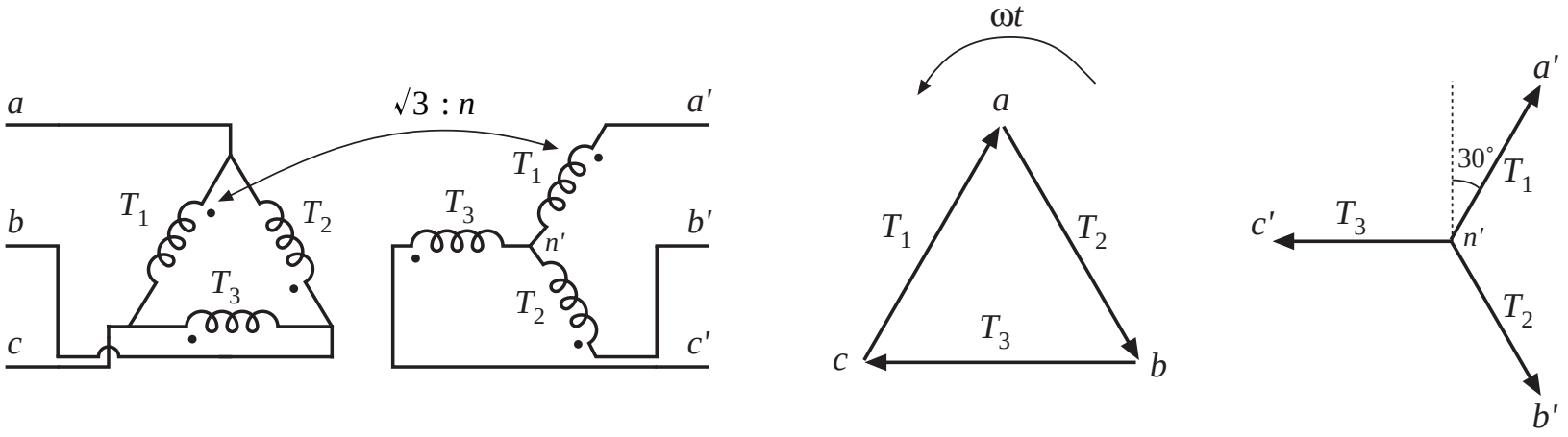


17.5 Transformer connections

Three-phase transformer connections can be used to shift the phase of the voltages and currents

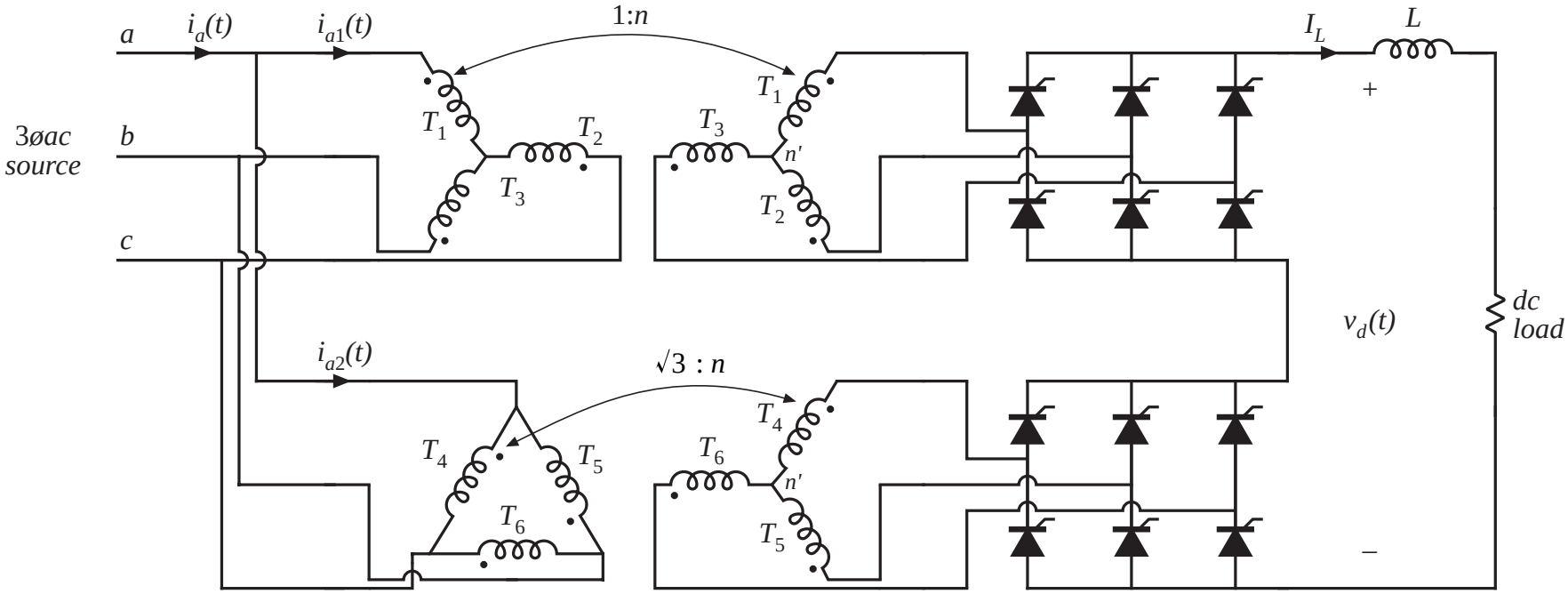
This shifted phase can be used to cancel out the low-order harmonics

Three-phase delta-wye transformer connection shifts phase by 30°:

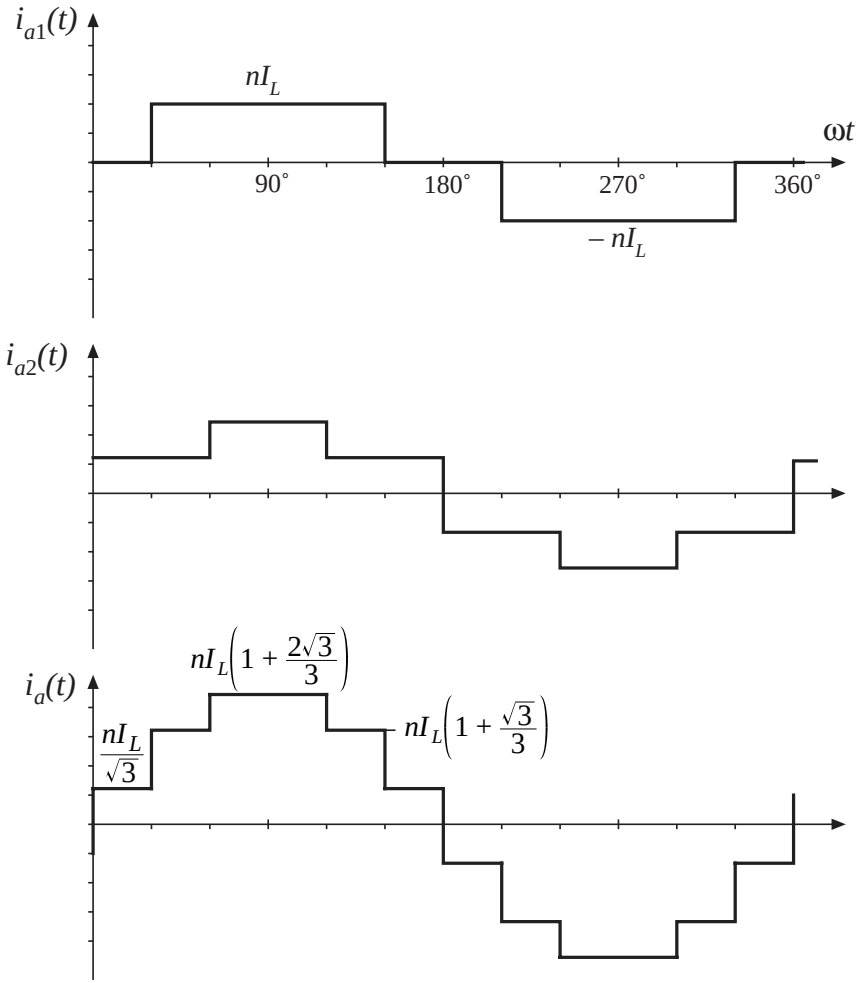


Primary voltages *Secondary voltages*

Twelve-pulse rectifier



Waveforms of 12 pulse rectifier



- Ac line current contains 1st, 11th, 13th, 23rd, 25th, etc. These harmonic amplitudes vary as $1/n$
- 5th, 7th, 17th, 19th, etc. harmonics are eliminated

Rectifiers with high pulse number

Eighteen-pulse rectifier:

- Use three six-pulse rectifiers
- Transformer connections shift phase by 0˚, +20˚, and –20˚
- No 5th, 7th, 11th, 13th harmonics

Twenty-four-pulse rectifier

- Use four six-pulse rectifiers
- Transformer connections shift phase by 0˚, 15˚, –15˚, and 30˚
- No 5th, 7th, 11th, 13th, 17th, or 19th harmonics

If p is pulse number, then rectifier produces line current harmonics of number $n = pk \pm 1$, with $k = 0, 1, 2, \ldots$

Chapter 18

Low Harmonic Rectifier Modeling and Control

18.1 Modeling losses and efficiency in CCM high-quality rectifiers

- Expression for controller duty cycle $d(t)$
- Expression for the dc load current
- Solution for converter efficiency η
- Design example

18.2 Controller schemes

- Average current control
- Feedforward
- Current programmed control
- Hysteretic control
- Nonlinear carrier control

18.3 Control system modeling

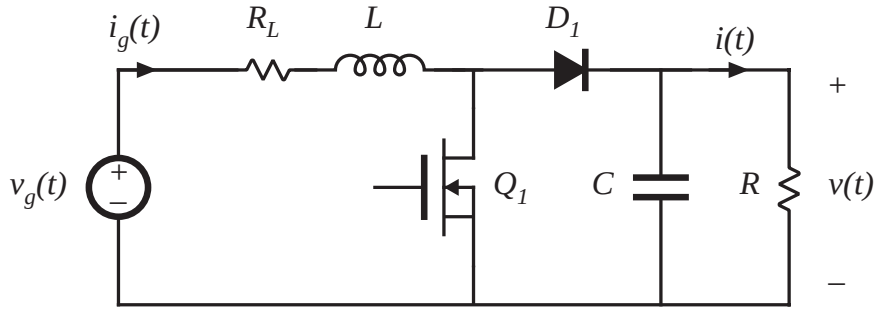
- Modeling the outer low-bandwidth control system
- Modeling the inner wide-bandwidth average current controller

18.1 Modeling losses and efficiency in CCM high-quality rectifiers

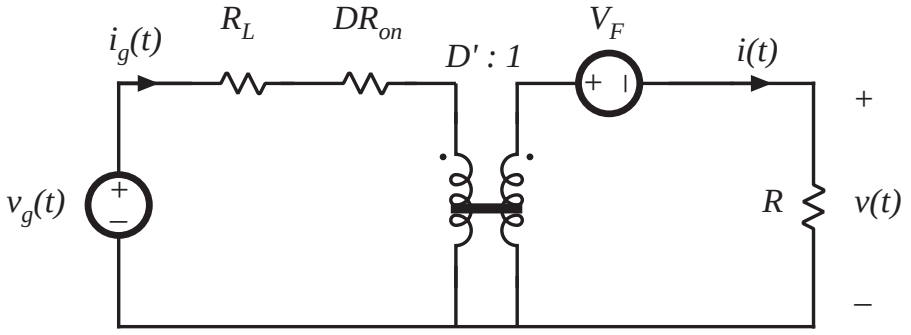
Objective: extend procedure of Chapter 3, to predict the output voltage, duty cycle variations, and efficiency, of PWM CCM low harmonic rectifiers.

Approach: Use the models developed in Chapter 3. Integrate over one ac line cycle to determine steady-state waveforms and average power.

Boost example



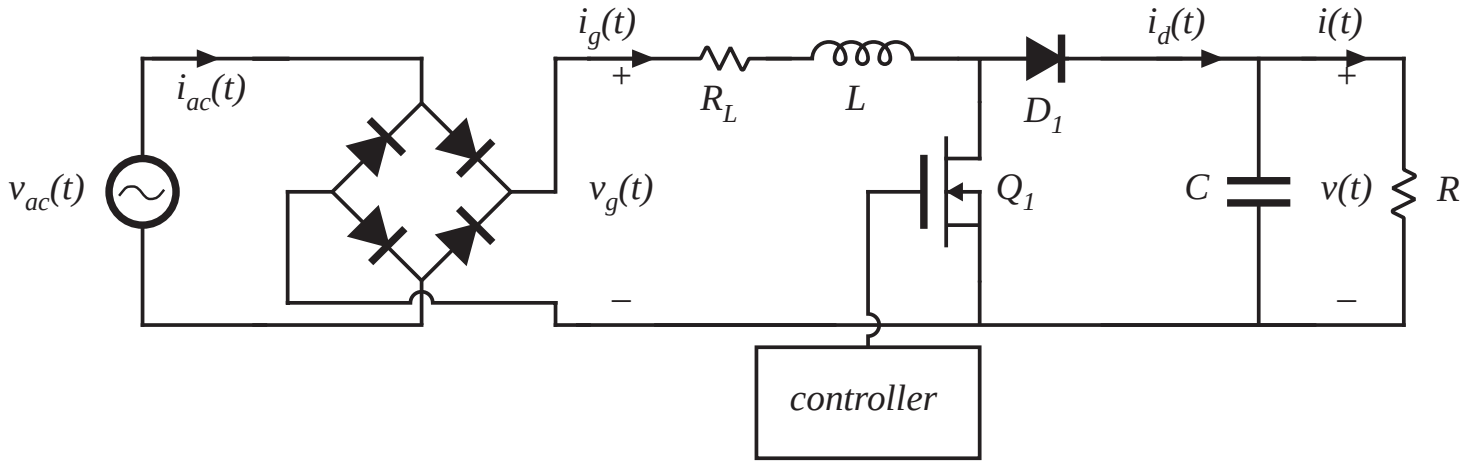
Dc-dc boost converter circuit



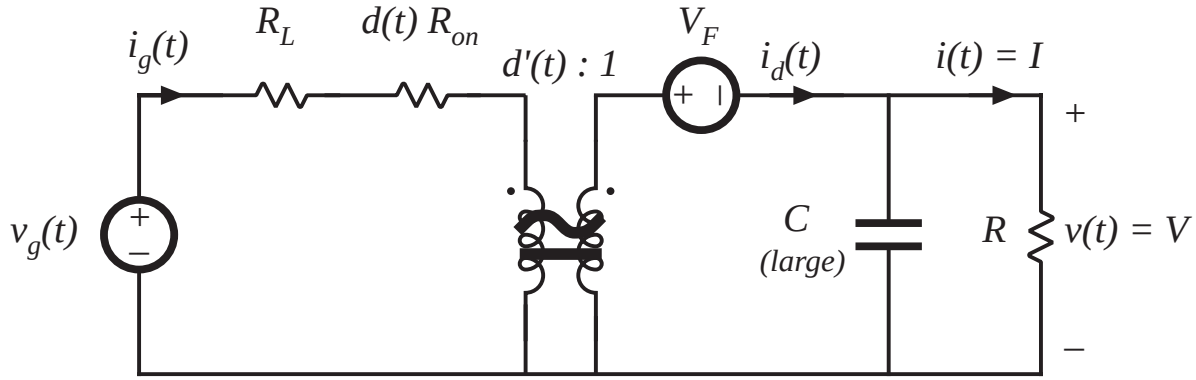
Averaged dc model

Modeling the ac-dc boost rectifier

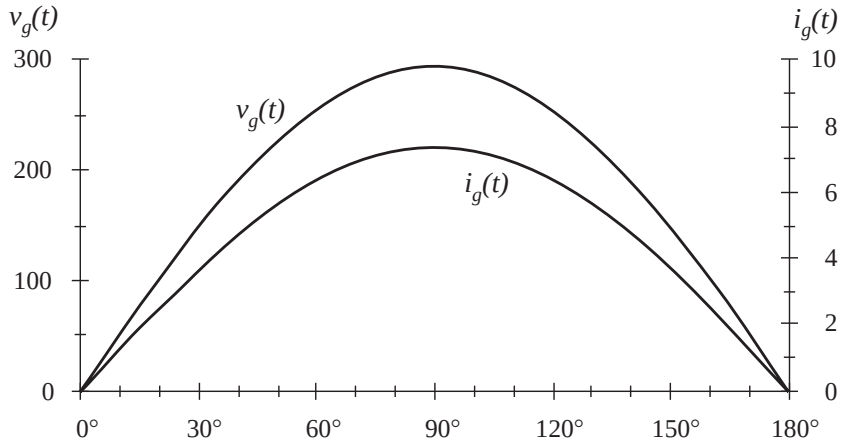
Boost rectifier circuit



Averaged model



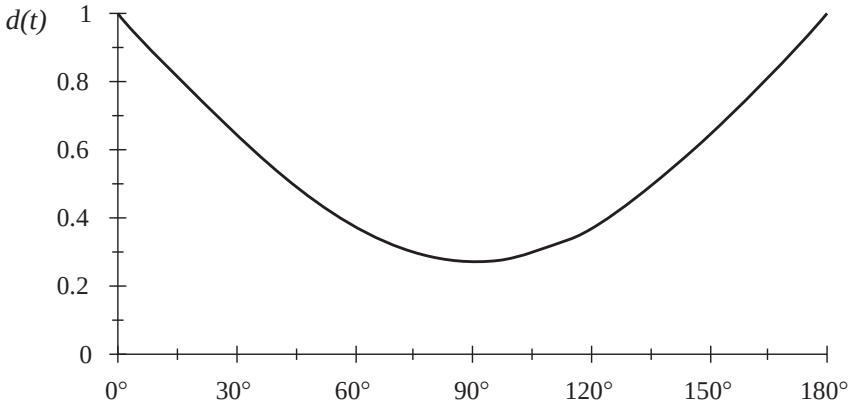
Boost rectifier waveforms

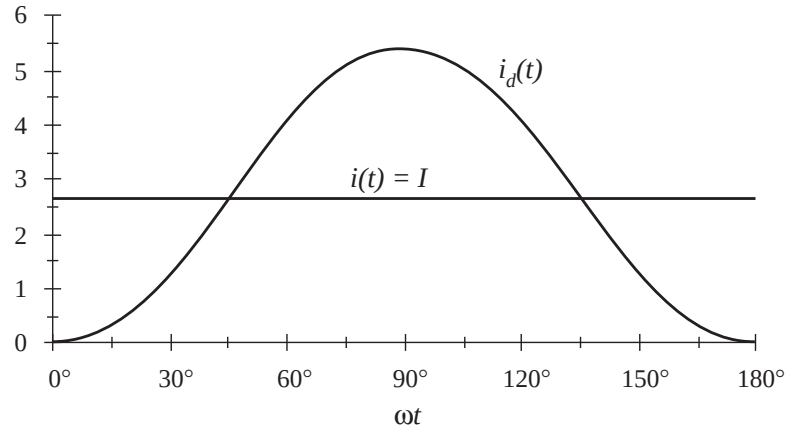


Typical waveforms

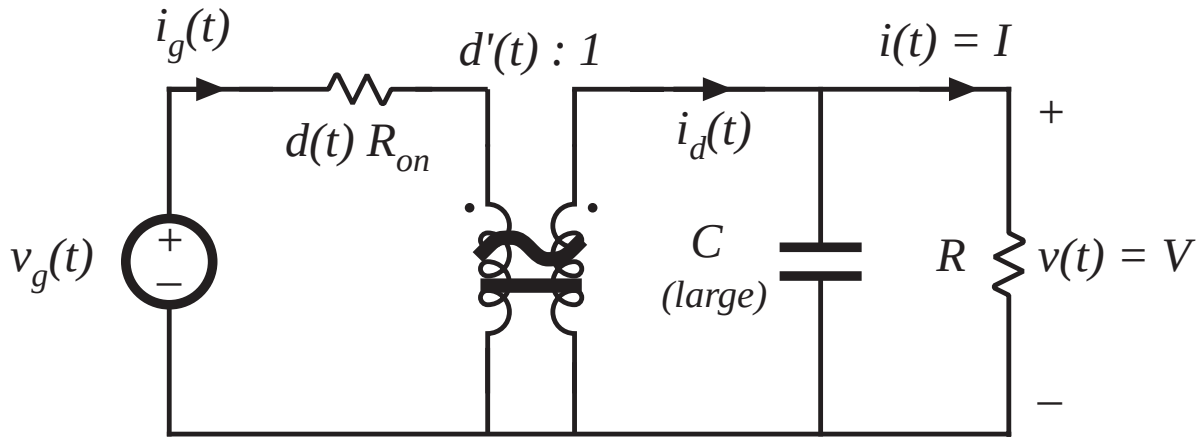
(low frequency components)

$$i_g(t) = \frac{v_g(t)}{R_e}$$





Example: boost rectifier with MOSFET on-resistance



Averaged model

Inductor dynamics are neglected, a good approximation when the ac line variations are slow compared to the converter natural frequencies

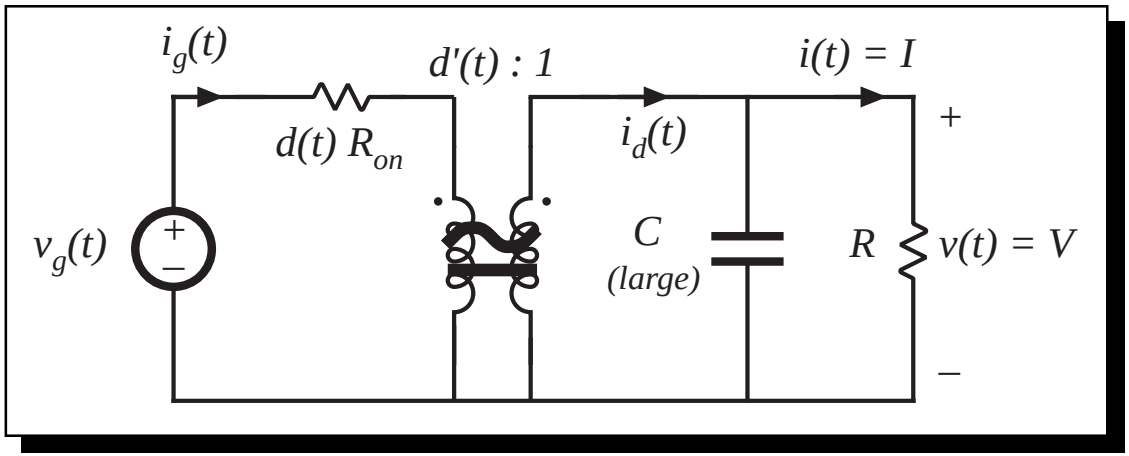
18.1.1 Expression for controller duty cycle $d(t)$

Solve input side of model:

$$i_g(t) d(t) R_{on} = v_g(t) - d'(t) v$$

with $$i_g(t) = \frac{v_g(t)}{R_e}$$

$$v_g(t) = V_M \left| \sin \omega t \right|$$



eliminate $i_g(t)$:

$$\frac{v_g(t)}{R_e} d(t) R_{on} = v_g(t) - d'(t) v$$

solve for $d(t)$:

$$d(t) = \frac{v - v_g(t)}{v - v_g(t) \dfrac{R_{on}}{R_e}}$$

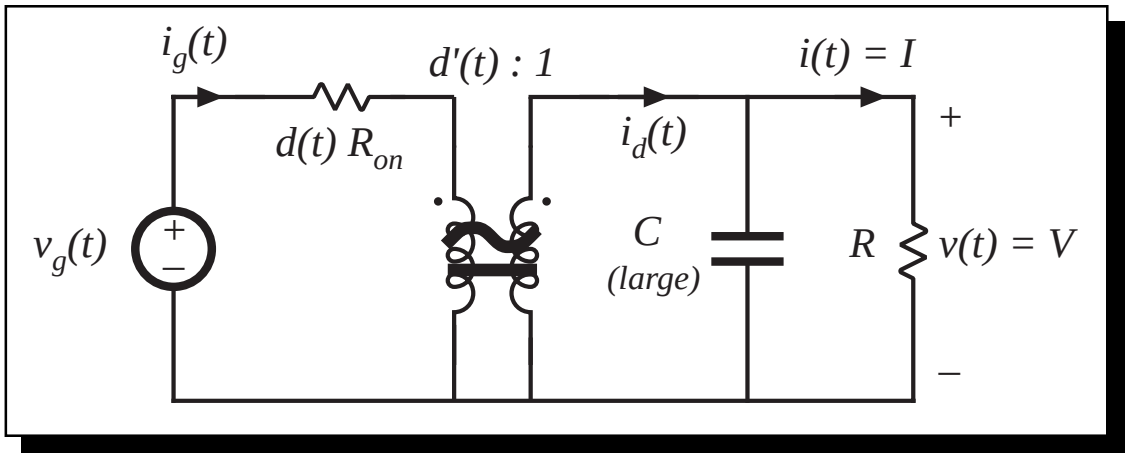
Again, these expressions neglect converter dynamics, and assume that the converter always operates in CCM.

18.1.2 Expression for the dc load current

Solve output side of model, using charge balance on capacitor C:

$$I = \left\langle i_d \right\rangle_{T_{ac}}$$

$$i_d(t) = d'(t) i_g(t) = d'(t) \frac{v_g(t)}{R_e}$$



But $d'(t)$ is:

$$d'(t) = \frac{v_g(t)\left(1 - \frac{R_{on}}{R_e}\right)}{v - v_g(t)\frac{R_{on}}{R_e}}$$

hence $i_d(t)$ can be expressed as

$$i_d(t) = \frac{v_g^2(t)}{R_e} \frac{\left(1 - \frac{R_{on}}{R_e}\right)}{v - v_g(t)\frac{R_{on}}{R_e}}$$

Next, average $i_d(t)$ over an ac line period, to find the dc load current I.

Dc load current I

Now substitute $v_g(t) = V_M \sin \omega t$, and integrate to find $\langle i_d(t) \rangle_{Tac}$:

$$I = \left\langle i_d \right\rangle_{T_{ac}} = \frac{2}{T_{ac}} \int_0^{T_{ac}/2} \left(\frac{V_M^2}{R_e} \right) \frac{\left(1 - \frac{R_{on}}{R_e} \right) \sin^2 \left(\omega t \right)}{\left(v - \frac{V_M R_{on}}{R_e} \sin \left(\omega t \right) \right)} \, dt$$

This can be written in the normalized form

$$I = \frac{2}{T_{ac}} \frac{V_M^2}{V R_e} \left(1 - \frac{R_{on}}{R_e} \right) \int_0^{T_{ac}/2} \frac{\sin^2 \left(\omega t \right)}{1 - a \sin \left(\omega t \right)} \, dt$$

with $$a = \left(\frac{V_M}{V} \right) \left(\frac{R_{on}}{R_e} \right)$$

Integration

By waveform symmetry, we need only integrate from 0 to $T_{ac}/4$. Also, make the substitution $\theta = \omega t$:

$$I = \frac{V_M^2}{VR_e}\left(1 - \frac{R_{on}}{R_e}\right)\frac{2}{\pi}\int_0^{\pi/2} \frac{\sin^2(\theta)}{1 - a\sin(\theta)}\, d\theta$$

This integral is obtained not only in the boost rectifier, but also in the buck-boost and other rectifier topologies. The solution is

$$\frac{4}{\pi}\int_0^{\pi/2} \frac{\sin^2(\theta)}{1 - a\sin(\theta)}\, d\theta = F(a) = \frac{2}{a^2\pi}\left(-2a - \pi + \frac{4\sin^{-1}(a) + 2\cos^{-1}(a)}{\sqrt{1-a^2}}\right)$$

- Result is in closed form
- a is a measure of the loss resistance relative to R_e
- a is typically much smaller than unity

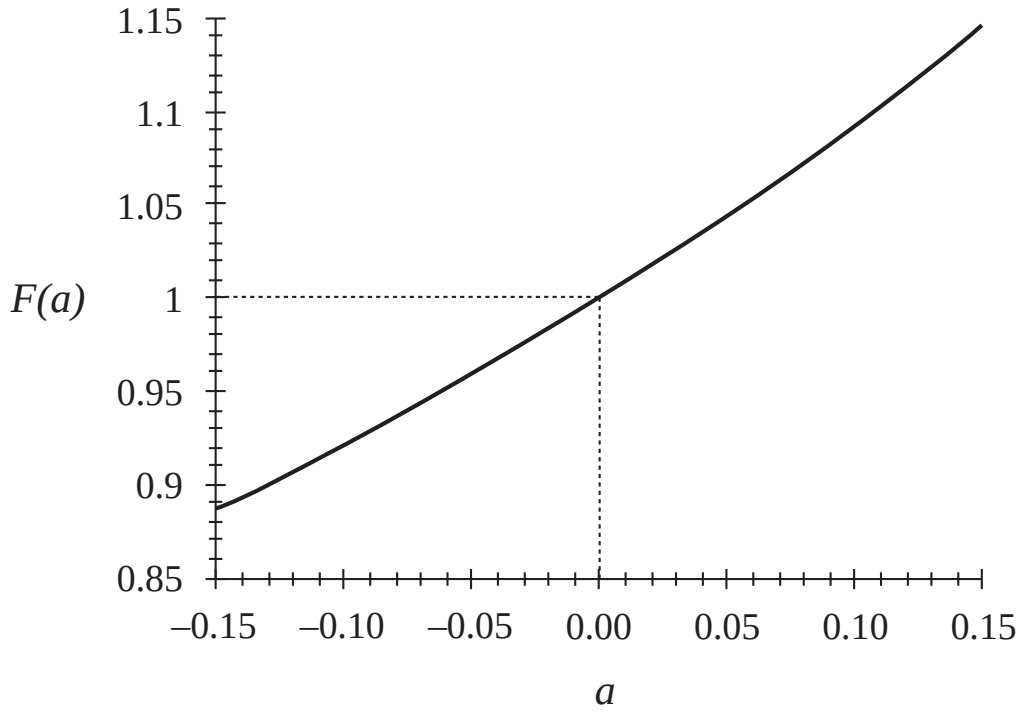
The integral $F(a)$

$$\frac{4}{\pi}\int_0^{\pi/2}\frac{\sin^2\left(\theta\right)}{1-a\sin\left(\theta\right)}\,d\theta = F(a) = \frac{2}{a^2\pi}\left(-2a-\pi+\frac{4\sin^{-1}\left(a\right)+2\cos^{-1}\left(a\right)}{\sqrt{1-a^2}}\right)$$

Approximation via polynomial:

$$F(a) \approx 1 + 0.862a + 0.78a^2$$

For $|a| \le 0.15$, this approximate expression is within 0.1% of the exact value. If the a^2 term is omitted, then the accuracy drops to ±2% for $|a| \le 0.15$. The accuracy of *F(a)* coincides with the accuracy of the rectifier efficiency η.



18.1.4 Solution for converter efficiency η

Converter average input power is

$$P_{in} = \left\langle p_{in}(t) \right\rangle_{T_{ac}} = \frac{V_M^2}{2R_e}$$

Average load power is

$$P_{out} = VI = \left(V\right)\left(\frac{V_M^2}{VR_e}\left(1 - \frac{R_{on}}{R_e}\right)\frac{F(a)}{2}\right) \qquad \text{with} \qquad a = \left(\frac{V_M}{V}\right)\left(\frac{R_{on}}{R_e}\right)$$

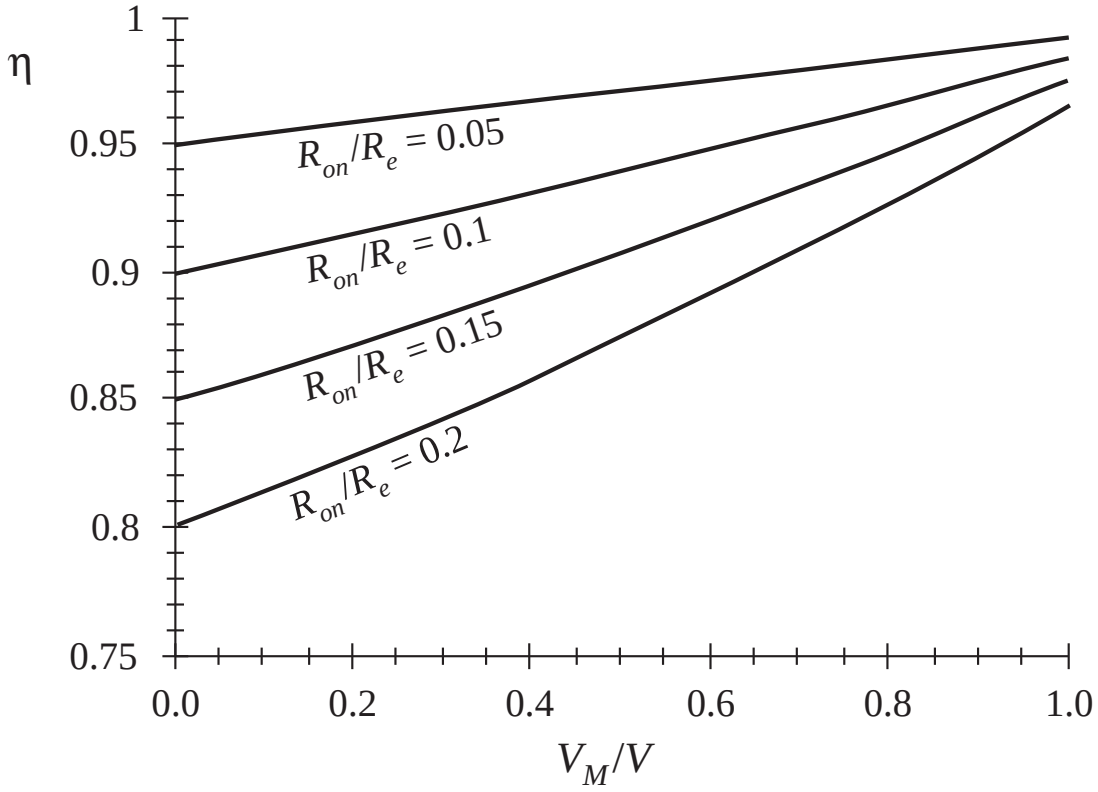
So the efficiency is

$$\eta = \frac{P_{out}}{P_{in}} = \left(1 - \frac{R_{on}}{R_e}\right) F(a)$$

Polynomial approximation:

$$\eta \approx \left(1 - \frac{R_{on}}{R_e}\right)\left(1 + 0.862\,\frac{V_M}{V}\,\frac{R_{on}}{R_e} + 0.78\left(\frac{V_M}{V}\,\frac{R_{on}}{R_e}\right)^2\right)$$

Boost rectifier efficiency



$$\eta = \frac{P_{out}}{P_{in}} = \left(1 - \frac{R_{on}}{R_e}\right) F(a)$$

- To obtain high efficiency, choose V slightly larger than V_M
- Efficiencies in the range 90% to 95% can then be obtained, even with R_{on} as high as $0.2R_e$
- Losses other than MOSFET on-resistance are not included here

18.1.5 Design example

Let us design for a given efficiency. Consider the following specifications:

Output voltage	390 V
Output power	500 W
rms input voltage	120 V
Efficiency	95%

Assume that losses other than the MOSFET conduction loss are negligible.

Average input power is

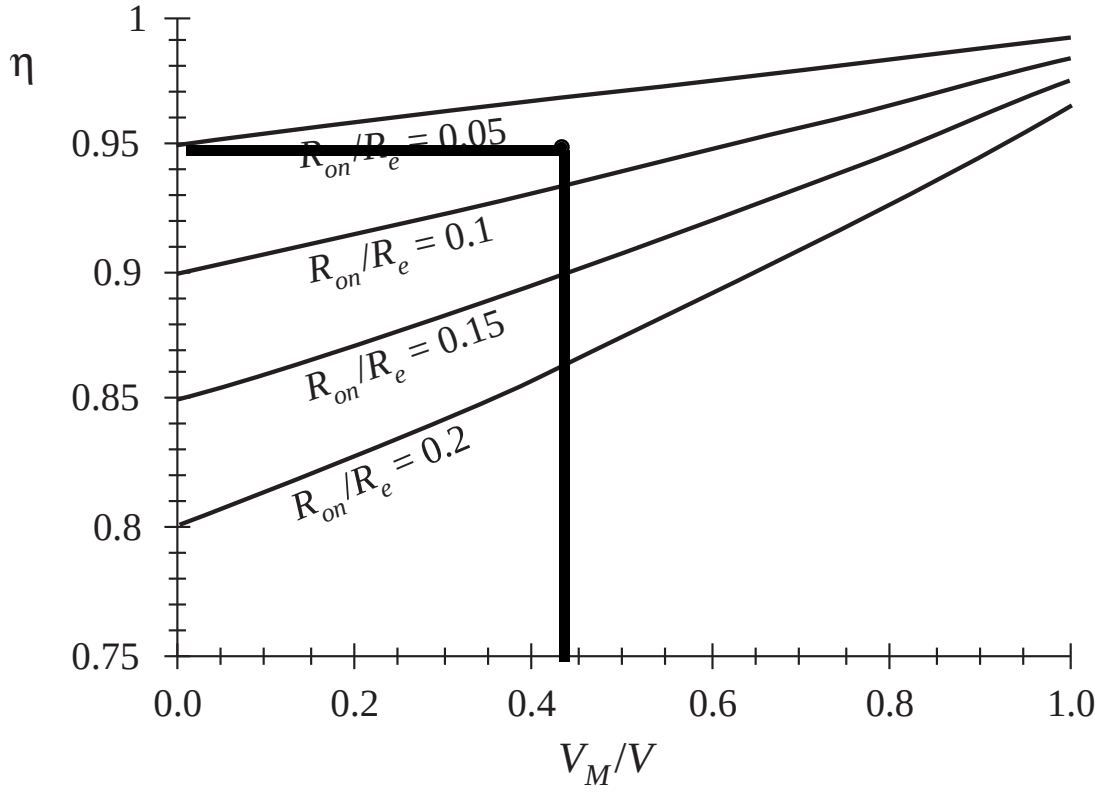
$$P_{in} = \frac{P_{out}}{\eta} = \frac{500\ \text{W}}{0.95} = 526\ \text{W}$$

Then the emulated resistance is

$$R_e = \frac{V_{g,\,rms}^2}{P_{in}} = \frac{(120\ \text{V})^2}{526\ \text{W}} = 27.4\ \Omega$$

Design example

Also, $\frac{V_M}{V} = \frac{120\sqrt{2}\ \text{V}}{390\ \text{V}} = 0.435$



95% efficiency with $V_M/V = 0.435$ occurs with $R_{on}/R_e \approx 0.075$.

So we require a MOSFET with on resistance of

$$R_{on} \le (0.075)\, R_e$$

$$= (0.075)\ (27.4\ \Omega) = 2\ \Omega$$

18.2 Controller schemes

Average current control

- Feedforward

Current programmed control

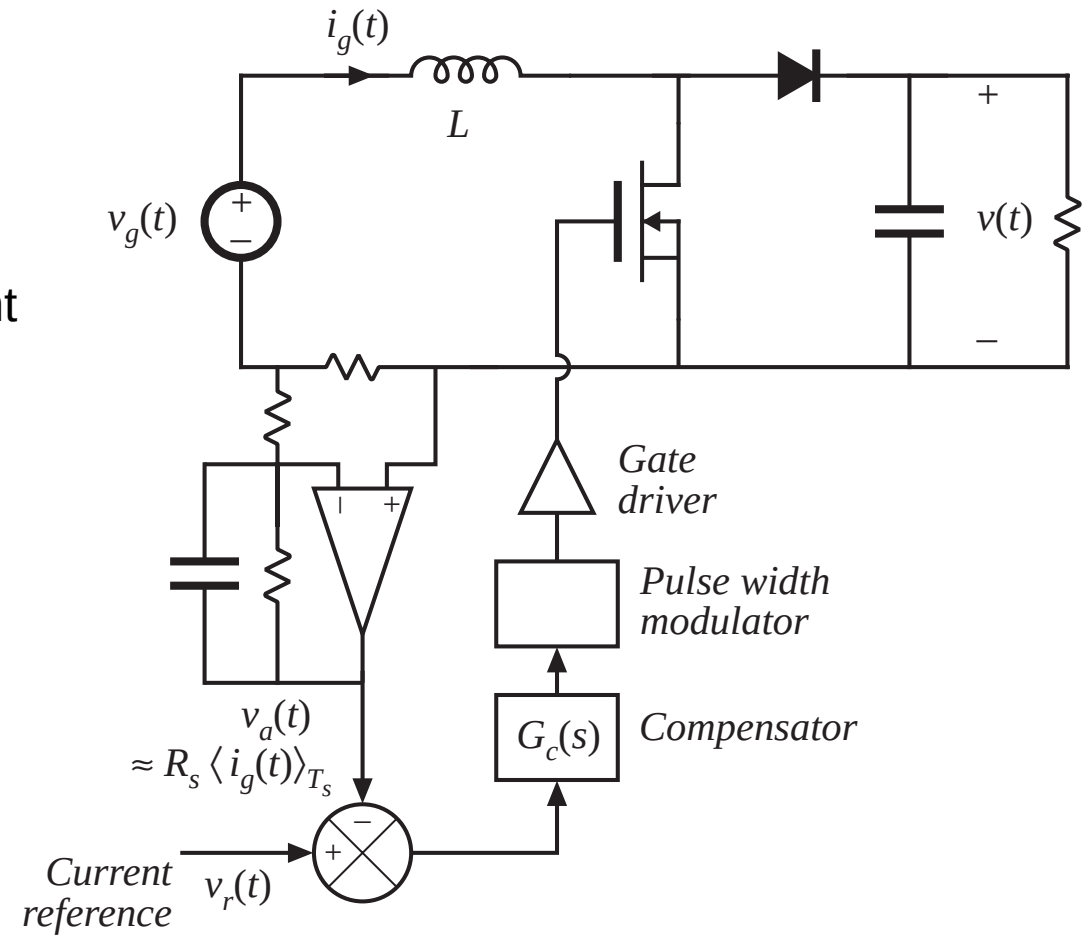
Hysteretic control

Nonlinear carrier control

18.2.1 Average current control

Boost example

Low frequency (average) component of input current is controlled to follow input voltage

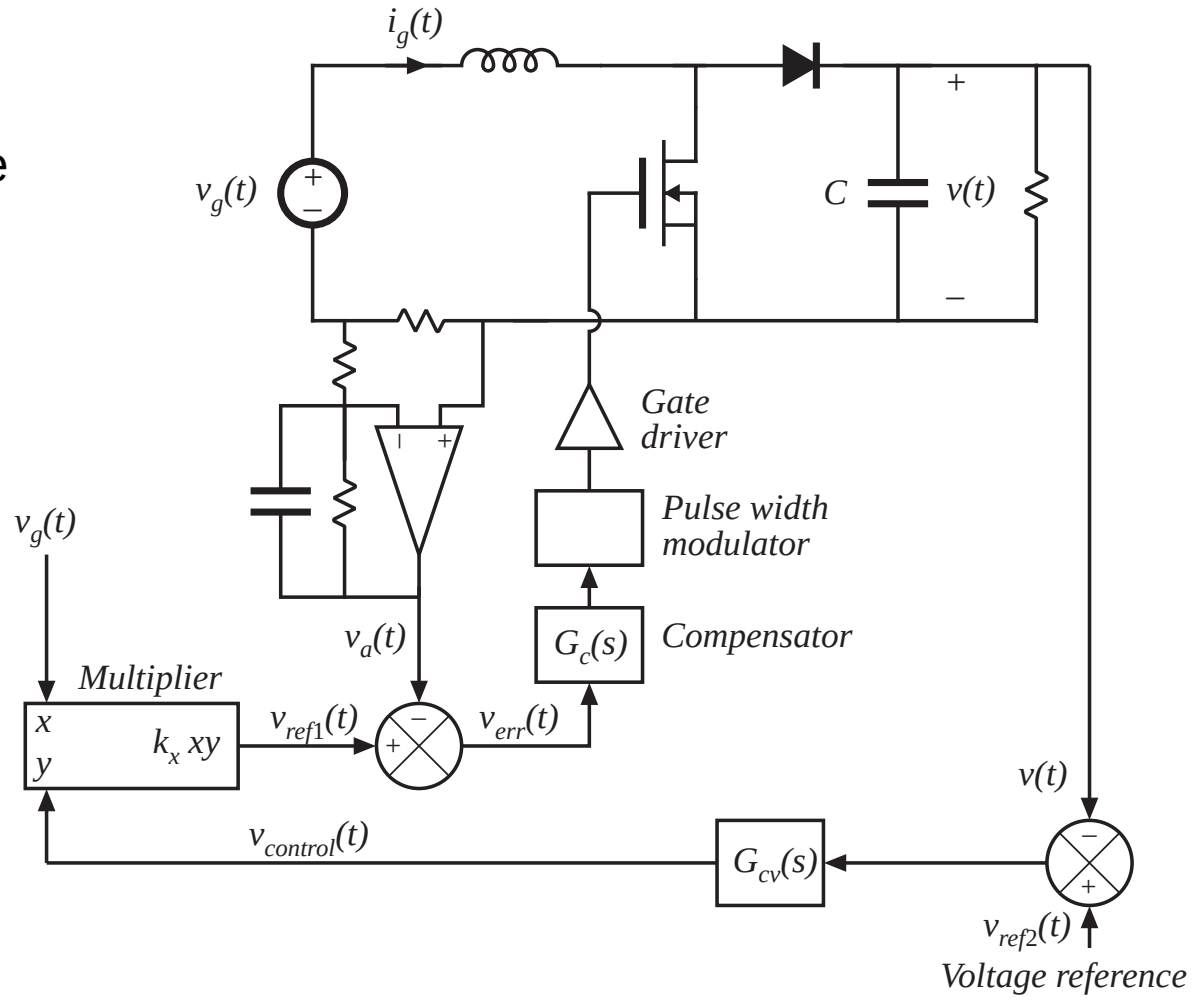


Use of multiplier to control average power

As discussed in Chapter 17, an output voltage feedback loop adjusts the emulated resistance R_e such that the rectifier power equals the dc load power:

$$P_{av} = \frac{V_{g,rms}^2}{R_e} = P_{load}$$

An analog multiplier introduces the dependence of R_e on $v(t)$.

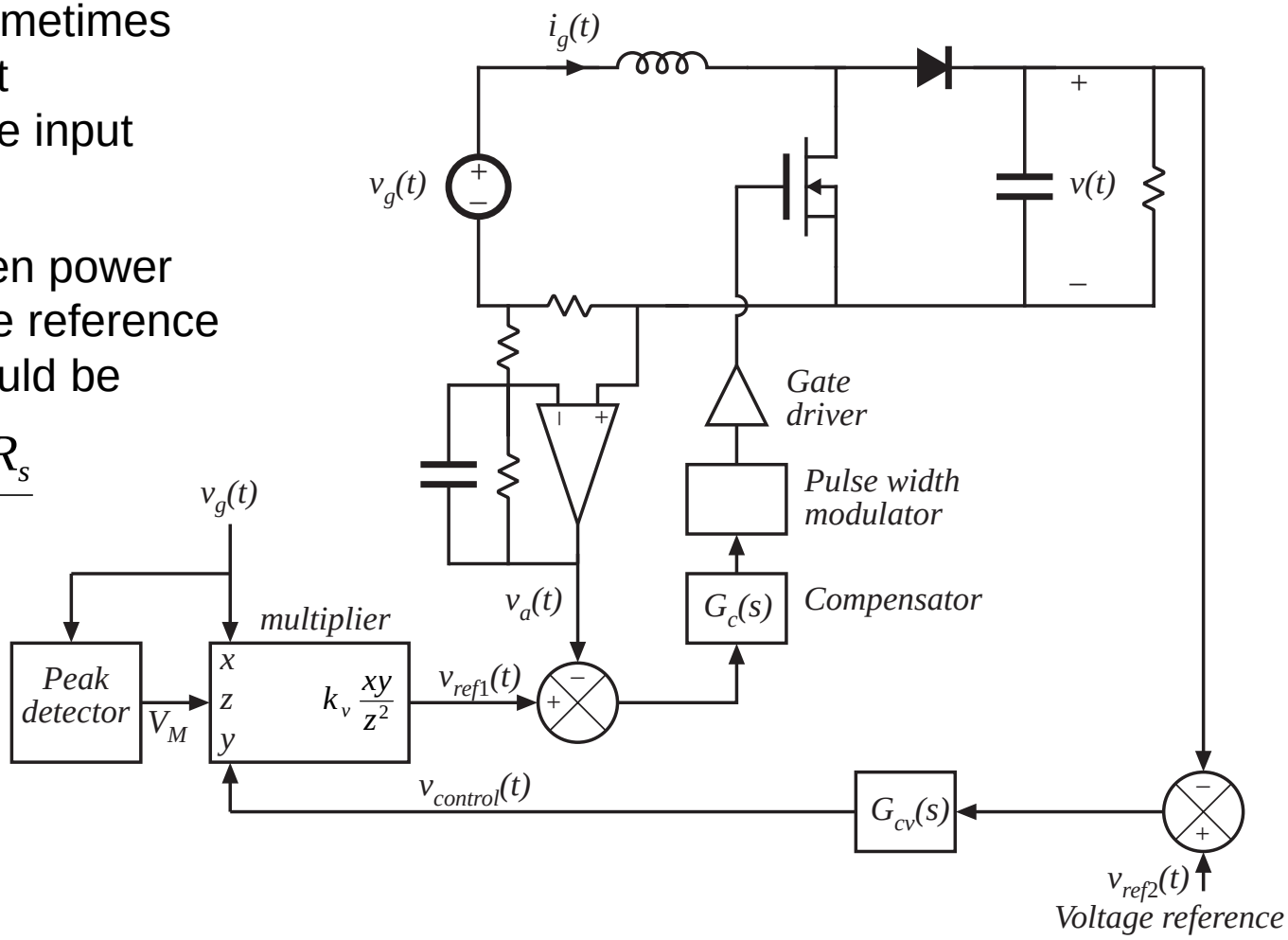


18.2.2 Feedforward

Feedforward is sometimes used to cancel out disturbances in the input voltage $v_g(t)$.

To maintain a given power throughput P_{av}, the reference voltage $v_{ref1}(t)$ should be

$$v_{ref1}(t) = \frac{P_{av} v_g(t) R_s}{V_{g,rms}^2}$$



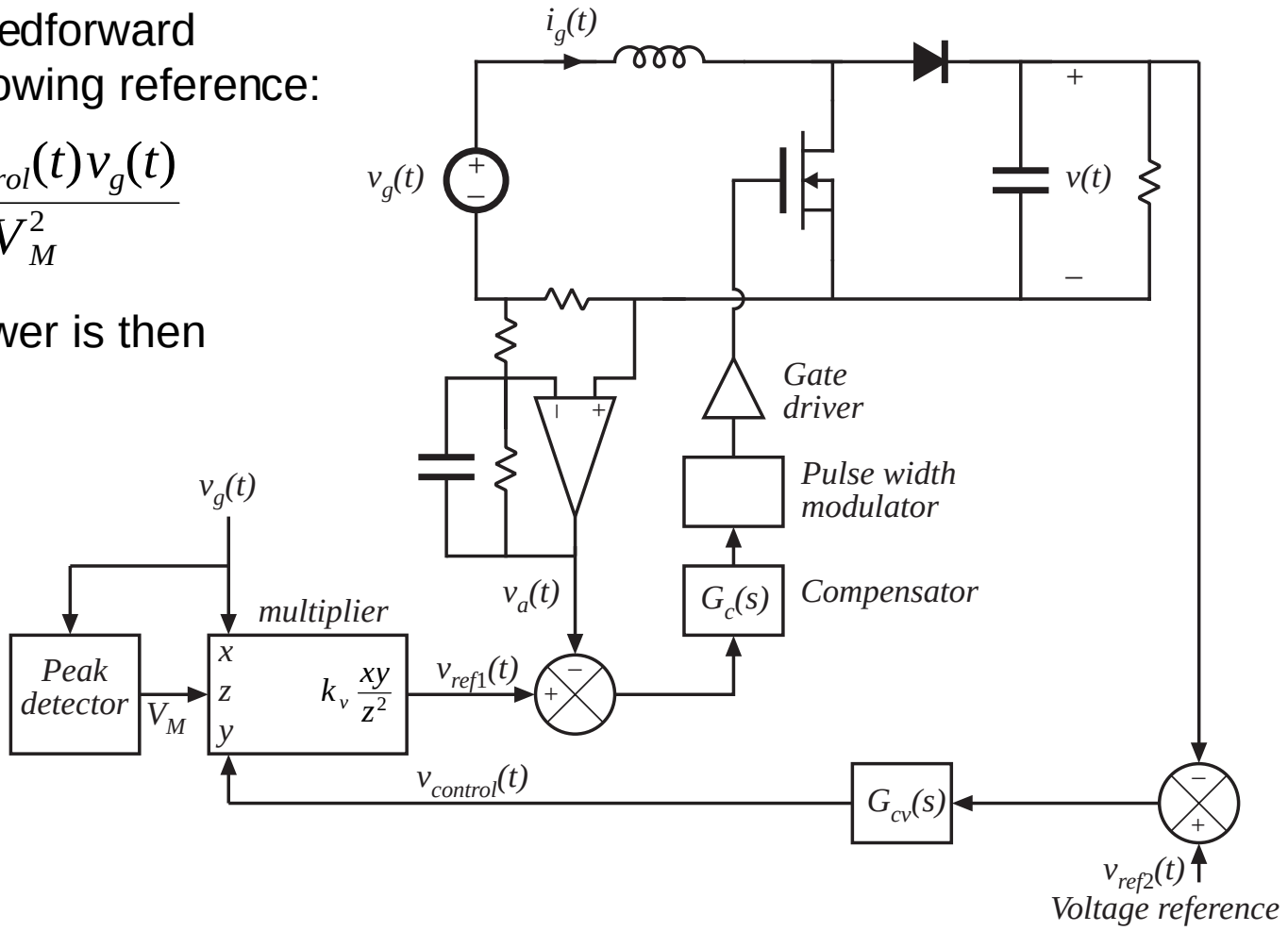
Feedforward, continued

Controller with feedforward produces the following reference:

$$v_{ref1}(t) = \frac{k_v v_{control}(t) v_g(t)}{V_M^2}$$

The average power is then given by

$$P_{av} = \frac{k_v v_{control}(t)}{2R_s}$$

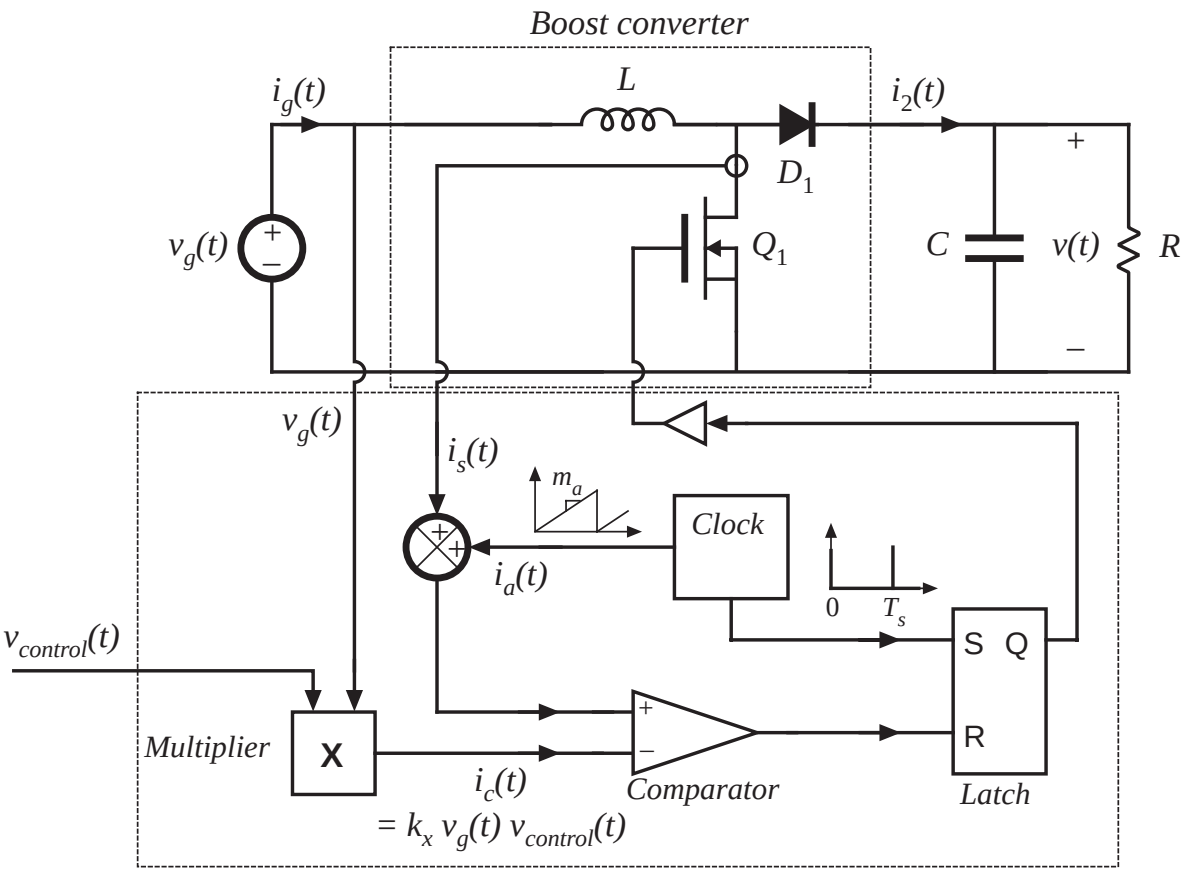


18.2.3 Current programmed control

Current programmed control is a natural approach to obtain input resistor emulation:

Peak transistor current is programmed to follow input voltage.

Peak transistor current differs from average inductor current, because of inductor current ripple and artificial ramp. This leads to significant input current waveform distortion.



Current-programmed controller

CPM boost converter: Static input characteristics

$$\left\langle i_g(t)\right\rangle_{T_s} = \begin{cases} v_g(t)\,\dfrac{L i_c^2(t) f_s}{\left(V - v_g(t)\right)\left(\dfrac{v_g(t)}{V} + \dfrac{m_a L}{V}\right)} & \text{in DCM} \\ i_c(t) + m_a T_s\left(\dfrac{v_g(t)}{V} - 1\right) + \dfrac{v_g^2(t) T_s}{2LV} & \text{in CCM} \end{cases}$$

Mode boundary: CCM occurs when

$$\left\langle i_g(t)\right\rangle_{T_s} > \frac{T_s V}{2L}\,\frac{v_g(t)}{V}\left(1 - \frac{v_g(t)}{V}\right)$$

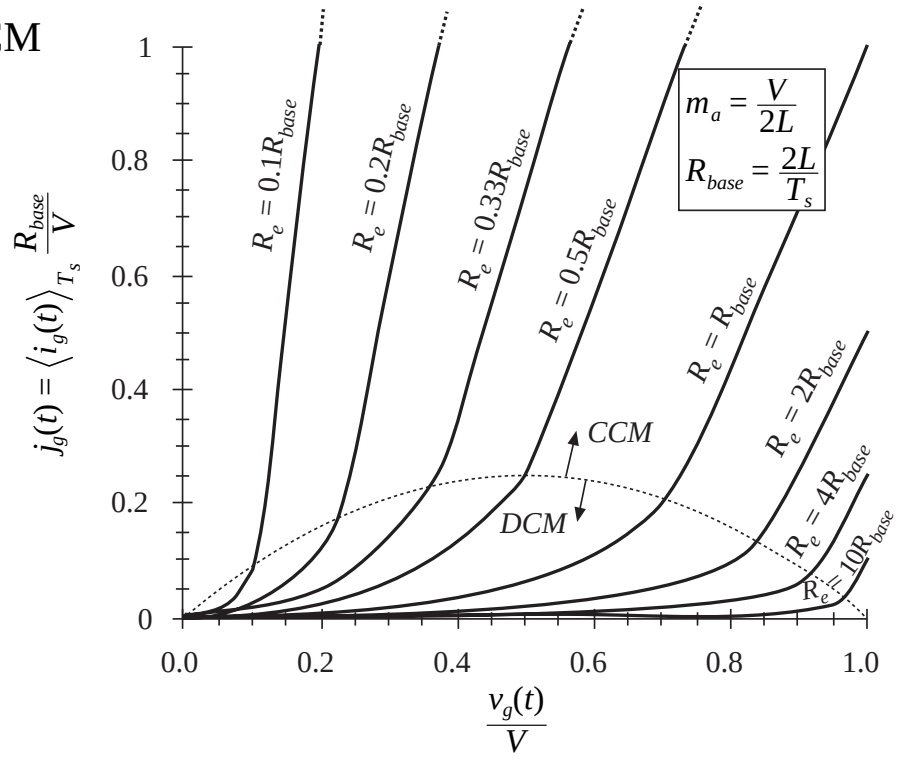
or, $$i_c(t) > \frac{T_s V}{L}\left(\frac{m_a L}{V} + \frac{v_g(t)}{V}\right)\left(1 - \frac{v_g(t)}{V}\right)$$

It is desired that $$i_c(t) = \frac{v_g(t)}{R_e}$$

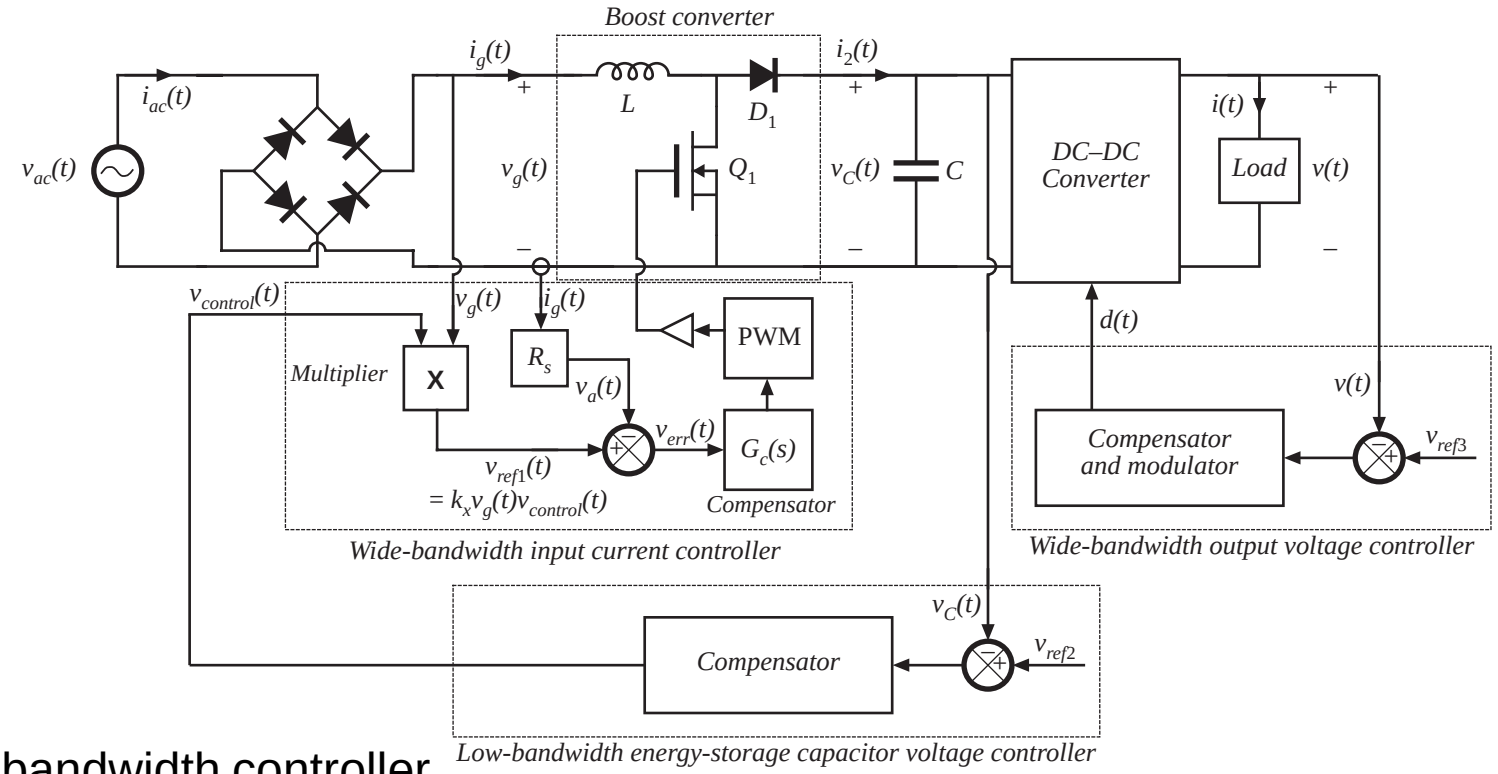
Minimum slope compensation:

$$m_a = \frac{V}{2L}$$

Static input characteristics of CPM boost, with minimum slope compensation:



18.3 Control system modeling
of high quality rectifiers



Two loops:

- Outer low-bandwidth controller
- Inner wide-bandwidth controller

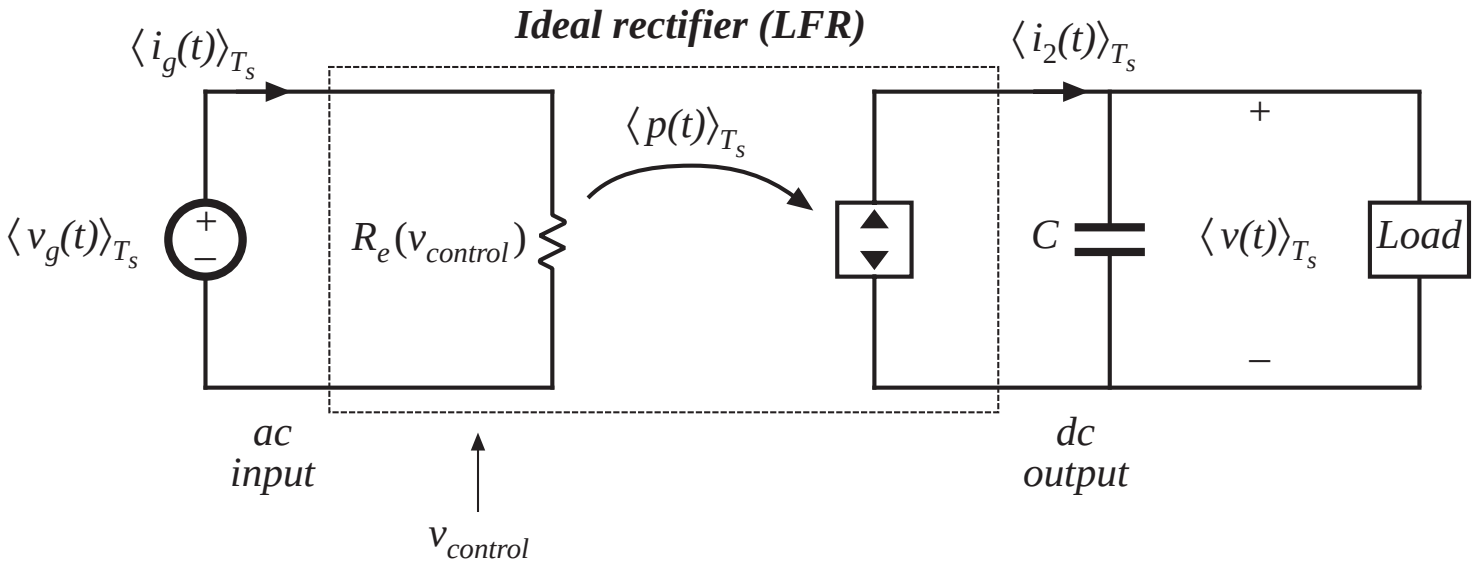
18.3.1 Modeling the outer low-bandwidth control system

This loop maintains power balance, stabilizing the rectifier output voltage against variations in load power, ac line voltage, and component values

The loop must be slow, to avoid introducing variations in R_e at the harmonics of the ac line frequency

Objective of our modeling efforts: low-frequency small-signal model that predicts transfer functions at frequencies below the ac line frequency

Large signal model
averaged over switching period T_s



Ideal rectifier model, assuming that inner wide-bandwidth loop operates ideally

High-frequency switching harmonics are removed via averaging

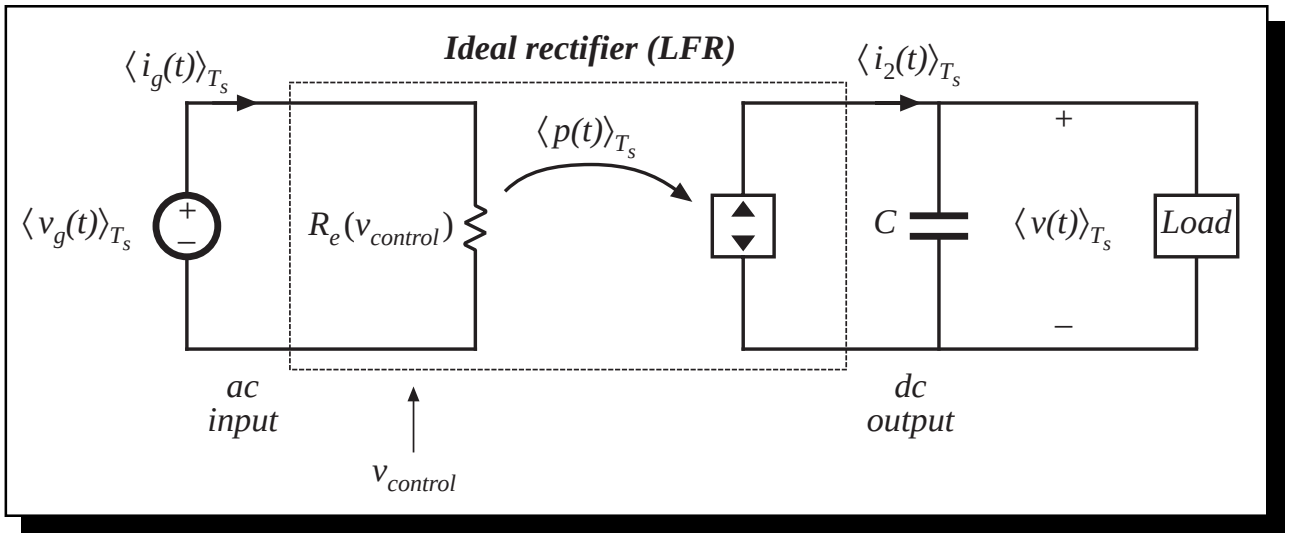
Ac line-frequency harmonics are included in model

Nonlinear and time-varying

Predictions of large-signal model

If the input voltage is

$$v_g(t) = \sqrt{2}\, v_{g,rms} \left| \sin\left(\omega t\right) \right|$$

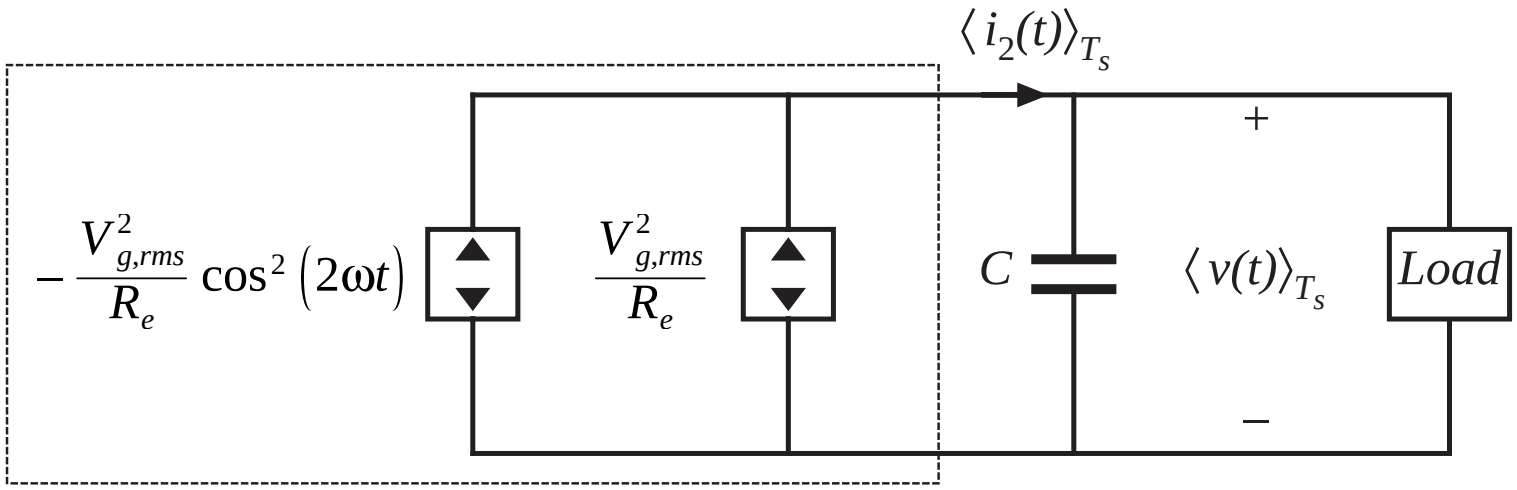


Then the instantaneous power is:

$$\left\langle p(t)\right\rangle_{T_s} = \frac{\left\langle v_g(t)\right\rangle_{T_s}^2}{R_e(v_{control}(t))} = \frac{v_{g,rms}^2}{R_e(v_{control}(t))}\left(1 - \cos\left(2\omega t\right)\right)$$

which contains a constant term plus a second-harmonic term

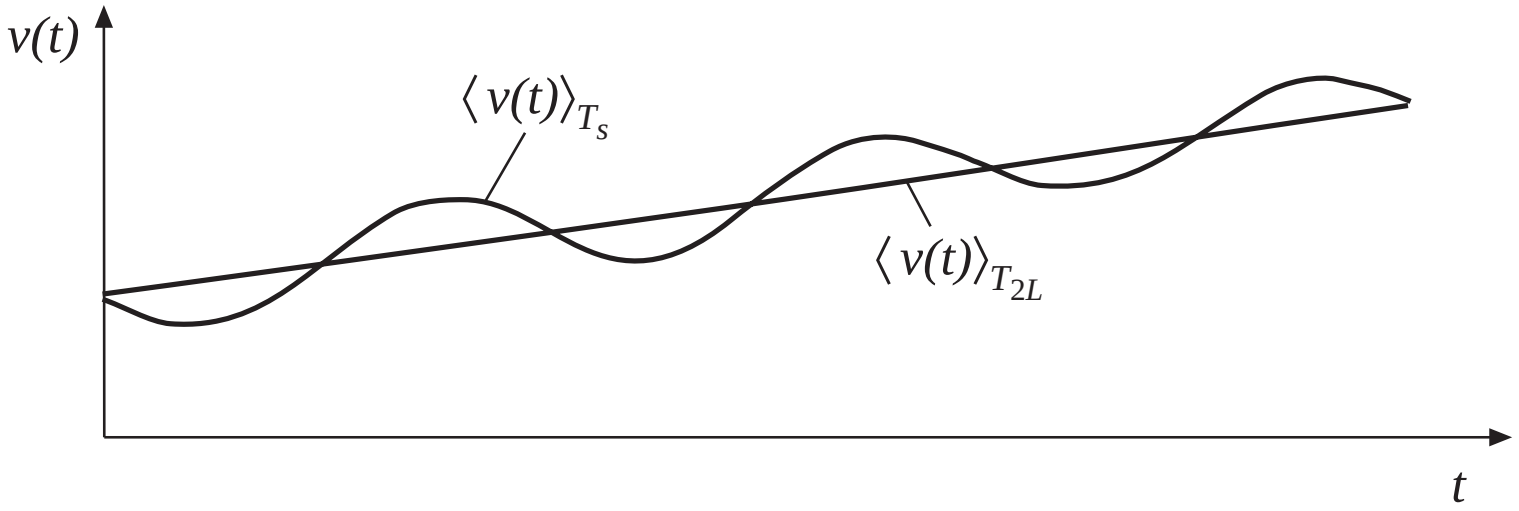
Separation of power source into its constant and time-varying components



Rectifier output port

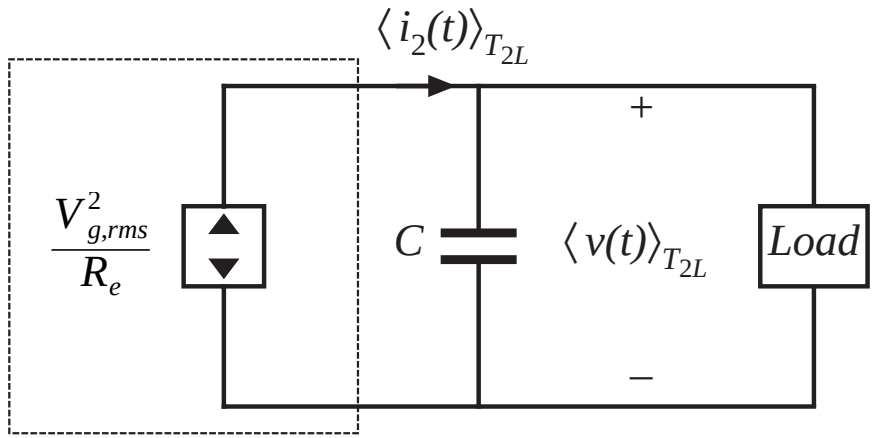
The second-harmonic variation in power leads to second-harmonic variations in the output voltage and current

Removal of even harmonics via averaging



$$T_{2L} = \frac{1}{2}\frac{2\pi}{\omega} = \frac{\pi}{\omega}$$

Resulting averaged model



Time invariant model

Power source is nonlinear

Perturbation and linearization

The averaged model predicts that the rectifier output current is

$$\left\langle i_2(t) \right\rangle_{T_{2L}} = \frac{\left\langle p(t) \right\rangle_{T_{2L}}}{\left\langle v(t) \right\rangle_{T_{2L}}} = \frac{v_{g,rms}^2(t)}{R_e(v_{control}(t)) \left\langle v(t) \right\rangle_{T_{2L}}}$$

$$= f\left(v_{g,rms}(t), \left\langle v(t) \right\rangle_{T_{2L}}, v_{control}(t) \right)$$

Let

$$\left\langle v(t) \right\rangle_{T_{2L}} = V + \hat{v}(t)$$

$$\left\langle i_2(t) \right\rangle_{T_{2L}} = I_2 + \hat{i}_2(t)$$

$$v_{g,rms} = V_{g,rms} + \hat{v}_{g,rms}(t)$$

$$v_{control}(t) = V_{control} + \hat{v}_{control}(t)$$

with

$$V >> \left| \hat{v}(t) \right|$$

$$I_2 >> \left| \hat{i}_2(t) \right|$$

$$V_{g,rms} >> \left| \hat{v}_{g,rms}(t) \right|$$

$$V_{control} >> \left| \hat{v}_{control}(t) \right|$$

Linearized result

$$I_2 + \hat{i}_2(t) = g_2 \hat{v}_{g,rms}(t) + j_2 \hat{v}(t) - \frac{\hat{v}_{control}(t)}{r_2}$$

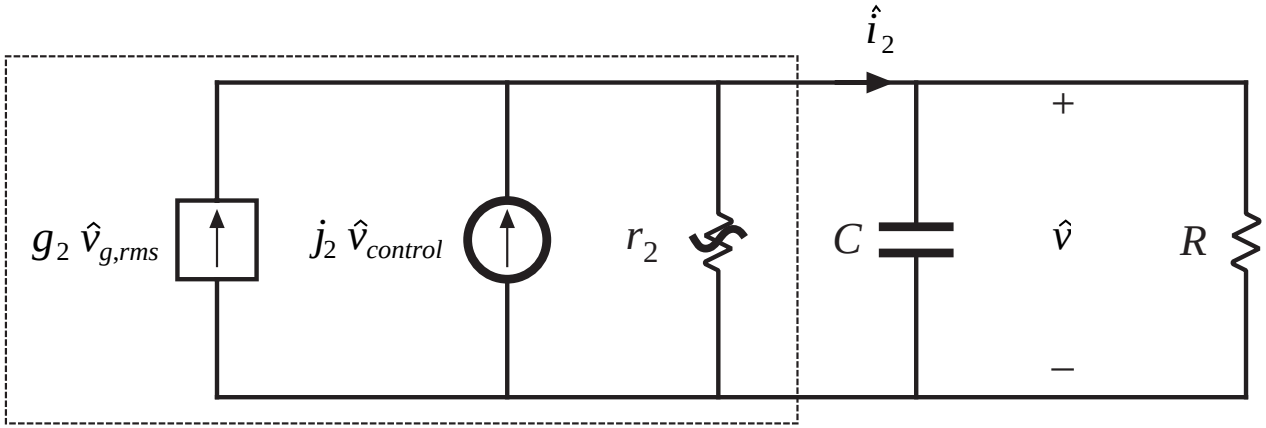
where

$$g_2 = \left. \frac{df\left(v_{g,rms}, V, V_{control}\right)}{dv_{g,rms}} \right|_{v_{g,rms} = V_{g,rms}} = \frac{2}{R_e(V_{control})} \frac{V_{g,rms}}{V}$$

$$\left(-\frac{1}{r_2}\right) = \left. \frac{df\left(V_{g,rms}, \langle v \rangle_{T_{2L}}, V_{control}\right)}{d\langle v \rangle_{T_{2L}}} \right|_{\langle v \rangle_{T_{2L}} = V} = -\frac{I_2}{V}$$

$$j_2 = \left. \frac{df\left(V_{g,rms}, V, v_{control}\right)}{dv_{control}} \right|_{v_{control} = V_{control}} = -\frac{V_{g,rms}^2}{V R_e^2(V_{control})} \left. \frac{dR_e(v_{control})}{dv_{control}} \right|_{v_{control} = V_{control}}$$

Small-signal equivalent circuit



Predicted transfer functions

Control-to-output

$$\frac{\hat{v}(s)}{\hat{v}_{control}(s)} = j_2\, R\|r_2\, \frac{1}{1 + sC\, R\|r_2}$$

Line-to-output

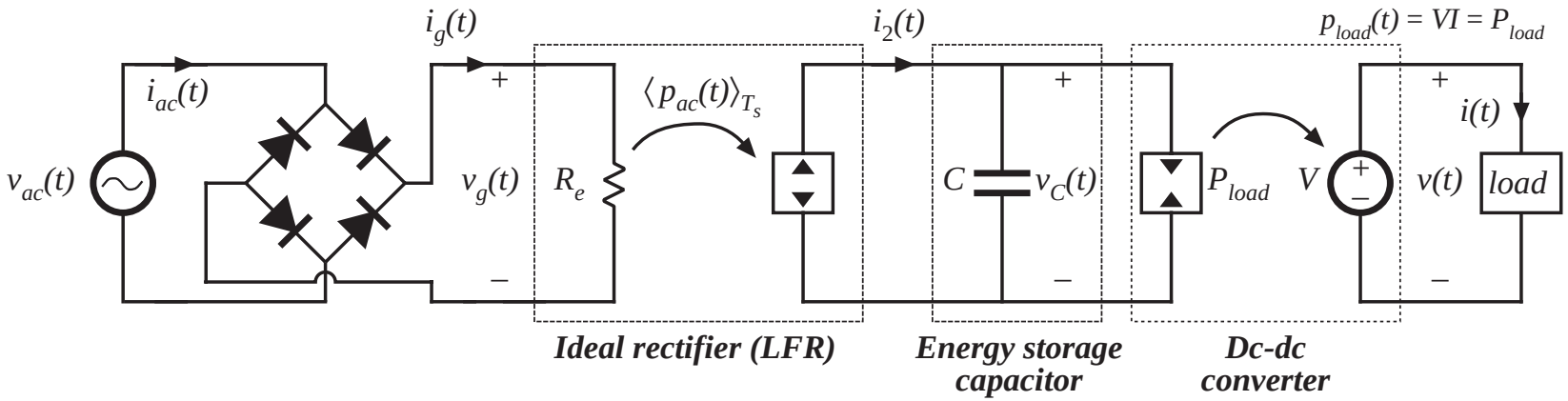
$$\frac{\hat{v}(s)}{\hat{v}_{g,rms}(s)} = g_2\, R\|r_2\, \frac{1}{1 + sC\, R\|r_2}$$

Model parameters

Table 18.1 Small-signal model parameters for several types of rectifier control schemes

Controller type	g_2	j_2	r_2
Average current control with feedforward, Fig. 18.9	0	$\frac{P_{av}}{VV_{control}}$	$\frac{V^2}{P_{av}}$
Current-programmed control, Fig. 18.10	$\frac{2P_{av}}{VV_{g,rms}}$	$\frac{P_{av}}{VV_{control}}$	$\frac{V^2}{P_{av}}$
Nonlinear-carrier charge control of boost rectifier, Fig. 18.14	$\frac{2P_{av}}{VV_{g,rms}}$	$\frac{P_{av}}{VV_{control}}$	$\frac{V^2}{2P_{av}}$
Boost with hysteretic control, Fig. 18.13(b)	$\frac{2P_{av}}{VV_{g,rms}}$	$\frac{P_{av}}{VT_{on}}$	$\frac{V^2}{P_{av}}$
DCM buck–boost, flyback, SEPIC, or Cuk converters	$\frac{2P_{av}}{VV_{g,rms}}$	$\frac{2P_{av}}{VD}$	$\frac{V^2}{P_{av}}$

Constant power load



Rectifier and dc-dc converter operate with same average power

Incremental resistance R of constant power load is negative, and is

$$R = -\frac{V^2}{P_{av}}$$

which is equal in magnitude and opposite in polarity to rectifier incremental output resistance r_2 for all controllers except NLC

Transfer functions with constant power load

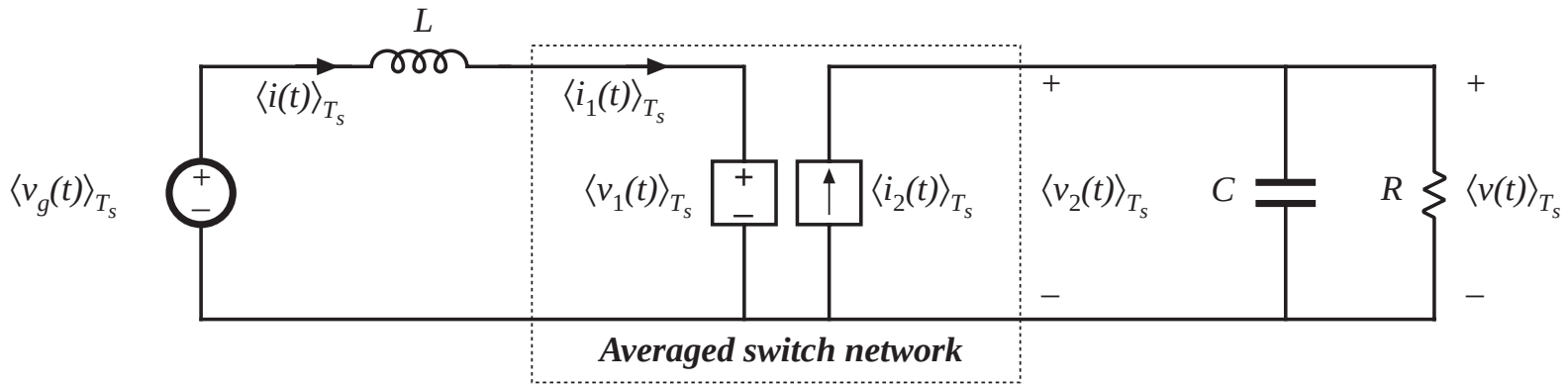
When $r_2 = -R$, the parallel combination $r_2 \parallel R$ becomes equal to zero. The small-signal transfer functions then reduce to

$$\frac{\hat{v}(s)}{\hat{v}_{control}(s)} = \frac{j_2}{sC}$$

$$\frac{\hat{v}(s)}{\hat{v}_{g,rms}(s)} = \frac{g_2}{sC}$$

18.3.2 Modeling the inner wide-bandwidth average current controller

Averaged (but not linearized) boost converter model, Fig. 7.42:



In Chapter 7, we perturbed and linearized using the assumptions

$$\left\langle v_g(t)\right\rangle_{T_s} = V_g + \hat{v}_g(t)$$

$$d(t) = D + \hat{d}(t) \quad \Rightarrow d'(t) = D' - \hat{d}(t)$$

$$\left\langle i(t)\right\rangle_{T_s} = \left\langle i_1(t)\right\rangle_{T_s} = I + \hat{i}(t)$$

$$\left\langle v(t)\right\rangle_{T_s} = \left\langle v_2(t)\right\rangle_{T_s} = V + \hat{v}(t)$$

$$\left\langle v_1(t)\right\rangle_{T_s} = V_1 + \hat{v}_1(t)$$

$$\left\langle i_2(t)\right\rangle_{T_s} = I_2 + \hat{i}_2(t)$$

Problem: variations in v_g, i_1 , and d are not small.

So we are faced with the design of a control system that exhibits significant nonlinear time-varying behavior.

Linearizing the equations of the boost rectifier

When the rectifier operates near steady-state, it is true that

$$\left\langle v(t) \right\rangle_{T_s} = V + \hat{v}(t)$$

with

$$\left| \hat{v}(t) \right| << \left| V \right|$$

In the special case of the boost rectifier, this is sufficient to linearize the equations of the average current controller.

The boost converter average inductor voltage is

$$L \frac{d\left\langle i_g(t) \right\rangle_{T_s}}{dt} = \left\langle v_g(t) \right\rangle_{T_s} - d'(t) V - d'(t) \hat{v}(t)$$

substitute:

$$L \frac{d\left\langle i_g(t) \right\rangle_{T_s}}{dt} = \left\langle v_g(t) \right\rangle_{T_s} - d'(t) V - d'(t) \hat{v}(t)$$

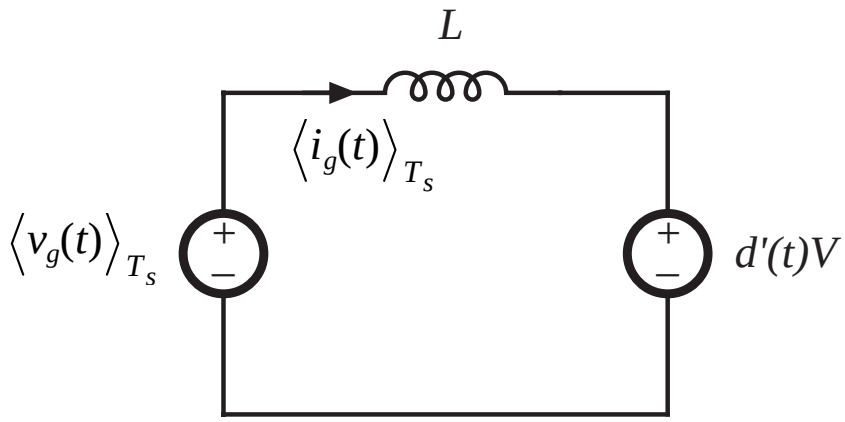
Linearized boost rectifier model

$$L \frac{d\left\langle i_g(t) \right\rangle_{T_s}}{dt} = \left\langle v_g(t) \right\rangle_{T_s} - d'(t)V - d'(t)\hat{v}(t)$$

The nonlinear term is much smaller than the linear ac term. Hence, it can be discarded to obtain

$$L \frac{d\left\langle i_g(t) \right\rangle_{T_s}}{dt} = \left\langle v_g(t) \right\rangle_{T_s} - d'(t)V$$

Equivalent circuit:



$$\frac{i_g(s)}{d(s)} = \frac{V}{sL}$$

The quasi-static approximation

The above approach is not sufficient to linearize the equations needed to design the rectifier averaged current controllers of buck-boost, Cuk, SEPIC, and other converter topologies. These are truly nonlinear time-varying systems.

An approximate approach that is sometimes used in these cases: the *quasi-static approximation*

Assume that the ac line variations are much slower than the converter dynamics, so that the rectifier always operates near equilibrium. The quiescent operating point changes slowly along the input sinusoid, and we can find the slowly-varying "equilibrium" duty ratio as in Section 18.1.

The converter small-signal transfer functions derived in Chapters 7 and 8 are evaluated, using the time-varying operating point. The poles, zeroes, and gains vary slowly as the operating point varies. An average current controller is designed, that has a positive phase margin at each operating point.

Quasi-static approximation: discussion

In the literature, several authors have reported success using this method

Should be valid provided that the converter dynamics are suffieiently fast, such that the converter always operates near the assumed operating points

No good condition on system parameters, which can justify the approximation, is presently known for the basic converter topologies

It is well-understood in the field of control systems that, when the converter dynamics are not sufficiently fast, then the quasi-static approximation yields neither necessary nor sufficient conditions for stability. Such behavior can be observed in rectifier systems. Worst-case analysis to prove stability should employ simulations.

Chapter 19
Resonant Conversion

Introduction to Resonant Conversion

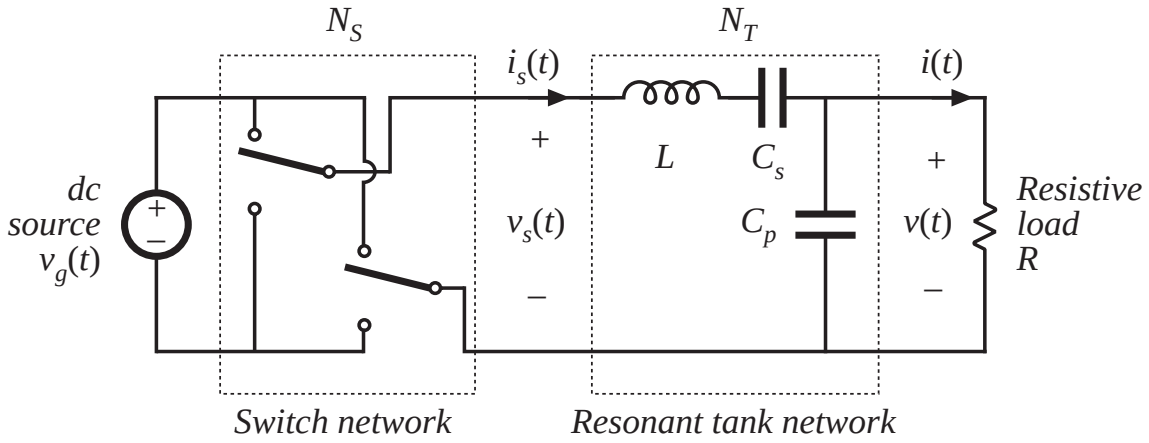
Resonant power converters contain resonant L-C networks whose voltage and current waveforms vary sinusoidally during one or more subintervals of each switching period. These sinusoidal variations are large in magnitude, and the small ripple approximation does not apply.

Some types of resonant converters:

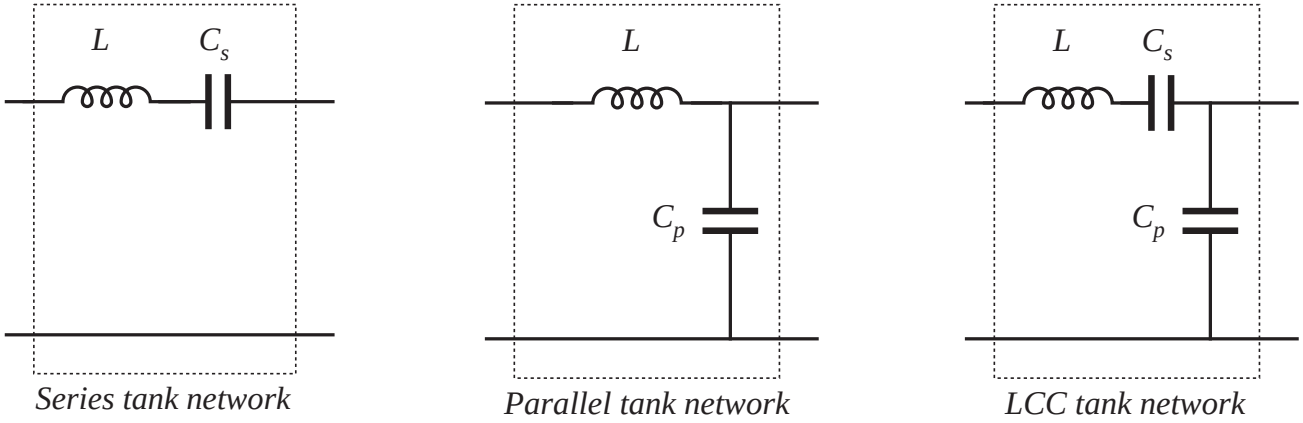
- Dc-to-high-frequency-ac inverters
- Resonant dc-dc converters
- Resonant inverters or rectifiers producing line-frequency ac

A basic class of resonant inverters

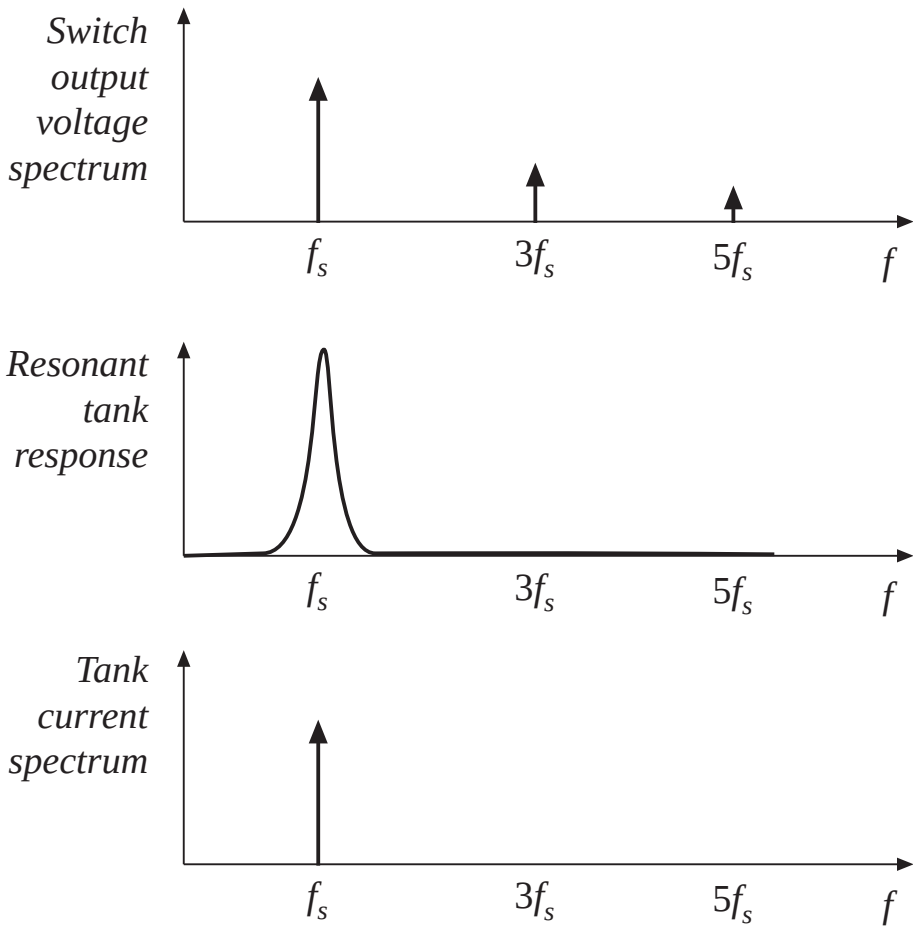
Basic circuit



Several resonant tank networks



Tank network responds only to fundamental component of switched waveforms

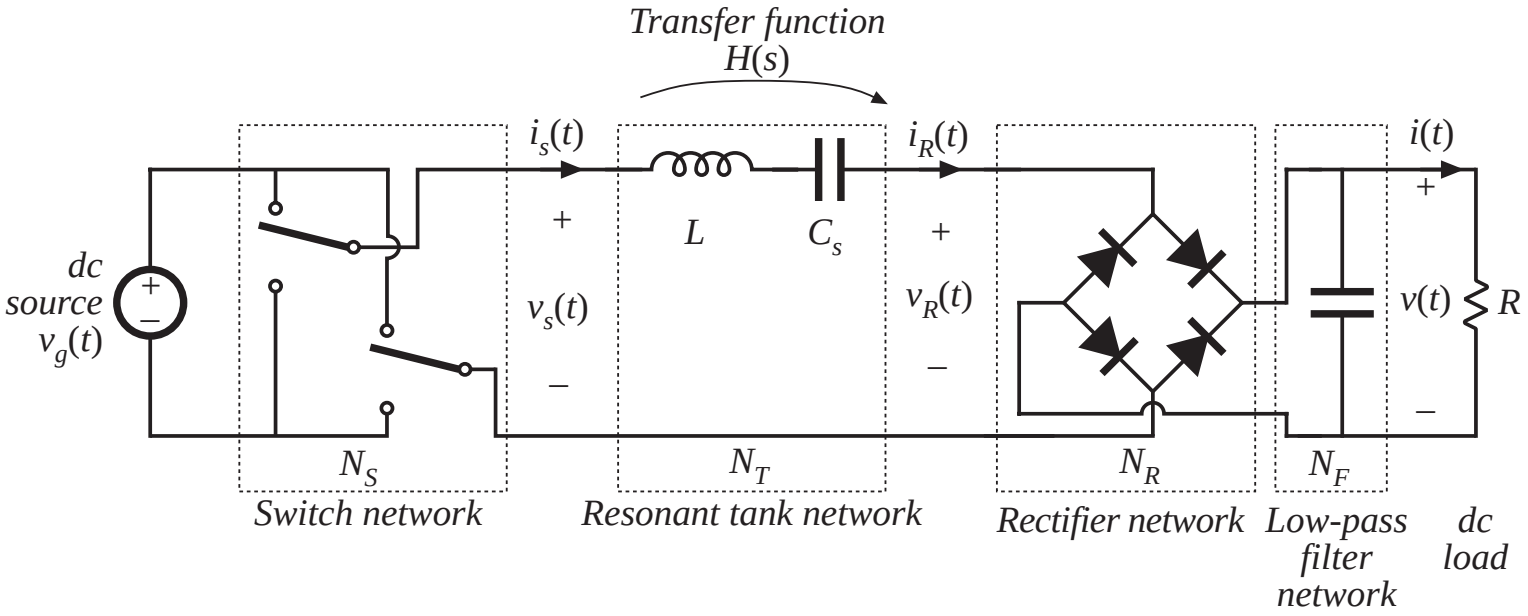


Tank current and output voltage are essentially sinusoids at the switching frequency f_s.

Output can be controlled by variation of switching frequency, closer to or away from the tank resonant frequency

Derivation of a resonant dc-dc converter

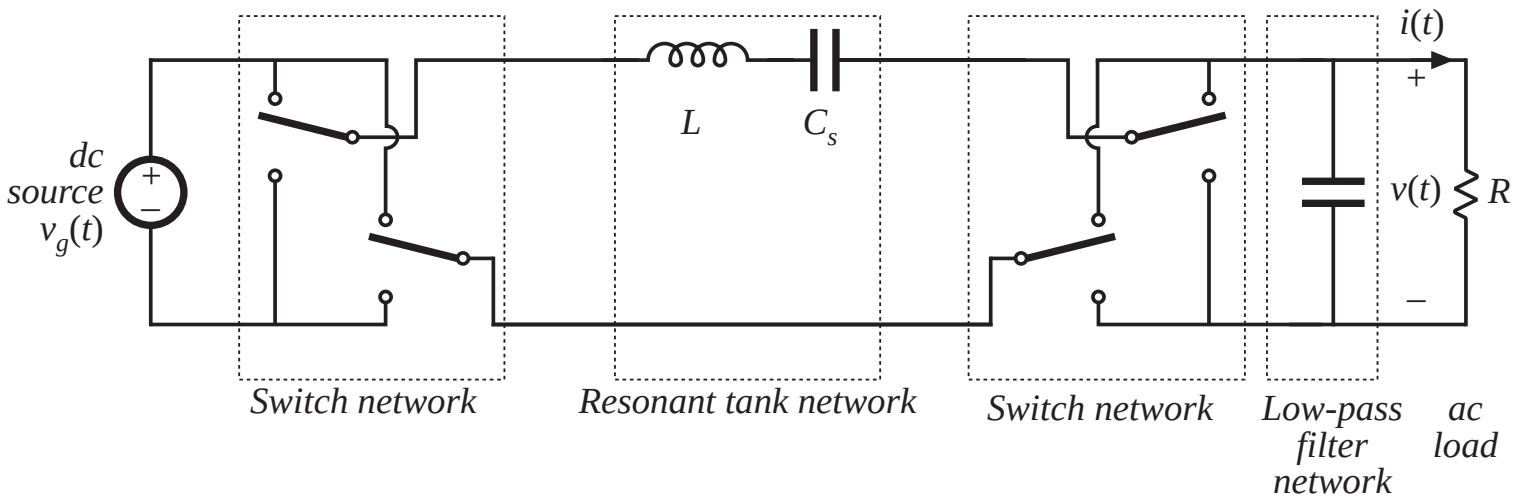
Rectify and filter the output of a dc-high-frequency-ac inverter



The series resonant dc-dc converter

A series resonant link inverter

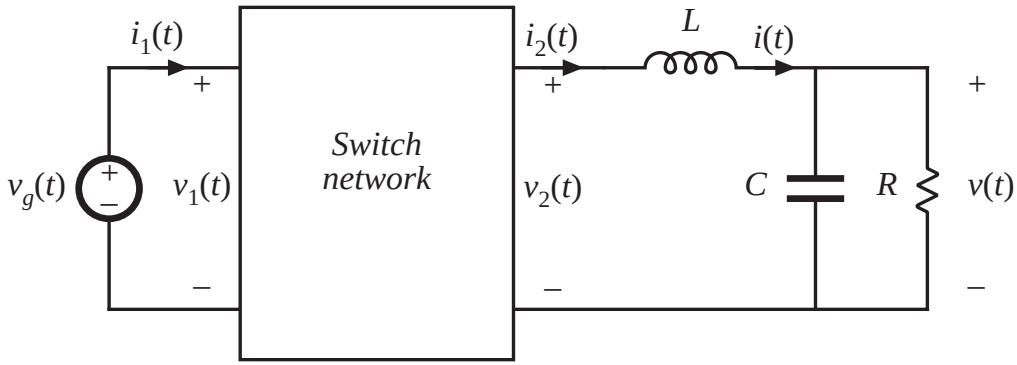
Same as dc-dc series resonant converter, except output rectifiers are replaced with four-quadrant switches:



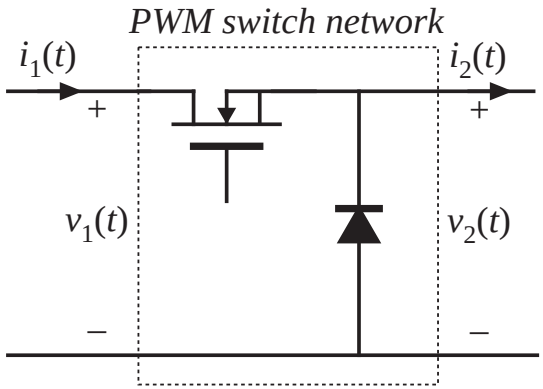
Quasi-resonant converters

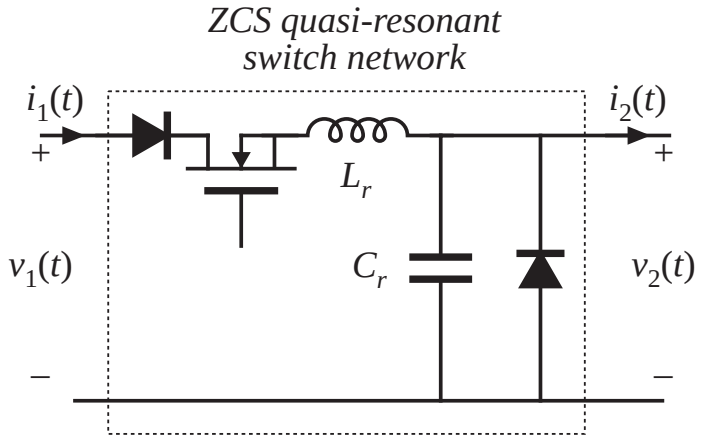
In a conventional PWM converter, replace the PWM switch network with a switch network containing resonant elements.

Buck converter example



Two switch networks:





Resonant conversion: advantages

The chief advantage of resonant converters: reduced switching loss

Zero-current switching

Zero-voltage switching

Turn-on or turn-off transitions of semiconductor devices can occur at zero crossings of tank voltage or current waveforms, thereby reducing or eliminating some of the switching loss mechanisms. Hence resonant converters can operate at higher switching frequencies than comparable PWM converters

Zero-voltage switching also reduces converter-generated EMI

Zero-current switching can be used to commutate SCRs

In specialized applications, resonant networks may be unavoidable

High voltage converters: significant transformer leakage inductance and winding capacitance leads to resonant network

Resonant conversion: disadvantages

Can optimize performance at one operating point, but not with wide range of input voltage and load power variations

Significant currents may circulate through the tank elements, even when the load is disconnected, leading to poor efficiency at light load

Quasi-sinusoidal waveforms exhibit higher peak values than equivalent rectangular waveforms

These considerations lead to increased conduction losses, which can offset the reduction in switching loss

Resonant converters are usually controlled by variation of switching frequency. In some schemes, the range of switching frequencies can be very large

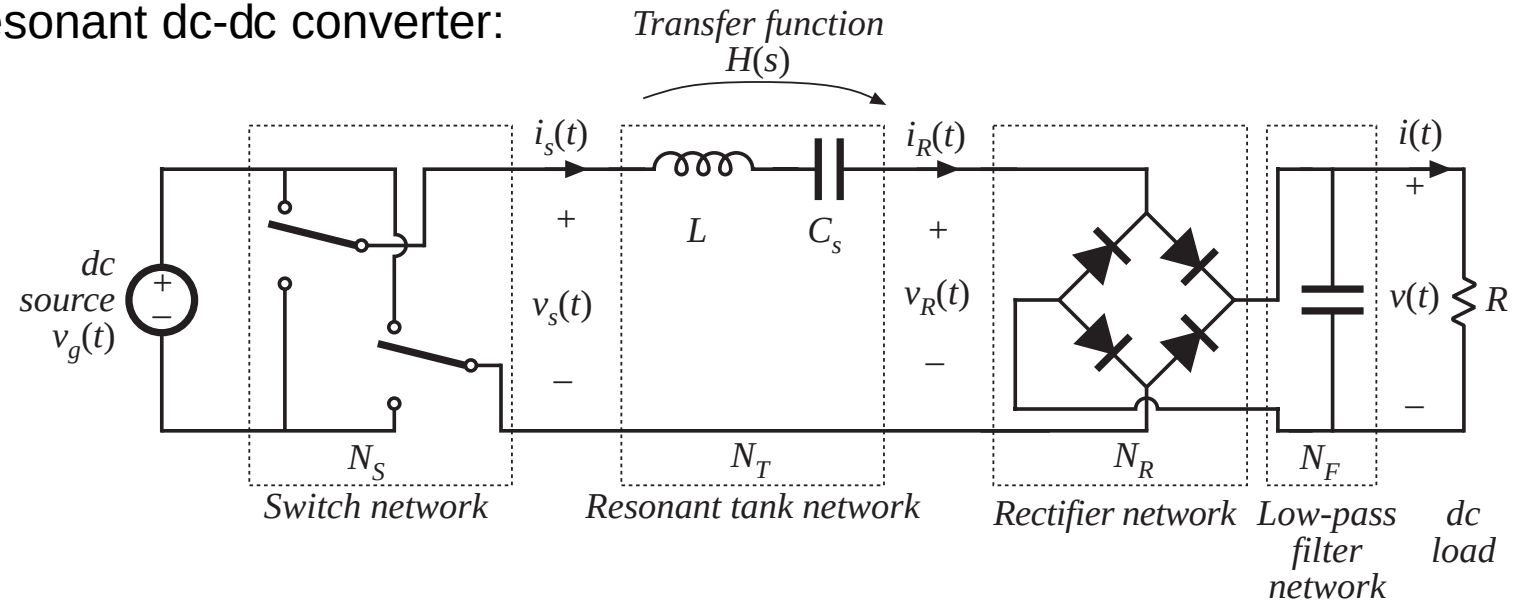
Complexity of analysis

Resonant conversion: Outline of discussion

- Simple steady-state analysis via sinusoidal approximation
- Simple and exact results for the series and parallel resonant converters
- Mechanisms of soft switching
- Circulating currents, and the dependence (or lack thereof) of conduction loss on load power
- Quasi-resonant converter topologies
- Steady-state analysis of quasi-resonant converters
- Ac modeling of quasi-resonant converters via averaged switch modeling

19.1 Sinusoidal analysis of resonant converters

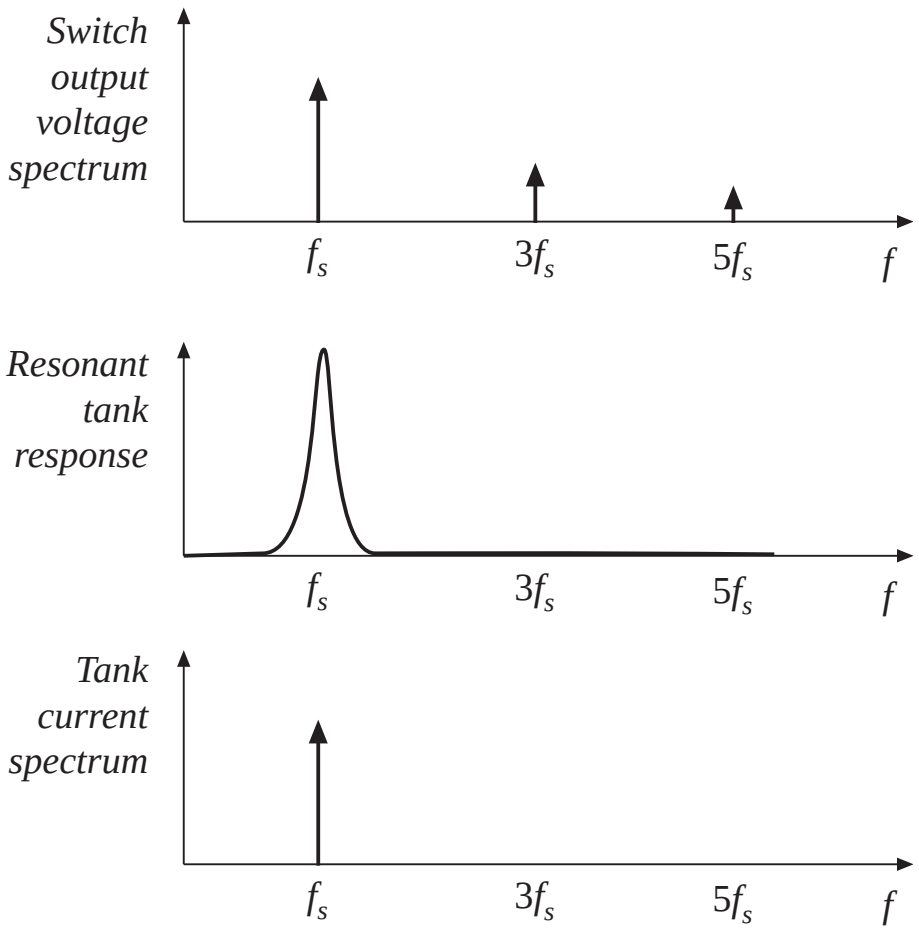
A resonant dc-dc converter:



If tank responds primarily to fundamental component of switch network output voltage waveform, then harmonics can be neglected.

Let us model all ac waveforms by their fundamental components.

The sinusoidal approximation

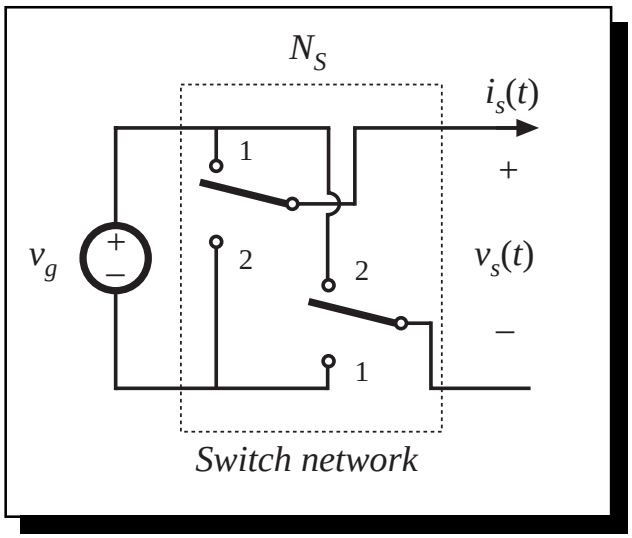


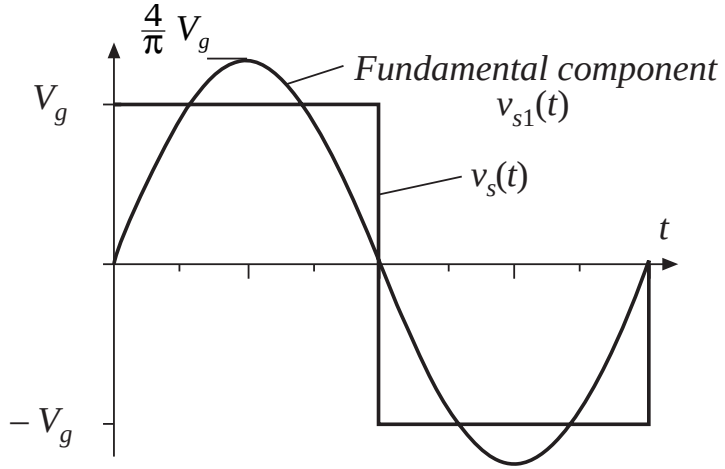
Tank current and output voltage are essentially sinusoids at the switching frequency f_s.

Neglect harmonics of switch output voltage waveform, and model only the fundamental component.

Remaining ac waveforms can be found via phasor analysis.

19.1.1 Controlled switch network model





If the switch network produces a square wave, then its output voltage has the following Fourier series:

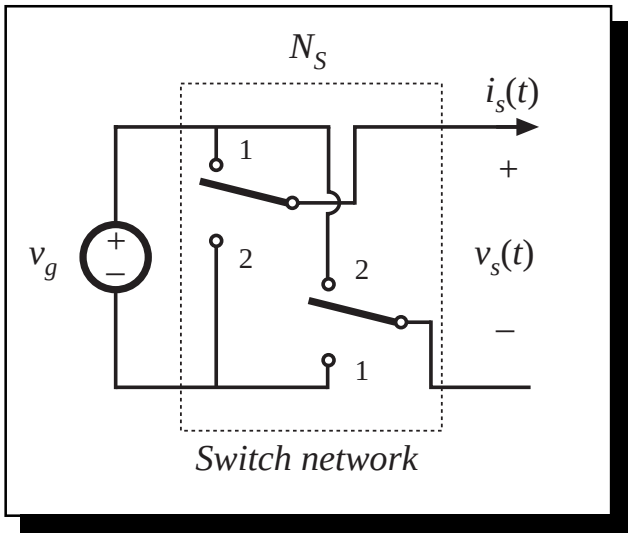
$$v_s(t) = \frac{4V_g}{\pi} \sum_{n = 1, 3, 5, \ldots} \frac{1}{n} \sin(n\omega_s t)$$

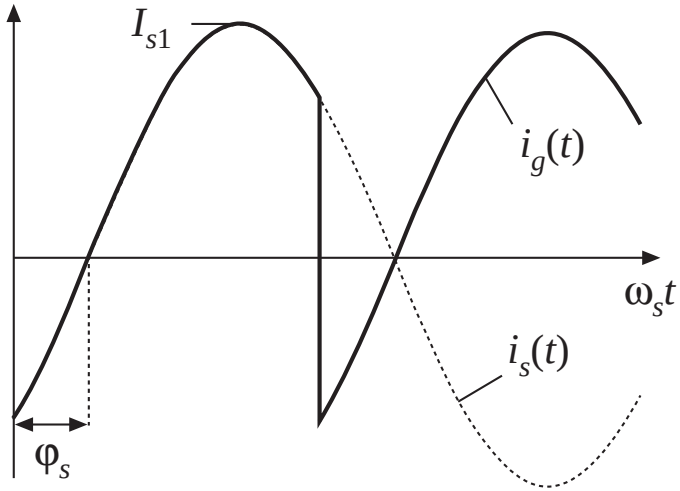
The fundamental component is

$$v_{s1}(t) = \frac{4V_g}{\pi} \sin(\omega_s t) = V_{s1} \sin(\omega_s t)$$

So model switch network output port with voltage source of value $v_{s1}(t)$

Model of switch network input port





Assume that switch network output current is

$$i_s(t) \approx I_{s1} \sin(\omega_s t - \varphi_s)$$

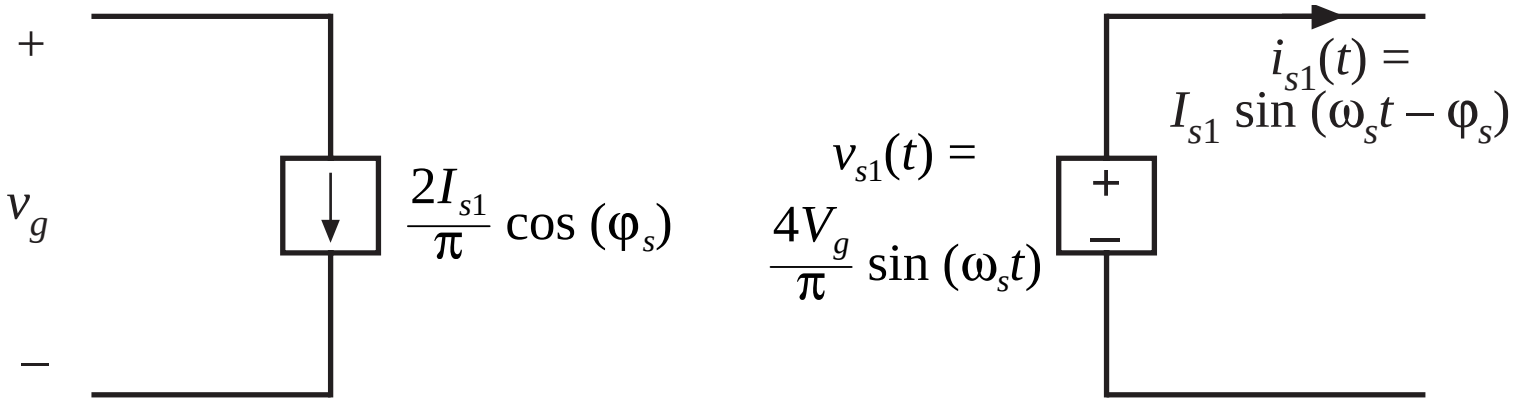
It is desired to model the dc component (average value) of the switch network input current.

$$\left\langle i_g(t) \right\rangle_{T_s} = \frac{2}{T_s} \int_0^{T_s/2} i_g(\tau)\, d\tau$$

$$\approx \frac{2}{T_s} \int_0^{T_s/2} I_{s1} \sin(\omega_s \tau - \varphi_s)\, d\tau$$

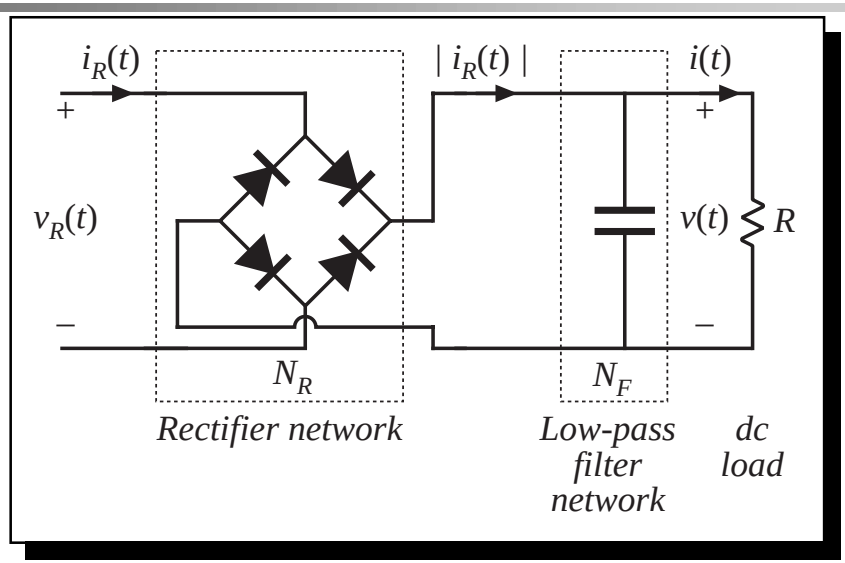
$$= \frac{2}{\pi} I_{s1} \cos(\varphi_s)$$

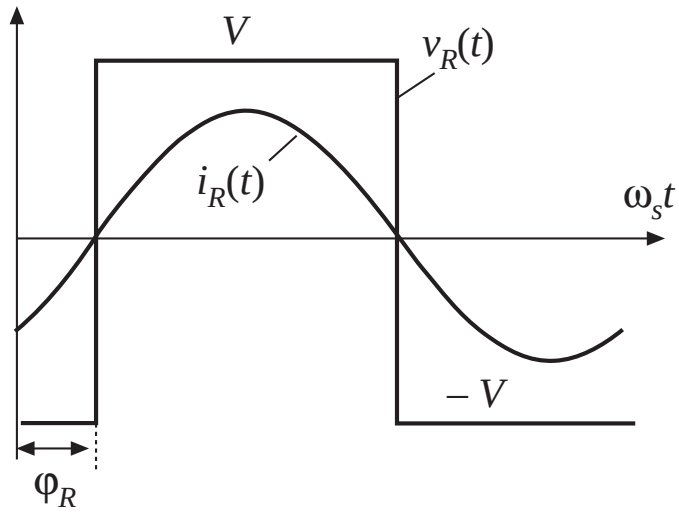
Switch network: equivalent circuit



- Switch network converts dc to ac
- Dc components of input port waveforms are modeled
- Fundamental ac components of output port waveforms are modeled
- Model is power conservative: predicted average input and output powers are equal

19.1.2 Modeling the rectifier and capacitive filter networks





Assume large output filter capacitor, having small ripple.

$v_R(t)$ is a square wave, having zero crossings in phase with tank output current $i_R(t)$.

If $i_R(t)$ is a sinusoid:

$$i_R(t) = I_{R1} \sin(\omega_s t - \varphi_R)$$

Then $v_R(t)$ has the following Fourier series:

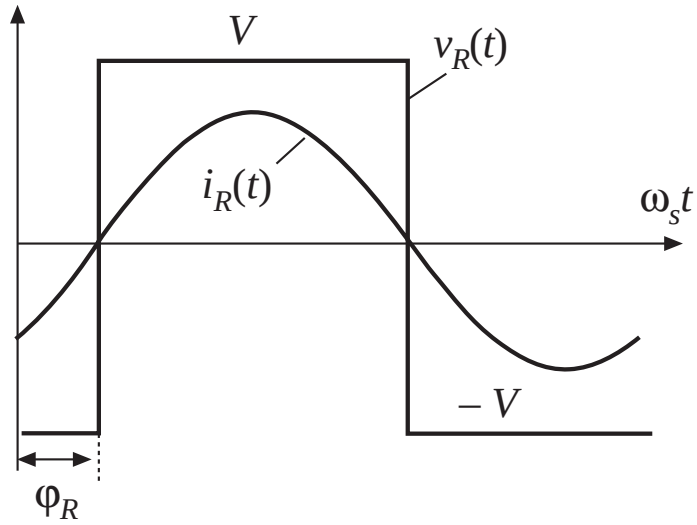
$$v_R(t) = \frac{4V}{\pi} \sum_{n = 1, 3, 5, \cdots}^{\infty} \frac{1}{n} \sin(n\omega_s t - \varphi_R)$$

Sinusoidal approximation: rectifier

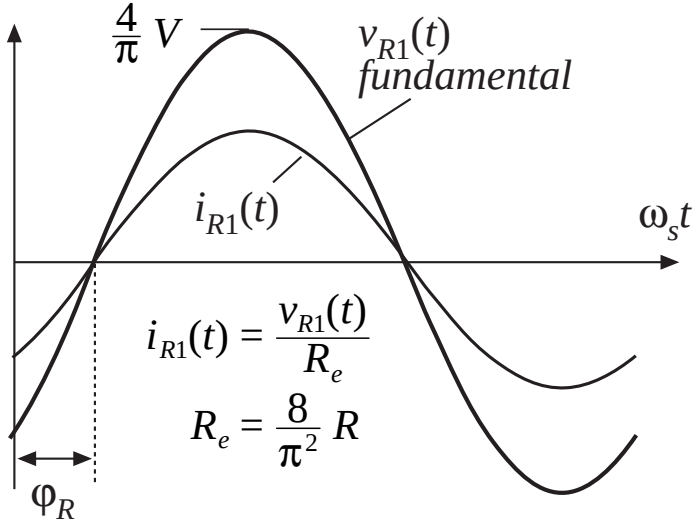
Again, since tank responds only to fundamental components of applied waveforms, harmonics in $v_R(t)$ can be neglected. $v_R(t)$ becomes

$$v_{R1}(t) = \frac{4V}{\pi} \sin(\omega_s t - \varphi_R) = V_{R1} \sin(\omega_s t - \varphi_R)$$

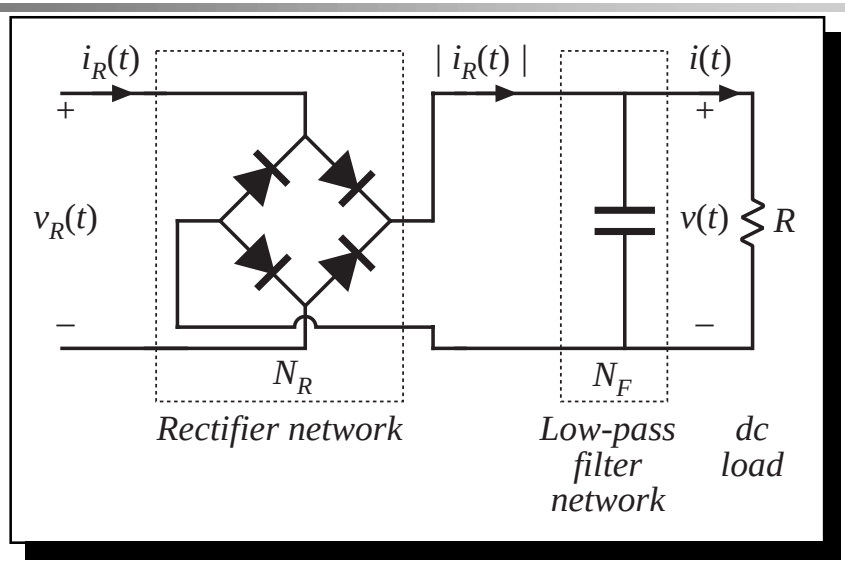
Actual waveforms

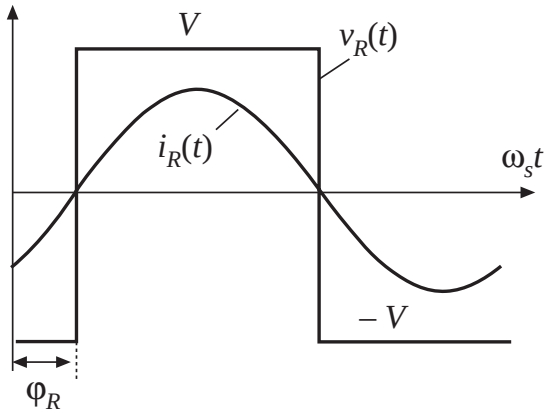


with harmonics ignored



Rectifier dc output port model





Output capacitor charge balance: dc load current is equal to average rectified tank output current

$$\left\langle \left| i_R(t) \right| \right\rangle_{T_s} = I$$

Hence

$$I = \frac{2}{T_S} \int_0^{T_s/2} I_{R1} \left| \sin(\omega_s t - \varphi_R) \right| dt$$

$$= \frac{2}{\pi} I_{R1}$$

Equivalent circuit of rectifier

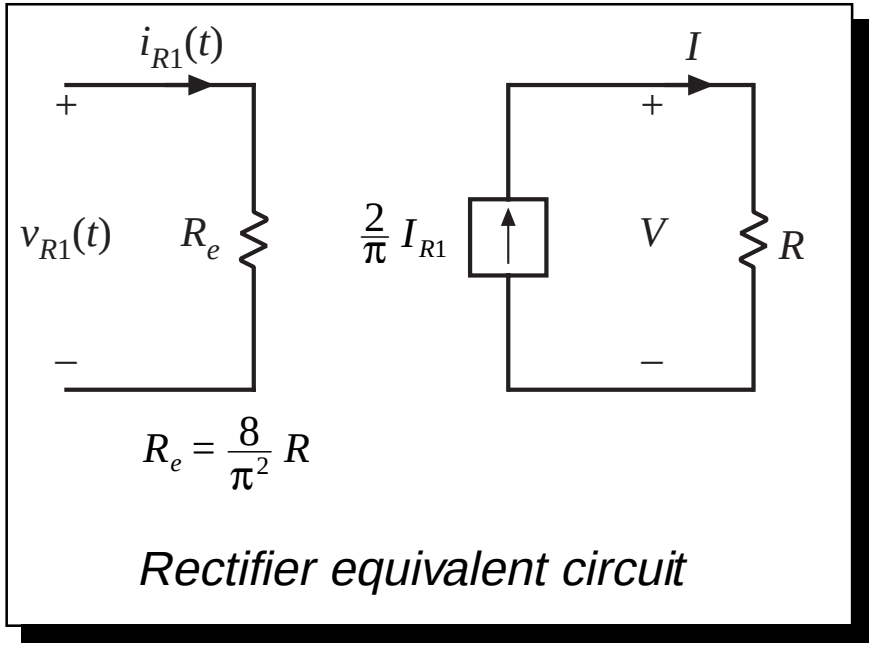
Rectifier input port:

Fundamental components of current and voltage are sinusoids that are in phase

Hence rectifier presents a resistive load to tank network

Effective resistance R_e is

$$R_e = \frac{v_{R1}(t)}{i_R(t)} = \frac{8}{\pi^2}\,\frac{V}{I}$$

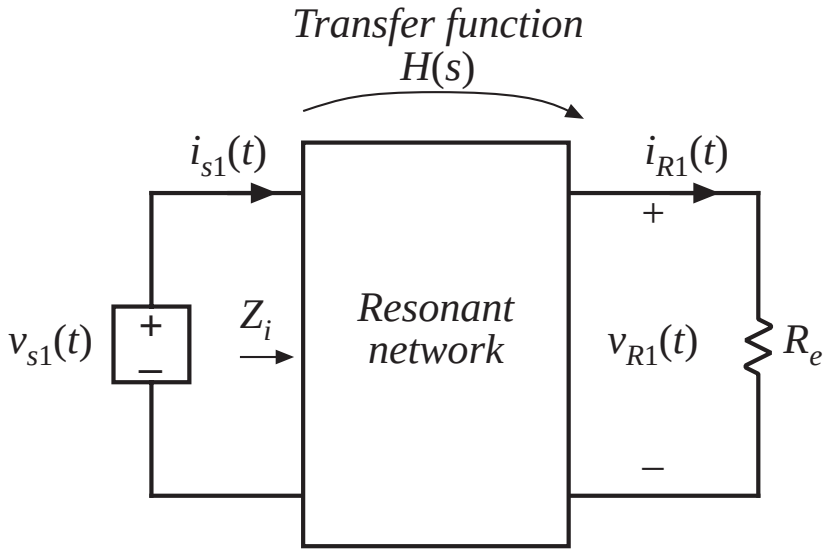


Rectifier equivalent circuit

With a resistive load R, this becomes

$$R_e = \frac{8}{\pi^2} R = 0.8106R$$

19.1.3 Resonant tank network



Model of ac waveforms is now reduced to a linear circuit. Tank network is excited by effective sinusoidal voltage (switch network output port), and is load by effective resistive load (rectifier input port).

Can solve for transfer function via conventional linear circuit analysis.

Solution of tank network waveforms

Transfer function:

$$\frac{v_{R1}(s)}{v_{s1}(s)} = H(s)$$

Ratio of peak values of input and output voltages:

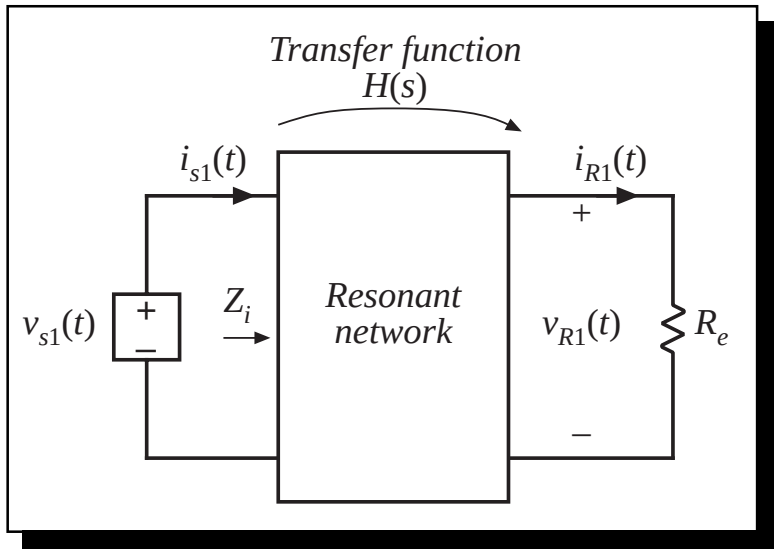
$$\frac{V_{R1}}{V_{s1}} = \left\| H(s) \right\|_{s = j\omega_s}$$

Solution for tank output current:

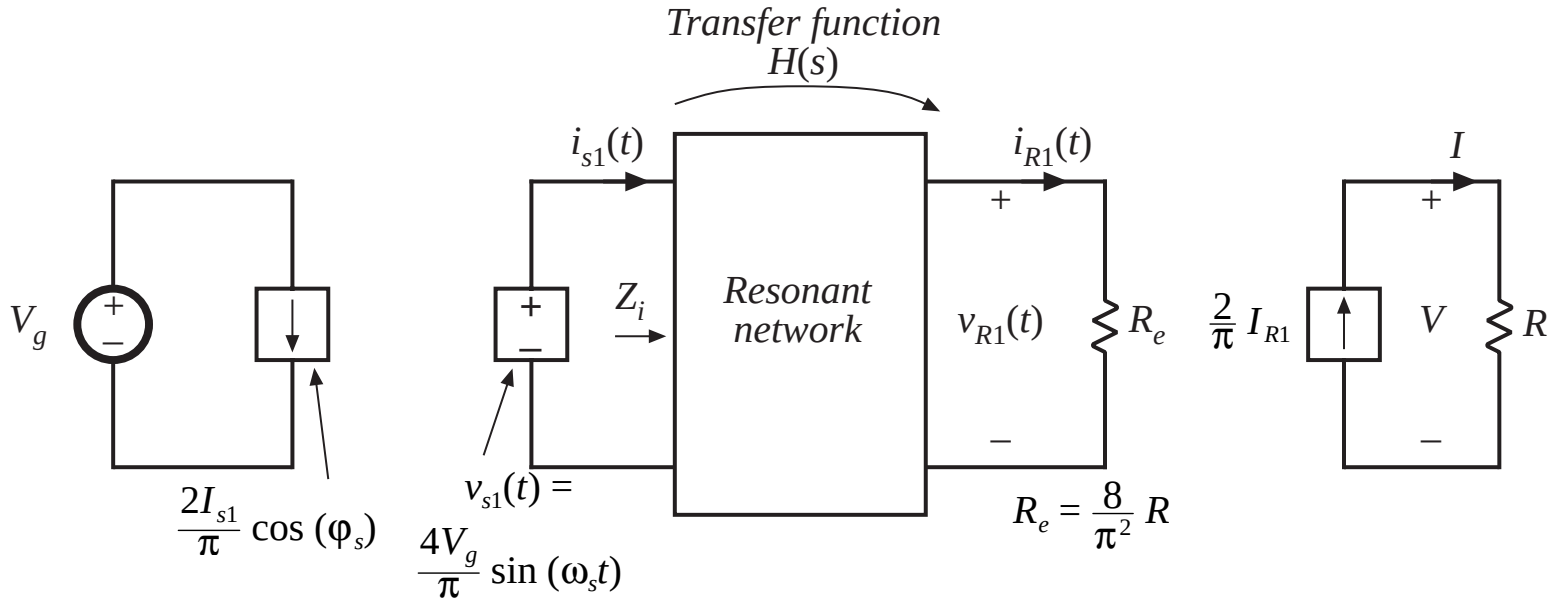
$$i_R(s) = \frac{v_{R1}(s)}{R_e} = \frac{H(s)}{R_e} v_{s1}(s)$$

which has peak magnitude

$$I_{R1} = \frac{\left\| H(s) \right\|_{s = j\omega_s}}{R_e} V_{s1}$$



19.1.4 Solution of converter voltage conversion ratio $M = V / V_g$



$$M = \frac{V}{V_g} = \underbrace{\left(R\right)}_{\left(\frac{V}{I}\right)} \underbrace{\left(\frac{2}{\pi}\right)}_{\left(\frac{I}{I_{R1}}\right)} \underbrace{\left(\frac{1}{R_e}\right)}_{\left(\frac{I_{R1}}{V_{R1}}\right)} \underbrace{\left(\left\| H(s) \right\|_{s = j\omega_s}\right)}_{\left(\frac{V_{R1}}{V_{s1}}\right)} \underbrace{\left(\frac{4}{\pi}\right)}_{\left(\frac{V_{s1}}{V_g}\right)}$$

Eliminate R_e:

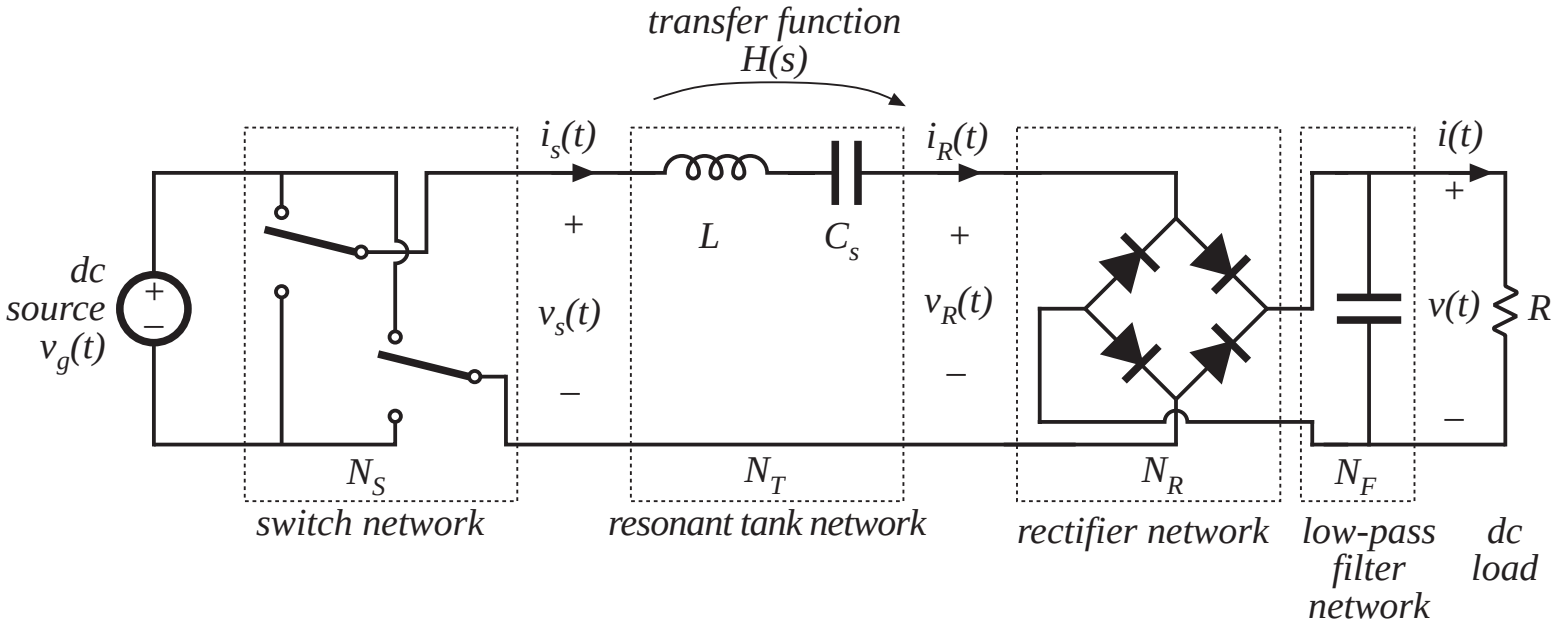
$$\frac{V}{V_g} = \left\| H(s) \right\|_{s = j\omega_s}$$

Conversion ratio M

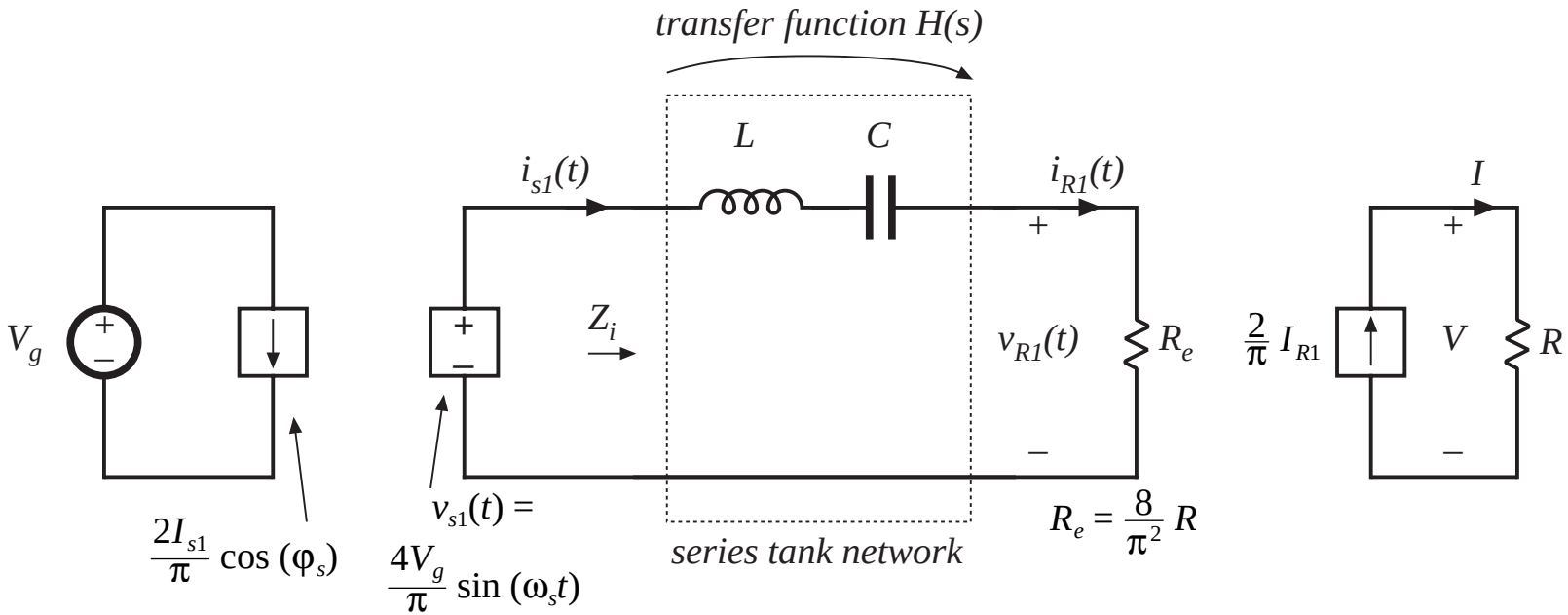
$$\frac{V}{V_g} = \left\| H(s) \right\|_{s = j\omega_s}$$

So we have shown that the conversion ratio of a resonant converter, having switch and rectifier networks as in previous slides, is equal to the magnitude of the tank network transfer function. This transfer function is evaluated with the tank loaded by the effective rectifier input resistance R_e.

19.2 Examples
19.2.1 Series resonant converter



Model: series resonant converter



$$H(s) = \frac{R_e}{Z_i(s)} = \frac{R_e}{R_e + sL + \frac{1}{sC}} = \frac{\left(\frac{s}{Q_e\omega_0}\right)}{1 + \left(\frac{s}{Q_e\omega_0}\right) + \left(\frac{s}{\omega_0}\right)^2}$$

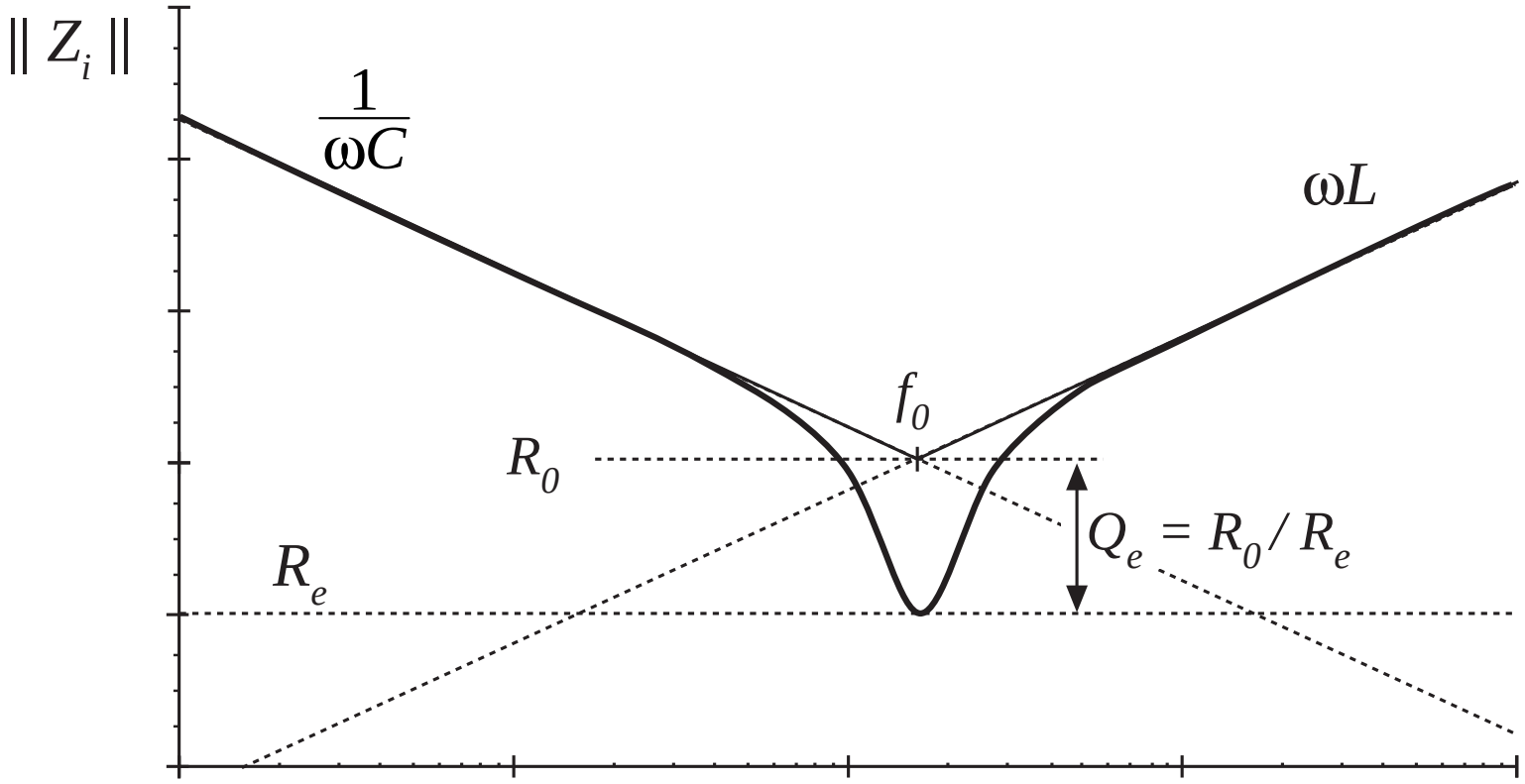
$$\omega_0 = \frac{1}{\sqrt{LC}} = 2\pi f_0$$

$$R_0 = \sqrt{\frac{L}{C}}$$

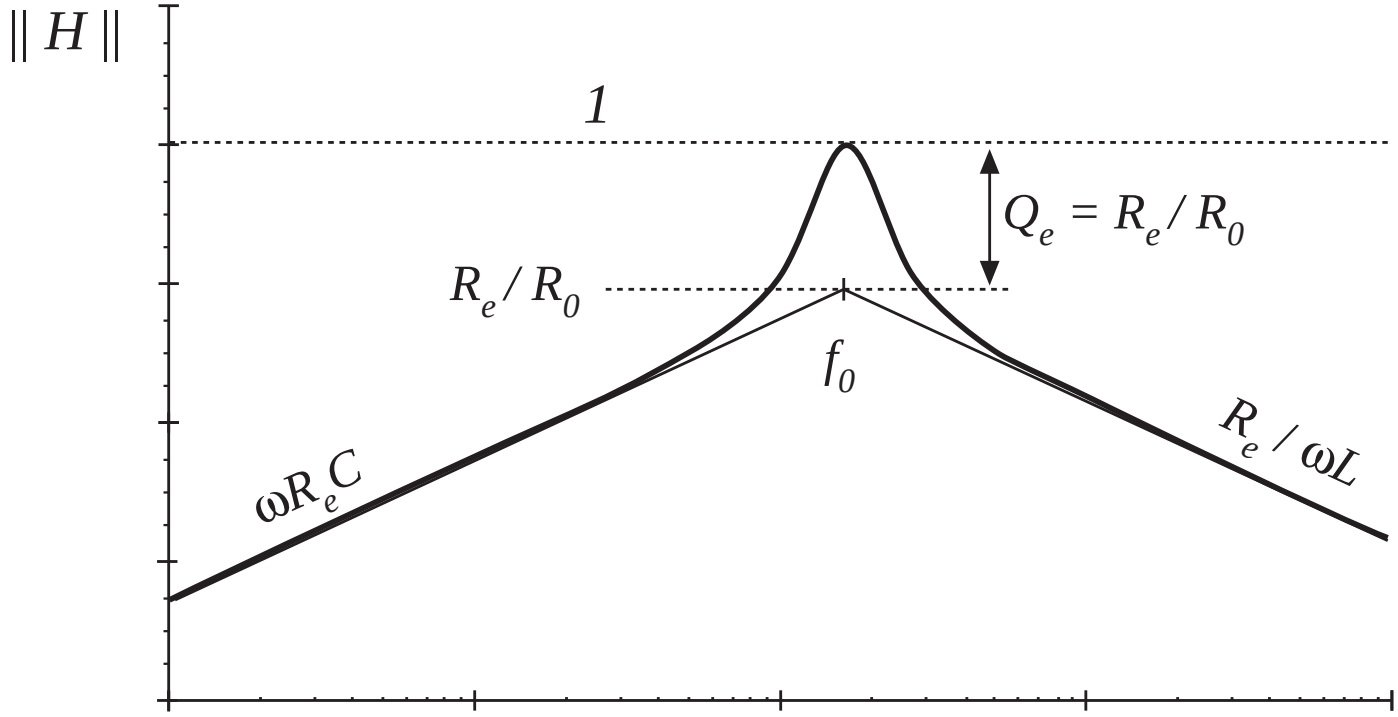
$$Q_e = \frac{R_0}{R_e}$$

$$M = \left\| H(j\omega_s) \right\| = \frac{1}{\sqrt{1 + Q_e^2 \left(\frac{1}{F} - F\right)^2}}$$

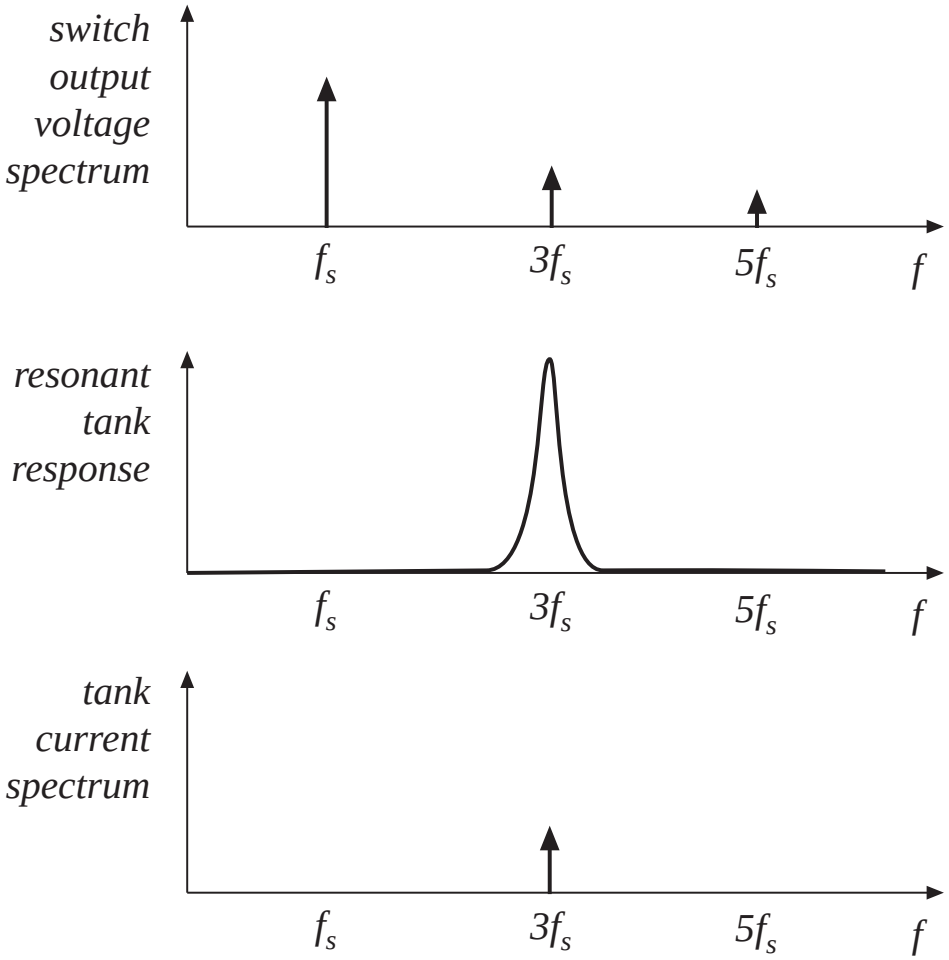
Construction of Z_i



Construction of *H*



19.2.2 Subharmonic modes of the SRC



Example: excitation of tank by third harmonic of switching frequency

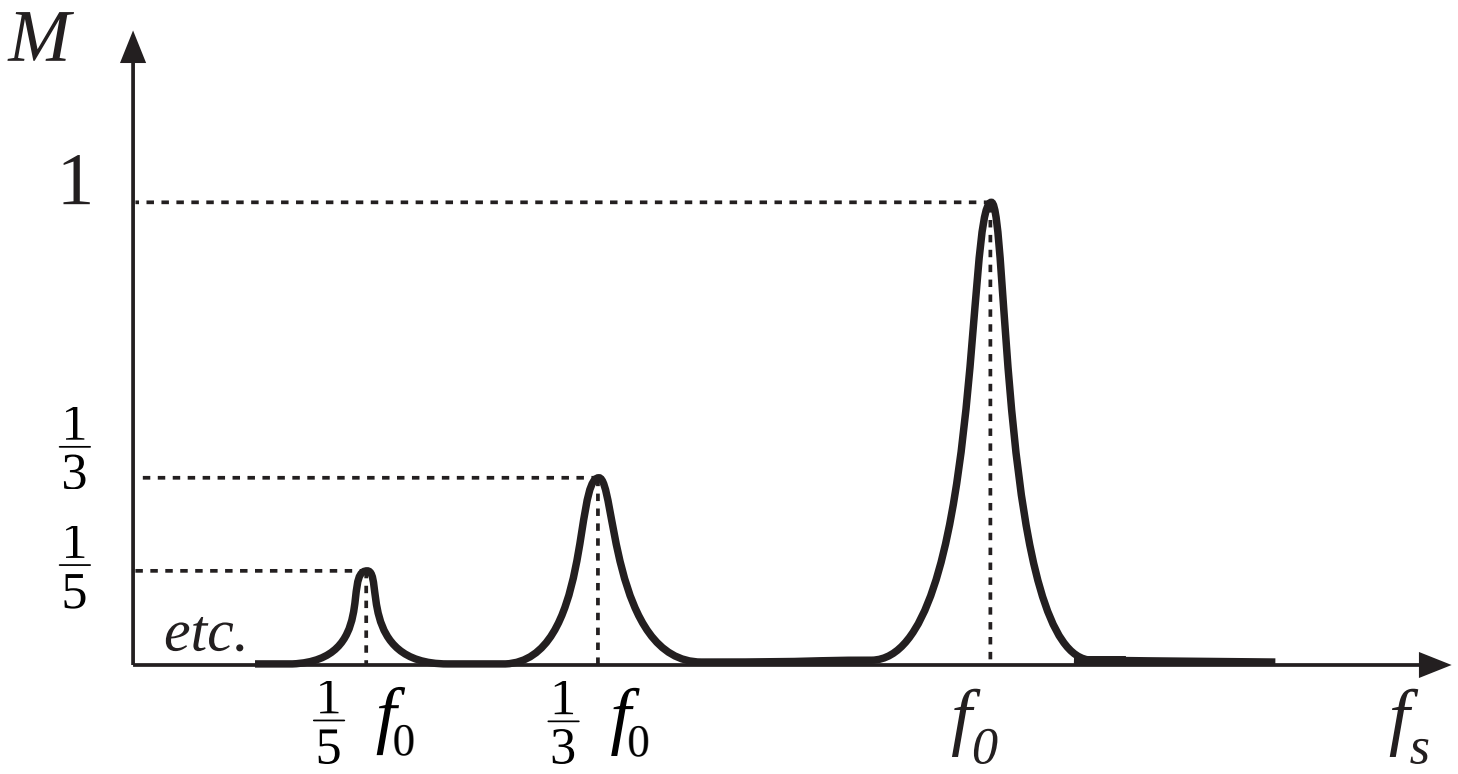
Can now approximate $v_s(t)$ by its third harmonic:

$$v_s(t) \approx v_{sn}(t) = \frac{4V_g}{n\pi} \sin(n\omega_s t)$$

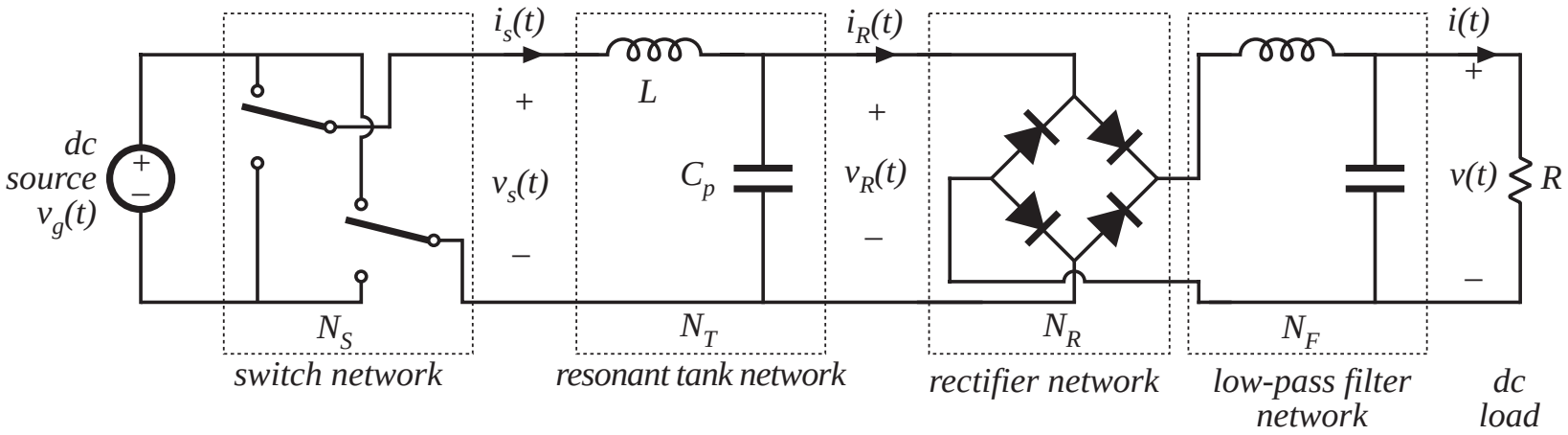
Result of analysis:

$$M = \frac{V}{V_g} = \frac{\| H(jn\omega_s) \|}{n}$$

Subharmonic modes of SRC



19.2.3 Parallel resonant dc-dc converter



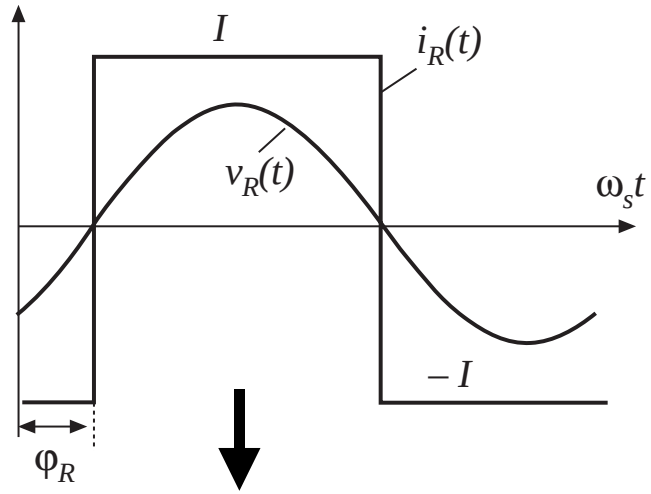
Differs from series resonant converter as follows:

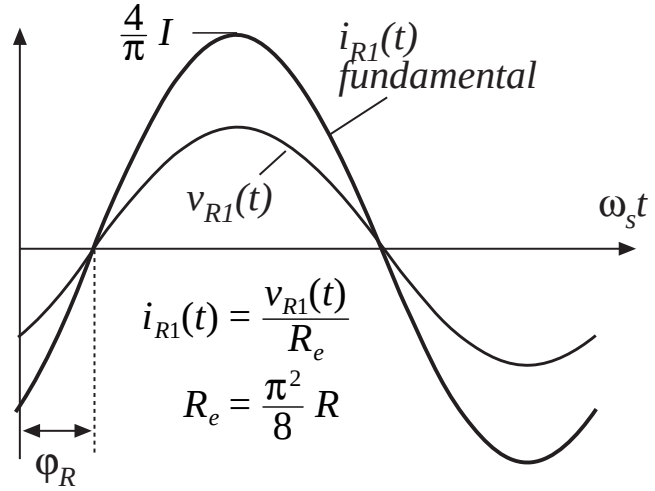
Different tank network

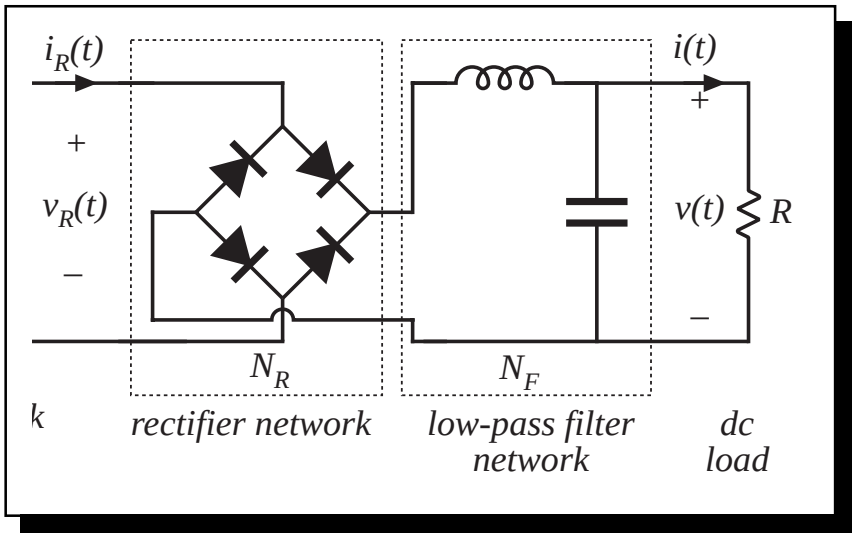
Rectifier is driven by sinusoidal voltage, and is connected to inductive-input low-pass filter

Need a new model for rectifier and filter networks

Model of uncontrolled rectifier with inductive filter network







Fundamental component of $i_R(t)$:

$$i_{R1}(t) = \frac{4I}{\pi} \sin(\omega_s t - \varphi_R)$$

Effective resistance R_e

Again define

$$R_e = \frac{v_{R1}(t)}{i_{R1}(t)} = \frac{\pi V_{R1}}{4I}$$

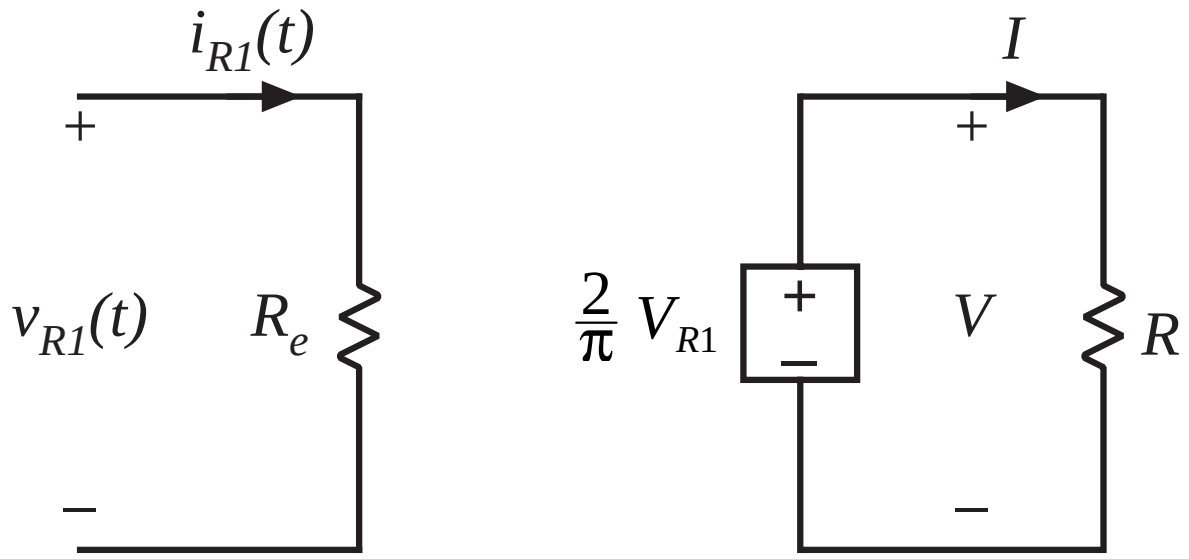
In steady state, the dc output voltage V is equal to the average value of $|\, v_R \,|$:

$$V = \frac{2}{T_S} \int_0^{T_S/2} V_{R1} \left| \sin(\omega_s t - \varphi_R) \right| dt = \frac{2}{\pi} V_{R1}$$

For a resistive load, $V = IR$. The effective resistance R_e can then be expressed

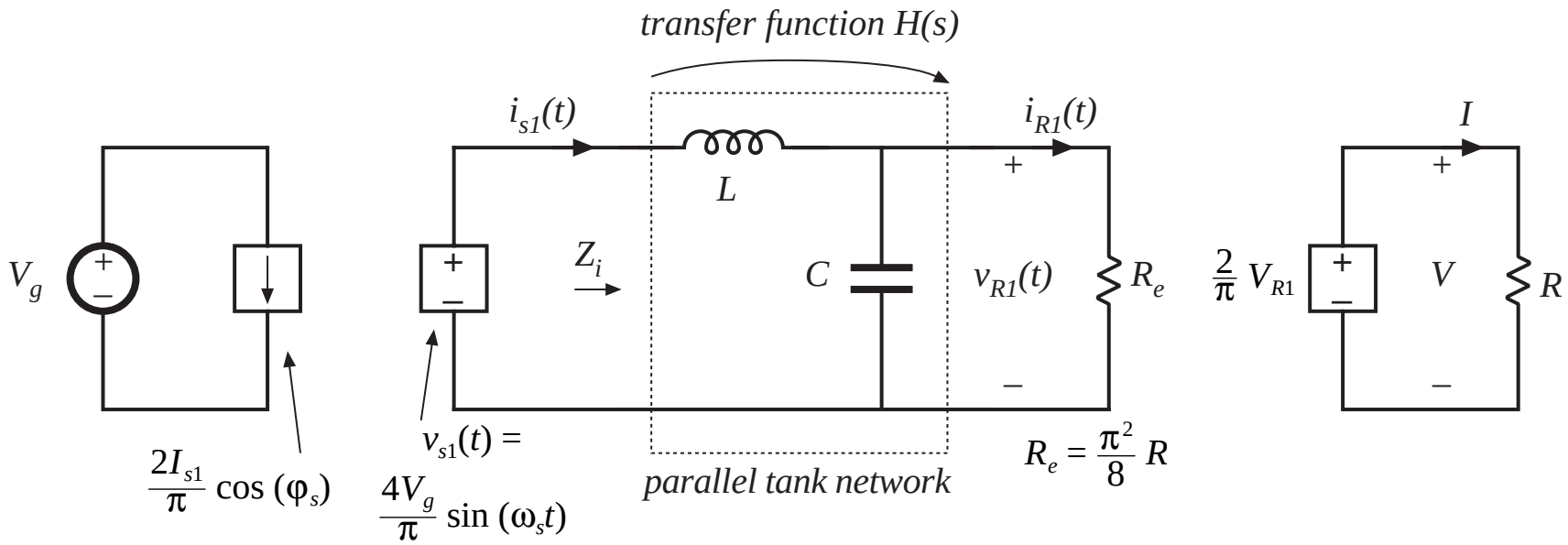
$$R_e = \frac{\pi^2}{8} R = 1.2337R$$

Equivalent circuit model of uncontrolled rectifier with inductive filter network



$$R_e = \frac{\pi^2}{8} R$$

Equivalent circuit model
Parallel resonant dc-dc converter

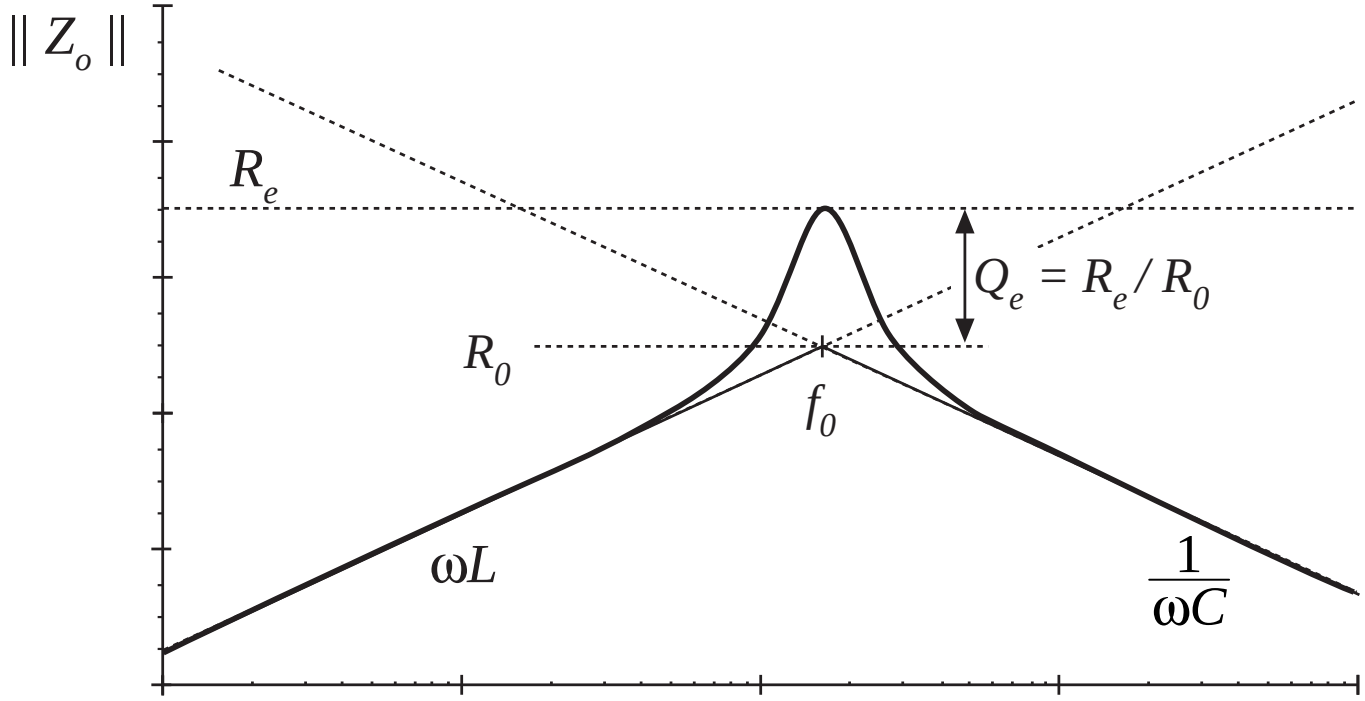


$$M = \frac{V}{V_g} = \frac{8}{\pi^2} \left\| H(s) \right\|_{s = j\omega_s}$$

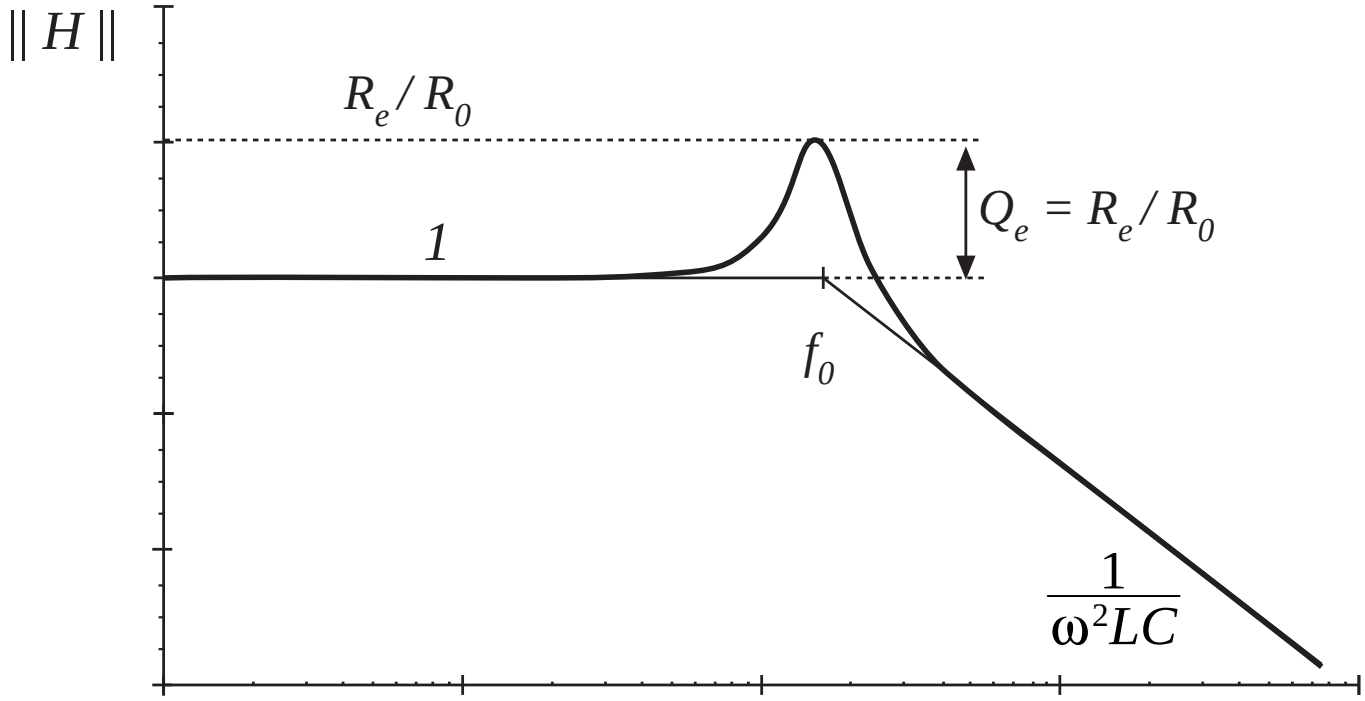
$$H(s) = \frac{Z_o(s)}{sL}$$

$$Z_o(s) = sL \parallel \frac{1}{sC} \parallel R_e$$

Construction of Z_o



Construction of H



Dc conversion ratio of the PRC

$$M = \frac{8}{\pi^2} \left\| \frac{Z_o(s)}{sL} \right\|_{s = j\omega_s} = \frac{8}{\pi^2} \left\| \frac{1}{1 + \frac{s}{Q_e \omega_0} + \left(\frac{s}{\omega_0} \right)^2} \right\|_{s = j\omega_s}$$

$$= \frac{8}{\pi^2} \frac{1}{\sqrt{\left(1 - F^2\right)^2 + \left(\frac{F}{Q_e} \right)^2}}$$

At resonance, this becomes

$$M = \frac{8}{\pi^2} \frac{R_e}{R_0} = \frac{R}{R_0}$$

- PRC can step up the voltage, provided $R > R_0$
- PRC can produce M approaching infinity, provided output current is limited to value less than V_g / R_0

19.3 Exact characteristics of the series and parallel resonant dc-dc converters

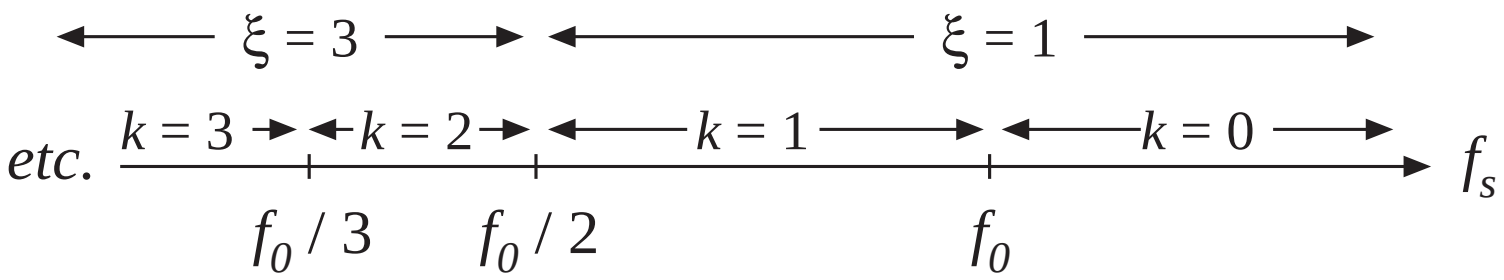
Define

$$\frac{f_0}{k+1} < f_s < \frac{f_0}{k} \qquad \text{or} \qquad \frac{1}{k+1} < F < \frac{1}{k}$$

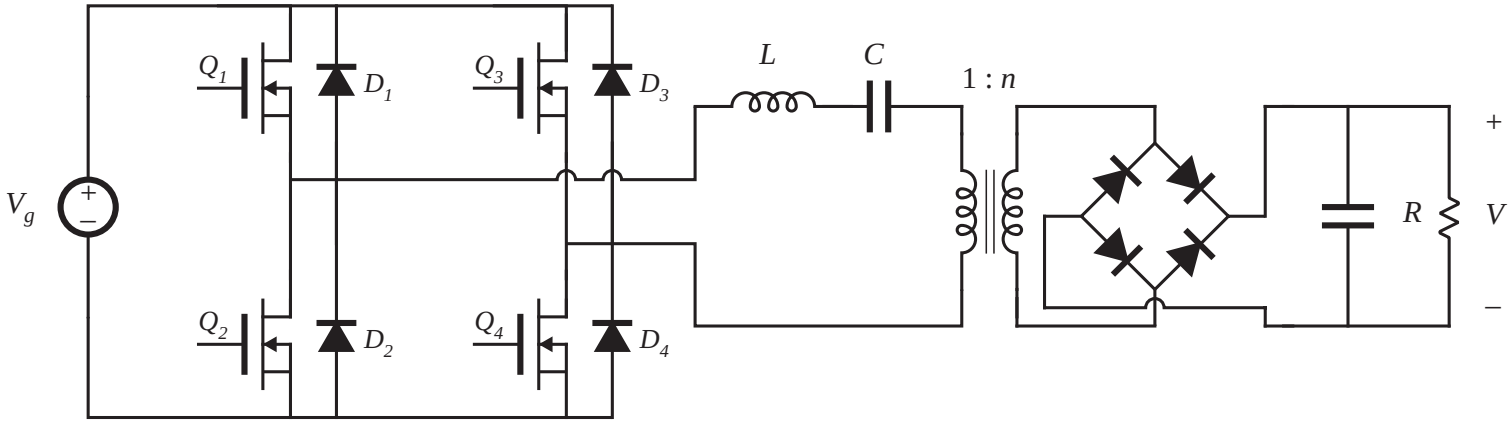
mode index k

$$\xi = k + \frac{1 + (-1)^k}{2}$$

subharmonic index ξ



19.3.1 Exact characteristics of the series resonant converter



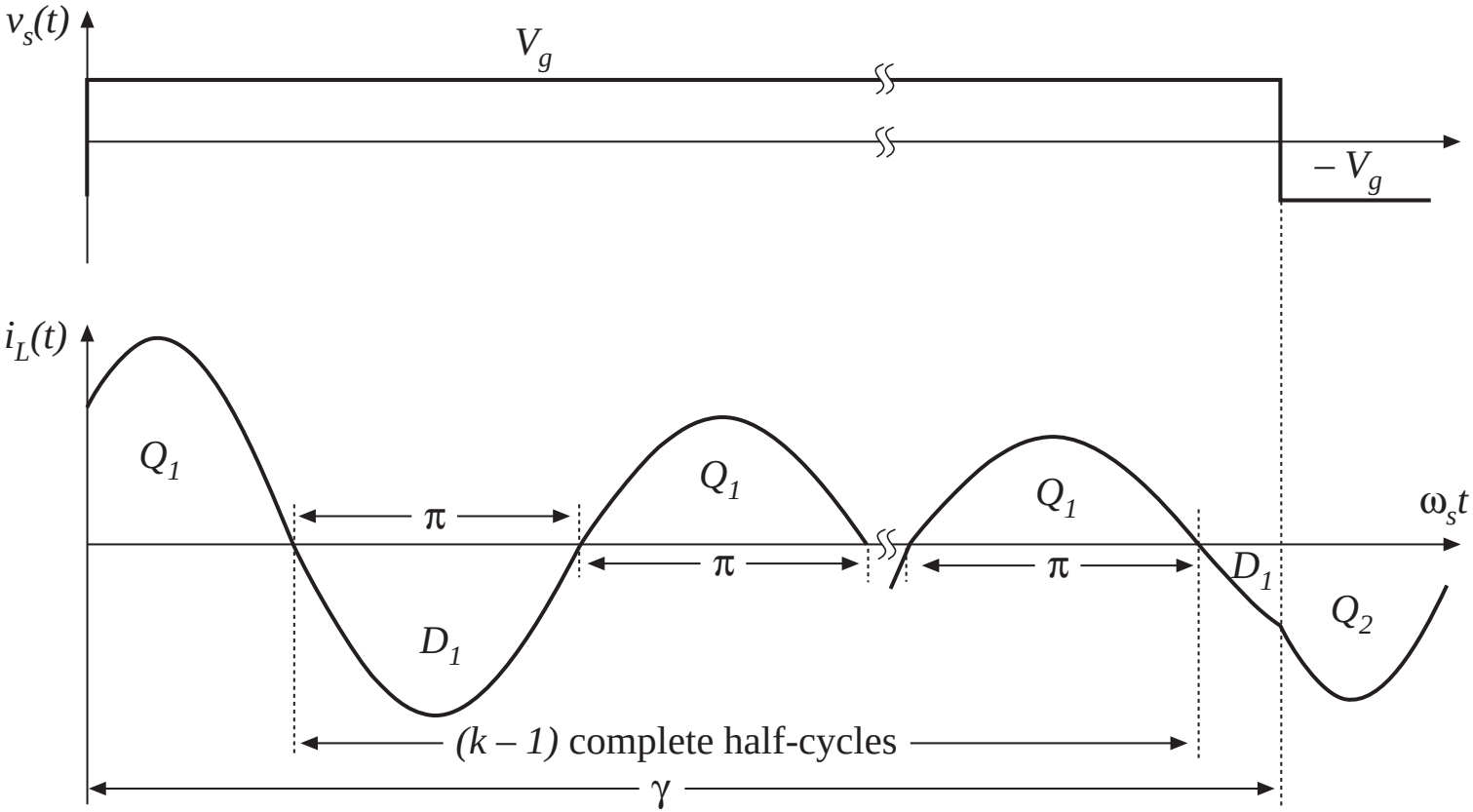
Normalized load voltage and current:

$$M = \frac{V}{nV_g} \qquad J = \frac{InR_0}{V_g}$$

Continuous conduction mode, SRC

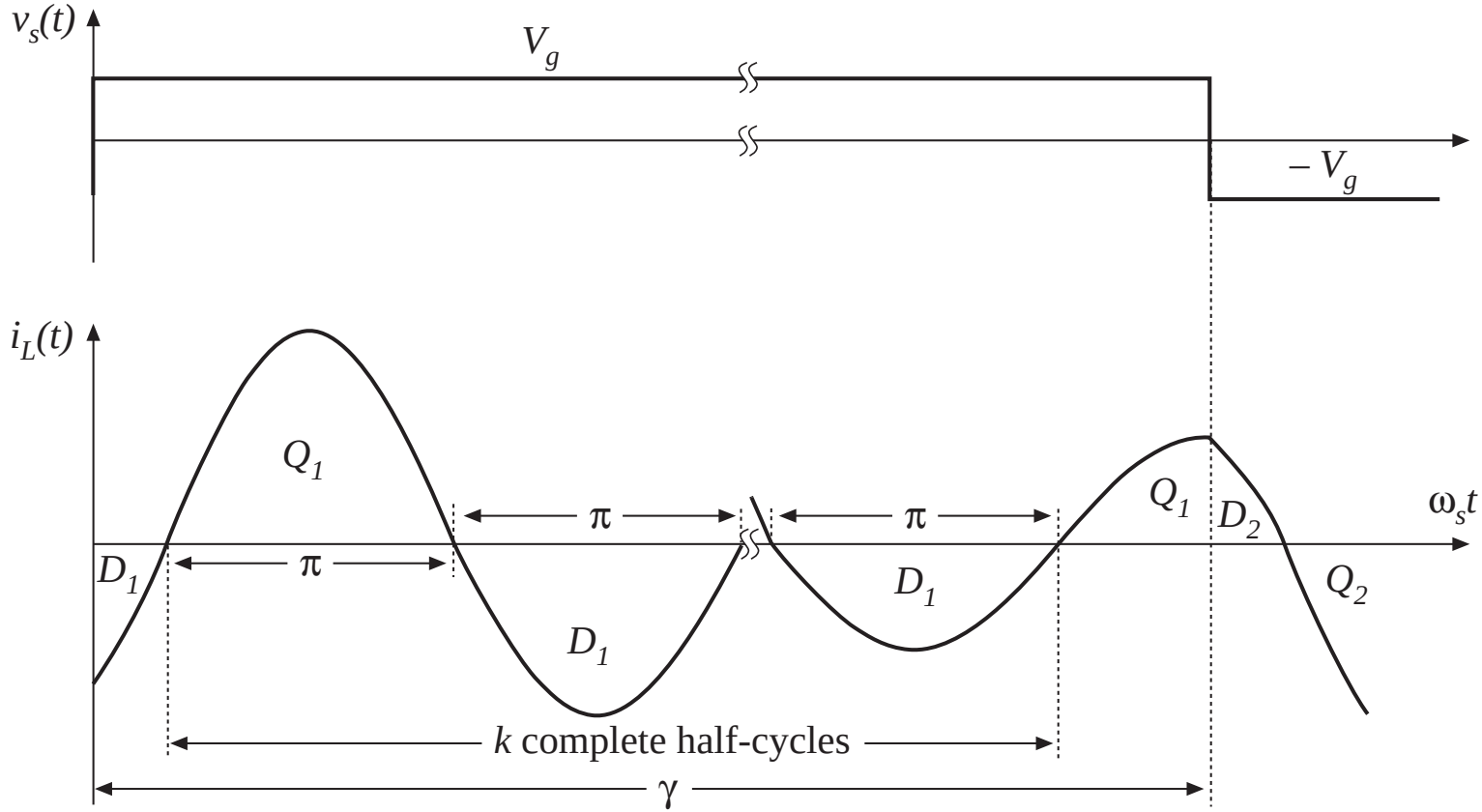
Tank current rings continuously for entire length of switching period

Waveforms for type k CCM, odd k :



Series resonant converter

Waveforms for type k CCM, even k :



Exact steady-state solution, CCM

Series resonant converter

$$M^2\xi^2 \sin^2\left(\frac{\gamma}{2}\right) + \frac{1}{\xi^2}\left(\frac{J\gamma}{2} + (-1)^k\right)^2 \cos^2\left(\frac{\gamma}{2}\right) = 1$$

where

$$M = \frac{V}{nV_g} \qquad J = \frac{InR_0}{V_g}$$

$$\gamma = \frac{\omega_0 T_s}{2} = \frac{\pi}{F}$$

- Output characteristic, i.e., the relation between M and J, is elliptical
- M is restricted to the range

$$0 \le M \le \frac{1}{\xi}$$

Control-plane characteristics

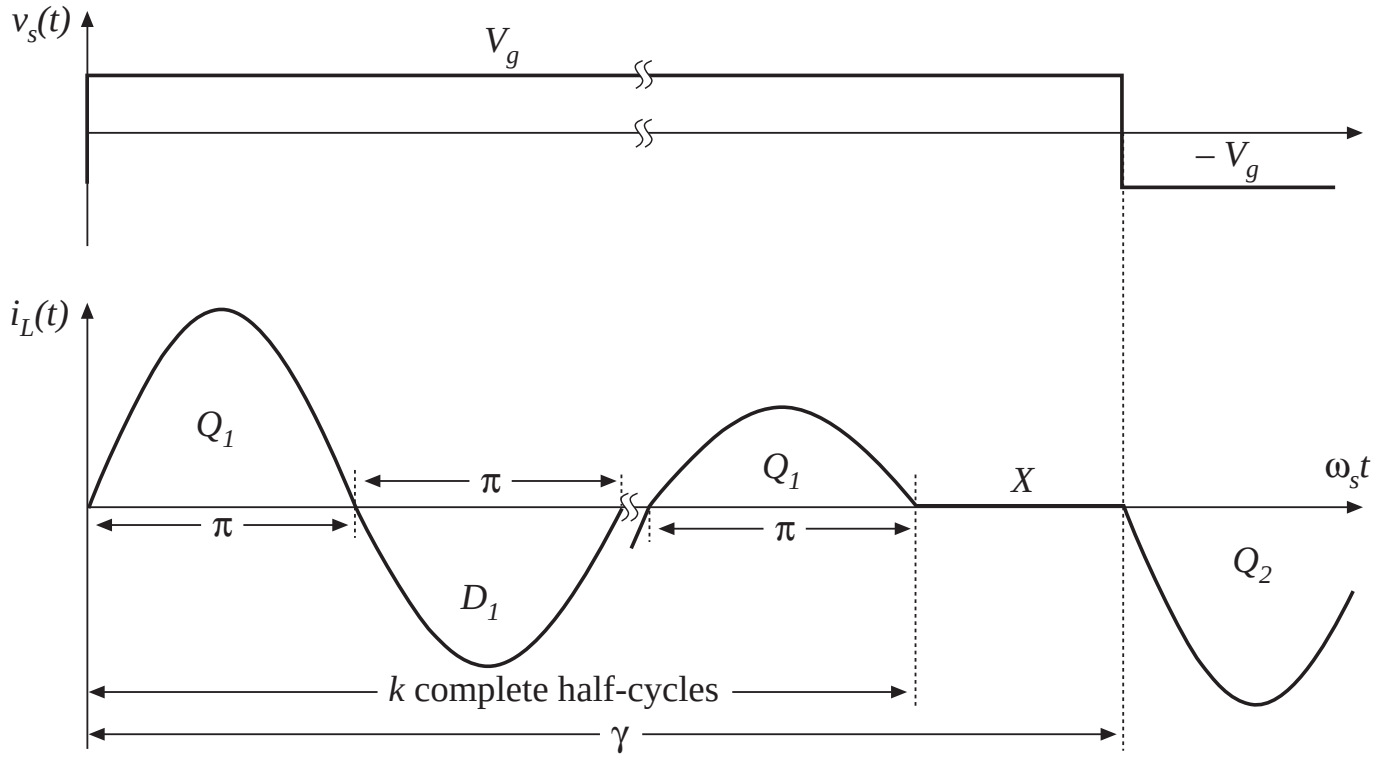
For a resistive load, eliminate J and solve for M vs. γ

$$M = \frac{\left(\frac{Q\gamma}{2}\right)}{\xi^4 \tan^2\left(\frac{\gamma}{2}\right) + \left(\frac{Q\gamma}{2}\right)^2} \left[(-1)^{k+1} + \sqrt{1 + \frac{\left[\xi^2 - \cos^2\left(\frac{\gamma}{2}\right)\right]\left[\xi^4 \tan^2\left(\frac{\gamma}{2}\right) + \left(\frac{Q\gamma}{2}\right)^2\right]}{\left(\frac{Q\gamma}{2}\right)^2 \cos^2\left(\frac{\gamma}{2}\right)}} \right]$$

Exact, closed-form, valid for any CCM

Discontinuous conduction mode

Type *k* DCM: during each half-switching-period, the tank rings for *k* complete half-cycles. The output diodes then become reverse-biased for the remainder of the half-switching-period.



Steady-state solution: type k DCM, odd k

$$M = \frac{1}{k}$$

Conditions for operation in type k DCM, odd k :

$$f_s < \frac{f_0}{k}$$

$$\frac{2(k+1)}{\gamma} > J > \frac{2(k-1)}{\gamma}$$

Steady-state solution: type k DCM, even k

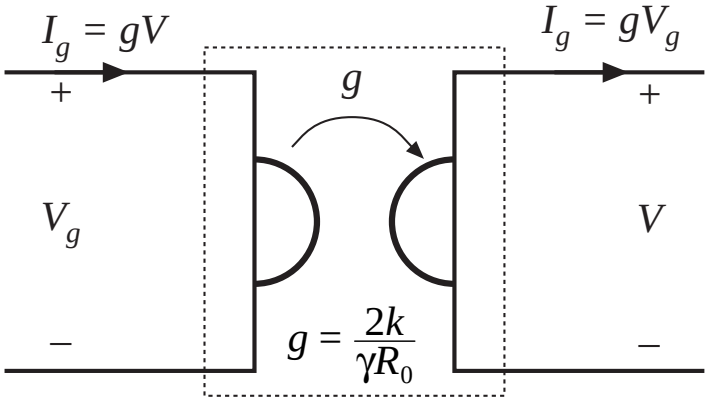
$$J = \frac{2k}{\gamma}$$

Conditions for operation in type k DCM, even k :

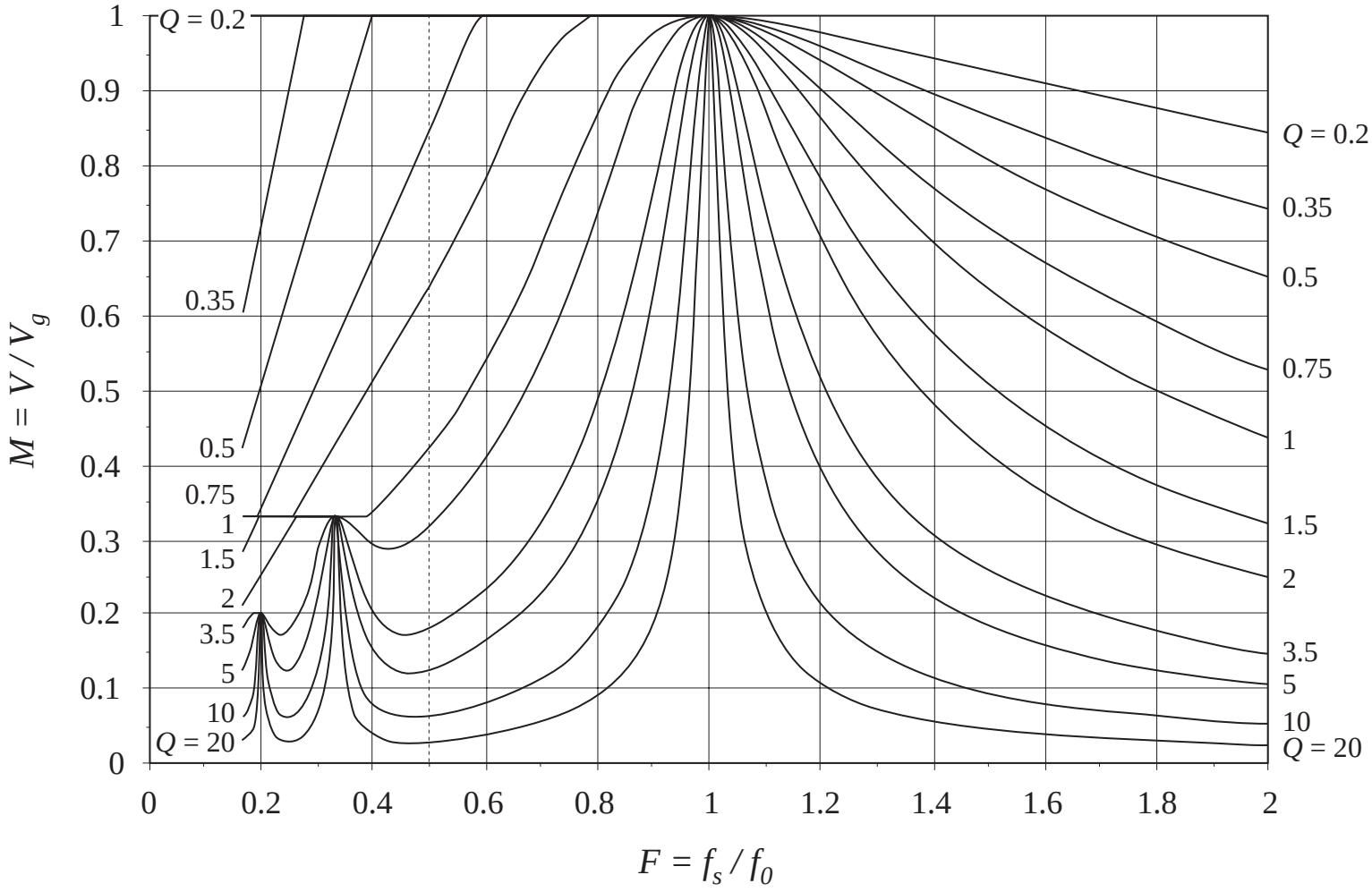
$$f_s < \frac{f_0}{k}$$

$$\frac{1}{k-1} > M > \frac{1}{k+1}$$

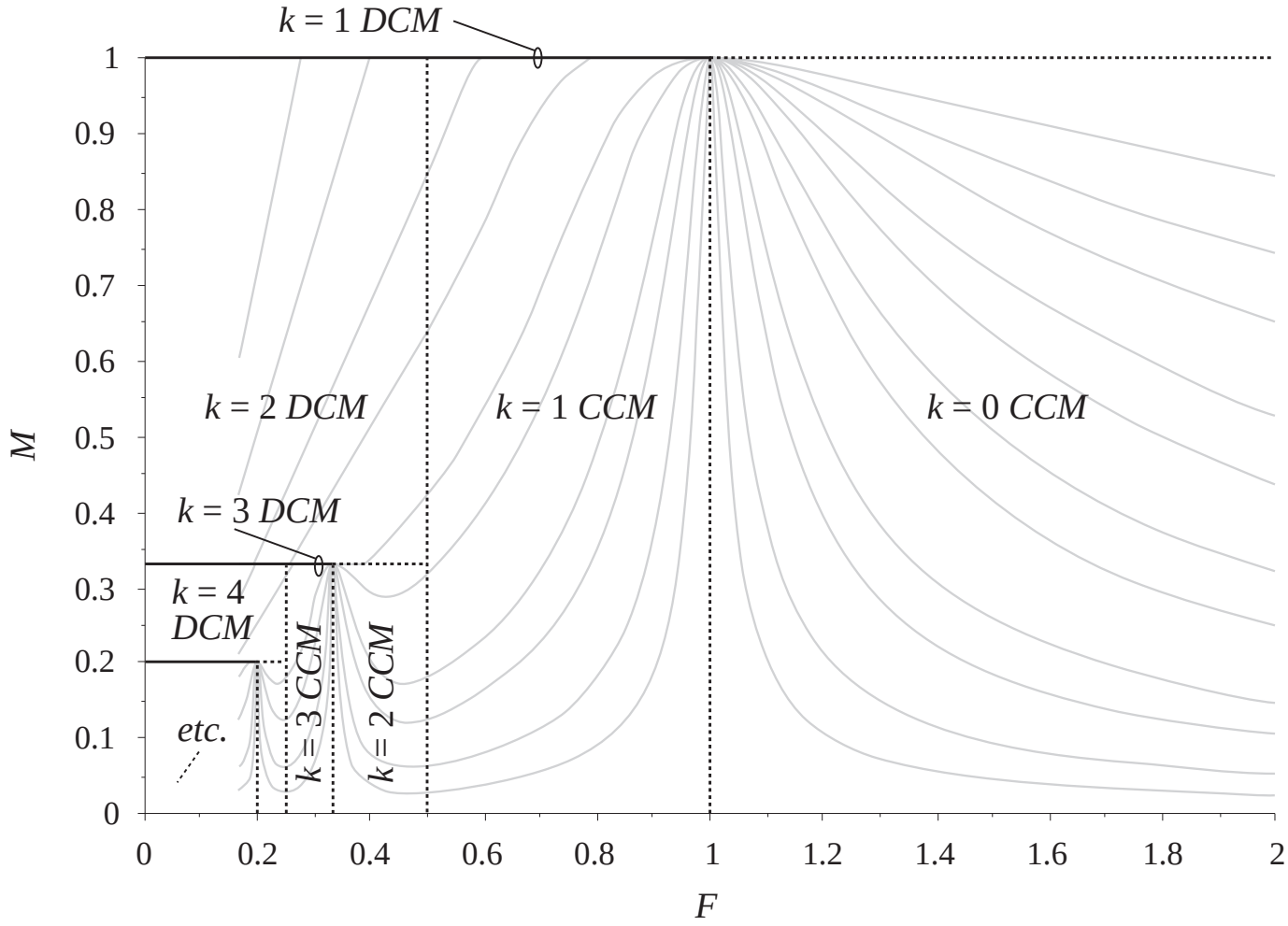
gyrator model, SRC operating in an even DCM:



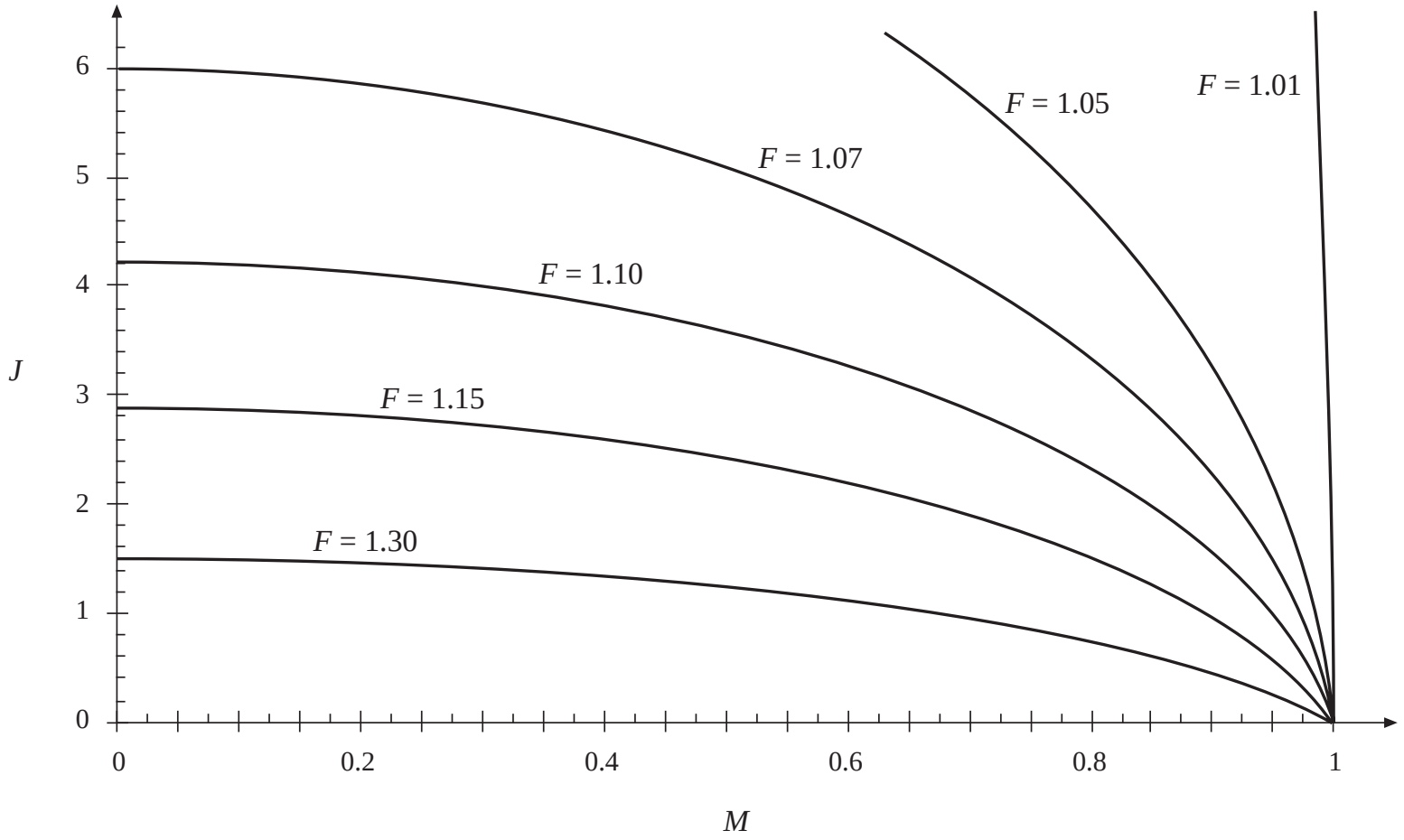
Control plane characteristics, SRC



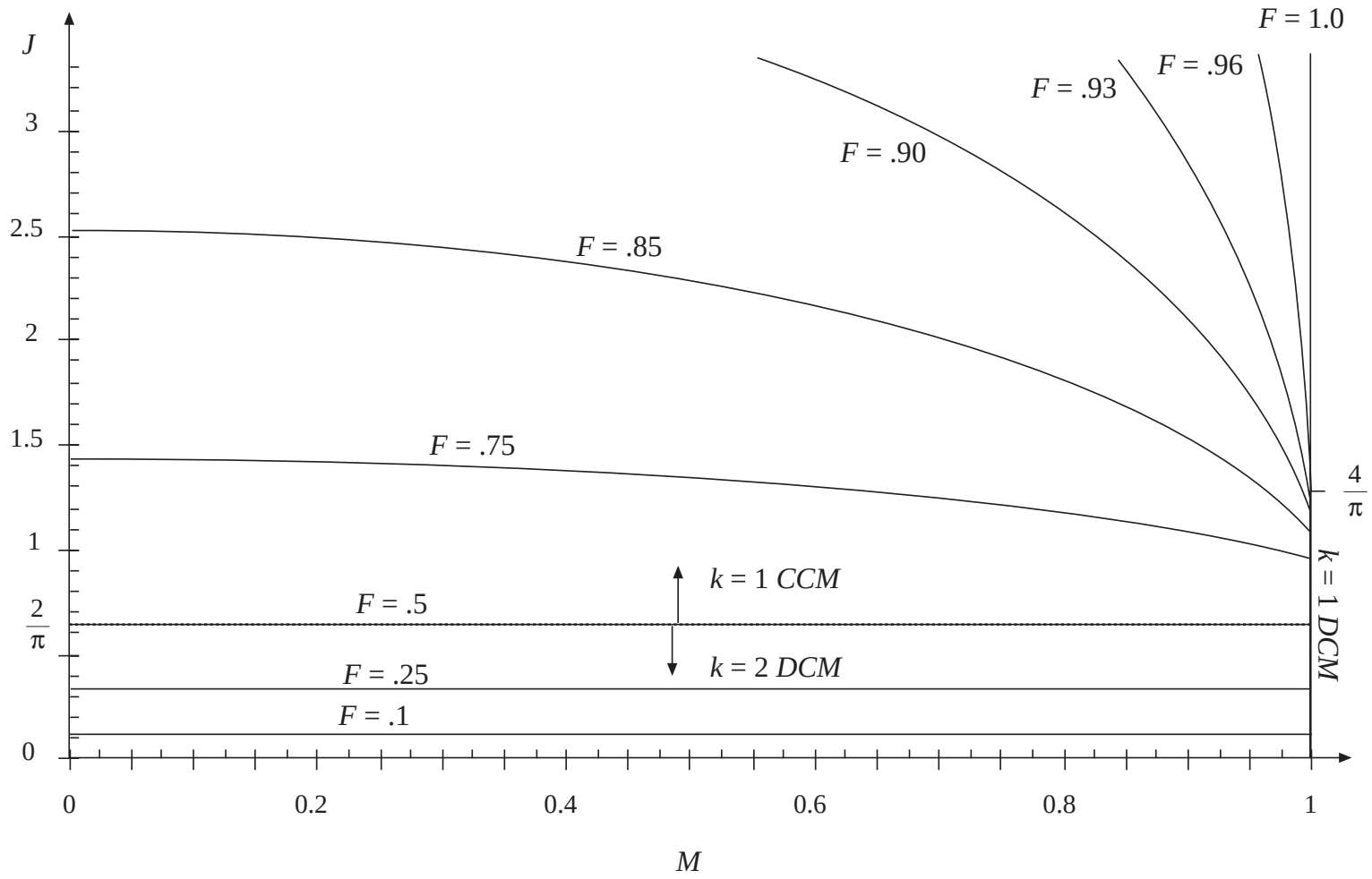
Mode boundaries, SRC



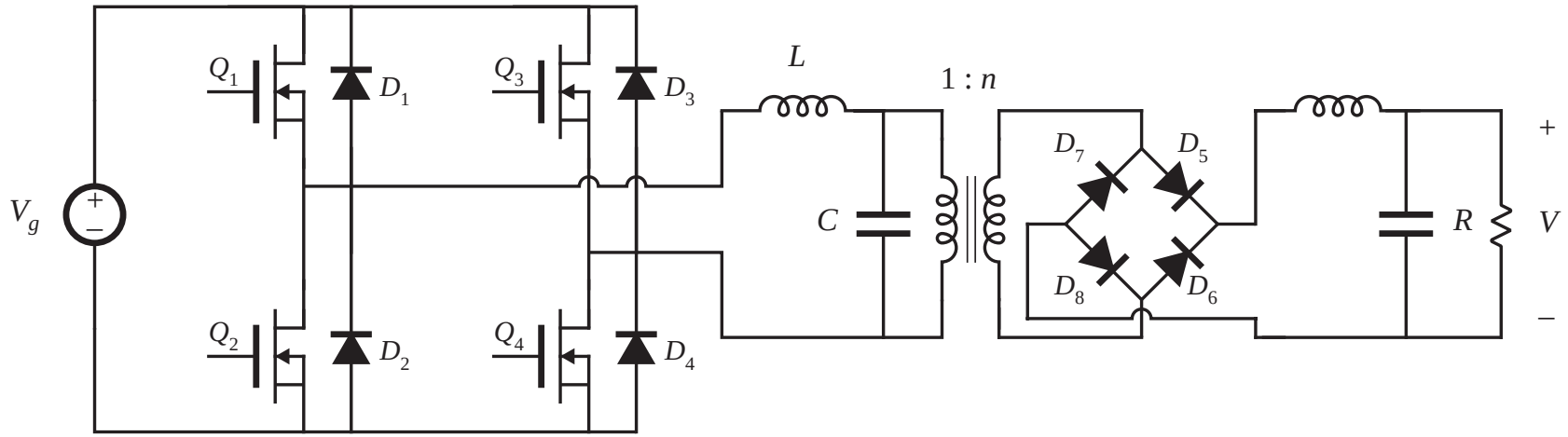
Output characteristics, SRC above resonance



Output characteristics, SRC below resonance



19.3.2 Exact characteristics of the parallel resonant converter



Normalized load voltage and current:

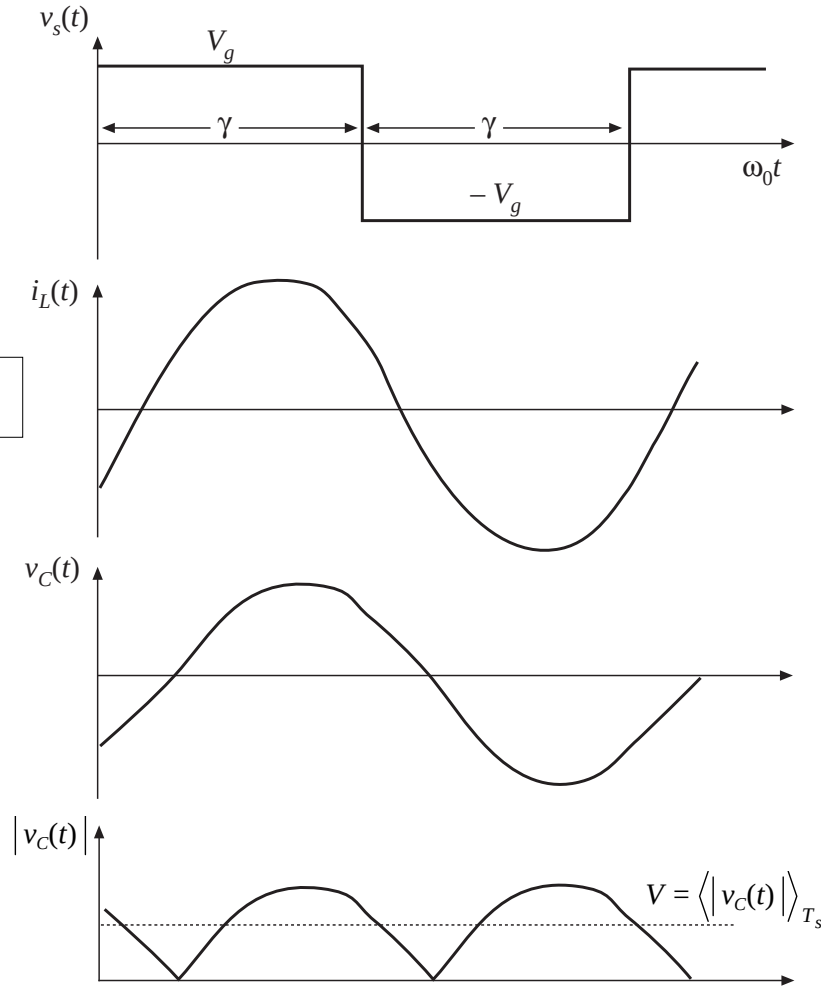
$$M = \frac{V}{nV_g} \qquad J = \frac{InR_0}{V_g}$$

Parallel resonant converter in CCM

CCM closed-form solution

$$M = \left(\frac{2}{\gamma}\right)\left(\varphi - \frac{\sin(\varphi)}{\cos\left(\frac{\gamma}{2}\right)}\right)$$

$$\varphi = \begin{cases} -\cos^{-1}\left(\cos\left(\frac{\gamma}{2}\right) + J\sin\left(\frac{\gamma}{2}\right)\right) & \text{for } 0 < \gamma < \pi \\ +\cos^{-1}\left(\cos\left(\frac{\gamma}{2}\right) + J\sin\left(\frac{\gamma}{2}\right)\right) & \text{for } \pi < \gamma < 2\pi \end{cases}$$



Parallel resonant converter in DCM

Mode boundary

$J > J_{crit}(\gamma)$ for DCM

$J < J_{crit}(\gamma)$ for CCM

$$J_{crit}(\gamma) = -\frac{1}{2}\sin(\gamma) + \sqrt{\sin^2\left(\frac{\gamma}{2}\right) + \frac{1}{4}\sin^2(\gamma)}$$

DCM equations

$$M_{C0} = 1 - \cos(\beta)$$

$$J_{L0} = J + \sin(\beta)$$

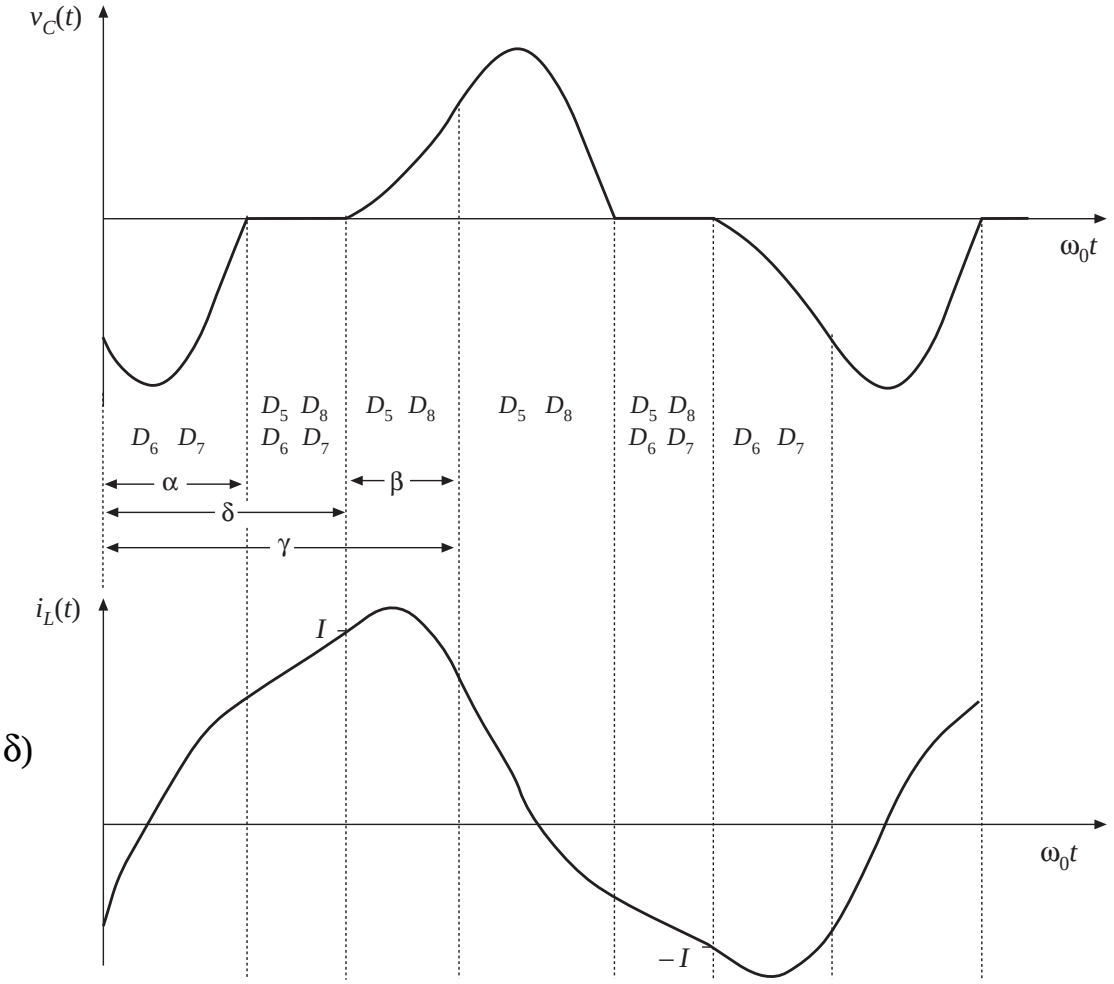
$$\cos(\alpha + \beta) - 2\cos(\alpha) = -1$$

$$-\sin(\alpha + \beta) + 2\sin(\alpha) + (\delta - \alpha) = 2J$$

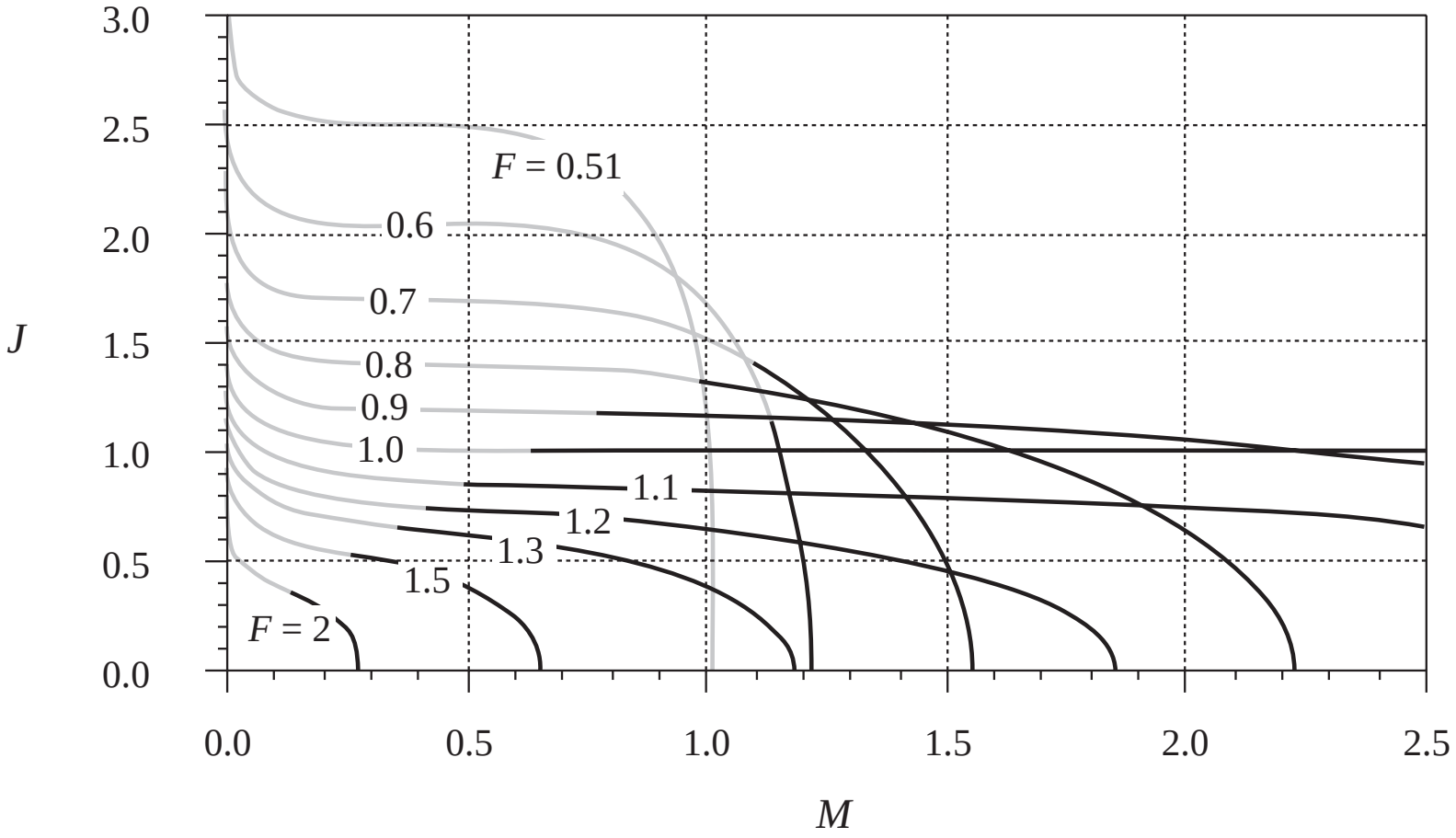
$$\beta + \delta = \gamma$$

$$M = 1 + \left(\frac{2}{\gamma}\right)(J - \delta)$$

(require iteration)



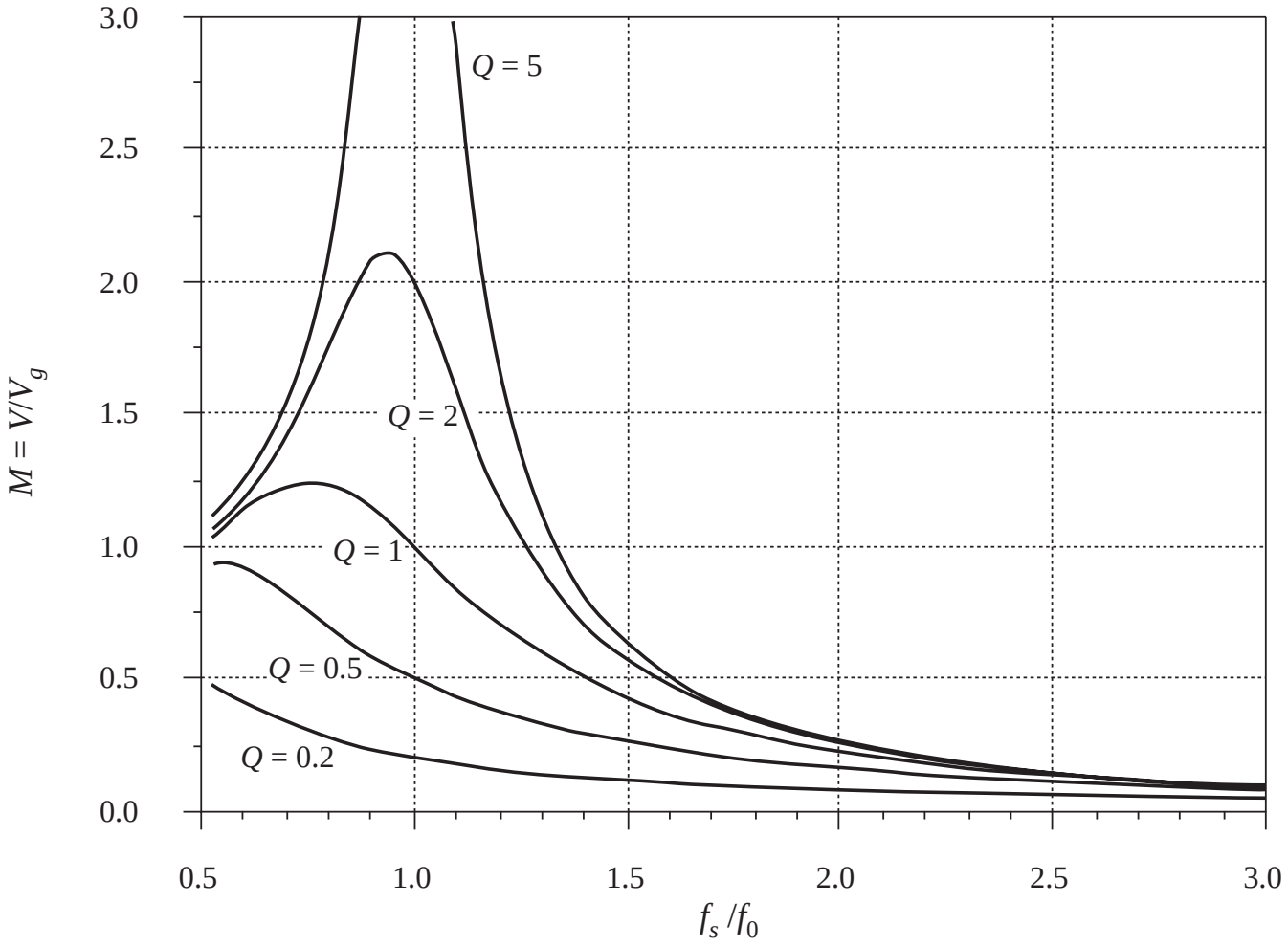
Output characteristics of the PRC



Solid curves: CCM Shaded curves: DCM

Control characteristics of the PRC

with resistive load



19.4 Soft switching

Soft switching can mitigate some of the mechanisms of switching loss and possibly reduce the generation of EMI

Semiconductor devices are switched on or off at the zero crossing of their voltage or current waveforms:

Zero-current switching: transistor turn-off transition occurs at zero current. Zero-current switching eliminates the switching loss caused by IGBT current tailing and by stray inductances. It can also be used to commutate SCR's.

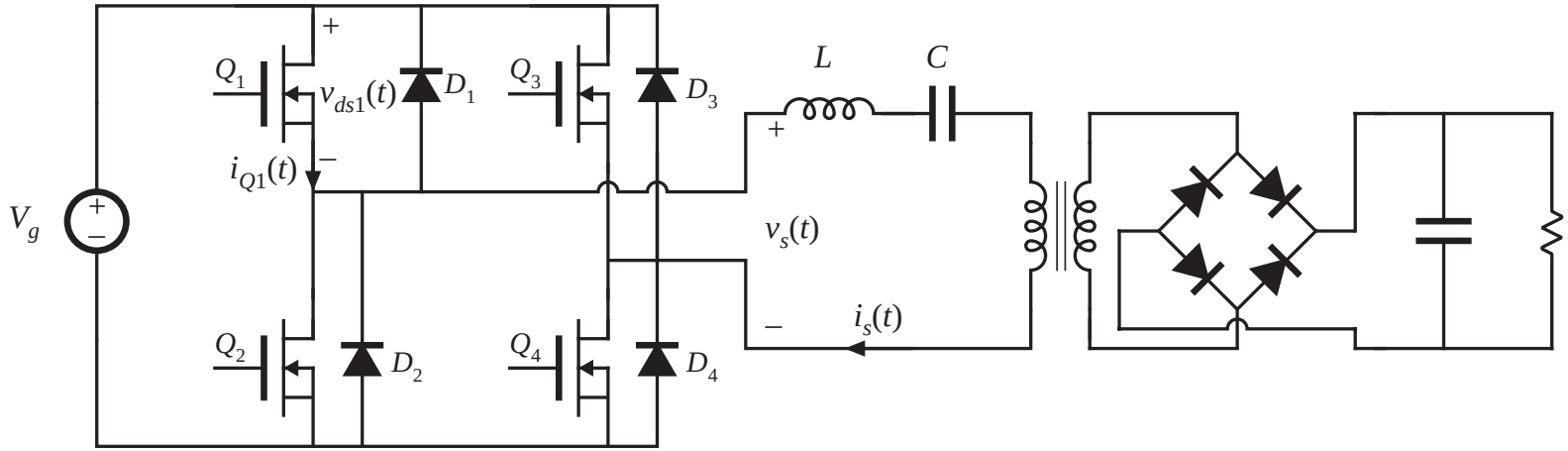
Zero-voltage switching: transistor turn-on transition occurs at zero voltage. Diodes may also operate with zero-voltage switching. Zero-voltage switching eliminates the switching loss induced by diode stored charge and device output capacitances.

Zero-voltage switching is usually preferred in modern converters.

Zero-voltage transition converters are modified PWM converters, in which an inductor charges and discharges the device capacitances. Zero-voltage switching is then obtained.

19.4.1 Operation of the full bridge below resonance: Zero-current switching

Series resonant converter example



Operation below resonance: input tank current leads voltage

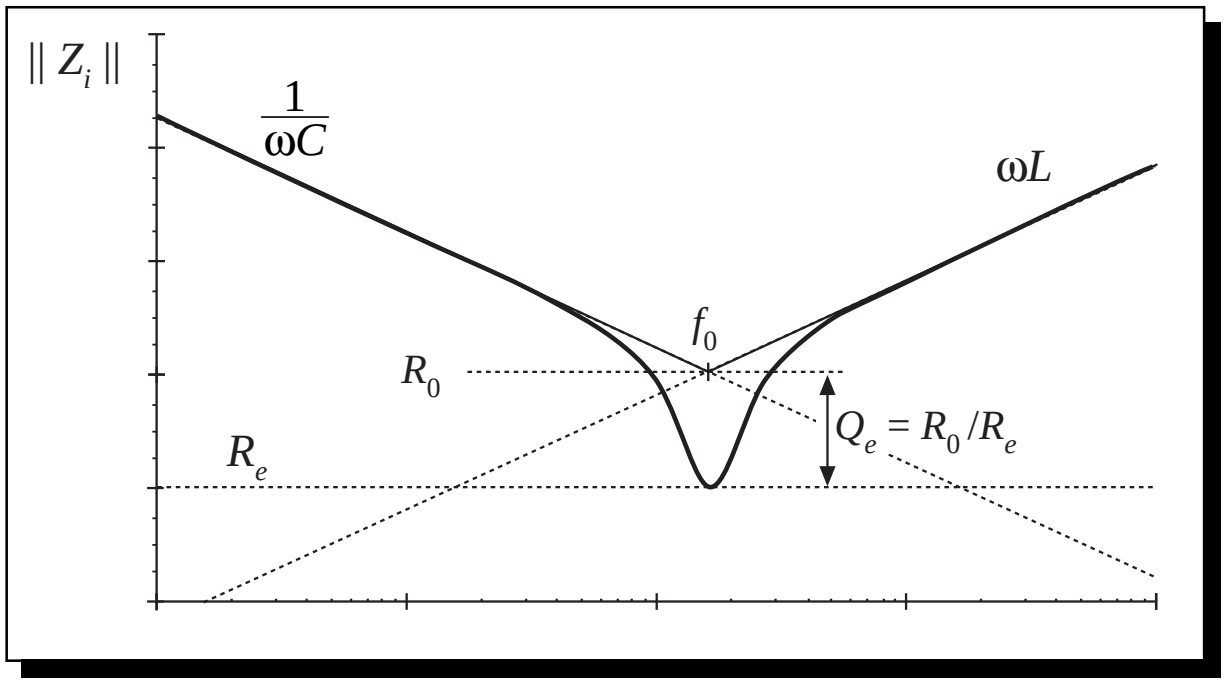
Zero-current switching (ZCS) occurs

Tank input impedance

Operation below resonance: tank input impedance Z_i is dominated by tank capacitor.

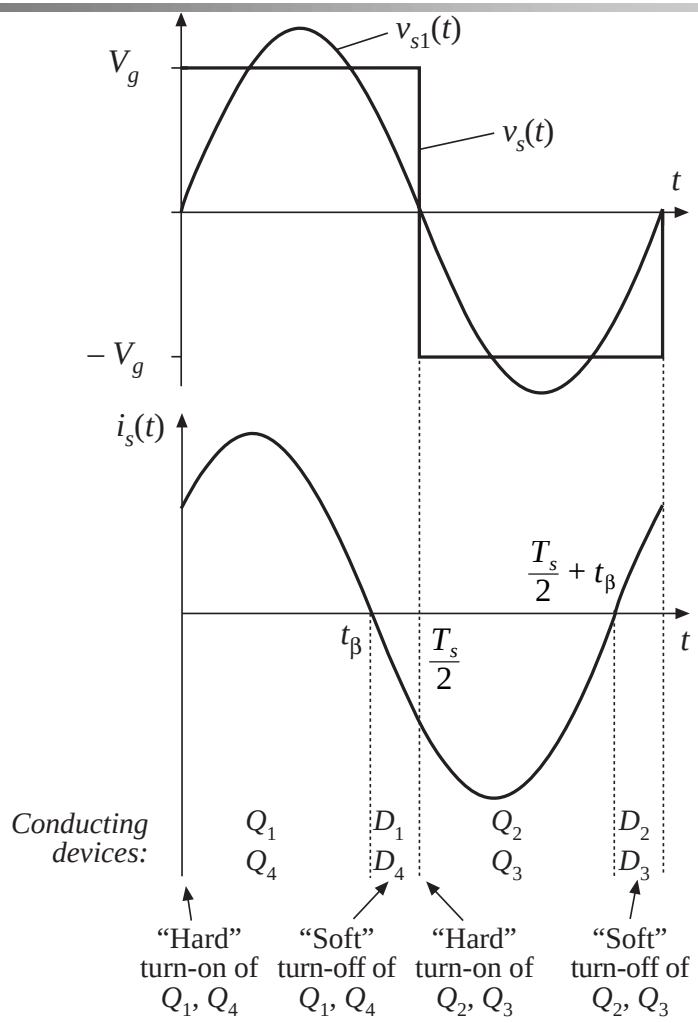
$\angle Z_i$ is positive, and tank input current leads tank input voltage.

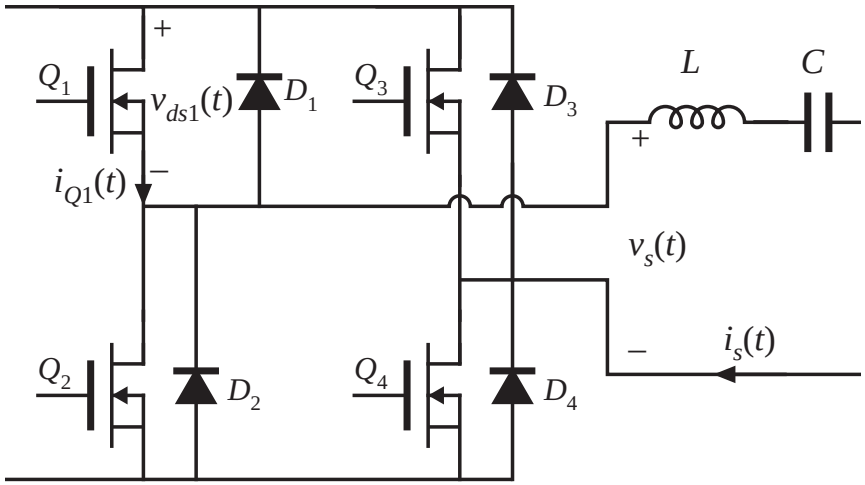
Zero crossing of the tank input current waveform $i_s(t)$ occurs before the zero crossing of the voltage $v_s(t)$.



Switch network waveforms, below resonance

Zero-current switching

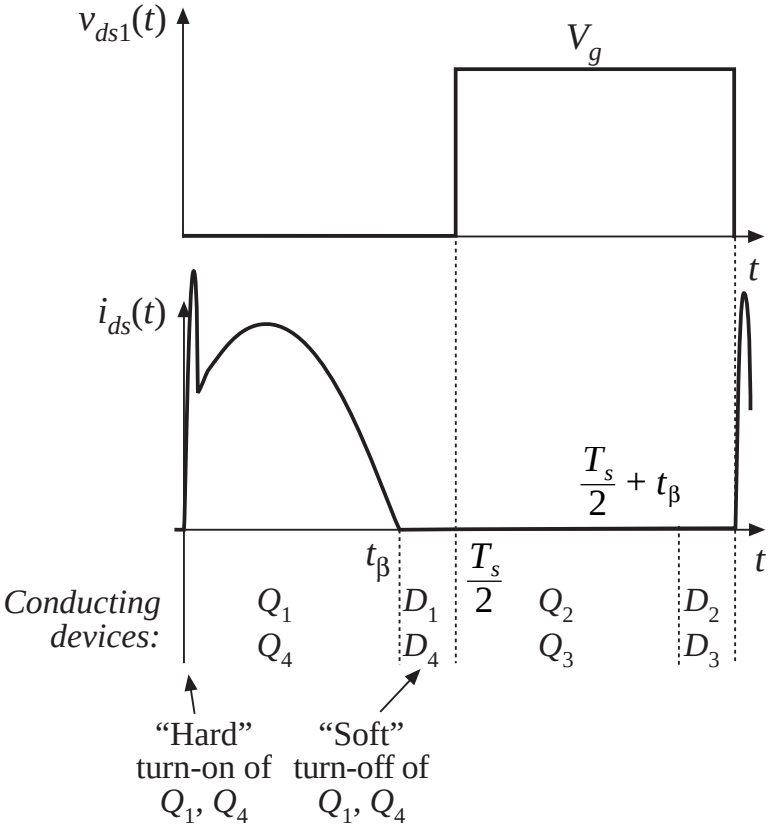


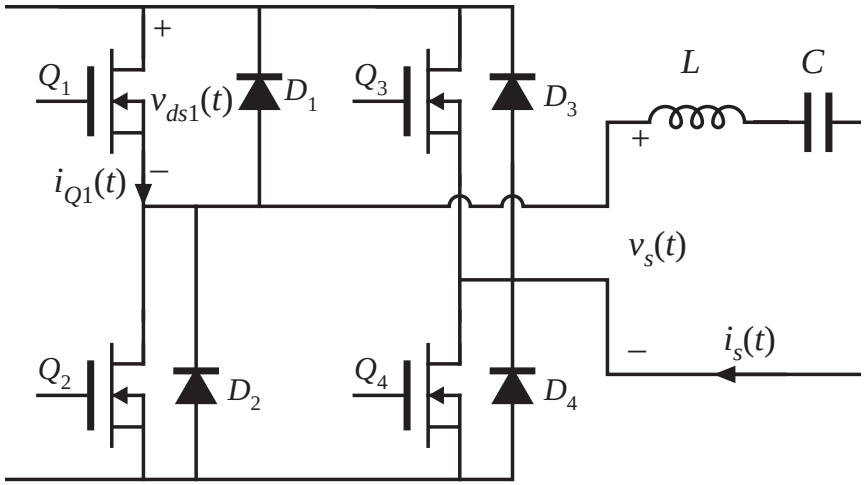


Conduction sequence: Q_1–D_1–Q_2–D_2

Q_1 is turned off during D_1 conduction interval, without loss

ZCS turn-on transition: hard switching

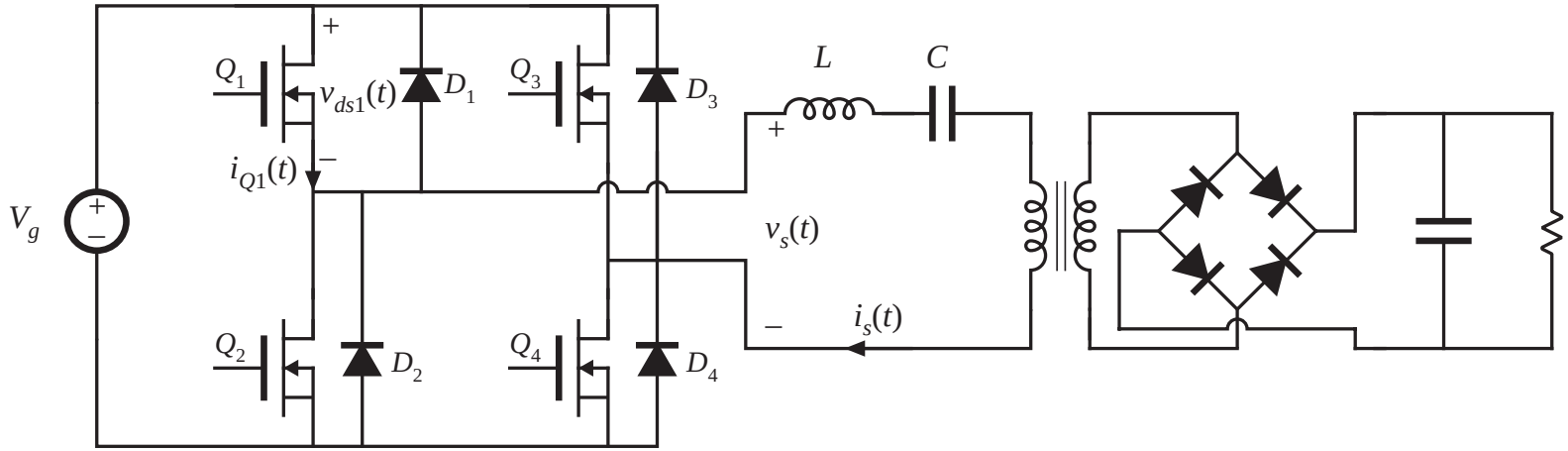




Q_1 turns on while D_2 is conducting. Stored charge of D_2 and of semiconductor output capacitances must be removed. Transistor turn-on transition is identical to hard-switched PWM, and switching loss occurs.

19.4.2 Operation of the full bridge below resonance: Zero-voltage switching

Series resonant converter example



Operation above resonance: input tank current lags voltage

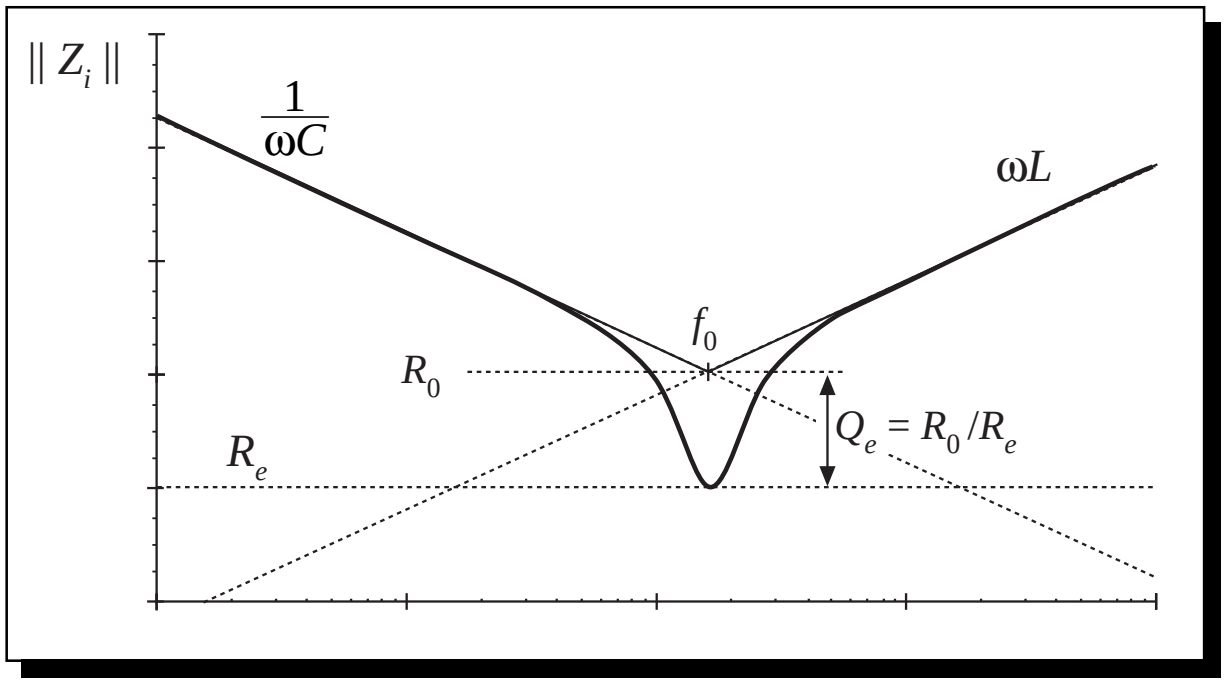
Zero-voltage switching (ZVS) occurs

Tank input impedance

Operation above resonance: tank input impedance Z_i is dominated by tank inductor.

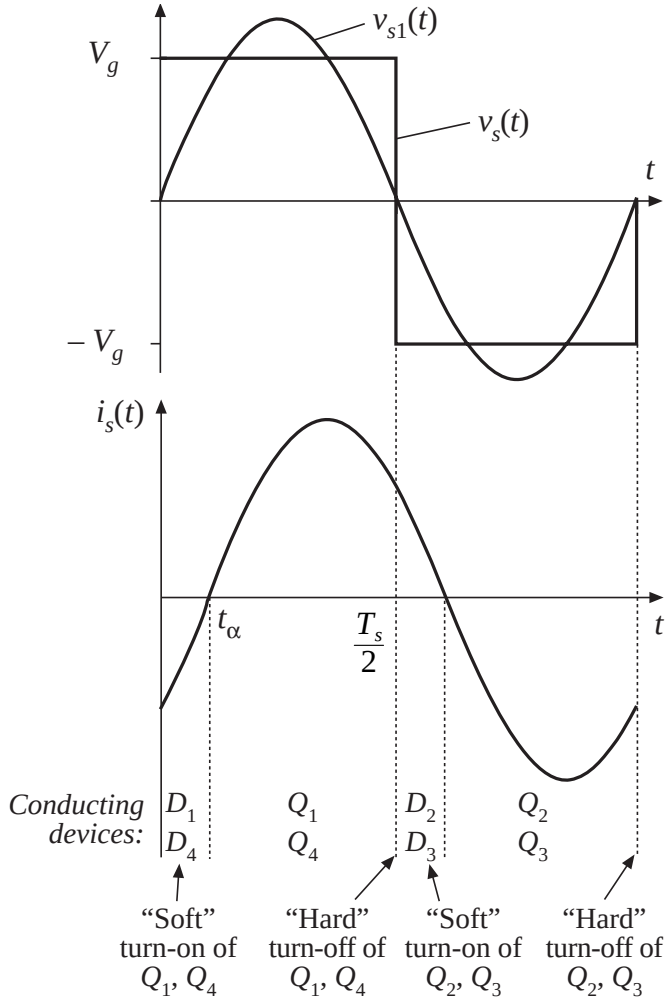
$\angle Z_i$ is negative, and tank input current lags tank input voltage.

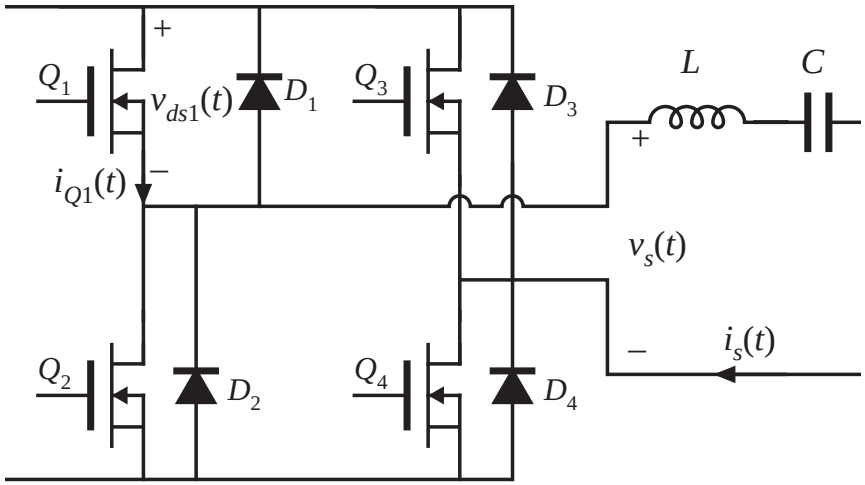
Zero crossing of the tank input current waveform $i_s(t)$ occurs after the zero crossing of the voltage $v_s(t)$.



Switch network waveforms, above resonance

Zero-voltage switching

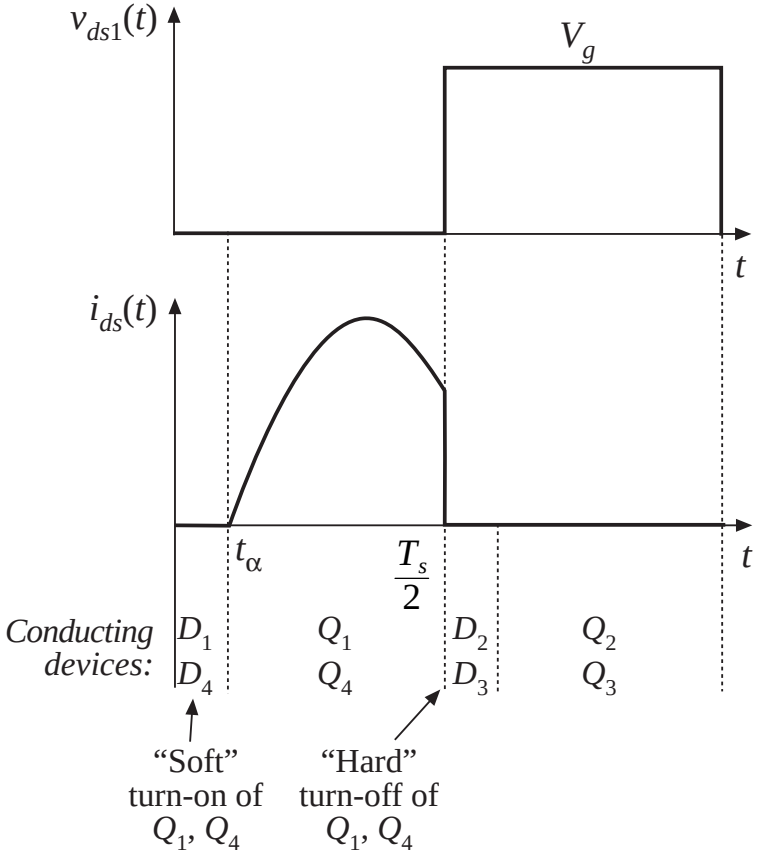


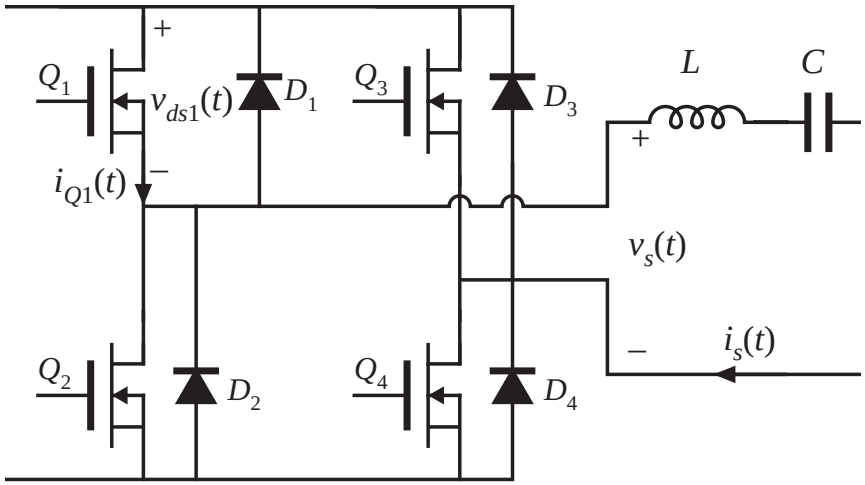


Conduction sequence: D_1–Q_1–D_2–Q_2

Q_1 is turned on during D_1 conduction interval, without loss

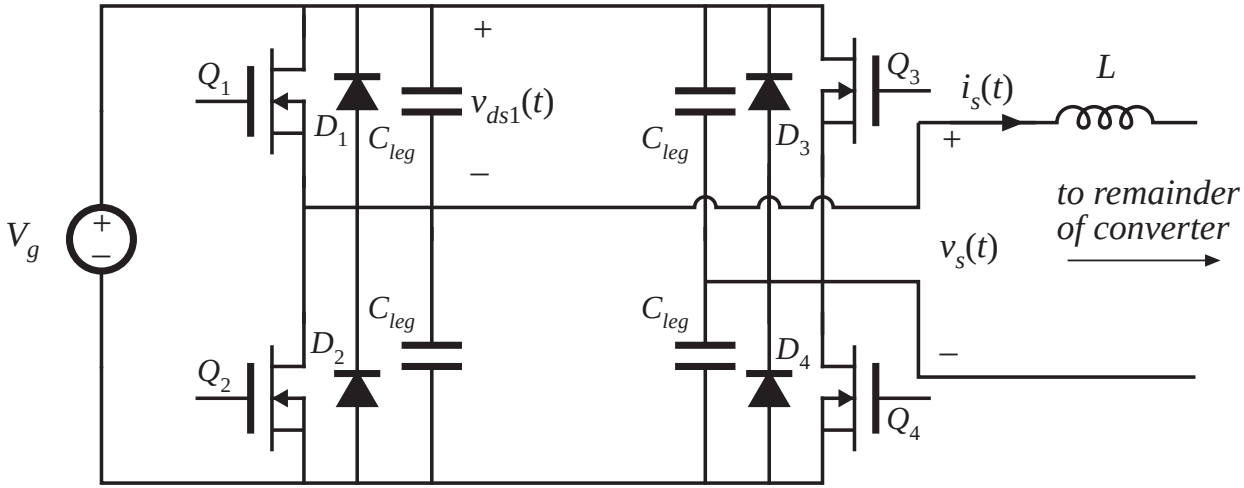
ZVS turn-off transition: hard switching?



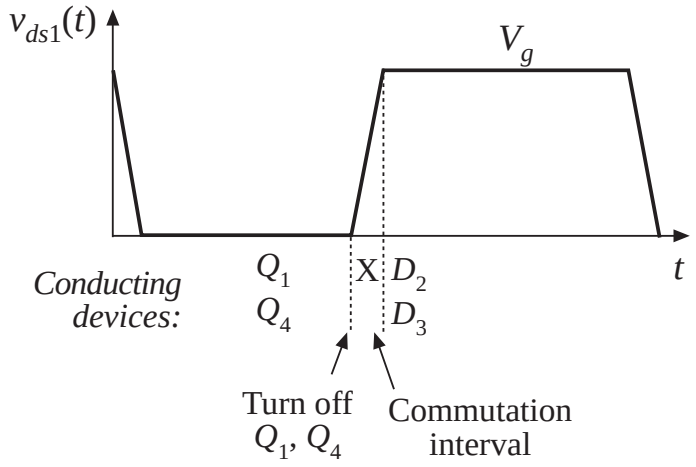


When Q_1 turns off, D_2 must begin conducting. Voltage across Q_1 must increase to V_g. Transistor turn-off transition is identical to hard-switched PWM. Switching loss may occur (but see next slide).

Soft switching at the ZVS turn-off transition



- Introduce small capacitors C_{leg} across each device (or use device output capacitances).
- Introduce delay between turn-off of Q_1 and turn-on of Q_2.

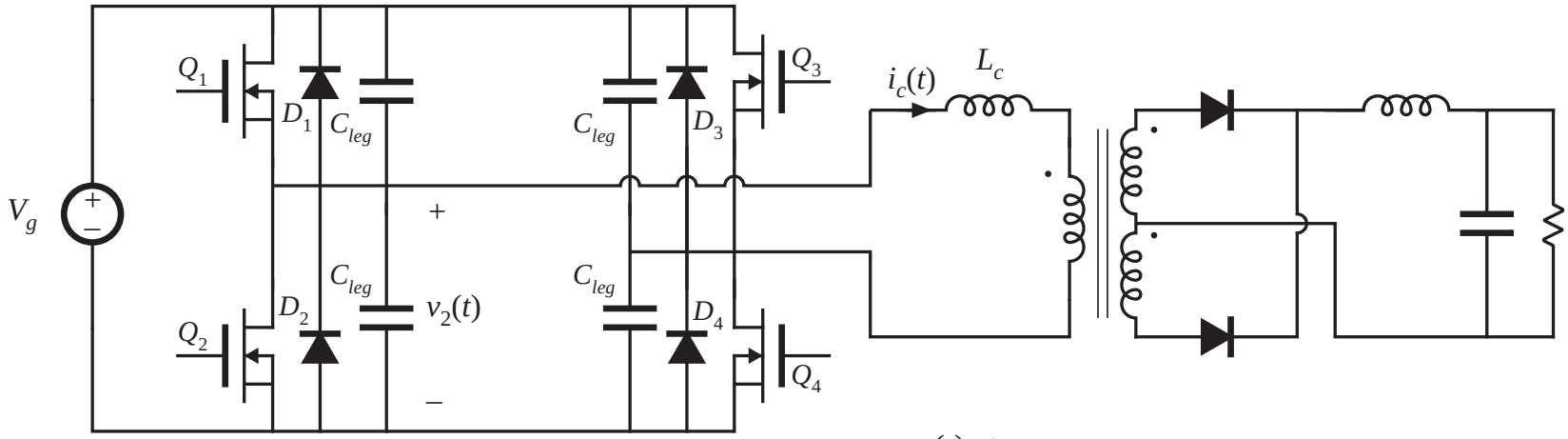


Tank current $i_s(t)$ charges and discharges C_{leg}. Turn-off transition becomes lossless. During commutation interval, no devices conduct.

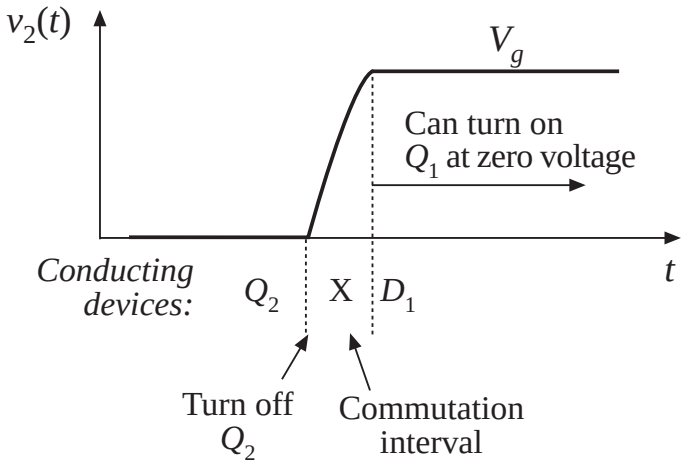
So zero-voltage switching exhibits low switching loss: losses due to diode stored charge and device output capacitances are eliminated.

19.4.3 The zero-voltage transition converter

Basic version based on full-bridge PWM buck converter



- Can obtain ZVS of all primary-side MOSFETs and diodes
- Secondary-side diodes switch at zero-current, with loss
- Phase-shift control



19.5 Load-dependent properties of resonant converters

Resonant inverter design objectives:

1. Operate with a specified load characteristic and range of operating points
   - With a nonlinear load, must properly match inverter output characteristic to load characteristic
2. Obtain zero-voltage switching or zero-current switching
   - Preferably, obtain these properties at all loads
   - Could allow ZVS property to be lost at light load, if necessary
3. Minimize transistor currents and conduction losses
   - To obtain good efficiency at light load, the transistor current should scale proportionally to load current (in resonant converters, it often doesn't!)

Topics of Discussion

Section 19.5

Inverter output *i*-*v* characteristics

Two theorems

- Dependence of transistor current on load current
- Dependence of zero-voltage/zero-current switching on load resistance
- Simple, intuitive frequency-domain approach to design of resonant converter

Examples and interpretation

- Series
- Parallel
- LCC

Inverter output characteristics

Let H_∞ be the open-circuit ($R \to \infty$) transfer function:

$$\left.\frac{v_o(j\omega)}{v_i(j\omega)}\right|_{R \to \infty} = H_\infty(j\omega)$$

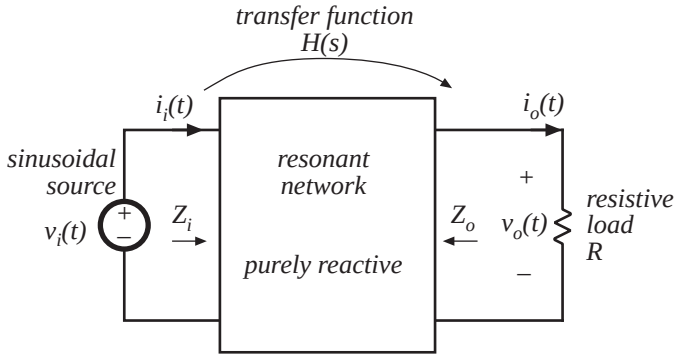
and let Z_{o0} be the output impedance (with $v_i \to$ short-circuit). Then,

$$v_o(j\omega) = H_\infty(j\omega)\, v_i(j\omega)\, \frac{R}{R + Z_{o0}(j\omega)}$$

The output voltage magnitude is:

$$\| v_o \|^2 = v_o v_o^* = \frac{\| H_\infty \|^2 \| v_i \|^2}{\left(1 + \| Z_{o0} \|^2 / R^2\right)}$$

with $R = \| v_o \| / \| i_o \|$



This result can be rearranged to obtain

$$\| v_o \|^2 + \| i_o \|^2 \| Z_{o0} \|^2 = \| H_\infty \|^2 \| v_i \|^2$$

Hence, at a given frequency, the output characteristic (i.e., the relation between $\|v_o\|$ and $\|i_o\|$) of any resonant inverter of this class is elliptical.

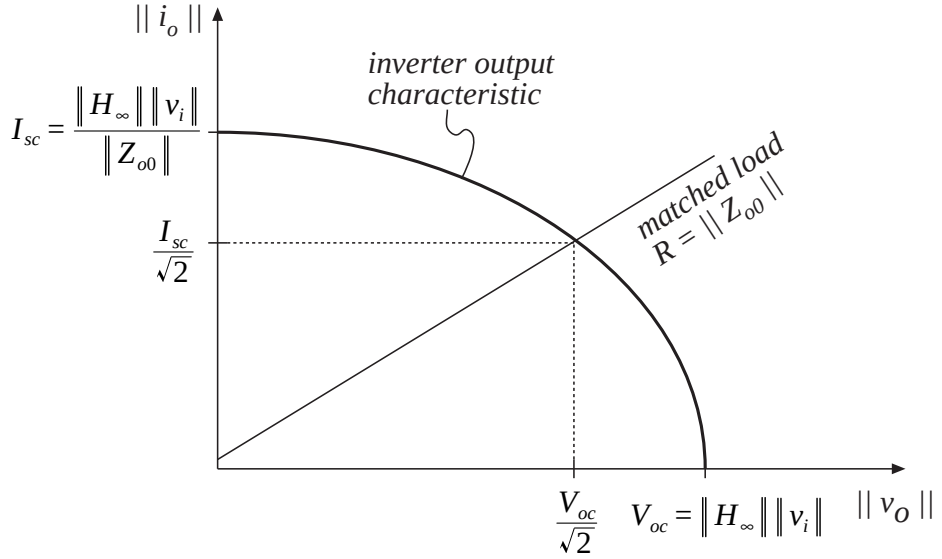
Inverter output characteristics

General resonant inverter output characteristics are elliptical, of the form

$$\frac{\left\| v_o \right\|^2}{V_{oc}^2} + \frac{\left\| i_o \right\|^2}{I_{sc}^2} = 1$$

with $$V_{oc} = \left\| H_\infty \right\| \left\| v_i \right\|$$

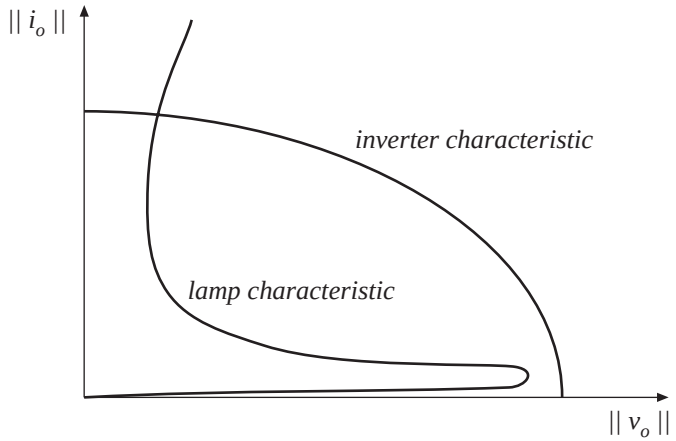
$$I_{sc} = \frac{\left\| H_\infty \right\| \left\| v_i \right\|}{\left\| Z_{o0} \right\|}$$



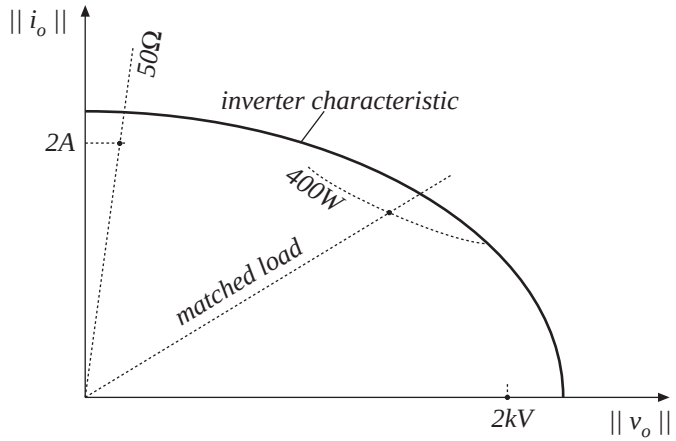
This result is valid provided that *(i)* the resonant network is purely reactive, and *(ii)* the load is purely resistive.

Matching ellipse to application requirements

Electronic ballast

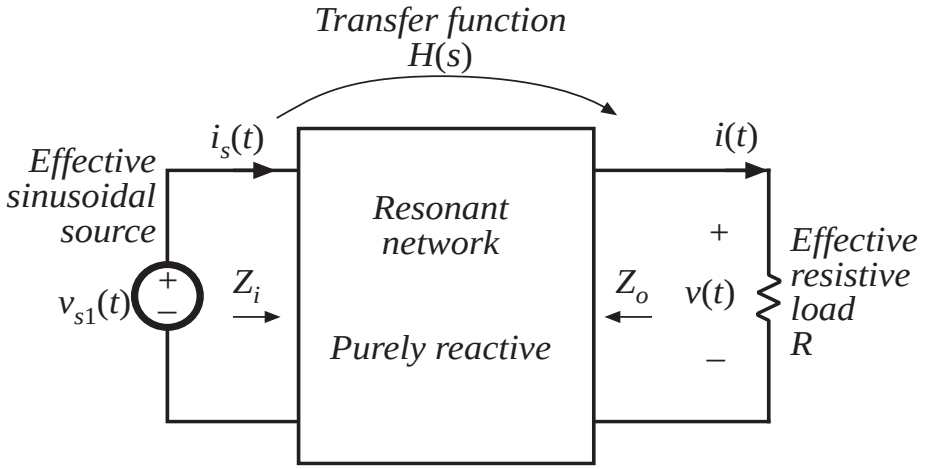


Electrosurgical generator



Input impedance of the resonant tank network

$$Z_i(s) = Z_{i0}(s)\,\frac{1 + \dfrac{R}{Z_{o0}(s)}}{1 + \dfrac{R}{Z_{o\infty}(s)}} = Z_{i\infty}(s)\,\frac{1 + \dfrac{Z_{o0}(s)}{R}}{1 + \dfrac{Z_{o\infty}(s)}{R}}$$



where

$$Z_{i0} = \left.\frac{v_i}{i_i}\right|_{R \to 0} \qquad Z_{i\infty} = \left.\frac{v_i}{i_i}\right|_{R \to \infty} \qquad Z_{o0} = \left.\frac{v_o}{-i_o}\right|_{v_i \to \text{short circuit}} \qquad Z_{o\infty} = \left.\frac{v_o}{-i_o}\right|_{v_i \to \text{open circuit}}$$

Other relations

Reciprocity

$$\frac{Z_{i0}}{Z_{i\infty}} = \frac{Z_{o0}}{Z_{o\infty}}$$

Tank transfer function

$$H(s) = \frac{H_\infty(s)}{1 + \frac{R}{Z_{o0}}}$$

where $$H_\infty = \left.\frac{v_o(s)}{v_i(s)}\right|_{R \to \infty}$$

$$\| H_\infty \|^2 = Z_{o0}\left(\frac{1}{Z_{i0}} - \frac{1}{Z_{i\infty}}\right)$$

If the tank network is purely reactive, then each of its impedances and transfer functions have zero real parts:

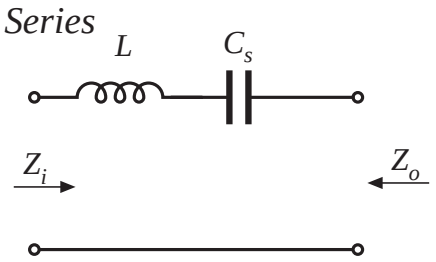
$$Z_{i0} = -Z_{i0}^*$$
$$Z_{i\infty} = -Z_{i\infty}^*$$
$$Z_{o0} = -Z_{o0}^*$$
$$Z_{o\infty} = -Z_{o\infty}^*$$
$$H_\infty = -H_\infty^*$$

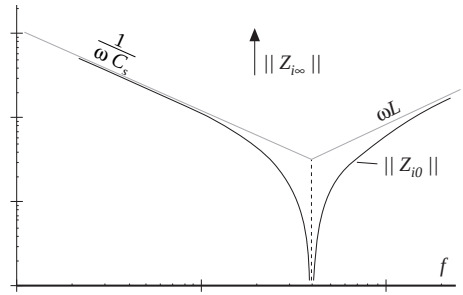
Hence, the input impedance magnitude is

$$\| Z_i \|^2 = Z_i Z_i^* = \| Z_{i0} \|^2 \frac{\left(1 + \frac{R^2}{\| Z_{o0} \|^2}\right)}{\left(1 + \frac{R^2}{\| Z_{o\infty} \|^2}\right)}$$

Z_{i0} *and* $Z_{i\infty}$ for 3 common inverters

Series

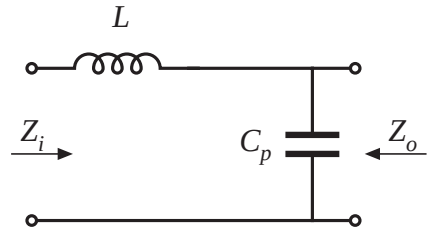


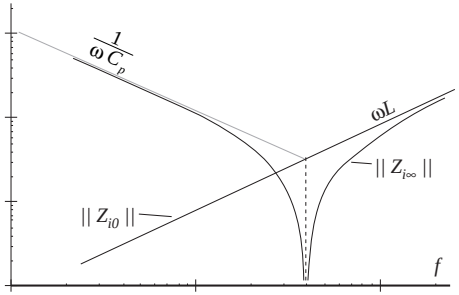


$$Z_{i0}(s) = sL + \frac{1}{sC_s}$$

$$Z_{i\infty}(s) = \infty$$

Parallel

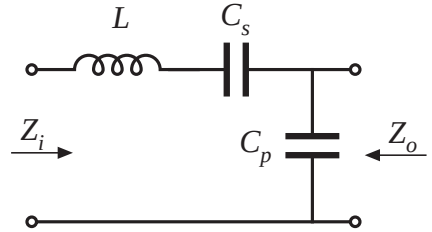


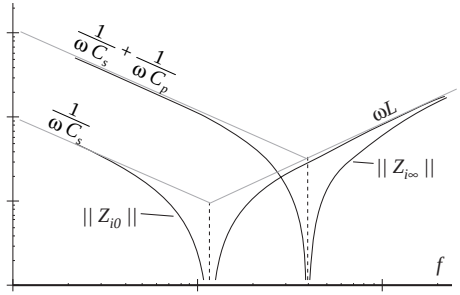


$$Z_{i0}(s) = sL$$

$$Z_{i\infty}(s) = sL + \frac{1}{sC_p}$$

LCC





$$Z_{i0}(s) = sL + \frac{1}{sC_s}$$

$$Z_{i\infty}(s) = sL + \frac{1}{sC_p} + \frac{1}{sC_s}$$

A Theorem relating transistor current variations to load resistance R

Theorem 1: If the tank network is purely reactive, then its input impedance $\| Z_i \|$ is a monotonic function of the load resistance R.

- So as the load resistance R varies from 0 to ∞, the resonant network input impedance $\| Z_i \|$ varies monotonically from the short-circuit value $\| Z_{i0} \|$ to the open-circuit value $\| Z_{i\infty} \|$.
- The impedances $\| Z_{i\infty} \|$ and $\| Z_{i0} \|$ are easy to construct.
- If you want to minimize the circulating tank currents at light load, maximize $\| Z_{i\infty} \|$.
- Note: for many inverters, $\| Z_{i\infty} \| < \| Z_{i0} \|$! The no-load transistor current is therefore greater than the short-circuit transistor current.

Proof of Theorem 1

Previously shown:

$$\| Z_i \|^2 = \| Z_{i0} \|^2 \frac{\left(1 + \frac{R}{\| Z_{o0} \|^2} \right)}{\left(1 + \frac{R}{\| Z_{o\infty} \|^2} \right)}$$

➡ Differentiate:

$$\frac{d \| Z_i \|^2}{d R} = 2 \| Z_{i0} \|^2 \frac{\left(\frac{1}{\| Z_{o0} \|^2} - \frac{1}{\| Z_{o\infty} \|^2} \right) R}{\left(1 + \frac{R^2}{\| Z_{o\infty} \|^2} \right)^2}$$

➡ Derivative has roots at:

(i) $R = 0$

(ii) $R = \infty$

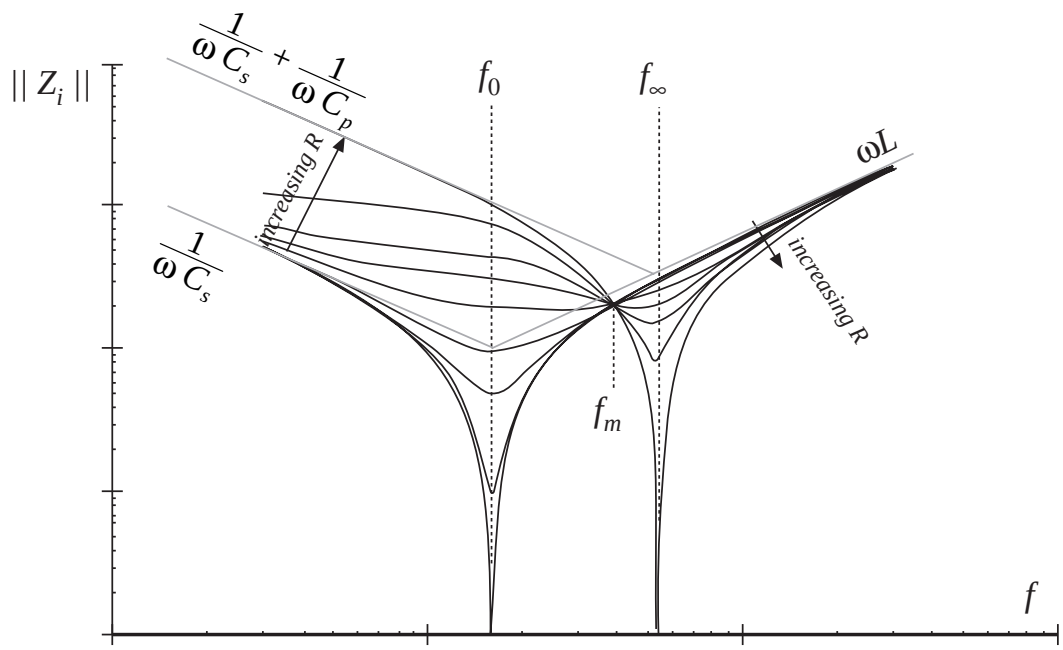
(iii) $\| Z_{o0} \| = \| Z_{o\infty} \|$, *or* $\| Z_{i0} \| = \| Z_{i\infty} \|$

So the resonant network input impedance is a monotonic function of R, over the range 0 < R < ∞.

In the special case $\| Z_{i0} \| = \| Z_{i\infty} \|$, $\| Z_i \|$ is independent of R.

Example: $|| Z_i ||$ of LCC

- for $f < f_m$, $|| Z_i ||$ increases with increasing R .
- for $f > f_m$, $|| Z_i ||$ decreases with increasing R .
- at a given frequency f, $|| Z_i ||$ is a monotonic function of R.
- It's not necessary to draw the entire plot: just construct $|| Z_{i0} ||$ and $|| Z_{i\infty} ||$.



Discussion: LCC

$\| Z_{i0} \|$ and $\| Z_{i\infty} \|$ both represent series resonant impedances, whose Bode diagrams are easily constructed.

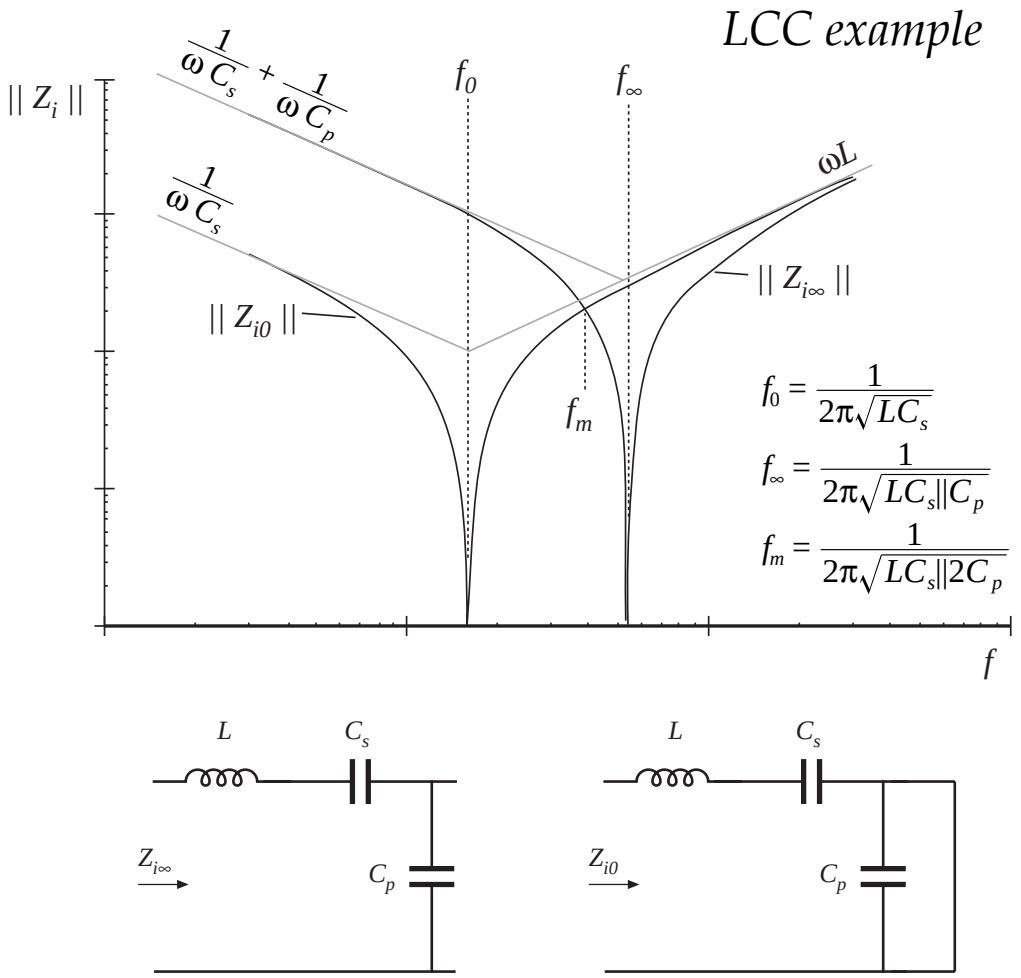
$\| Z_{i0} \|$ and $\| Z_{i\infty} \|$ intersect at frequency f_m.

For $f < f_m$

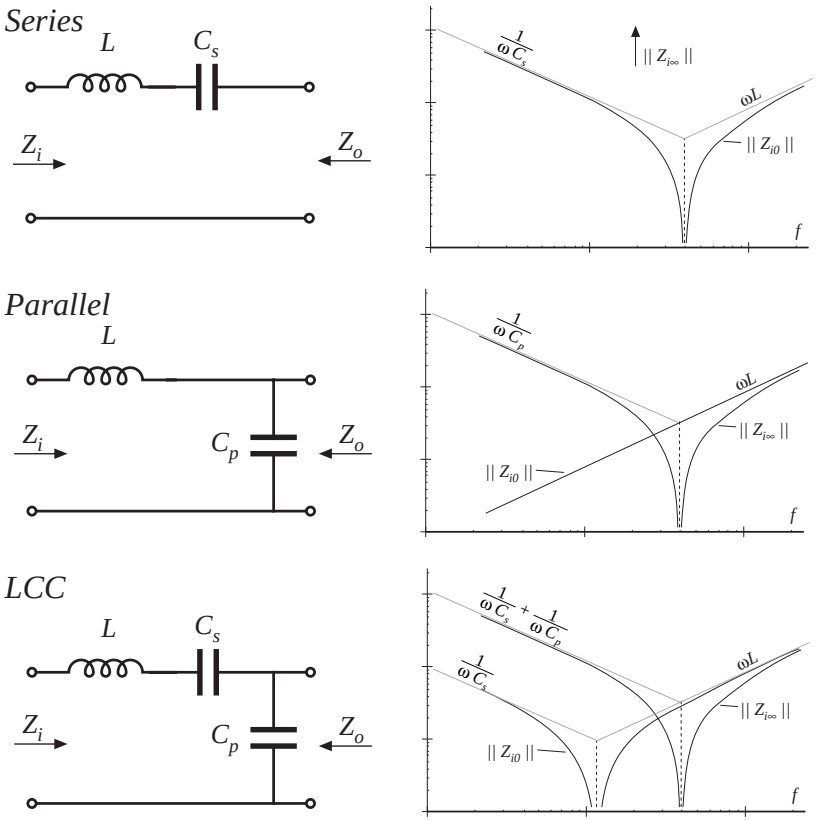
then $\| Z_{i0} \| < \| Z_{i\infty} \|$; hence transistor current decreases as load current decreases

For $f > f_m$

then $\| Z_{i0} \| > \| Z_{i\infty} \|$; hence transistor current increases as load current decreases, and transistor current is greater than or equal to short-circuit current for all R



Discussion -series and parallel



- No-load transistor current = 0, both above and below resonance.
- ZCS below resonance, ZVS above resonance
- Above resonance: no-load transistor current is *greater* than short-circuit transistor current. ZVS.
- Below resonance: no-load transistor current is less than short-circuit current (for $f < f_m$), but determined by $\| Z_{i\infty} \|$. ZCS.

A Theorem relating the ZVS/ZCS boundary to load resistance R

Theorem 2: If the tank network is purely reactive, then the boundary between zero-current switching and zero-voltage switching occurs when the load resistance *R* is equal to the critical value R_{crit}, given by

$$R_{crit} = \| Z_{o0} \| \sqrt{\frac{-Z_{i\infty}}{Z_{i0}}}$$

It is assumed that zero-current switching (ZCS) occurs when the tank input impedance is capacitive in nature, while zero-voltage switching (ZVS) occurs when the tank is inductive in nature. This assumption gives a necessary but not sufficient condition for ZVS when significant semiconductor output capacitance is present.

Proof of Theorem 2

Previously shown:

$$Z_i = Z_{i\infty} \frac{1 + \frac{Z_{o0}}{R}}{1 + \frac{Z_{o\infty}}{R}}$$

If ZCS occurs when Z_i is capacitive, while ZVS occurs when Z_i is inductive, then the boundary is determined by $\angle Z_i = 0$. Hence, the critical load R_{crit} is the resistance which causes the imaginary part of Z_i to be zero:

$$\mathrm{Im}\left(Z_i(R_{crit}) \right) = 0$$

Note that $Z_{i\infty}$, Z_{o0}, and $Z_{o\infty}$ have zero real parts. Hence,

$$\mathrm{Im}\left(Z_i(R_{crit}) \right) = \mathrm{Im}\left(Z_{i\infty} \right) \mathrm{Re}\left(\frac{1 + \frac{Z_{o0}}{R_{crit}}}{1 + \frac{Z_{o\infty}}{R_{crit}}} \right)$$

$$= \mathrm{Im}\left(Z_{i\infty} \right) \mathrm{Re}\left(\frac{1 - \frac{Z_{o0} Z_{o\infty}}{R_{crit}^2}}{1 + \frac{\| Z_{o\infty} \|^2}{R_{crit}^2}} \right)$$

Solution for R_{crit} yields

$$R_{crit} = \| Z_{o0} \| \sqrt{\frac{-Z_{i\infty}}{Z_{i0}}}$$

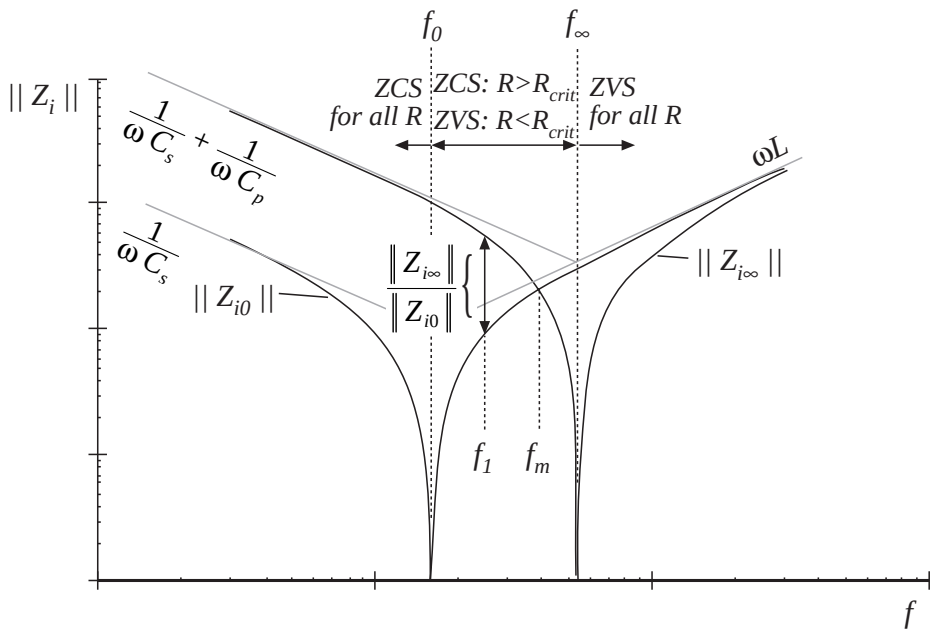
Discussion —Theorem 2

$$R_{crit} = \left\| Z_{o0} \right\| \sqrt{\frac{-Z_{i\infty}}{Z_{i0}}}$$

- Again, $Z_{i\infty}$, Z_{i0}, and Z_{o0} are pure imaginary quantities.
- If $Z_{i\infty}$ and Z_{i0} have the same phase (both inductive or both capacitive), then there is no real solution for R_{crit}.
- Hence, if at a given frequency $Z_{i\infty}$ and Z_{i0} are both capacitive, then ZCS occurs for all loads. If $Z_{i\infty}$ and Z_{i0} are both inductive, then ZVS occurs for all loads.
- If $Z_{i\infty}$ and Z_{i0} have opposite phase (one is capacitive and the other is inductive), then there is a real solution for R_{crit}. The boundary between ZVS and ZCS operation is then given by $R = R_{crit}$.
- Note that $R = \| Z_{o0} \|$ corresponds to operation at matched load with maximum output power. The boundary is expressed in terms of this matched load impedance, and the ratio $Z_{i\infty} / Z_{i0}$.

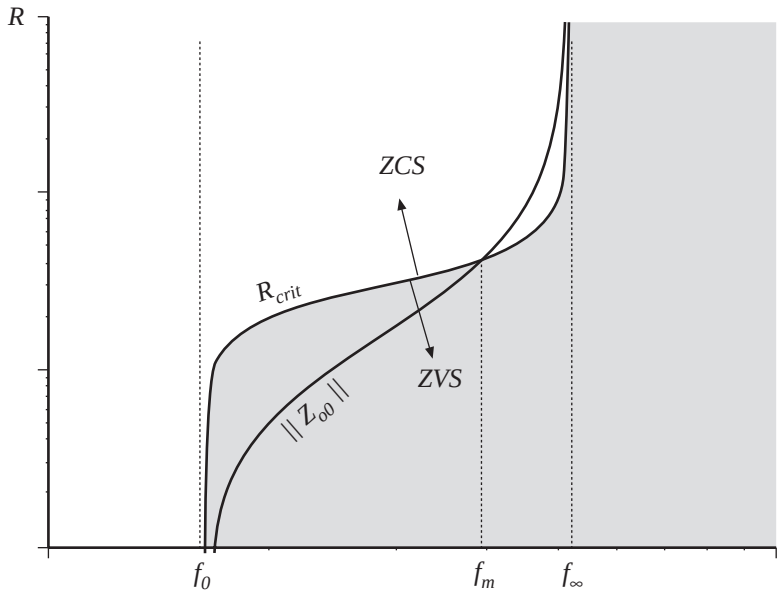
LCC example

- For $f > f_\infty$, ZVS occurs for all R.
- For $f < f_0$, ZCS occurs for all R.
- For $f_0 < f < f_\infty$, ZVS occurs for $R < R_{crit}$, and ZCS occurs for $R > R_{crit}$.
- Note that $R = \| Z_{o0} \|$ corresponds to operation at matched load with maximum output power. The boundary is expressed in terms of this matched load impedance, and the ratio $Z_{i\infty} / Z_{i0}$.

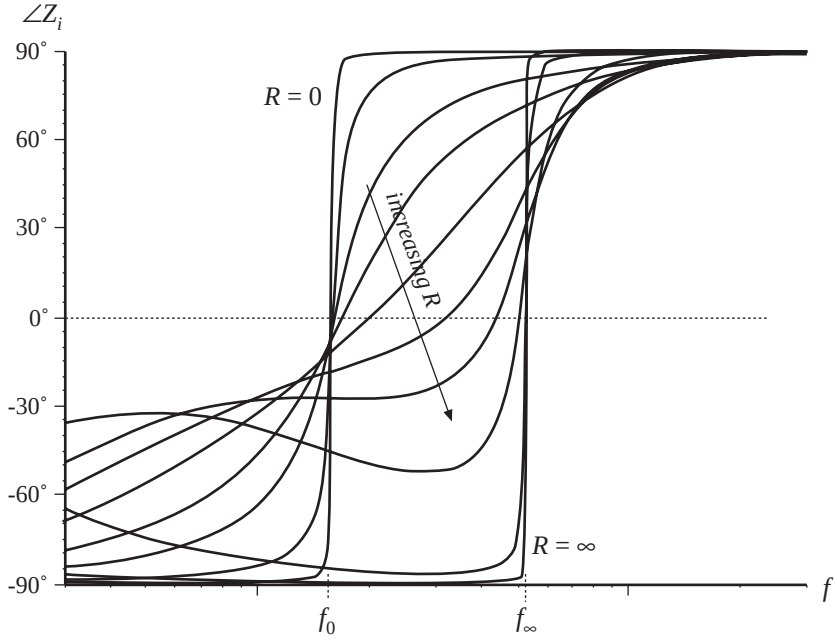


$$R_{crit} = \| Z_{o0} \| \sqrt{\frac{-Z_{i\infty}}{Z_{i0}}}$$

LCC example, continued



Typical dependence of R_{crit} and matched-load impedance $||Z_{o0}||$ on frequency f, LCC example.



Typical dependence of tank input impedance phase vs. load R and frequency, LCC example.

19.6 Summary of Key Points

1. The sinusoidal approximation allows a great deal of insight to be gained into the operation of resonant inverters and dc–dc converters. The voltage conversion ratio of dc–dc resonant converters can be directly related to the tank network transfer function. Other important converter properties, such as the output characteristics, dependence (or lack thereof) of transistor current on load current, and zero-voltage- and zero-current-switching transitions, can also be understood using this approximation. The approximation is accurate provided that the effective Q–factor is sufficiently large, and provided that the switching frequency is sufficiently close to resonance.
2. Simple equivalent circuits are derived, which represent the fundamental components of the tank network waveforms, and the dc components of the dc terminal waveforms.

Summary of key points

3. Exact solutions of the ideal dc–dc series and parallel resonant converters are listed here as well. These solutions correctly predict the conversion ratios, for operation not only in the fundamental continuous conduction mode, but in discontinuous and subharmonic modes as well.
4. Zero-voltage switching mitigates the switching loss caused by diode recovered charge and semiconductor device output capacitances. When the objective is to minimize switching loss and EMI, it is preferable to operate each MOSFET and diode with zero-voltage switching.
5. Zero-current switching leads to natural commutation of SCRs, and can also mitigate the switching loss due to current tailing in IGBTs.

Summary of key points

6. The input impedance magnitude $\| Z_i \|$, and hence also the transistor current magnitude, are monotonic functions of the load resistance R. The dependence of the transistor conduction loss on the load current can be easily understood by simply plotting $\| Z_i \|$ in the limiting cases as $R \to \infty$ and as $R \to 0$, or $\| Z_{i\infty} \|$ and $\| Z_{i0} \|$.
7. The ZVS/ZCS boundary is also a simple function of $Z_{i\infty}$ and Z_{i0}. If ZVS occurs at open-circuit and at short-circuit, then ZVS occurs for all loads. If ZVS occurs at short-circuit, and ZCS occurs at open-circuit, then ZVS is obtained at matched load provided that $\| Z_{i\infty} \| > \| Z_{i0} \|$.
8. The output characteristics of all resonant inverters considered here are elliptical, and are described completely by the open-circuit transfer function magnitude $\| H_\infty \|$, and the output impedance $\| Z_{o0} \|$. These quantities can be chosen to match the output characteristics to the application requirements.

Chapter 20

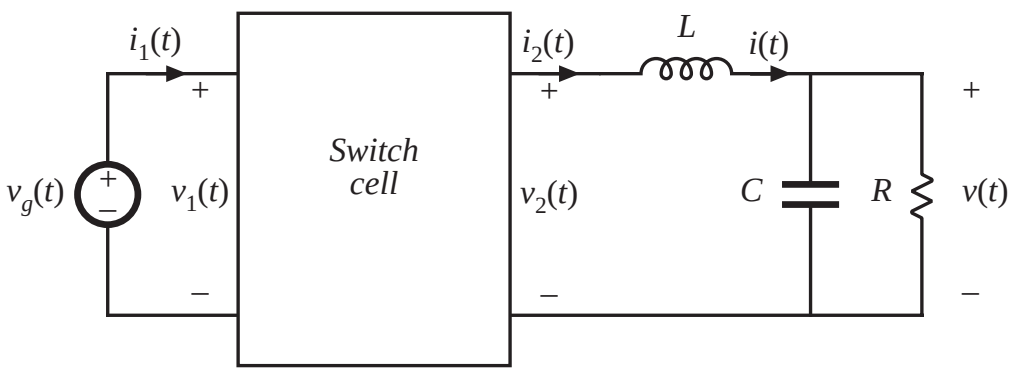
Quasi-Resonant Converters

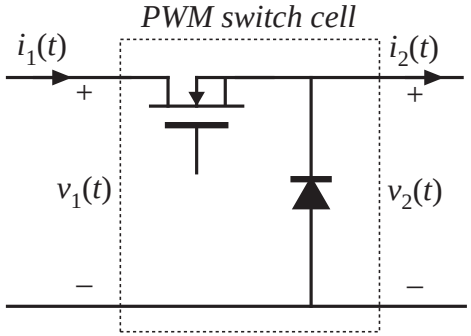
The resonant switch concept

A quite general idea:

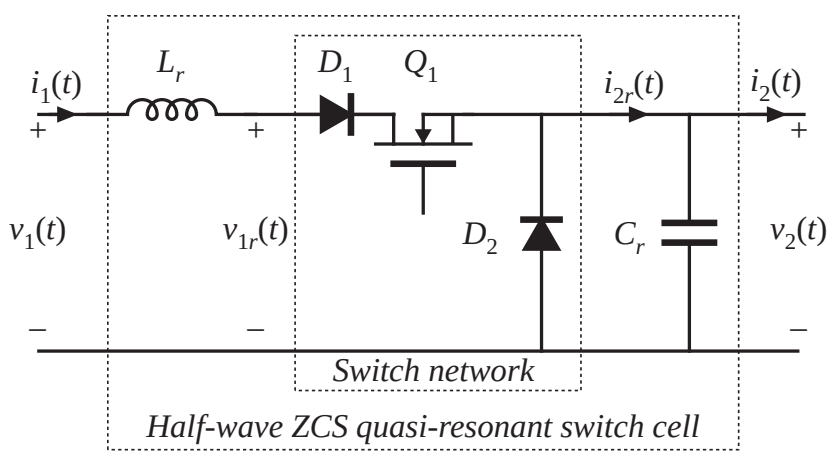
1. PWM switch network is replaced by a resonant switch network
2. This leads to a quasi-resonant version of the original PWM converter

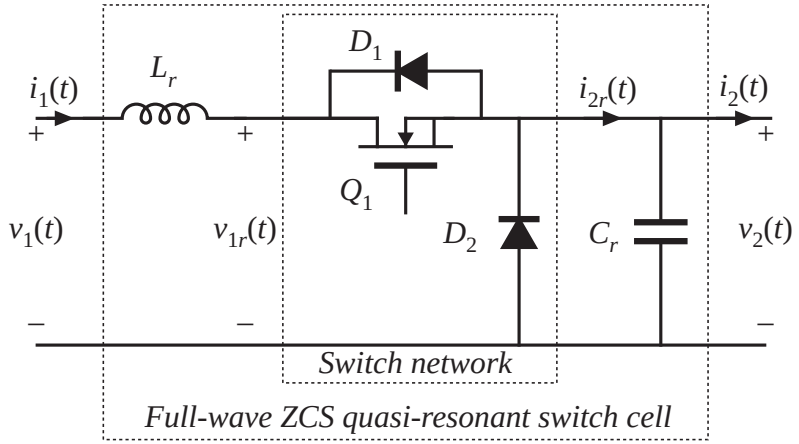
Example: realization of the switch cell in the buck converter



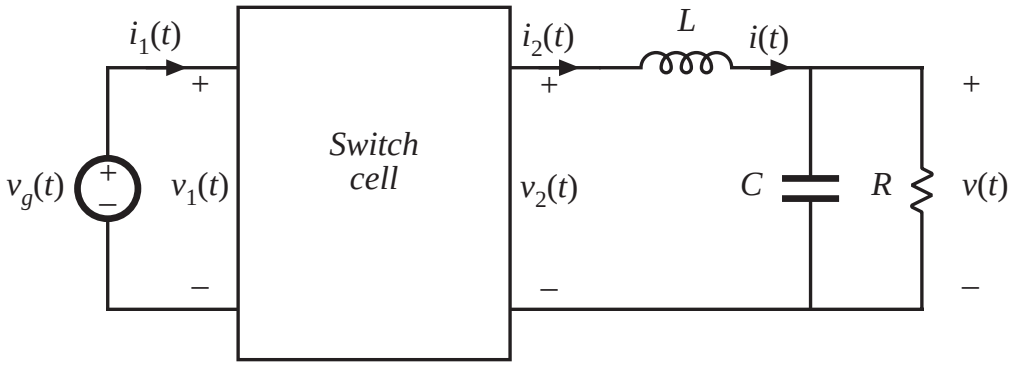


Two quasi-resonant switch cells





Insert either of the above switch cells into the buck converter, to obtain a ZCS quasi-resonant version of the buck converter. L_r and C_r are small in value, and their resonant frequency f_0 is greater than the switching frequency f_s.



$$f_0 = \frac{1}{2\pi\sqrt{L_r C_r}} = \frac{\omega_0}{2\pi}$$

20.1 The zero-current-switching quasi-resonant switch cell

Tank inductor L_r in series with transistor: transistor switches at zero crossings of inductor current waveform

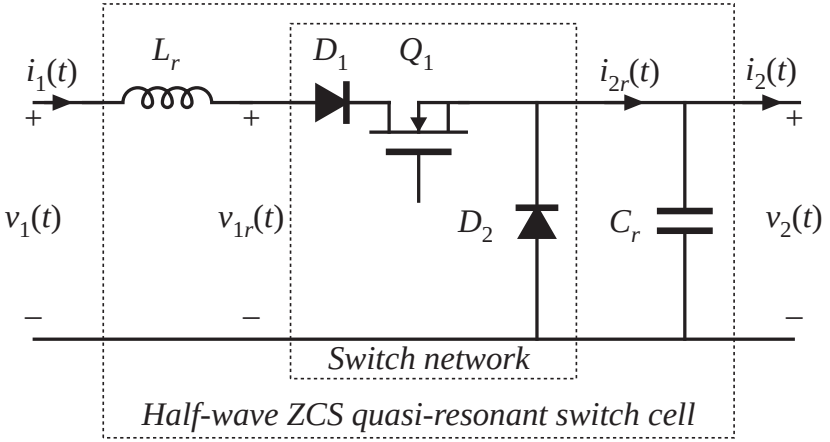
Tank capacitor C_r in parallel with diode D_2 : diode switches at zero crossings of capacitor voltage waveform

Two-quadrant switch is required:

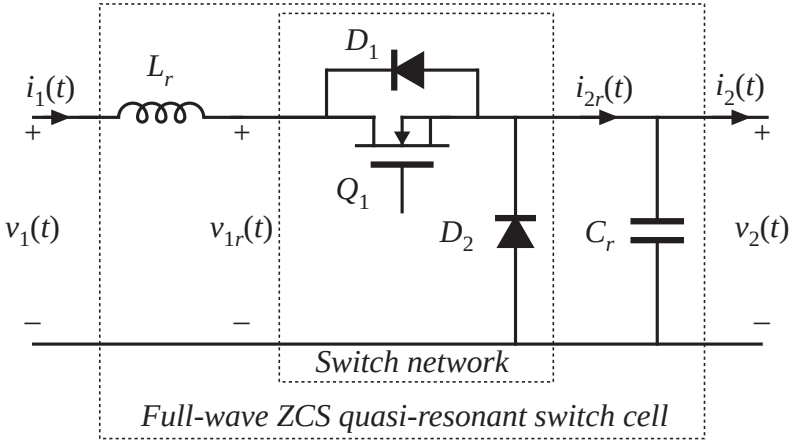
Half-wave: Q_1 and D_1 in series, transistor turns off at first zero crossing of current waveform

Full-wave: Q_1 and D_1 in parallel, transistor turns off at second zero crossing of current waveform

Performances of half-wave and full-wave cells differ significantly.



Half-wave ZCS quasi-resonant switch cell



Full-wave ZCS quasi-resonant switch cell

Averaged switch modeling of ZCS cells

It is assumed that the converter filter elements are large, such that their switching ripples are small. Hence, we can make the small ripple approximation as usual, for these elements:

$$i_2(t) \approx \left\langle i_2(t) \right\rangle_{T_s}$$

$$v_1(t) \approx \left\langle v_1(t) \right\rangle_{T_s}$$

In steady state, we can further approximate these quantities by their dc values:

$$i_2(t) \approx I_2$$

$$v_1(t) \approx V_1$$

Modeling objective: find the average values of the terminal waveforms

$\langle v_2(t) \rangle_{T_s}$ and $\langle i_1(t) \rangle_{T_s}$

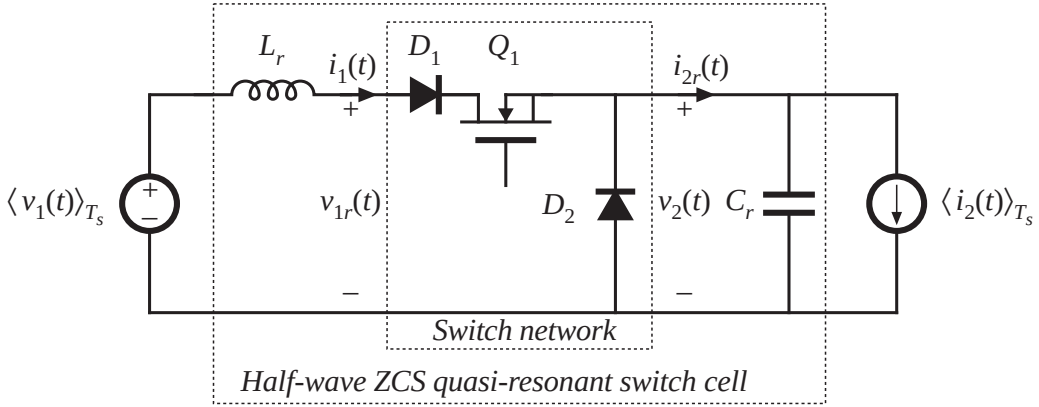
The switch conversion ratio μ

A generalization of the duty cycle $d(t)$

The switch conversion ratio μ is the ratio of the average terminal voltages of the switch network. It can be applied to non-PWM switch networks. For the CCM PWM case, $\mu = d$.

If $V/V_g = M(d)$ for a PWM CCM converter, then $V/V_g = M(\mu)$ for the same converter with a switch network having conversion ratio μ.

Generalized switch averaging, and μ, are defined and discussed in Section 10.3.



$$i_2(t) \approx \left\langle i_2(t) \right\rangle_{T_s} \qquad \mu = \frac{\left\langle v_2(t) \right\rangle_{T_s}}{\left\langle v_{1r}(t) \right\rangle_{T_s}} = \frac{\left\langle i_1(t) \right\rangle_{T_s}}{\left\langle i_{2r}(t) \right\rangle_{T_s}}$$

$$v_1(t) \approx \left\langle v_1(t) \right\rangle_{T_s}$$

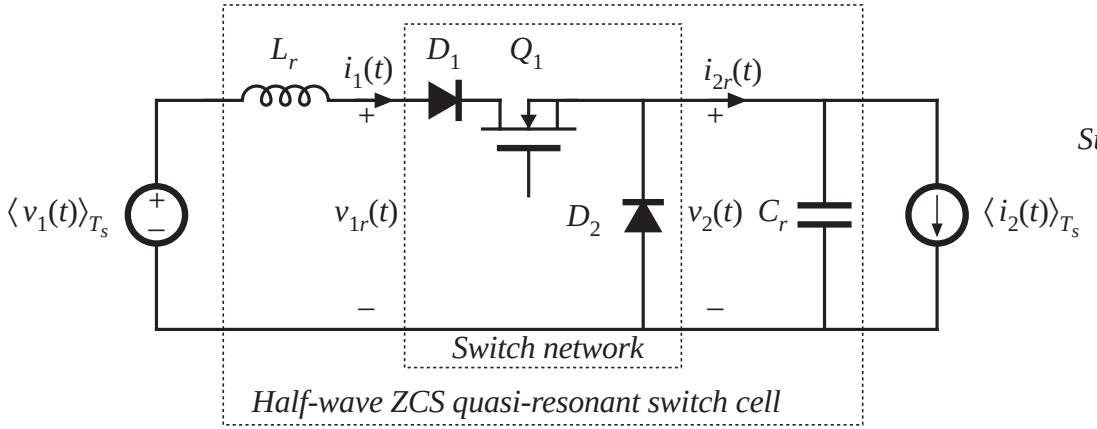
In steady state:

$$i_2(t) \approx I_2 \qquad \mu = \frac{V_2}{V_1} = \frac{I_1}{I_2}$$

$$v_1(t) \approx V_1$$

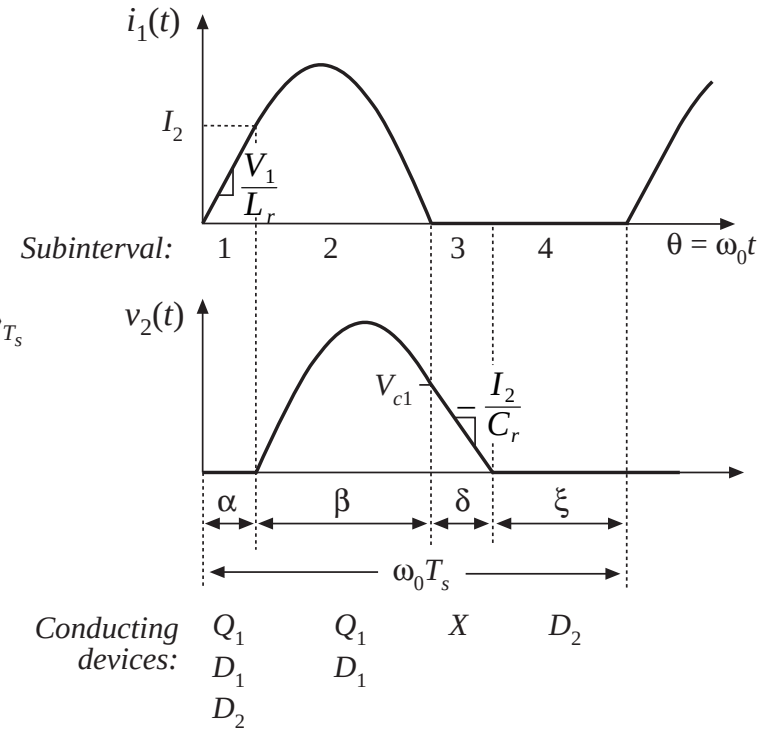
20.1.1 Waveforms of the half-wave ZCS quasi-resonant switch cell

The half-wave ZCS quasi-resonant switch cell, driven by the terminal quantities $\langle v_1(t) \rangle_{Ts}$ and $\langle i_2(t) \rangle_{Ts}$.



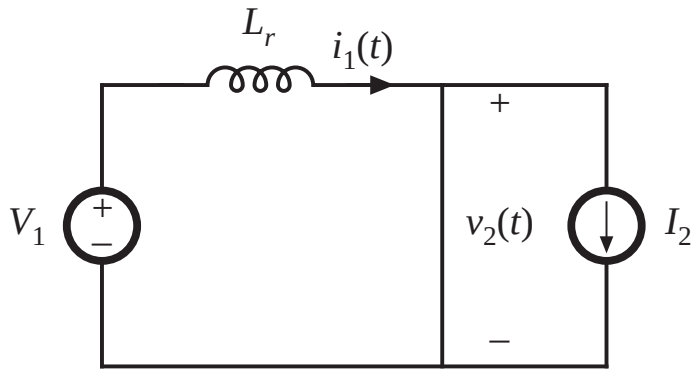
Each switching period contains four subintervals

Waveforms:



Subinterval 1

Diode D_2 is initially conducting the filter inductor current I_2. Transistor Q_1 turns on, and the tank inductor current i_1 starts to increase. So all semiconductor devices conduct during this subinterval, and the circuit reduces to:



Circuit equations:

$$\frac{di_1(t)}{dt} = \frac{V_1}{L_r} \qquad \text{with } i_1(0) = 0$$

Solution: $$i_1(t) = \frac{V_1}{L_r}\, t = \omega_0 t\, \frac{V_1}{R_0}$$

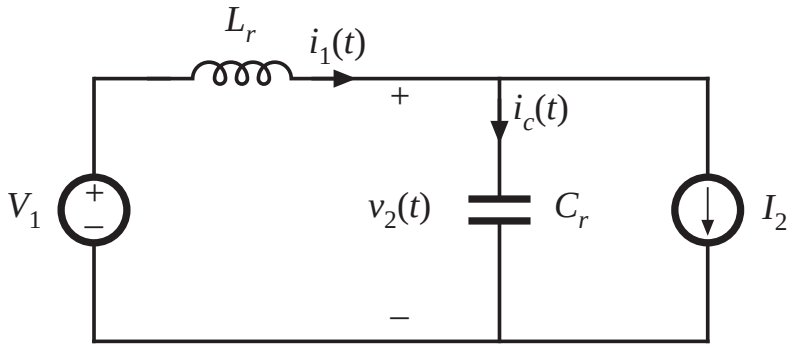
where $$R_0 = \sqrt{\frac{L_r}{C_r}}$$

This subinterval ends when diode D_2 becomes reverse-biased. This occurs at time $\omega_0 t = \alpha$, when $i_1(t) = I_2$.

$$i_1(\alpha) = \alpha\, \frac{V_1}{R_0} = I_2 \qquad \alpha = \frac{I_2 R_0}{V_1}$$

Subinterval 2

Diode D_2 is off. Transistor Q_1 conducts, and the tank inductor and tank capacitor ring sinusoidally. The circuit reduces to:



The circuit equations are

$$L_r \frac{di_1(\omega_0 t)}{dt} = V_1 - v_2(\omega_0 t)$$

$$C_r \frac{dv_2(\omega_0 t)}{dt} = i_1(\omega_0 t) - I_2$$

$$v_2(\alpha) = 0$$

$$i_1(\alpha) = I_2$$

The solution is

$$i_1(\omega_0 t) = I_2 + \frac{V_1}{R_0} \sin\left(\omega_0 t - \alpha\right)$$

$$v_2(\omega_0 t) = V_1 \left(1 - \cos\left(\omega_0 t - \alpha\right)\right)$$

The dc components of these waveforms are the dc solution of the circuit, while the sinusoidal components have magnitudes that depend on the initial conditions and on the characteristic impedance R_0.

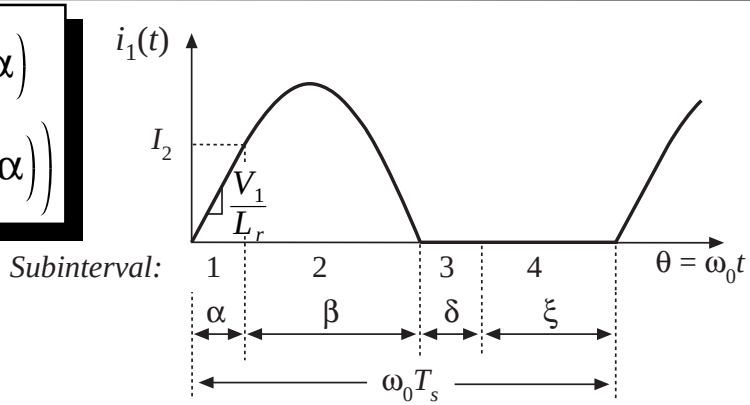
Subinterval 2
continued

Peak inductor current:

$$I_{1pk} = I_2 + \frac{V_1}{R_0}$$

$$i_1(\omega_0 t) = I_2 + \frac{V_1}{R_0} \sin\left(\omega_0 t - \alpha\right)$$

$$v_2(\omega_0 t) = V_1 \left(1 - \cos\left(\omega_0 t - \alpha\right)\right)$$



This subinterval ends at the first zero crossing of $i_1(t)$. Define β = angular length of subinterval 2. Then

$$i_1(\alpha + \beta) = I_2 + \frac{V_1}{R_0} \sin\left(\beta\right) = 0$$

$$\sin\left(\beta\right) = -\frac{I_2 R_0}{V_1}$$

Must use care to select the correct branch of the arcsine function. Note (from the $i_1(t)$ waveform) that $\beta > \pi$.

Hence

$$\beta = \pi + \sin^{-1}\left(\frac{I_2 R_0}{V_1}\right)$$

$$-\frac{\pi}{2} < \sin^{-1}\left(x\right) \leq \frac{\pi}{2}$$

$$I_2 < \frac{V_1}{R_0}$$

Boundary of zero current switching

If the requirement

$$I_2 < \frac{V_1}{R_0}$$

is violated, then the inductor current never reaches zero. In consequence, the transistor cannot switch off at zero current.

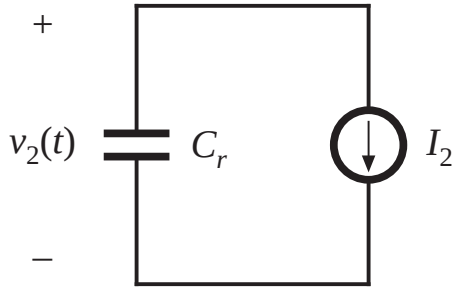
The resonant switch operates with zero current switching only for load currents less than the above value. The characteristic impedance must be sufficiently small, so that the ringing component of the current is greater than the dc load current.

Capacitor voltage at the end of subinterval 2 is

$$v_2(\alpha + \beta) = V_{c1} = V_1 \left(1 + \sqrt{1 - \left(\frac{I_2 R_0}{V_1} \right)^2} \right)$$

Subinterval 3

All semiconductor devices are off. The circuit reduces to:



The circuit equations are

$$C_r \frac{dv_2(\omega_0 t)}{dt} = -I_2$$

$$v_2(\alpha + \beta) = V_{c1}$$

The solution is

$$v_2(\omega_0 t) = V_{c1} - I_2 R_0 \left(\omega_0 t - \alpha - \beta\right)$$

Subinterval 3 ends when the tank capacitor voltage reaches zero, and diode D_2 becomes forward-biased. Define δ = angular length of subinterval 3. Then

$$v_2(\alpha + \beta + \delta) = V_{c1} - I_2 R_0 \delta = 0$$

$$\delta = \frac{V_{c1}}{I_2 R_0} = \frac{V_1}{I_2 R_0}\left(1 - \sqrt{1 - \left(\frac{I_2 R_0}{V_1}\right)^2}\right)$$

Subinterval 4

Subinterval 4, of angular length ξ, is identical to the diode conduction interval of the conventional PWM switch network.

Diode D_2 conducts the filter inductor current I_2

The tank capacitor voltage $v_2(t)$ is equal to zero.

Transistor Q_1 is off, and the input current $i_1(t)$ is equal to zero.

The length of subinterval 4 can be used as a control variable. Increasing the length of this interval reduces the average output voltage.

Maximum switching frequency

The length of the fourth subinterval cannot be negative, and the switching period must be at least long enough for the tank current and voltage to return to zero by the end of the switching period.

The angular length of the switching period is

$$\omega_0 T_s = \alpha + \beta + \delta + \xi = \frac{2\pi f_0}{f_s} = \frac{2\pi}{F}$$

where the normalized switching frequency F is defined as

$$F = \frac{f_s}{f_0}$$

So the minimum switching period is

$$\omega_0 T_s \geq \alpha + \beta + \delta$$

Substitute previous solutions for subinterval lengths:

$$\frac{2\pi}{F} \geq \frac{I_2 R_0}{V_1} + \pi + \sin^{-1}\left(\frac{I_2 R_0}{V_1}\right) + \frac{V_1}{I_2 R_0}\left(1 - \sqrt{1 - \left(\frac{I_2 R_0}{V_1}\right)^2}\right)$$

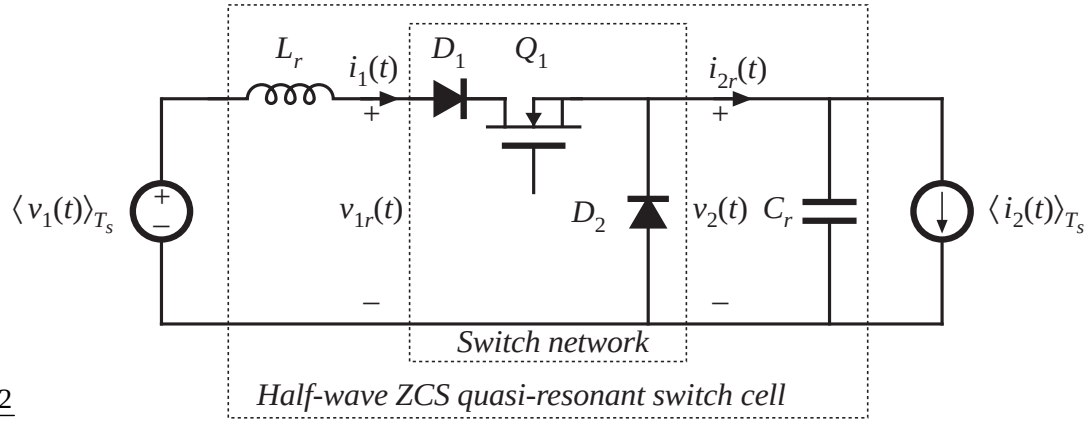
20.1.2 The average terminal waveforms

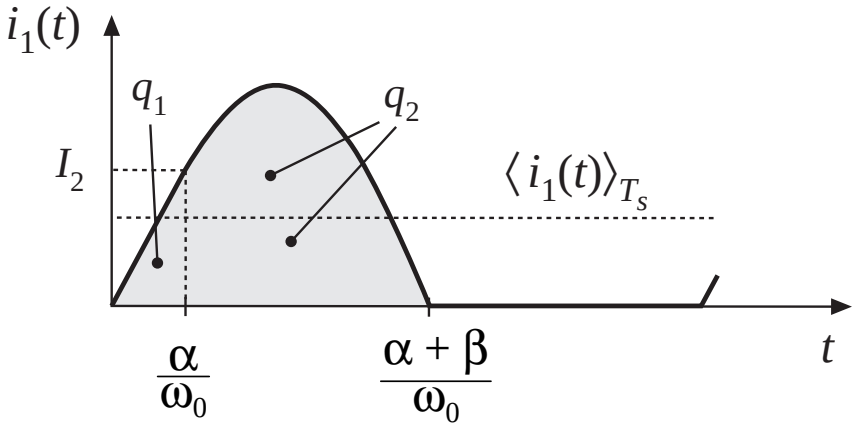
Averaged switch modeling: we need to determine the average values of $i_1(t)$ and $v_2(t)$. The average switch input current is given by

$$\left\langle i_1(t) \right\rangle_{T_s} = \frac{1}{T_s} \int_t^{t+T_s} i_1(t)\,dt = \frac{q_1 + q_2}{T_s}$$

q_1 and q_2 are the areas under the current waveform during subintervals 1 and 2. q_1 is given by the triangle area formula:

$$q_1 = \int_0^{\frac{\alpha}{\omega_0}} i_1(t)\,dt = \frac{1}{2}\left(\frac{\alpha}{\omega_0}\right)\left(I_2\right)$$





Charge arguments: computation of q_2

$$q_2 = \int_{\frac{\alpha}{\omega_0}}^{\frac{\alpha+\beta}{\omega_0}} i_1(t)\,dt$$

Node equation for subinterval 2:

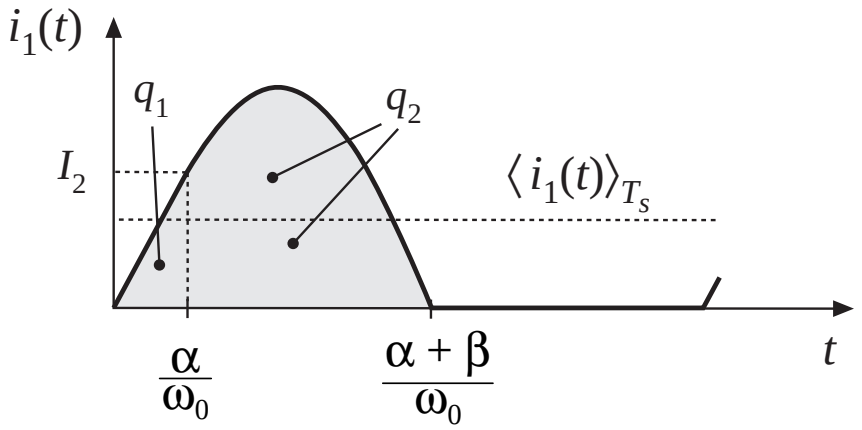
$$i_1(t) = i_C(t) + I_2$$

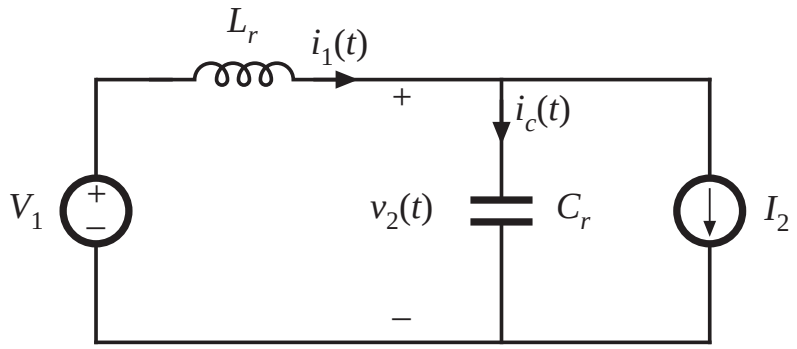
Substitute:

$$q_2 = \int_{\frac{\alpha}{\omega_0}}^{\frac{\alpha+\beta}{\omega_0}} i_C(t)\,dt \; + \; \int_{\frac{\alpha}{\omega_0}}^{\frac{\alpha+\beta}{\omega_0}} I_2\,dt$$

Second term is integral of constant I_2:

$$\int_{\frac{\alpha}{\omega_0}}^{\frac{\alpha+\beta}{\omega_0}} I_2\,dt \; = \; I_2 \, \frac{\beta}{\omega_0}$$





Circuit during subinterval 2

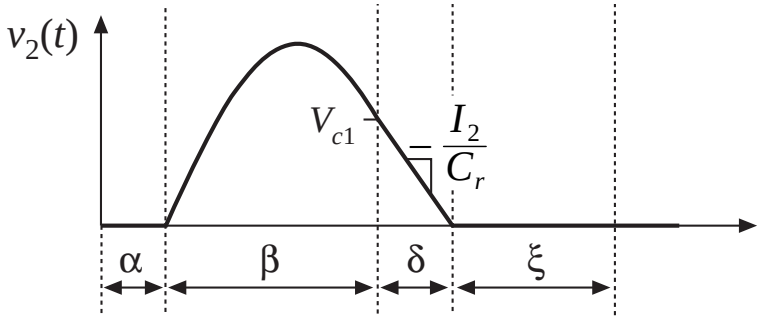
Charge arguments
continued

$$q_2 = \int_{\frac{\alpha}{\omega_0}}^{\frac{\alpha+\beta}{\omega_0}} i_C(t)dt \; + \; \int_{\frac{\alpha}{\omega_0}}^{\frac{\alpha+\beta}{\omega_0}} I_2 dt$$

First term: integral of the capacitor current over subinterval 2. This can be related to the change in capacitor voltage :

$$\int_{\frac{\alpha}{\omega_0}}^{\frac{\alpha+\beta}{\omega_0}} i_C(t)dt \; = \; C\left(v_2\left(\frac{\alpha+\beta}{\omega_0}\right) - v_2\left(\frac{\alpha}{\omega_0}\right)\right)$$

$$\int_{\frac{\alpha}{\omega_0}}^{\frac{\alpha+\beta}{\omega_0}} i_C(t)dt \; = \; C\left(V_{c1} - 0\right) = CV_{c1}$$



Substitute results for the two integrals:

$$q_2 = CV_{c1} + I_2 \frac{\beta}{\omega_0}$$

Substitute into expression for average switch input current:

$$\left\langle i_1(t)\right\rangle_{T_s} = \frac{\alpha I_2}{2\omega_0 T_s} + \frac{CV_{c1}}{T_s} + \frac{\beta I_2}{\omega_0 T_s}$$

Switch conversion ratio μ

$$\mu = \frac{\left\langle i_1(t) \right\rangle_{T_s}}{I_2} = \frac{\alpha}{2\omega_0 T_s} + \frac{CV_{c1}}{I_2 T_s} + \frac{\beta}{\omega_0 T_s}$$

Eliminate α, β, V_{c1} using previous results:

$$\mu = F \frac{1}{2\pi} \left[\frac{1}{2} J_s + \pi + \sin^{-1}(J_s) + \frac{1}{J_s} \left(1 + \sqrt{1 - J_s^2} \right) \right]$$

where

$$J_s = \frac{I_2 R_0}{V_1}$$

Analysis result: switch conversion ratio μ

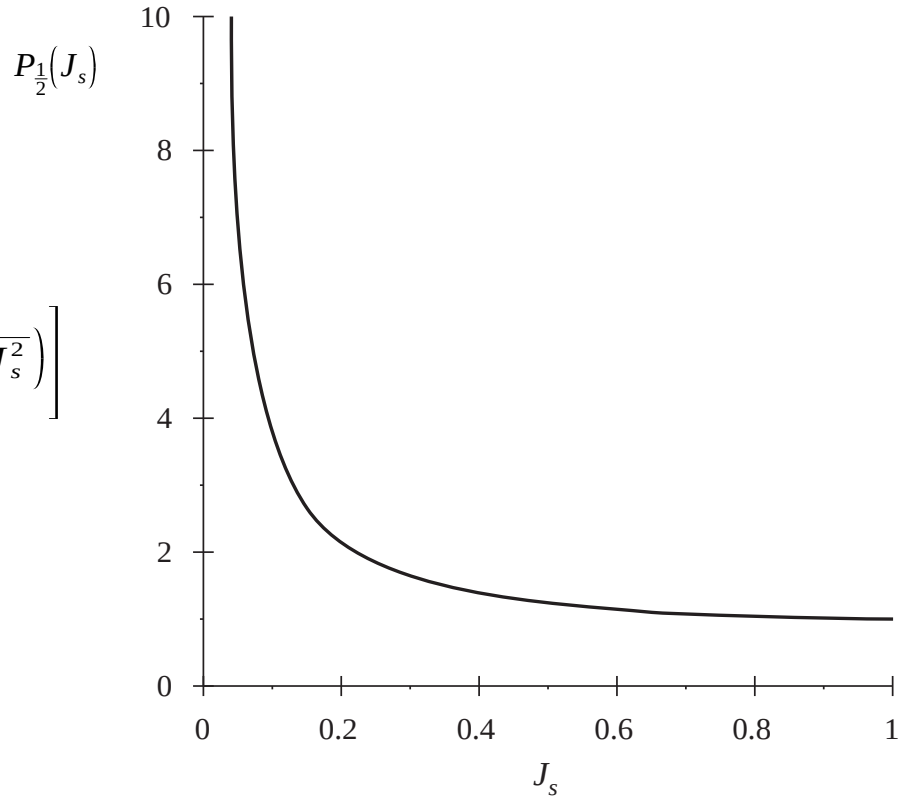
Switch conversion ratio: $$\mu = F \frac{1}{2\pi} \left[\frac{1}{2} J_s + \pi + \sin^{-1}(J_s) + \frac{1}{J_s} \left(1 + \sqrt{1 - J_s^2} \right) \right]$$

with $$J_s = \frac{I_2 R_0}{V_1}$$

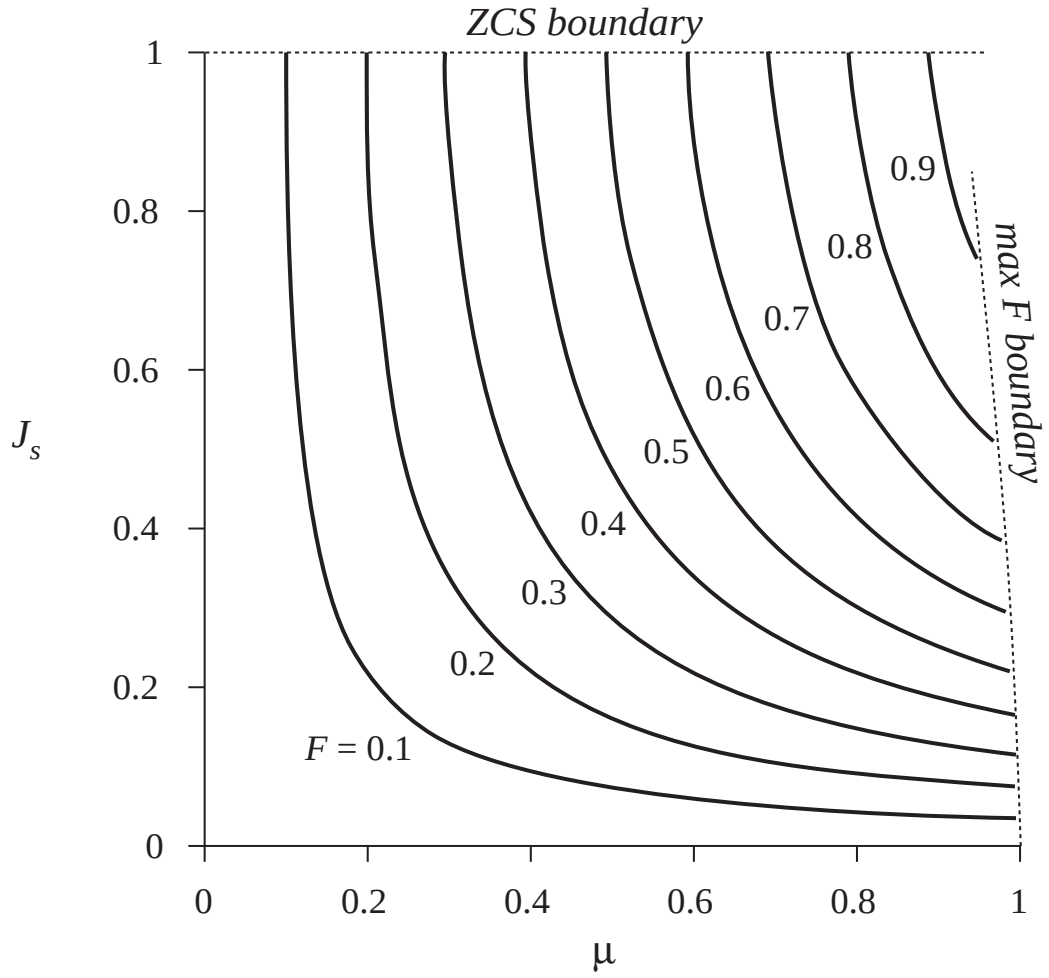
This is of the form

$$\mu = F P_{\frac{1}{2}}\left(J_s\right)$$

$$P_{\frac{1}{2}}\left(J_s\right) = \frac{1}{2\pi} \left[\frac{1}{2} J_s + \pi + \sin^{-1}(J_s) + \frac{1}{J_s} \left(1 + \sqrt{1 - J_s^2} \right) \right]$$



Characteristics of the half-wave ZCS resonant switch



Switch characteristics:

$$\mu = F P_{\frac{1}{2}}\left(J_s\right)$$

Mode boundary:

$$J_s \leq 1$$

$$\mu \leq 1 - \frac{J_s F}{4\pi}$$

Buck converter containing half-wave ZCS quasi-resonant switch

Conversion ratio of the buck converter is (from inductor volt-second balance):

$$M = \frac{V}{V_g} = \mu$$

For the buck converter,

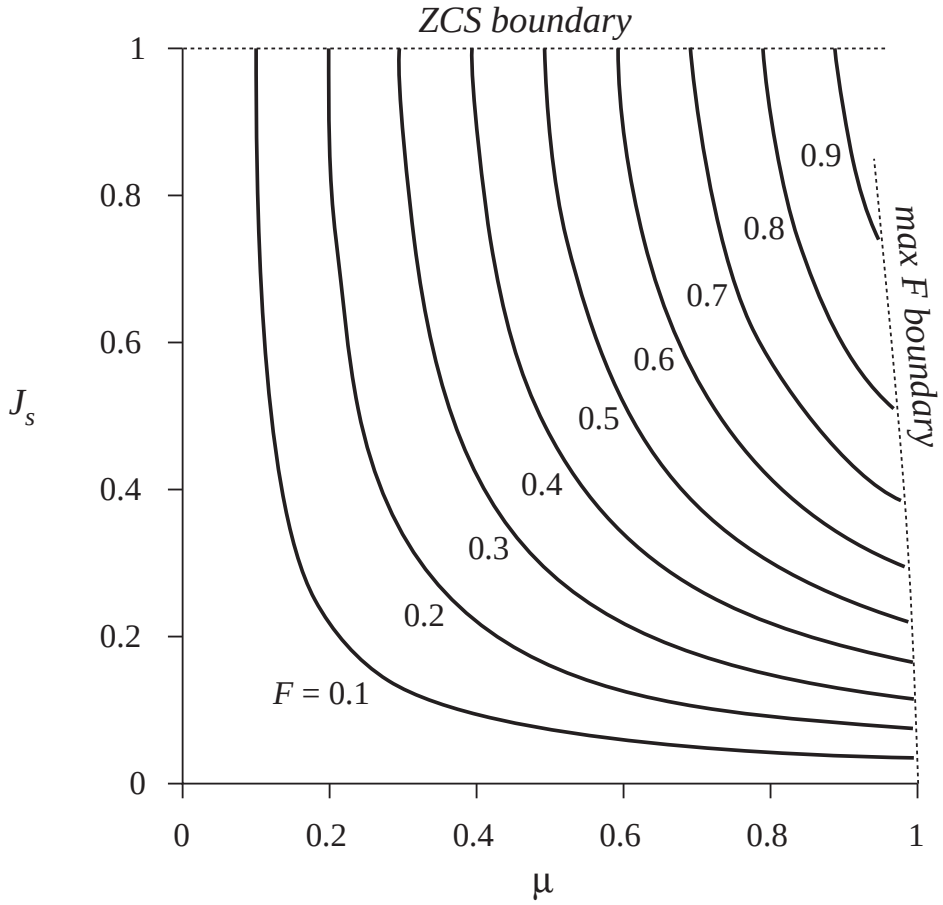
$$J_s = \frac{IR_0}{V_g}$$

ZCS occurs when

$$I \le \frac{V_g}{R_0}$$

Output voltage varies over the range

$$0 \le V \le V_g - \frac{FIR_0}{4\pi}$$



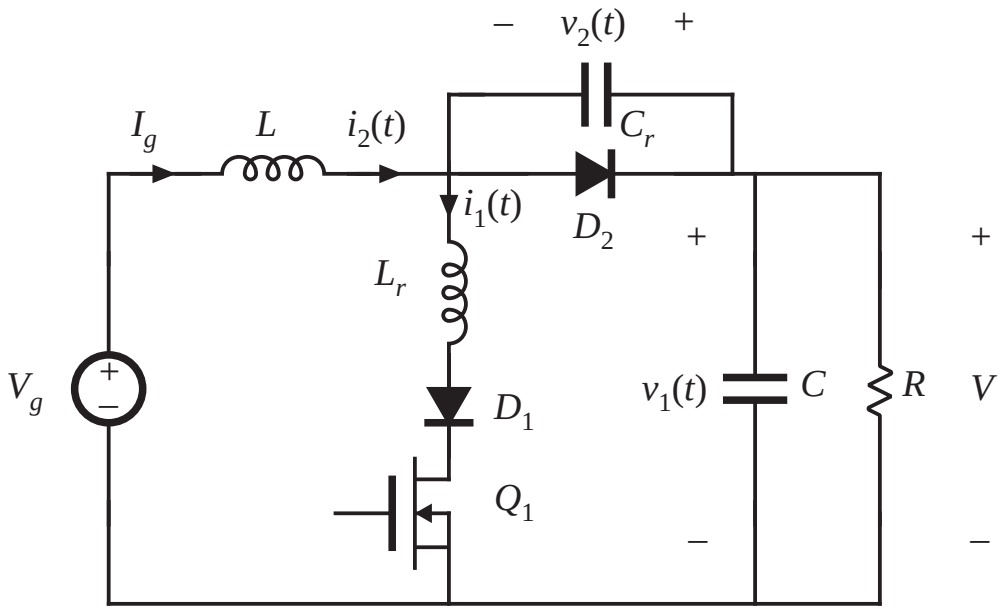
Boost converter example

For the boost converter,

$$M = \frac{V}{V_g} = \frac{1}{1-\mu}$$

$$J_s = \frac{I_2 R_0}{V_1} = \frac{I_g R_0}{V}$$

$$I_g = \frac{I}{1-\mu}$$



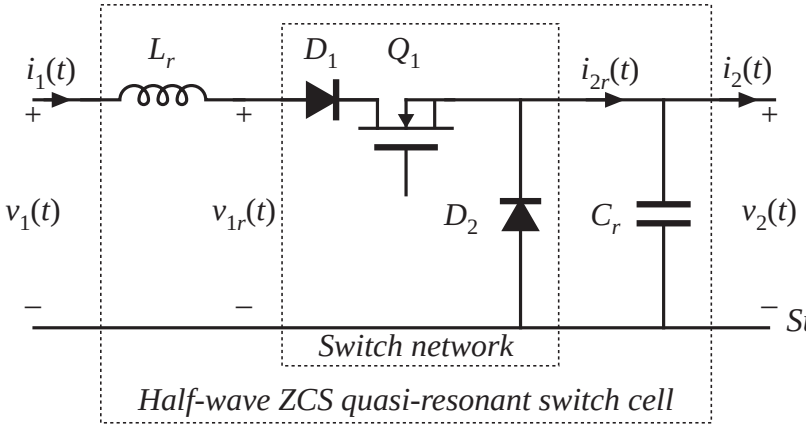
Half-wave ZCS equations:

$$\mu = F P_{\frac{1}{2}}(J_s)$$

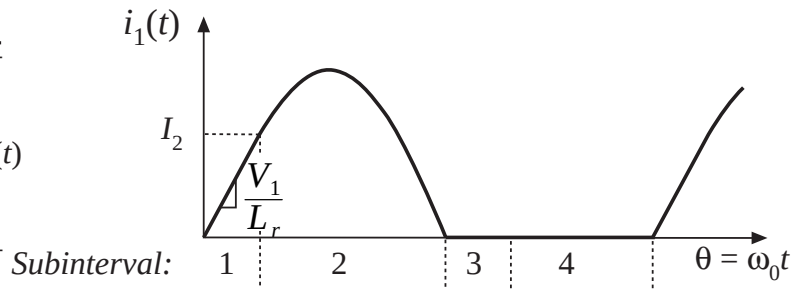
$$P_{\frac{1}{2}}(J_s) = \frac{1}{2\pi}\left|\frac{1}{2}J_s + \pi + \sin^{-1}(J_s) + \frac{1}{J_s}\left(1+\sqrt{1-J_s^2}\right)\right|$$

20.1.3 The full-wave ZCS quasi-resonant switch cell

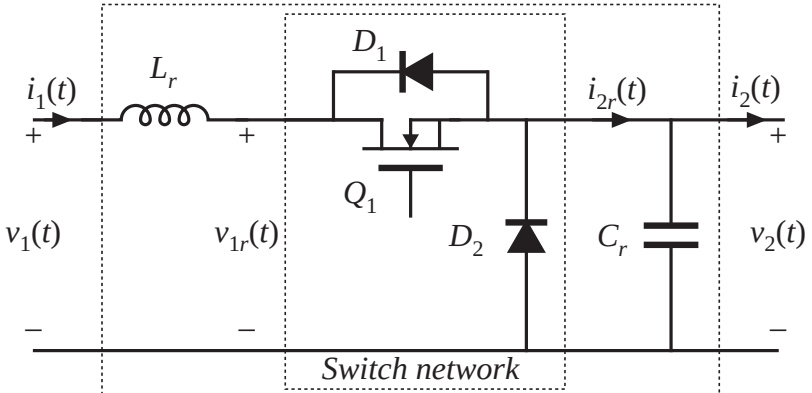
Half wave



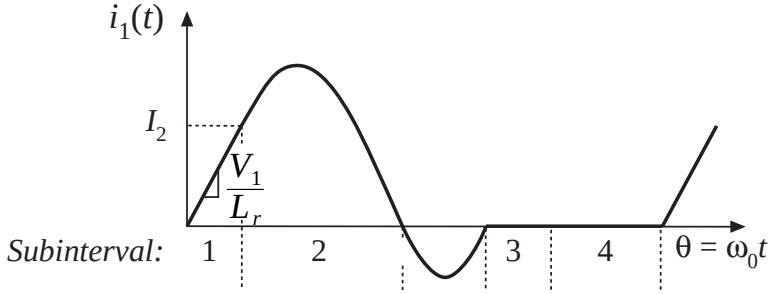
Half-wave ZCS quasi-resonant switch cell



Full wave



Full-wave ZCS quasi-resonant switch cell



Analysis: full-wave ZCS

Analysis in the full-wave case is nearly the same as in the half-wave case. The second subinterval ends at the second zero crossing of the tank inductor current waveform. The following quantities differ:

$$\beta = \begin{cases} \pi + \sin^{-1}\left(J_s\right) & \text{(half wave)} \\ 2\pi - \sin^{-1}\left(J_s\right) & \text{(full wave)} \end{cases}$$

$$V_{c1} = \begin{cases} V_1\left(1 + \sqrt{1 - J_s^2}\right) & \text{(half wave)} \\ V_1\left(1 - \sqrt{1 - J_s^2}\right) & \text{(full wave)} \end{cases}$$

In either case, μ is given by

$$\mu = \frac{\left\langle i_1(t) \right\rangle_{T_s}}{I_2} = \frac{\alpha}{2\omega_0 T_s} + \frac{CV_{c1}}{I_2 T_s} + \frac{\beta}{\omega_0 T_s}$$

Full-wave cell: switch conversion ratio μ

$$P_1(J_s) = \frac{1}{2\pi}\left|\frac{1}{2}J_s + 2\pi - \sin^{-1}(J_s) + \frac{1}{J_s}\left(1 - \sqrt{1 - J_s^2}\right)\right|$$

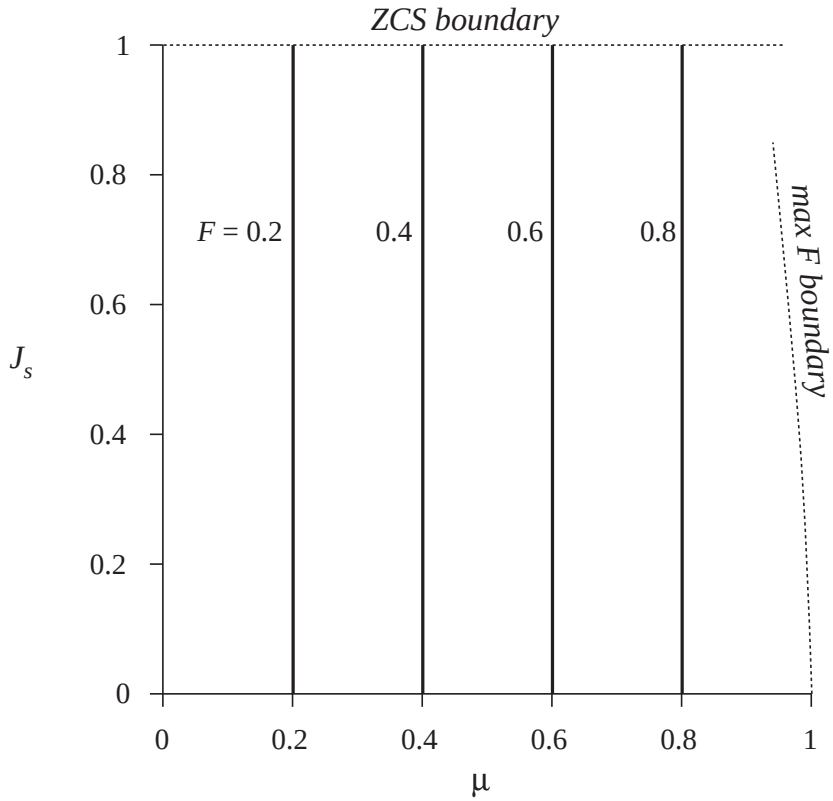
$$\mu = F P_1(J_s)$$

Full-wave case: P_1 can be approximated as

$$P_1(J_s) \approx 1$$

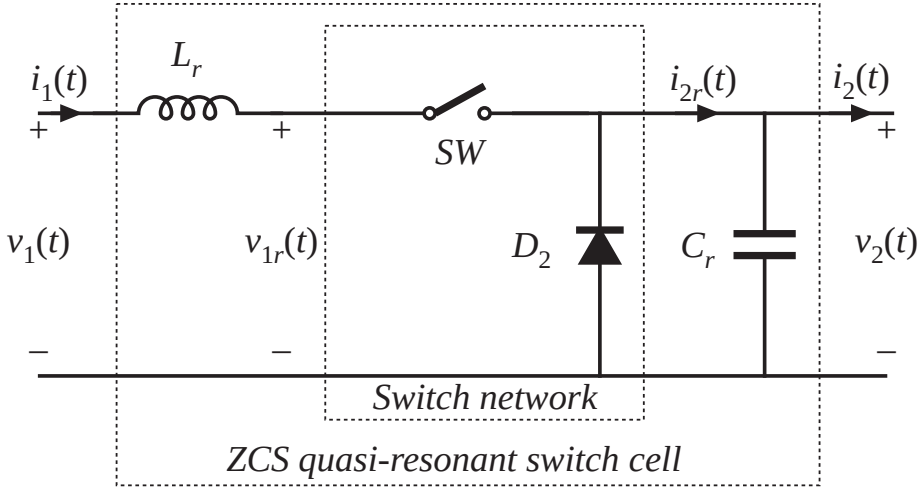
so

$$\mu \approx F = \frac{f_s}{f_0}$$



20.2 Resonant switch topologies

Basic ZCS switch cell:



SPST switch *SW*:

- Voltage-bidirectional two-quadrant switch for half-wave cell
- Current-bidirectional two-quadrant switch for full-wave cell

Connection of resonant elements:

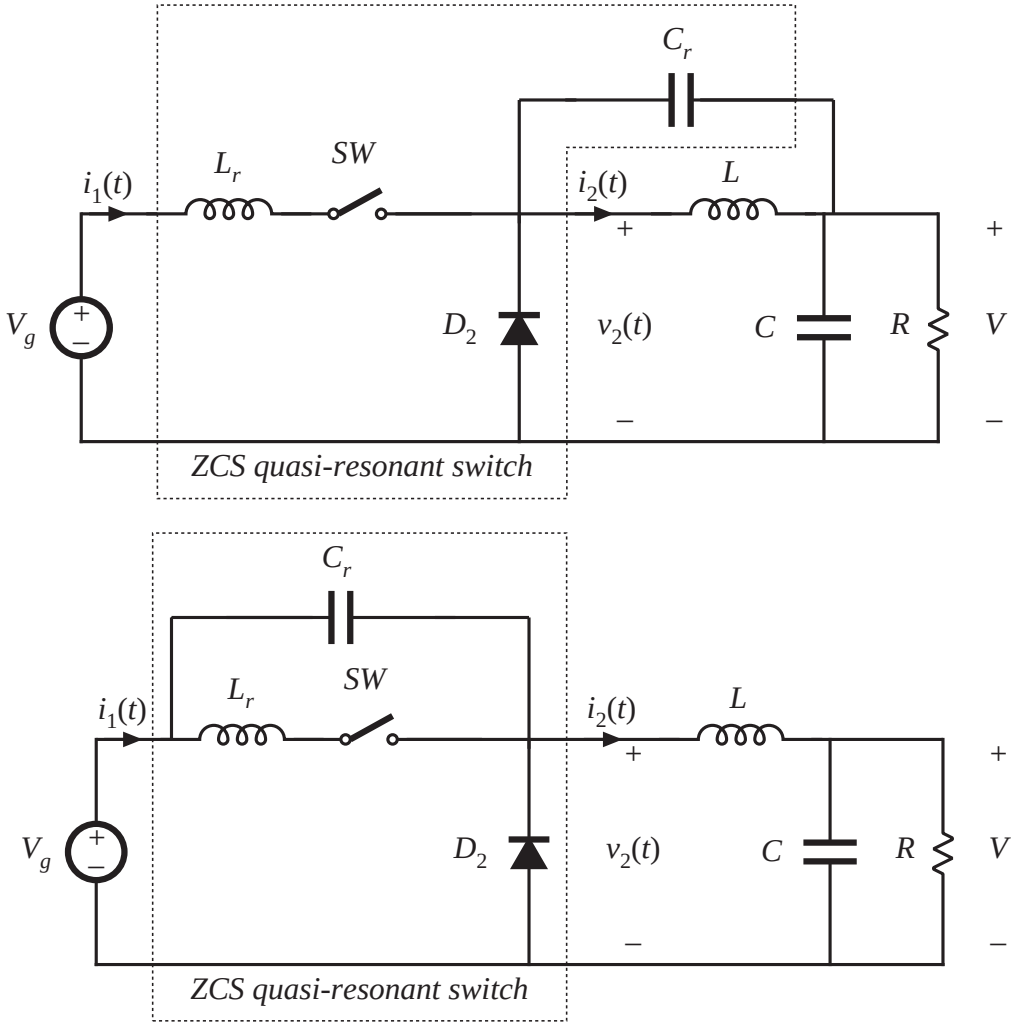
Can be connected in other ways that preserve high-frequency components of tank waveforms

Connection of tank capacitor

Connection of tank capacitor to two other points at ac ground.

This simply changes the dc component of tank capacitor voltage.

The ac high-frequency components of the tank waveforms are unchanged.



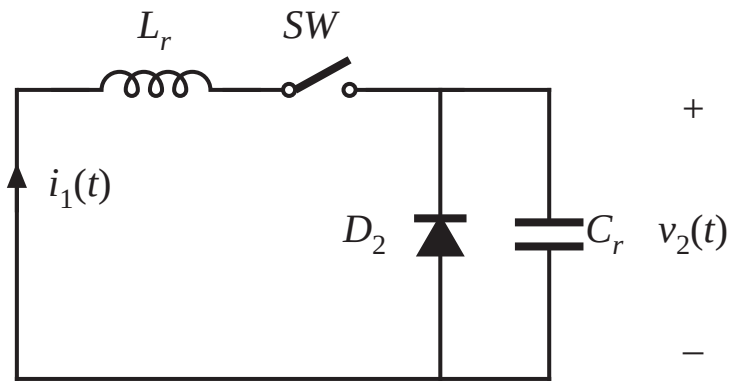
A test to determine the topology of a resonant switch network

Replace converter elements by their high-frequency equivalents:

- Independent voltage source V_g: short circuit
- Filter capacitors: short circuits
- Filter inductors: open circuits

The resonant switch network remains.

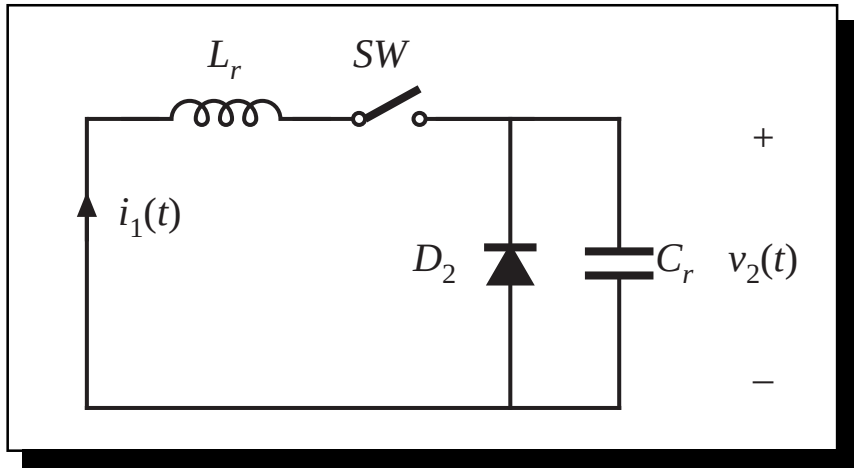
If the converter contains a ZCS quasi-resonant switch, then the result of these operations is



Zero-current and zero-voltage switching

ZCS quasi-resonant switch:

- Tank inductor is in series with switch; hence *SW* switches at zero current
- Tank capacitor is in parallel with diode D_2; hence D_2 switches at zero voltage

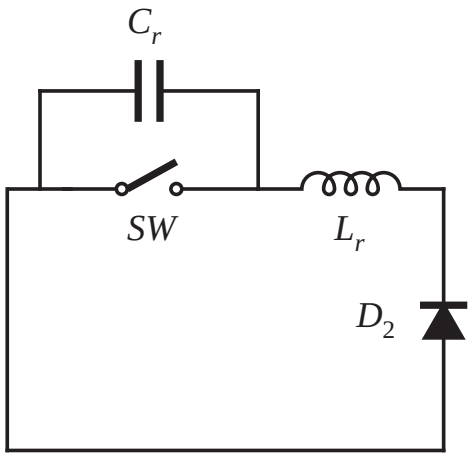


Discussion

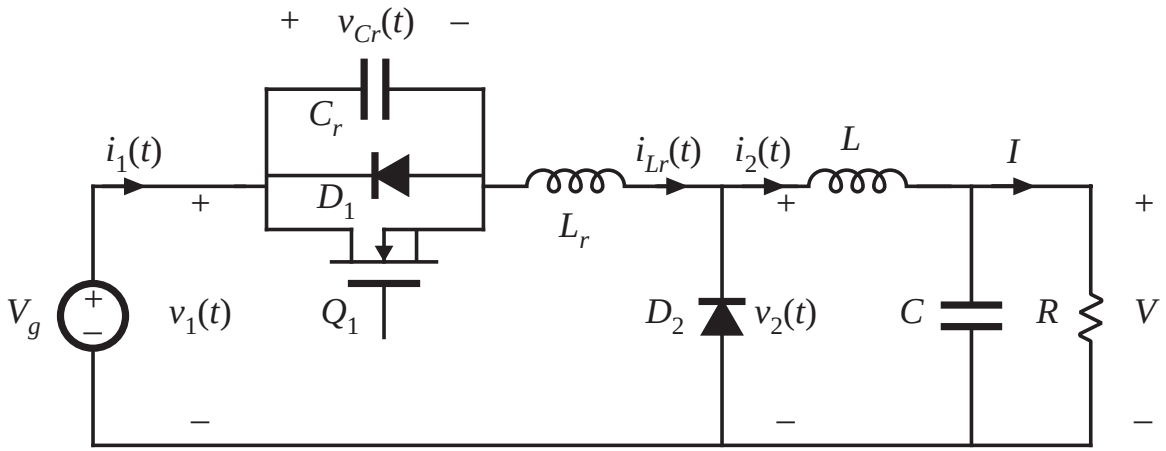
- Zero voltage switching of D_2 eliminates switching loss arising from D_2 stored charge.
- Zero current switching of SW: device Q_1 and D_1 output capacitances lead to switching loss. In full-wave case, stored charge of diode D_1 leads to switching loss.
- Peak transistor current is $(1 + J_s)\, V_g/R_0$, or more than twice the PWM value.

20.2.1 The zero-voltage-switching quasi-resonant switch cell

When the previously-described operations are followed, then the converter reduces to



A full-wave version based on the PWM buck converter:



ZVS quasi-resonant switch cell

Switch conversion ratio

$$\mu = 1 - FP_{\frac{1}{2}}\left(\frac{1}{J_s}\right) \qquad \textit{half-wave}$$

$$\mu = 1 - FP_{1}\left(\frac{1}{J_s}\right) \qquad \textit{full-wave}$$

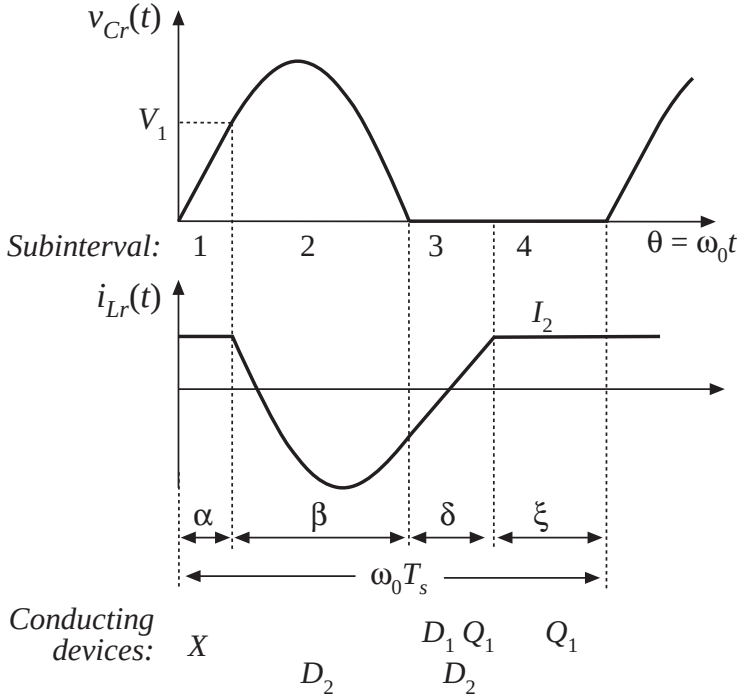
ZVS boundary

$$J_s \geq 1$$

peak transistor voltage $V_{cr,pk} = (1 + J_s)\, V_1$

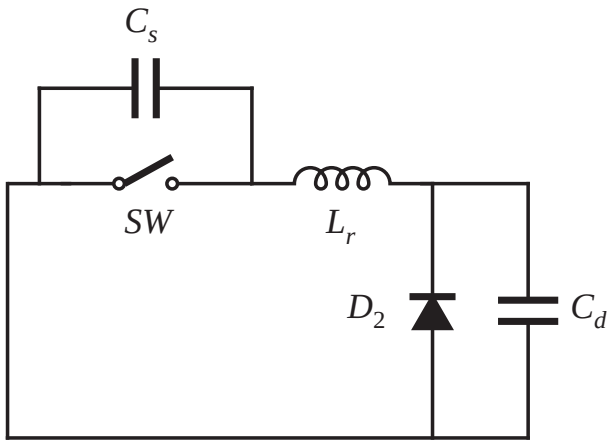
A problem with the quasi-resonant ZVS switch cell: peak transistor voltage becomes very large when zero voltage switching is required for a large range of load currents.

Tank waveforms

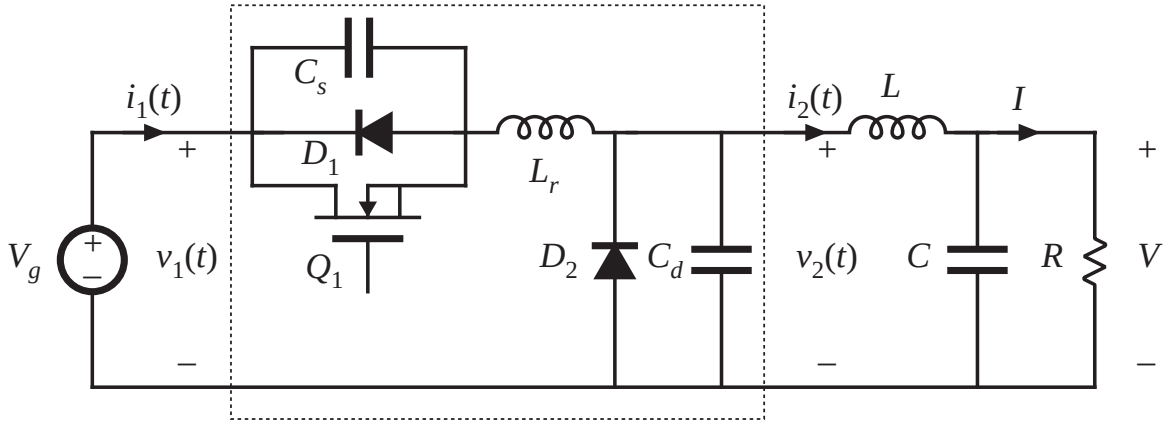


20.2.2 The ZVS multiresonant switch

When the previously-described operations are followed, then the converter reduces to



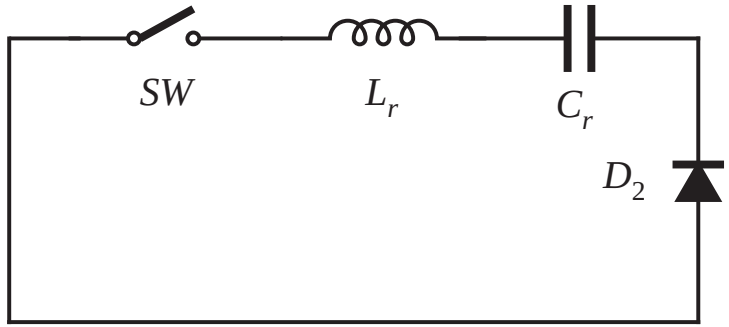
A half-wave version based on the PWM buck converter:



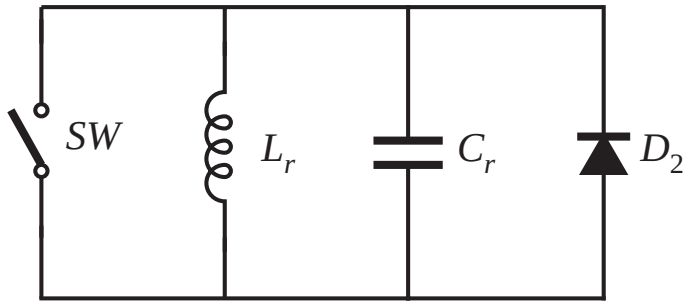
20.2.3 Quasi-square-wave resonant switches

When the previously-described operations are followed, then the converter reduces to

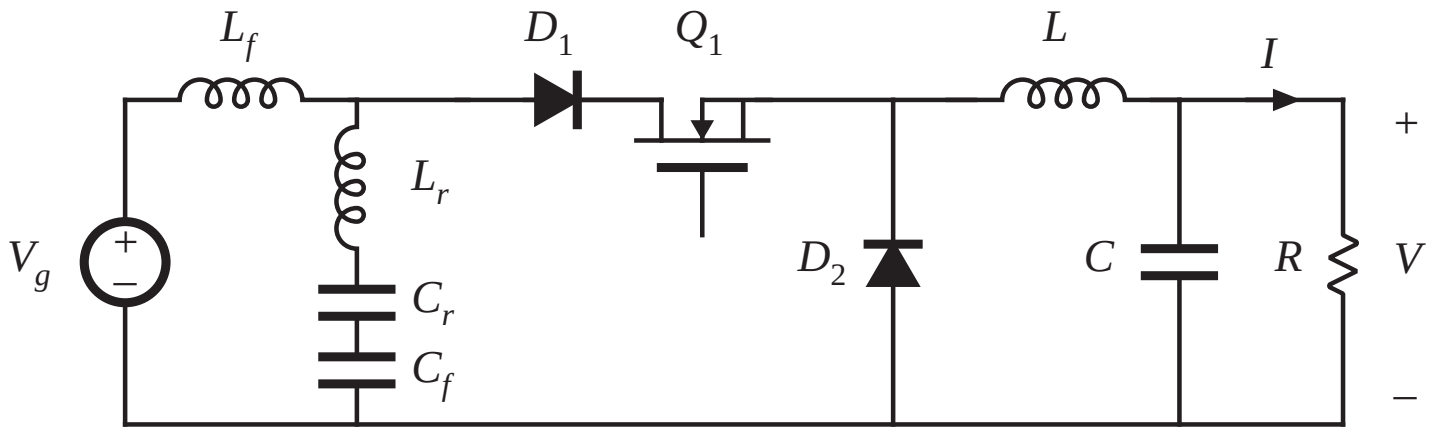
ZCS



ZVS

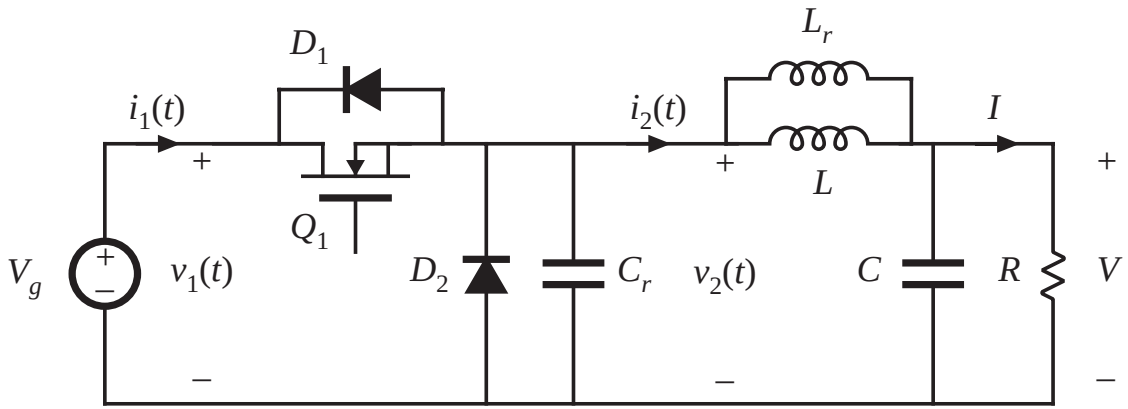


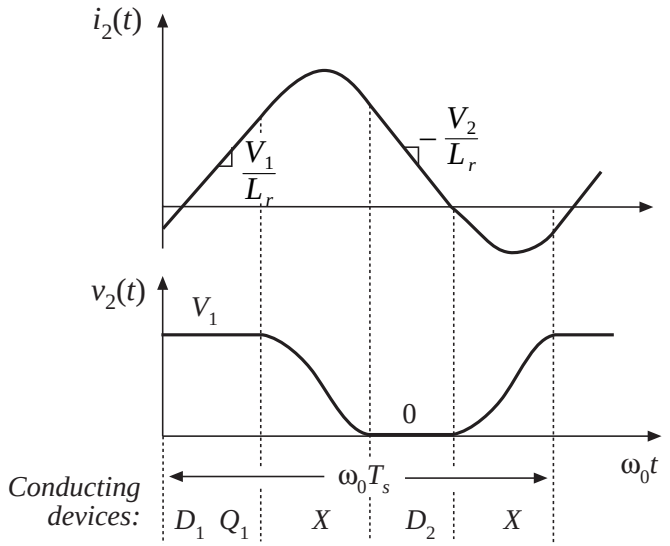
A quasi-square-wave ZCS buck with input filter



- The basic ZCS QSW switch cell is restricted to $0 \leq \mu \leq 0.5$
- Peak transistor current is equal to peak transistor current of PWM cell
- Peak transistor voltage is increased
- Zero-current switching in all semiconductor devices

A quasi-square-wave ZVS buck



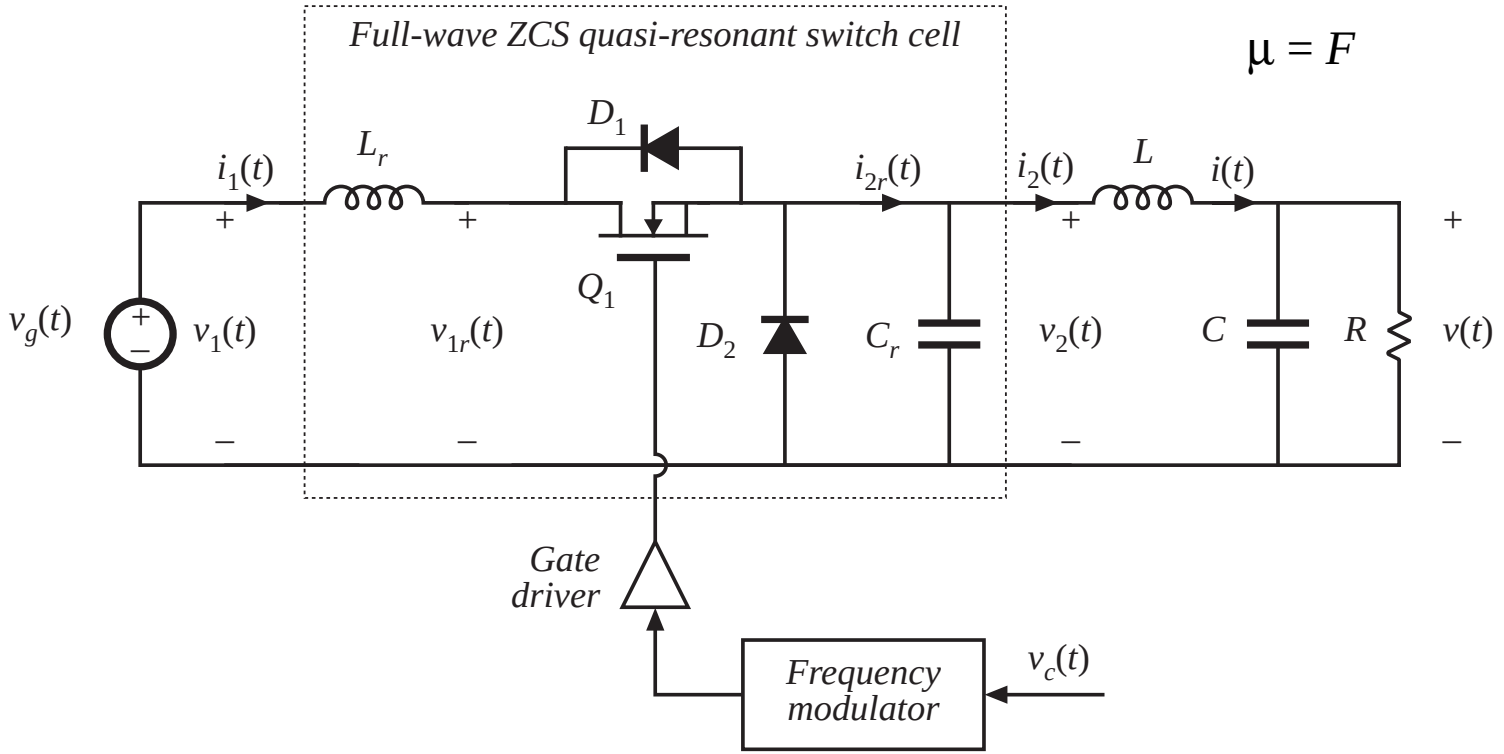


- The basic ZVS QSW switch cell is restricted to $0.5 \le \mu \le 1$
- Peak transistor voltage is equal to peak transistor voltage of PWM cell
- Peak transistor current is increased
- Zero-voltage switching in all semiconductor devices

20.3 Ac modeling of quasi-resonant converters

Use averaged switch modeling technique: apply averaged PWM model, with d replaced by μ

Buck example with full-wave ZCS quasi-resonant cell:



Small-signal ac model

Averaged switch equations:

$$\left\langle v_2(t) \right\rangle_{T_s} = \mu \left\langle v_{1r}(t) \right\rangle_{T_s}$$

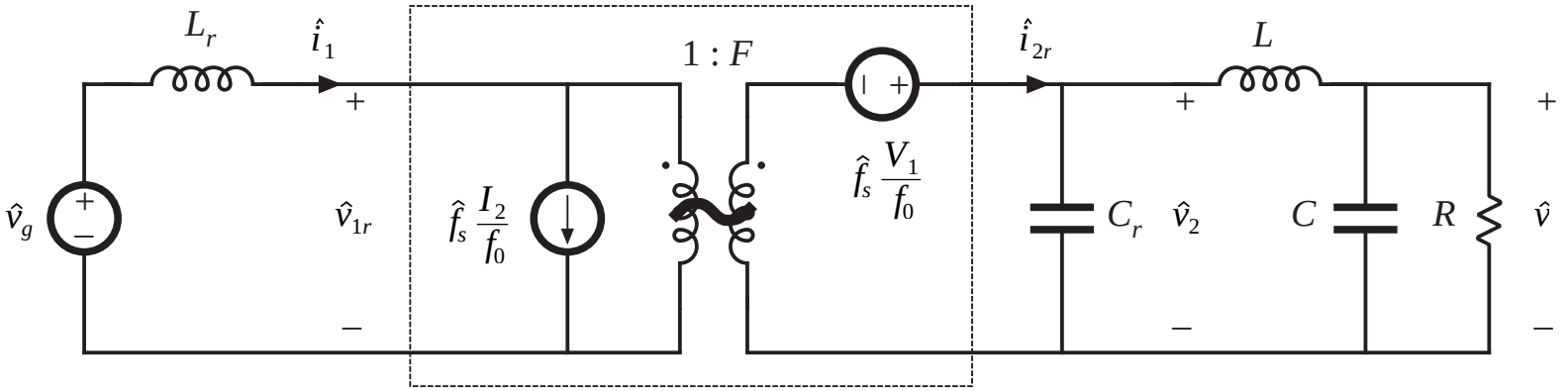
$$\left\langle i_1(t) \right\rangle_{T_s} = \mu \left\langle i_{2r}(t) \right\rangle_{T_s}$$

Linearize:

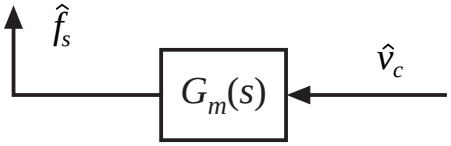
$$\hat{i}_1(t) = \hat{f}_s(t) \frac{I_2}{f_0}$$

$$\hat{v}_2(t) = \frac{F_s}{f_0} \hat{v}_{1r}(t) + \hat{f}_s(t) \frac{V_1}{f_0}$$

Resulting ac model:

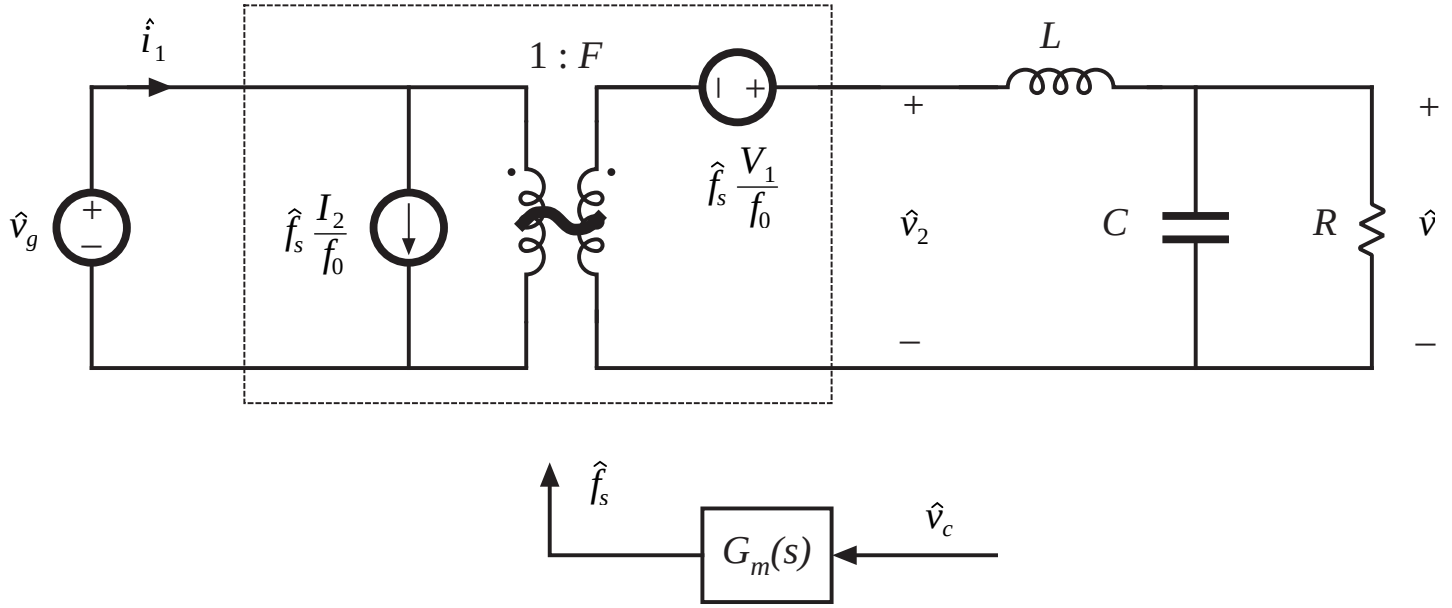


$$\mu = F$$



Low-frequency model

Tank dynamics occur only at frequency near or greater than switching frequency —discard tank elements



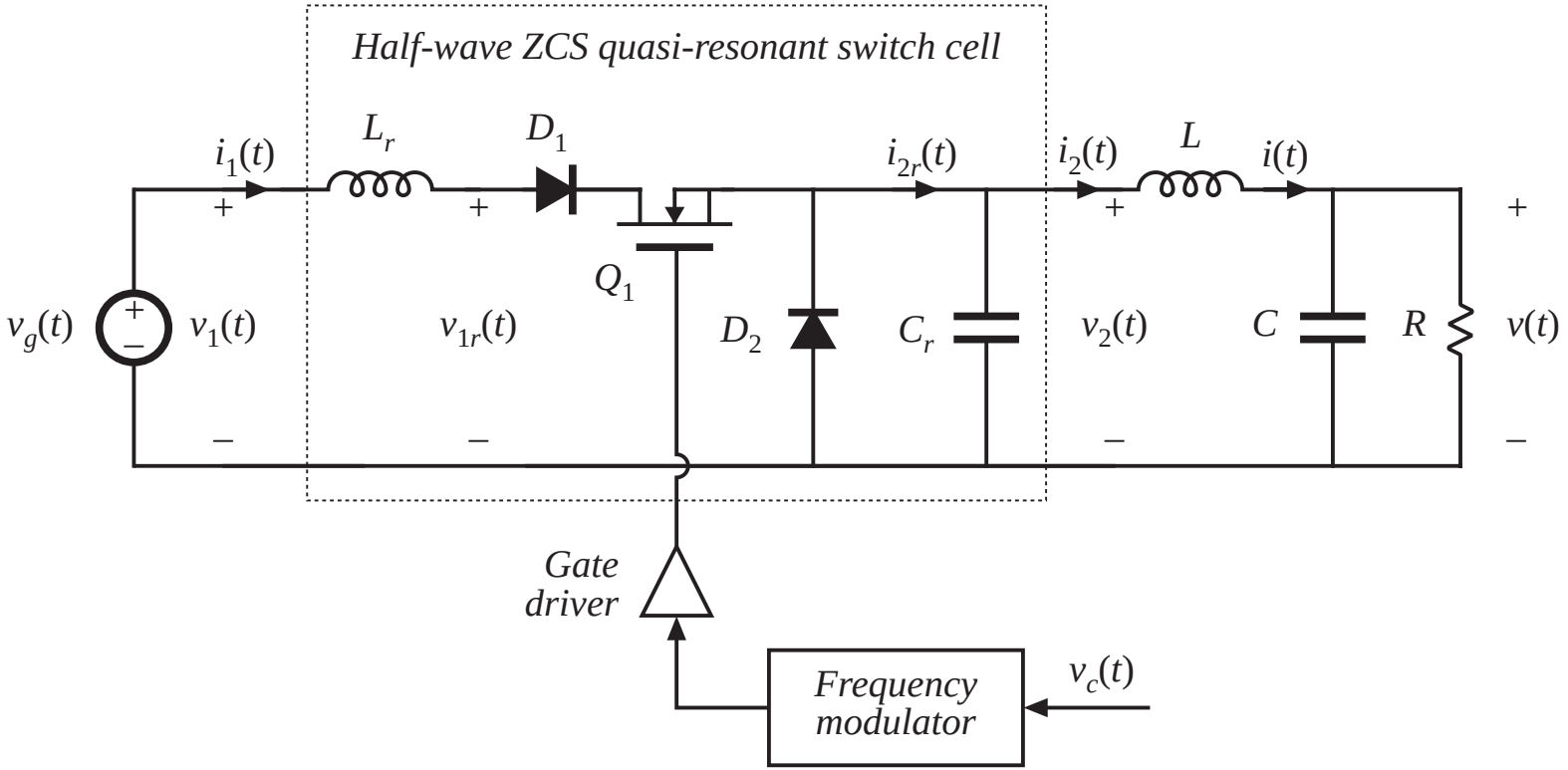
—same as PWM buck, with d replaced by F

Example 2: Half-wave ZCS quasi-resonant buck

Now, μ depends on j_s:

$$\mu(t) = \frac{f_s(t)}{f_0} P_{\frac{1}{2}}\left(j_s(t)\right)$$

$$j_s(t) = R_0 \frac{\left\langle i_{2r}(t) \right\rangle_{T_s}}{\left\langle v_{1r}(t) \right\rangle_{T_s}}$$



Small-signal modeling

Perturbation and linearization of $\mu(v_{1r}, i_{2r}, f_s)$:

$$\hat{\mu}(t) = K_v \hat{v}_{1r}(t) + K_i \hat{i}_{2r}(t) + K_c \hat{f}_s(t)$$

with

$$K_v = -\frac{\partial \mu}{\partial j_s} \frac{R_0 I_2}{V_1^2}$$

$$K_i = -\frac{\partial \mu}{\partial j_s} \frac{R_0}{V_1}$$

$$K_c = \frac{\mu_0}{F_s}$$

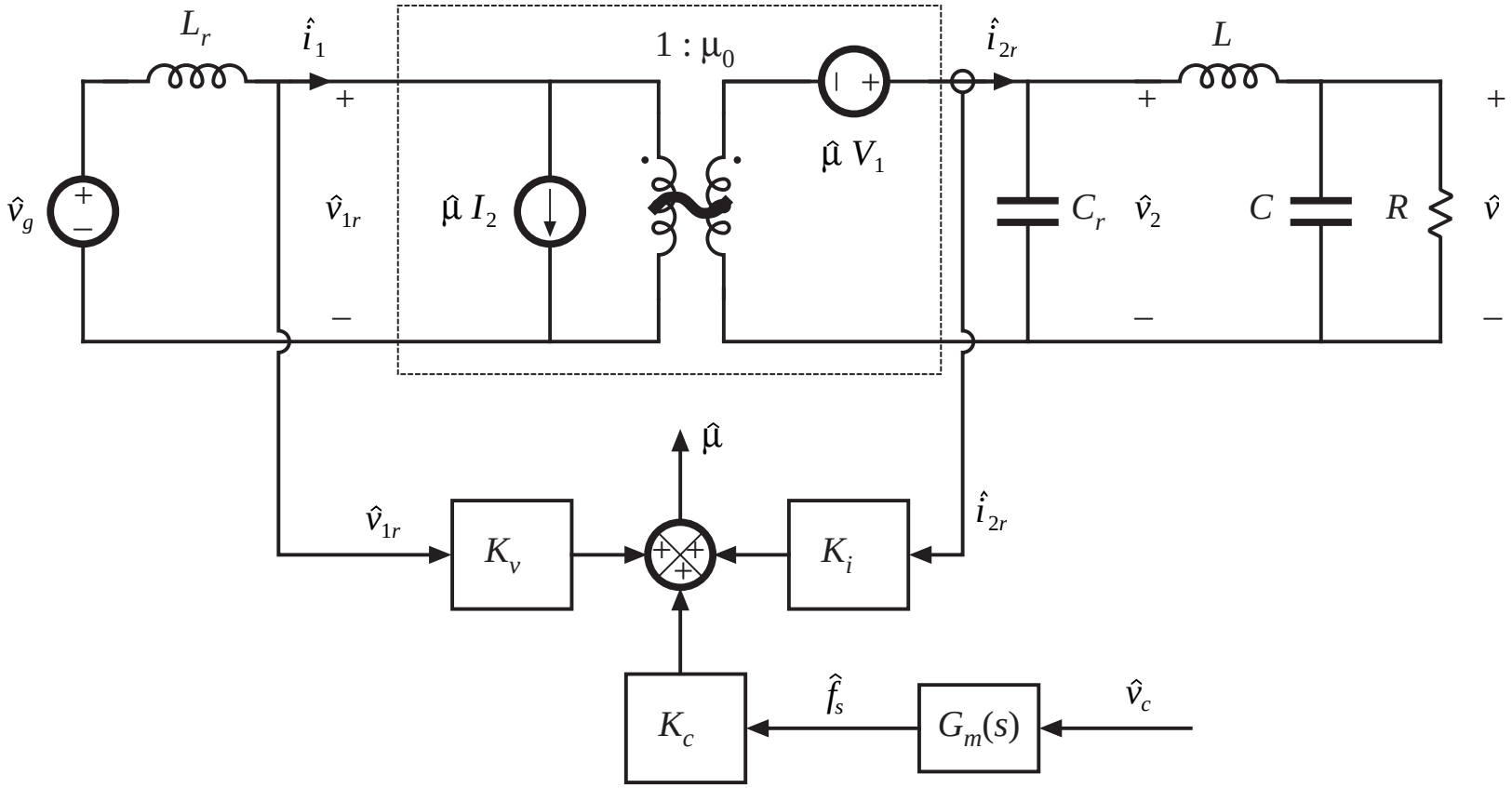
$$\frac{\partial \mu}{\partial j_s} = \frac{F_s}{2\pi f_0} \left(\frac{1}{2} - \frac{1 + \sqrt{1 - J_s^2}}{J_s^2} \right)$$

Linearized terminal equations of switch network:

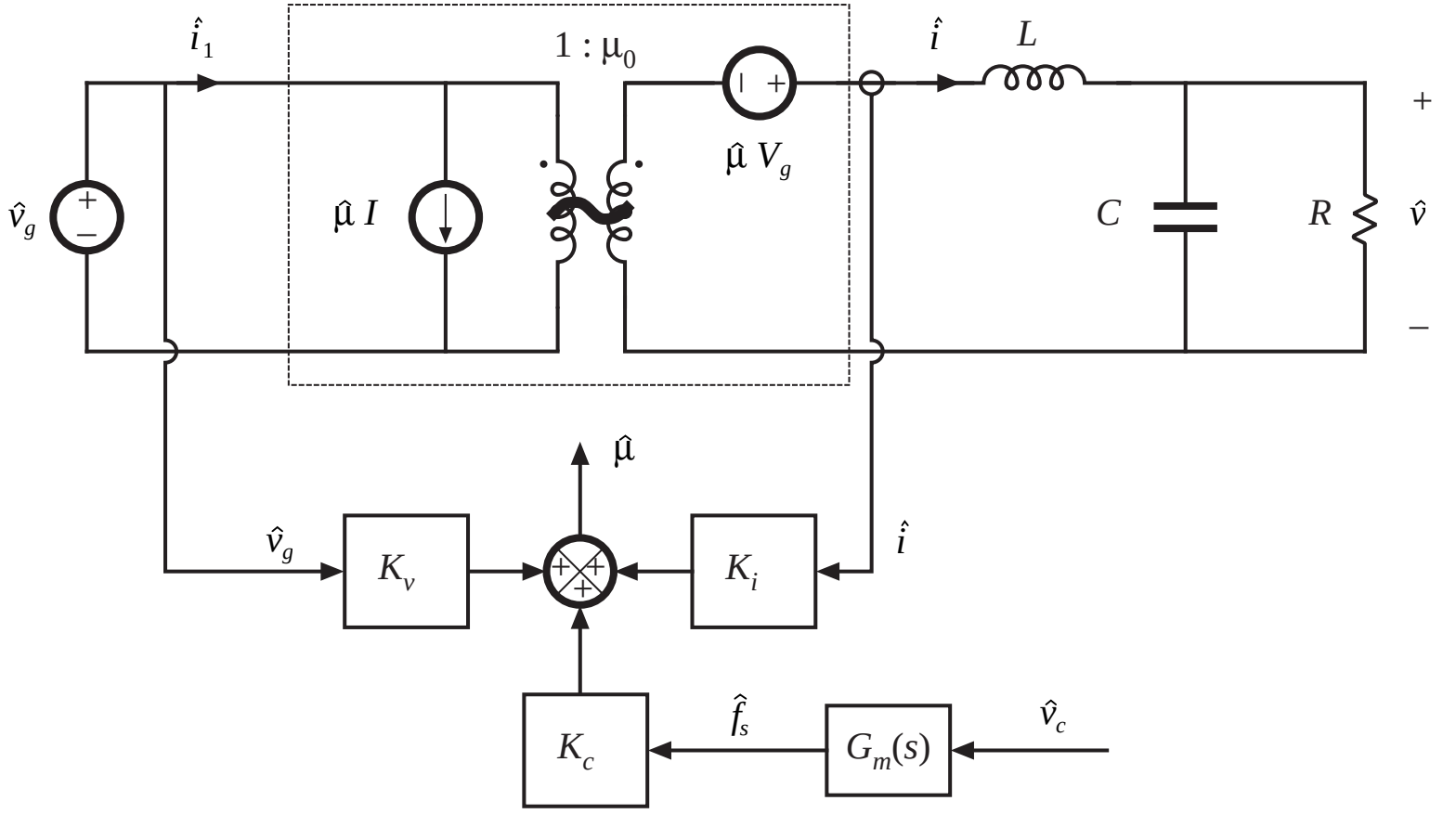
$$\hat{i}_1(t) = \hat{\mu}(t)\, I_2 + \hat{i}_{2r}(t)\, \mu_0$$

$$\hat{v}_2(t) = \mu_0\, \hat{v}_{1r}(t) + \hat{\mu}(t)\, V_1$$

Equivalent circuit model



Low frequency model: set tank elements to zero



Predicted small-signal transfer functions

Half-wave ZCS buck

$$G_{vg}(s) = G_{g0} \frac{1}{1 + \frac{1}{Q}\frac{s}{\omega_0} + \left(\frac{s}{\omega_0}\right)^2}$$

$$G_{vc}(s) = G_{c0} \frac{1}{1 + \frac{1}{Q}\frac{s}{\omega_0} + \left(\frac{s}{\omega_0}\right)^2}$$

Full-wave: poles and zeroes are same as PWM

Half-wave: effective feedback reduces Q-factor and dc gains

$$G_{g0} = \frac{\mu_0 + K_v V_g}{1 + \frac{K_i V_g}{R}}$$

$$G_{c0} = \frac{K_c V_g}{1 + \frac{K_i V_g}{R}}$$

$$\omega_0 = \sqrt{\frac{1 + \frac{K_i V_g}{R}}{L_r C_r}}$$

$$Q = \frac{\sqrt{1 + \frac{K_i V_g}{R}}}{\frac{R_0}{R} + K_i V_g \frac{R}{R_0}}$$

$$R_0 = \sqrt{\frac{L_r}{C_r}}$$

20.4 Summary of key points

1. In a resonant switch converter, the switch network of a PWM converter is replaced by a switch network containing resonant elements. The resulting hybrid converter combines the properties of the resonant switch network and the parent PWM converter.
2. Analysis of a resonant switch cell involves determination of the switch conversion ratio μ. The resonant switch waveforms are determined, and are then averaged. The switch conversion ratio μ is a generalization of the PWM CCM duty cycle d. The results of the averaged analysis of PWM converters operating in CCM can be directly adapted to the related resonant switch converter, simply by replacing d with μ.
3. In the zero-current-switching quasi-resonant switch, diode D_2 operates with zero-voltage switching, while transistor Q_1 and diode D_1 operate with zero-current switching.

Summary of key points

4. In the zero-voltage-switching quasi-resonant switch, the transistor Q_1 and diode D_1 operate with zero-voltage switching, while diode D_2 operates with zero-current switching.
5. Full-wave versions of the quasi-resonant switches exhibit very simple control characteristics: the conversion ratio μ is essentially independent of load current. However, these converters exhibit reduced efficiency at light load, due to the large circulating currents. In addition, significant switching loss is incurred due to the recovered charge of diode D_1.
6. Half-wave versions of the quasi-resonant switch exhibit conversion ratios that are strongly dependent on the load current. These converters typically operate with wide variations of switching frequency.
7. In the zero-voltage-switching multiresonant switch, all semiconductor devices operate with zero-voltage switching. In consequence, very low switching loss is observed.

Summary of key points

8. In the quasi-square-wave zero-voltage-switching resonant switches, all semiconductor devices operate with zero-voltage switching, and with peak voltages equal to those of the parent PWM converter. The switch conversion ratio is restricted to the range $0.5 \leq \mu \leq 1$.
9. The small-signal ac models of converters containing resonant switches are similar to the small-signal models of their parent PWM converters. The averaged switch modeling approach can be employed to show that the quantity $d(t)$ is simply replaced by $\mu(t)$.
10. In the case of full-wave quasi-resonant switches, μ depends only on the switching frequency, and therefore the transfer function poles and zeroes are identical to those of the parent PWM converter.
11. In the case of half-wave quasi-resonant switches, as well as other types of resonant switches, the conversion ratio μ is a strong function of the switch terminal quantities v_1 and i_2. This leads to effective feedback, which modifies the poles, zeroes, and gains of the transfer functions.

Appendix 2

Magnetics Design Tables

Geometrical data for several standard ferrite core shapes are listed here. The geometrical constant K_g is a measure of core size, useful for designing inductors and transformers which attain a given copper loss [1]. The K_g method for inductor design is described in Chapter 13. K_g is defined as

$$K_g = \frac{A_c^2 W_A}{MLT} \tag{A2.1}$$

where A_c is the core cross-sectional area, W_A is the window area, and MLT is the winding mean-length-per-turn. The geometrical constant K_{gfe} is a similar measure of core size, which is useful for designing ac inductors and transformers when the total copper plus core loss is constrained. The K_{gfe} method for magnetics design is described in Chapter 14. K_{gfe} is defined as

$$K_{gfe} = \frac{W_A \; A_c^{2(1-1/\beta)}}{MLT \; l_e^{2/\beta}} \; u(\beta) \tag{A2.2}$$

where l_e is the core mean magnetic path length, and β is the core loss exponent:

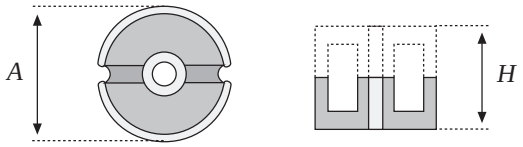
$$P_{fe} = K_{fe} B_{\max}^{\beta} \tag{A2.3}$$

For modern ferrite materials, β typically lies in the range 2.6 to 2.8. The quantity $u(\beta)$ is defined as

$$u(\beta) = \left[\left(\frac{\beta}{2} \right)^{-\left(\frac{\beta}{\beta+2} \right)} + \left(\frac{\beta}{2} \right)^{\left(\frac{2}{\beta+2} \right)} \right]^{-\left(\frac{\beta+2}{\beta} \right)} \tag{A2.4}$$

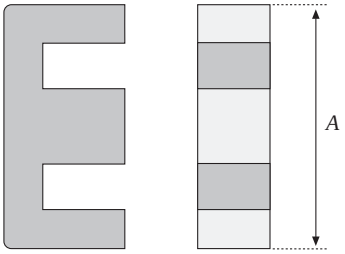
$u(\beta)$ is equal to 0.305 for $\beta = 2.7$. This quantity varies by roughly 5% over the range $2.6 \leq \beta \leq 2.8$. Values of K_{gfe} are tabulated for $\beta = 2.7$; variation of K_{gfe} over the range $2.6 \leq \beta \leq 2.8$ is typically quite small.

A2.1 Pot core data



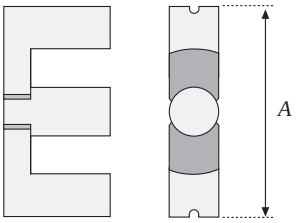
Core type (*AH*) (mm)	Geometrical constant K_g cm^5	Geometrical constant K_{gfe} cm^x	Cross-sectional area A_c (cm^2)	Bobbin winding area W_A (cm^2)	Mean length per turn MLT (cm)	Magnetic path length l_m (cm)	Thermal resistance R_{th} (°C/W)	Core weight (g)
704	$0.738 \cdot 10^{-6}$	$1.61 \cdot 10^{-6}$	0.070	$0.22 \cdot 10^{-3}$	1.46	1.0		0.5
905	$0.183 \cdot 10^{-3}$	$256 \cdot 10^{-6}$	0.101	0.034	1.90	1.26		1.0
1107	$0.667 \cdot 10^{-3}$	$554 \cdot 10^{-6}$	0.167	0.055	2.30	1.55		1.8
1408	$2.107 \cdot 10^{-3}$	$1.1 \cdot 10^{-3}$	0.251	0.097	2.90	2.00	100	3.2
1811	$9.45 \cdot 10^{-3}$	$2.6 \cdot 10^{-3}$	0.433	0.187	3.71	2.60	60	7.3
2213	$27.1 \cdot 10^{-3}$	$4.9 \cdot 10^{-3}$	0.635	0.297	4.42	3.15	38	13
2616	$69.1 \cdot 10^{-3}$	$8.2 \cdot 10^{-3}$	0.948	0.406	5.28	3.75	30	20
3019	0.180	$14.2 \cdot 10^{-3}$	1.38	0.587	6.20	4.50	23	34
3622	0.411	$21.7 \cdot 10^{-3}$	2.02	0.748	7.42	5.30	19	57
4229	1.15	$41.1 \cdot 10^{-3}$	2.66	1.40	8.60	6.81	13.5	104

A2.2 EE core data



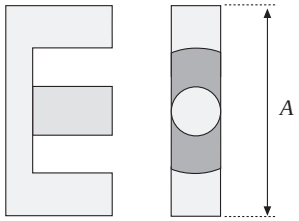
Core type (*A*) (mm)	Geometrical constant K_g cm^5	Geometrical constant K_{gfe} cm^x	Cross-sectional area A_c (cm^2)	Bobbin winding area W_A (cm^2)	Mean length per turn MLT (cm)	Magnetic path length l_m (cm)	Core weight (g)
EE12	$0.731 \cdot 10^{-3}$	$0.458 \cdot 10^{-3}$	0.14	0.085	2.28	2.7	2.34
EE16	$2.02 \cdot 10^{-3}$	$0.842 \cdot 10^{-3}$	0.19	0.190	3.40	3.45	3.29
EE19	$4.07 \cdot 10^{-3}$	$1.3 \cdot 10^{-3}$	0.23	0.284	3.69	3.94	4.83
EE22	$8.26 \cdot 10^{-3}$	$1.8 \cdot 10^{-3}$	0.41	0.196	3.99	3.96	8.81
EE30	$85.7 \cdot 10^{-3}$	$6.7 \cdot 10^{-3}$	1.09	0.476	6.60	5.77	32.4
EE40	0.209	$11.8 \cdot 10^{-3}$	1.27	1.10	8.50	7.70	50.3
EE50	0.909	$28.4 \cdot 10^{-3}$	2.26	1.78	10.0	9.58	116
EE60	1.38	$36.4 \cdot 10^{-3}$	2.47	2.89	12.8	11.0	135
EE70/68/19	5.06	$127 \cdot 10^{-3}$	3.24	6.75	14.0	9.0	280

A2.3 EC core data



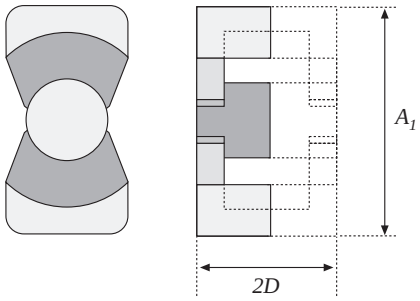
Core type (*A*) (mm)	Geometrical constant K_g cm^5	Geometrical constant K_{gfe} cm^x	Cross-sectional area A_c (cm^2)	Bobbin winding area W_A (cm^2)	Mean length per turn MLT (cm)	Magnetic path length l_m (cm)	Thermal resistance R_{th} (°C/W)	Core weight (g)
EC35	0.131	$9.9 \cdot 10^{-3}$	0.843	0.975	5.30	7.74	18.5	35.5
EC41	0.374	$19.5 \cdot 10^{-3}$	1.21	1.35	5.30	8.93	16.5	57.0
EC52	0.914	$31.7 \cdot 10^{-3}$	1.80	2.12	7.50	10.5	11.0	111
EC70	2.84	$56.2 \cdot 10^{-3}$	2.79	4.71	12.9	14.4	7.5	256

A2.4 ETD core data



Core type (*A*) (mm)	Geometrical constant K_g cm^5	Geometrical constant K_{gfe} cm^x	Cross-sectional area A_c (cm^2)	Bobbin winding area W_A (cm^2)	Mean length per turn MLT (cm)	Magnetic path length l_m (cm)	Thermal resistance R_{th} (˚C/W)	Core weight (g)
ETD29	0.0978	$8.5 \cdot 10^{-3}$	0.76	0.903	5.33	7.20		30
ETD34	0.193	$13.1 \cdot 10^{-3}$	0.97	1.23	6.00	7.86	19	40
ETD39	0.397	$19.8 \cdot 10^{-3}$	1.25	1.74	6.86	9.21	15	60
ETD44	0.846	$30.4 \cdot 10^{-3}$	1.74	2.13	7.62	10.3	12	94
ETD49	1.42	$41.0 \cdot 10^{-3}$	2.11	2.71	8.51	11.4	11	124

A2.5 PQ core data



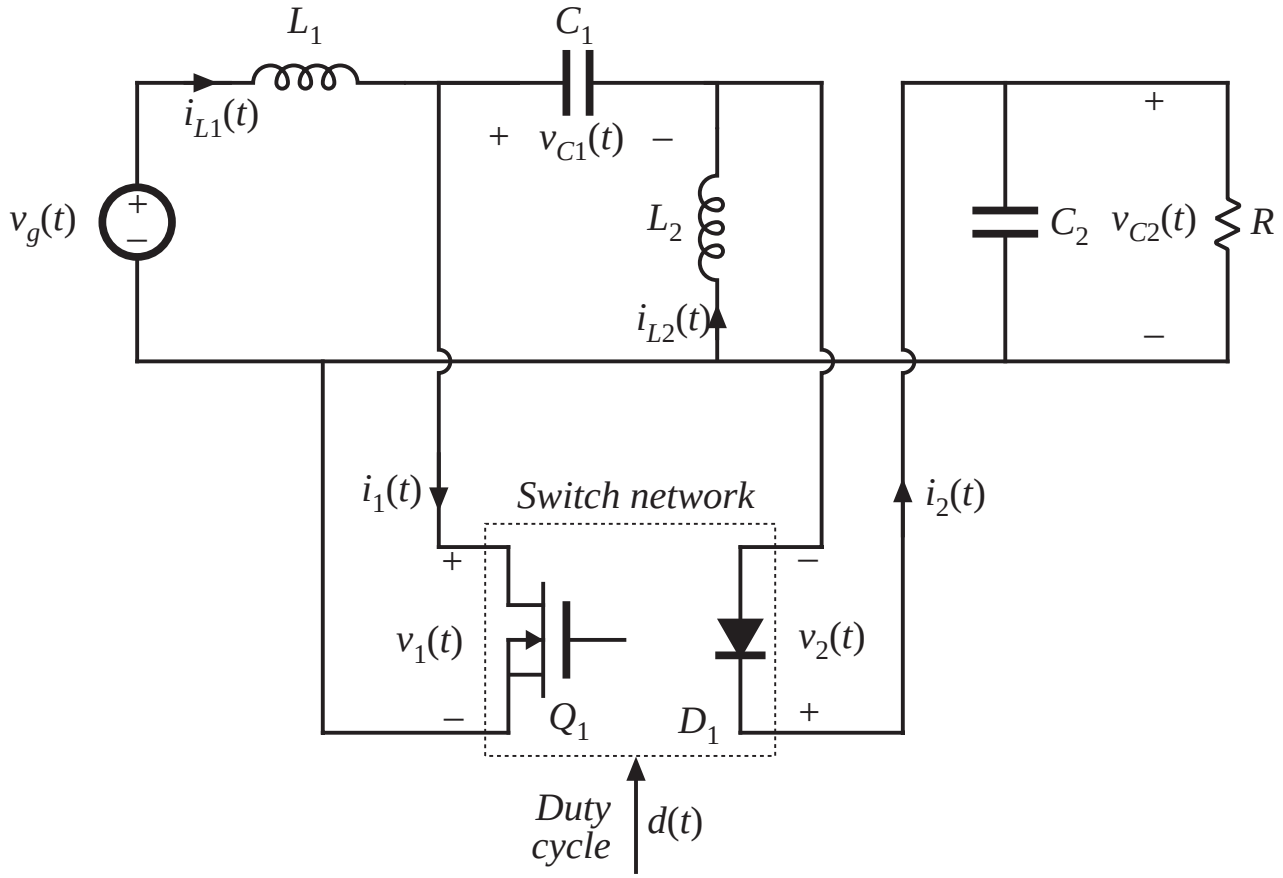
Core type (A_1/2*D*) (mm)	Geometrical constant K_g cm^5	Geometrical constant K_{gfe} cm^x	Cross-sectional area A_c (cm^2)	Bobbin winding area W_A (cm^2)	Mean length per turn MLT (cm)	Magnetic path length l_m (cm)	Core weight (g)
PQ 20/16	$22.4 \cdot 10^{-3}$	$3.7 \cdot 10^{-3}$	0.62	0.256	4.4	3.74	13
PQ 20/20	$33.6 \cdot 10^{-3}$	$4.8 \cdot 10^{-3}$	0.62	0.384	4.4	4.54	15
PQ 26/20	$83.9 \cdot 10^{-3}$	$7.2 \cdot 10^{-3}$	1.19	0.333	5.62	4.63	31
PQ 26/25	0.125	$9.4 \cdot 10^{-3}$	1.18	0.503	5.62	5.55	36
PQ 32/20	0.203	$11.7 \cdot 10^{-3}$	1.70	0.471	6.71	5.55	42
PQ 32/30	0.384	$18.6 \cdot 10^{-3}$	1.61	0.995	6.71	7.46	55
PQ 35/35	0.820	$30.4 \cdot 10^{-3}$	1.96	1.61	7.52	8.79	73
PQ 40/40	1.20	$39.1 \cdot 10^{-3}$	2.01	2.50	8.39	10.2	95

A2.6 American wire gauge data

AWG#	Bare area, 10^{-3} cm^2	Resistance, 10^{-6} Ω/cm	Diameter, cm
0000	1072.3	1.608	1.168
000	850.3	2.027	1.040
00	674.2	2.557	0.927
0	534.8	3.224	0.825
1	424.1	4.065	0.735
2	336.3	5.128	0.654
3	266.7	6.463	0.583
4	211.5	8.153	0.519
5	167.7	10.28	0.462
6	133.0	13.0	0.411
7	105.5	16.3	0.366
8	83.67	20.6	0.326
9	66.32	26.0	0.291
10	52.41	32.9	0.267
11	41.60	41.37	0.238
12	33.08	52.09	0.213
13	26.26	69.64	0.190
14	20.02	82.80	0.171
15	16.51	104.3	0.153
16	13.07	131.8	0.137
17	10.39	165.8	0.122
18	8.228	209.5	0.109
19	6.531	263.9	0.0948
20	5.188	332.3	0.0874
21	4.116	418.9	0.0785
22	3.243	531.4	0.0701
23	2.508	666.0	0.0632
24	2.047	842.1	0.0566
25	1.623	1062.0	0.0505
26	1.280	1345.0	0.0452
27	1.021	1687.6	0.0409
28	0.8046	2142.7	0.0366
29	0.6470	2664.3	0.0330
30	0.5067	3402.2	0.0294
31	0.4013	4294.6	0.0267
32	0.3242	5314.9	0.0241
33	0.2554	6748.6	0.0236
34	0.2011	8572.8	0.0191
35	0.1589	10849	0.0170
36	0.1266	13608	0.0152
37	0.1026	16801	0.0140
38	0.08107	21266	0.0124
39	0.06207	27775	0.0109
40	0.04869	35400	0.0096
41	0.03972	43405	0.00863
42	0.03166	54429	0.00762
43	0.02452	70308	0.00685

Appendix 3: Averaged switch modeling of a CCM SEPIC

SEPIC example: write circuit with switch network explicitly identified



A few points regarding averaged switch modeling

- The switch network can be defined arbitrarily, as long as

  its terminal voltages and currents are independent, and

  the switch network contains no reactive elements.

- It is ***not*** necessary that some of the switch network terminal quantities

  coincide with inductor currents or capacitor voltages of the converter, or

  be nonpulsating.

- The object is simply to write the averaged equations of the switch network; i.e., to express the average values of half of the switch network terminal waveforms as functions of

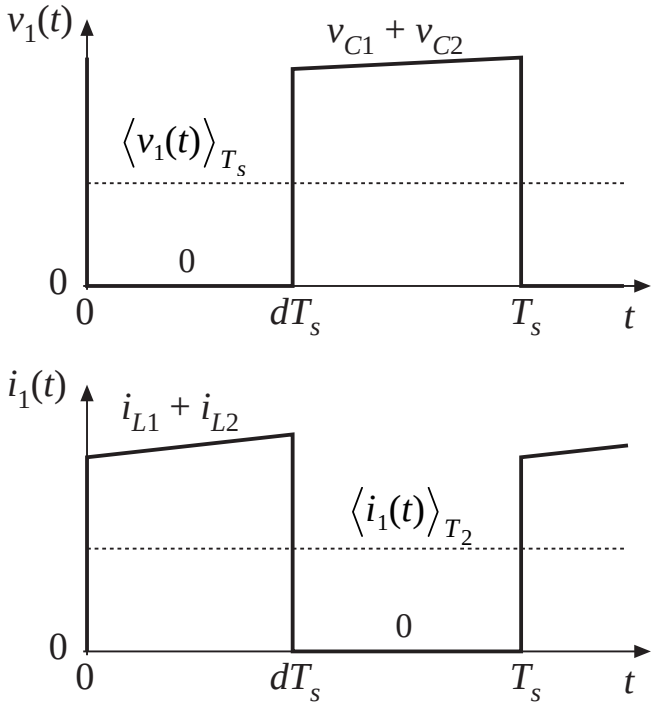
  the average values of the remaining switch network terminal waveforms, and

  the control input.

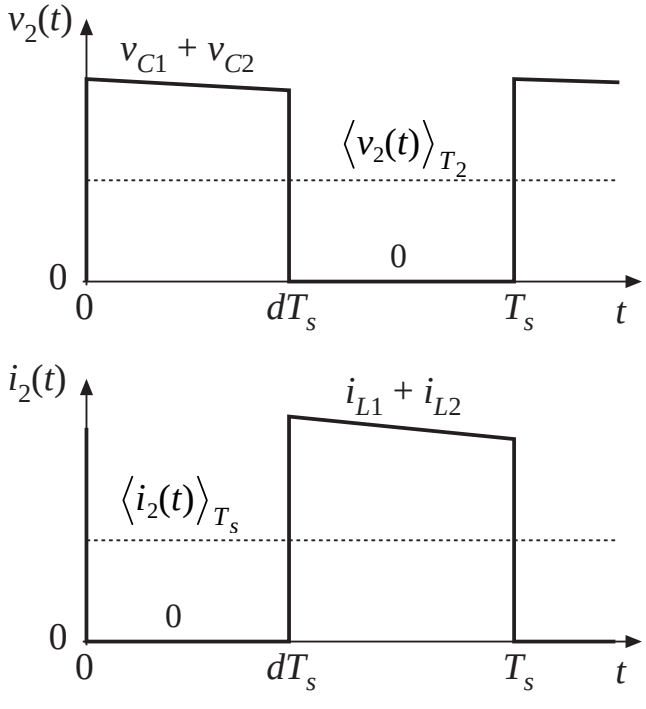
SEPIC CCM waveforms

Sketch terminal waveforms of switch network

Port 1



Port 2



Expressions for average values of switch network terminal waveforms

Use small ripple approximation

$$\left\langle v_1(t)\right\rangle_{T_s} = d'(t)\left(\left\langle v_{C1}(t)\right\rangle_{T_s} + \left\langle v_{C2}(t)\right\rangle_{T_s}\right)$$

$$\left\langle i_1(t)\right\rangle_{T_s} = d(t)\left(\left\langle i_{L1}(t)\right\rangle_{T_s} + \left\langle i_{L2}(t)\right\rangle_{T_s}\right)$$

$$\left\langle v_2(t)\right\rangle_{T_s} = d(t)\left(\left\langle v_{C1}(t)\right\rangle_{T_s} + \left\langle v_{C2}(t)\right\rangle_{T_s}\right)$$

$$\left\langle i_2(t)\right\rangle_{T_s} = d'(t)\left(\left\langle i_{L1}(t)\right\rangle_{T_s} + \left\langle i_{L2}(t)\right\rangle_{T_s}\right)$$

Need next to eliminate the capacitor voltages and inductor currents from these expressions, to write the equations of the switch network.

Derivation of switch network equations (Algebra steps)

We can write

$$\left\langle i_{L1}(t)\right\rangle_{T_s} + \left\langle i_{L2}(t)\right\rangle_{T_s} = \frac{\left\langle i_1(t)\right\rangle_{T_s}}{d(t)}$$

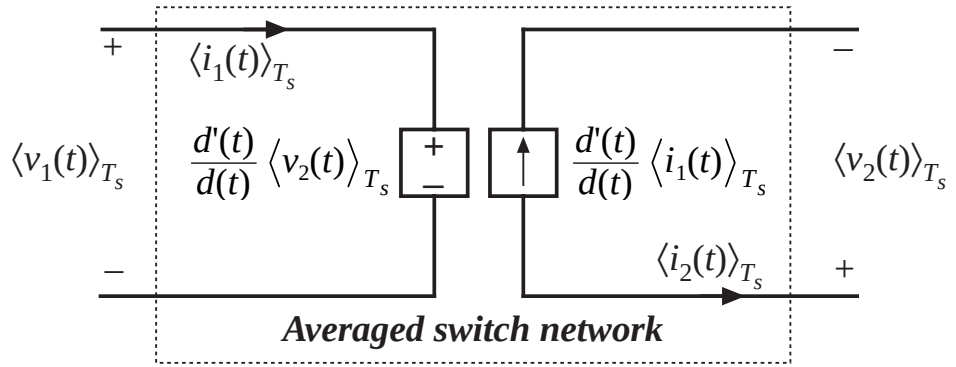
$$\left\langle v_{C1}(t)\right\rangle_{T_s} + \left\langle v_{C2}(t)\right\rangle_{T_s} = \frac{\left\langle v_2(t)\right\rangle_{T_s}}{d(t)}$$

Hence

$$\left\langle v_1(t)\right\rangle_{T_s} = \frac{d'(t)}{d(t)} \left\langle v_2(t)\right\rangle_{T_s}$$

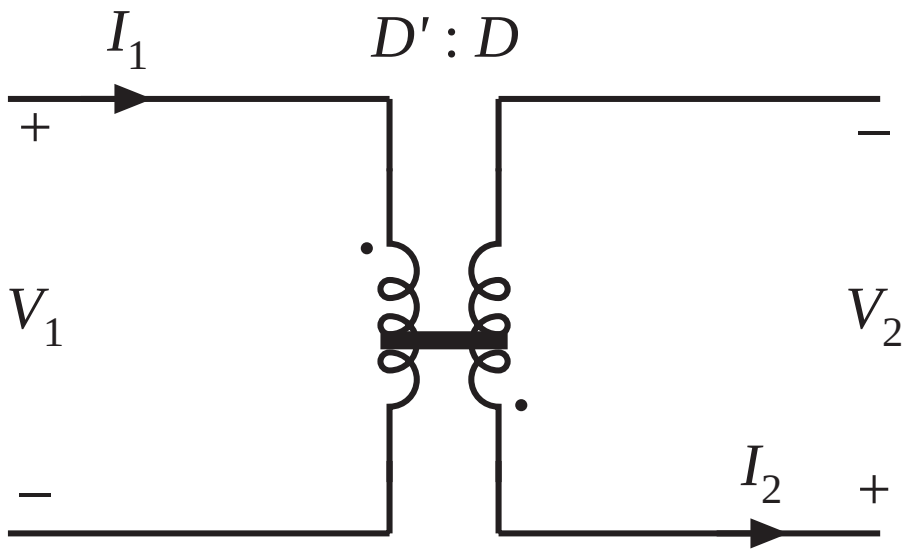
$$\left\langle i_2(t)\right\rangle_{T_s} = \frac{d'(t)}{d(t)} \left\langle i_1(t)\right\rangle_{T_s}$$

Result



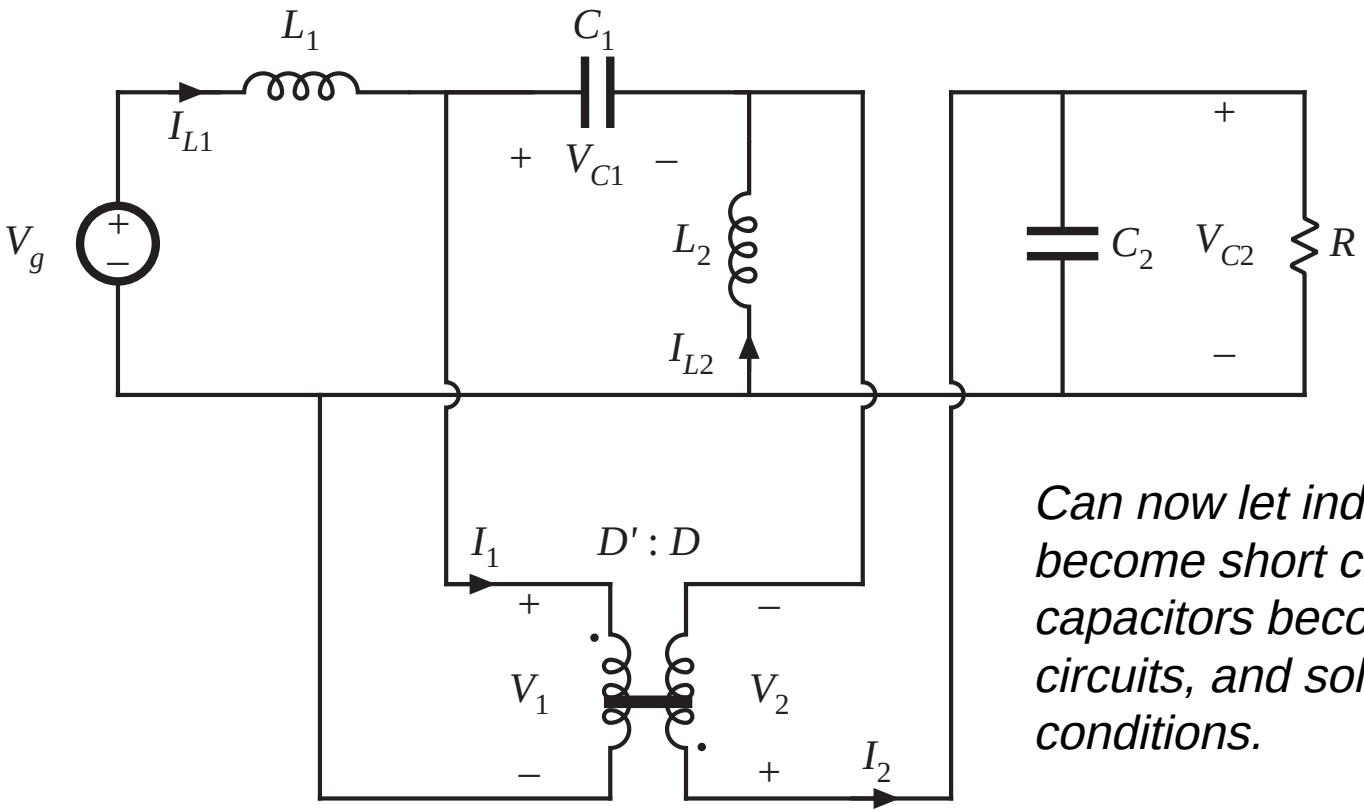
Modeling the switch network via averaged dependent sources

Steady-state switch model: Dc transformer model



Steady-state CCM SEPIC model

Replace switch network with dc transformer model



Can now let inductors become short circuits, capacitors become open circuits, and solve for dc conditions.

Small-signal model

Perturb and linearize the switch network averaged waveforms, as usual:

$$d(t) = D + \hat{d}(t)$$

$$\left\langle v_1(t) \right\rangle_{T_s} = V_1 + \hat{v}_1(t)$$

$$\left\langle i_1(t) \right\rangle_{T_s} = I_1 + \hat{i}_1(t)$$

$$\left\langle v_2(t) \right\rangle_{T_s} = V_2 + \hat{v}_2(t)$$

$$\left\langle i_2(t) \right\rangle_{T_s} = I_2 + \hat{i}_2(t)$$

Voltage equation becomes

$$\left(D + \hat{d}\right)\left(V_1 + \hat{v}_1\right) = \left(D' - \hat{d}\right)\left(V_2 + \hat{v}_2\right)$$

Eliminate nonlinear terms and solve for v_1 terms:

$$\left(V_1 + \hat{v}_1\right) = \frac{D'}{D}\left(V_2 + \hat{v}_2\right) - \hat{d}\left(\frac{V_1 + V_2}{D}\right)$$

$$= \frac{D'}{D}\left(V_2 + \hat{v}_2\right) - \hat{d}\left(\frac{V_1}{DD'}\right)$$

Linearization, continued

Current equation becomes

$$\left(D + \hat{d}\right)\left(I_2 + \hat{i}_2\right) = \left(D' - \hat{d}\right)\left(I_1 + \hat{i}_1\right)$$

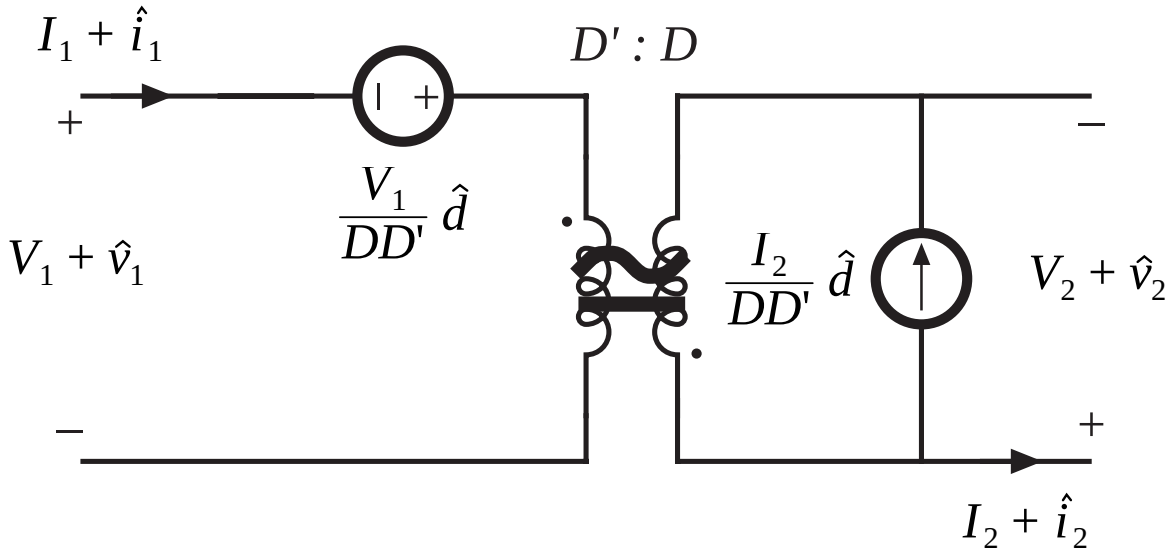
Eliminate nonlinear terms
and solve for i_2 terms:

$$\left(I_2 + \hat{i}_2\right) = \frac{D'}{D}\left(I_1 + \hat{i}_1\right) - \hat{d}\left(\frac{I_1 + I_2}{D}\right)$$

$$= \frac{D'}{D}\left(I_1 + \hat{i}_1\right) - \hat{d}\left(\frac{I_2}{DD'}\right)$$

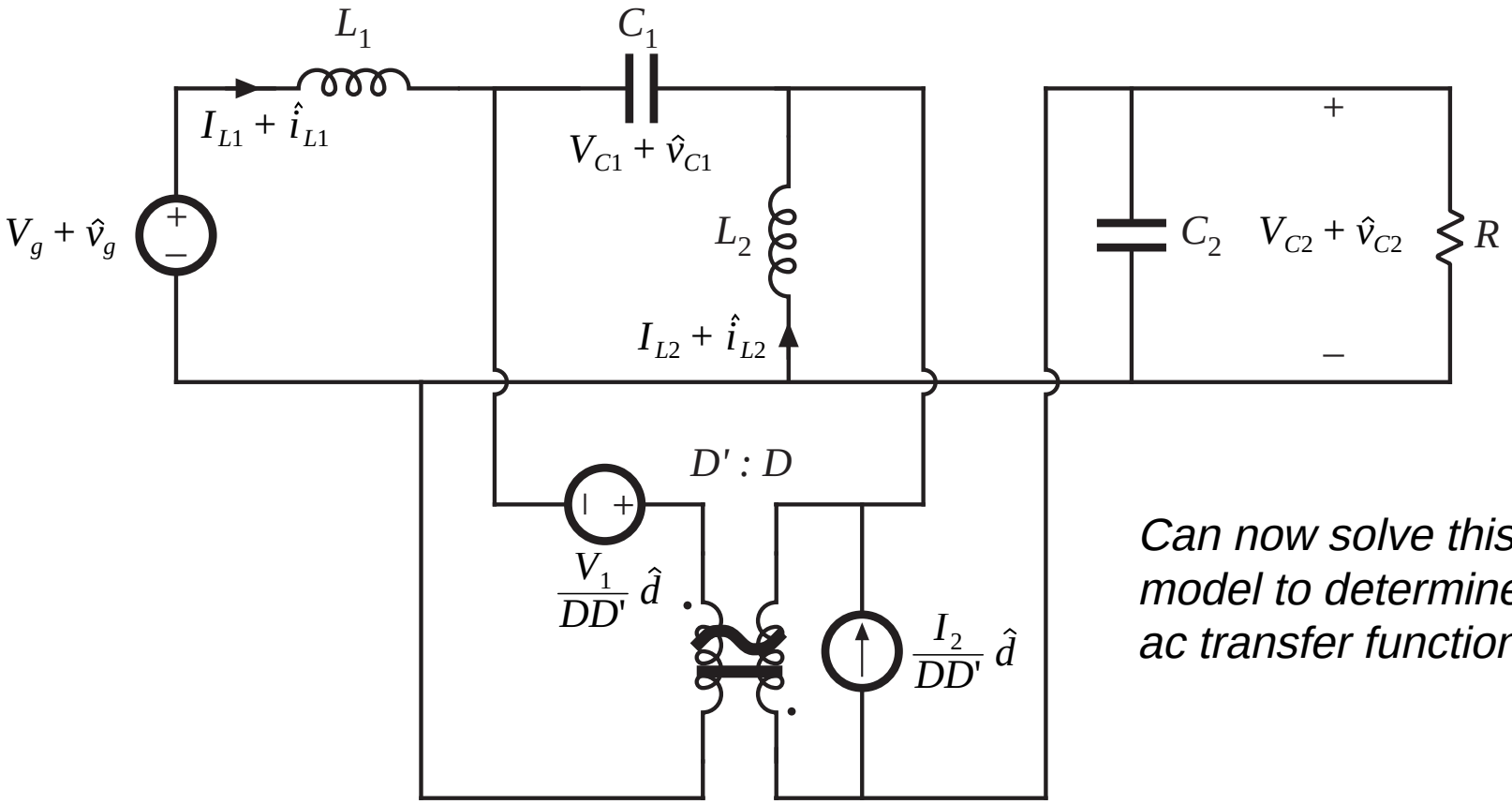
Switch network: Small-signal ac model

Reconstruct equivalent circuit in the usual manner:



Small-signal ac model of the CCM SEPIC

Replace switch network with small-signal ac model:



Can now solve this model to determine ac transfer functions